

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTELLECTUAL VENTURES MANAGEMENT, LLC
Petitioner

v.

XILINX, INC.
Patent Owner

Case IPR2012-00018
Patent 7,566,960 B1

Before SALLY C. MEDLEY, KARL D. EASTHOM, and
JUSTIN T. ARBES, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

Petitioner Intellectual Ventures Management, LLC (“IVM”) filed a Petition (Paper 6) (“Pet.”) seeking *inter partes* review of claims 1-13 of Patent 7,566,960 B1 (“the ’960 patent”) pursuant to 35 U.S.C. §§ 311-319. On February 12, 2013, the Board granted the Petition and instituted an *inter partes* review of all claims on four grounds of unpatentability (Paper 13) (“Dec. on Inst.”).

Subsequent to institution, Patent Owner Xilinx, Inc. (“Xilinx”) filed a Patent Owner Response (Paper 17) (“PO Resp.”), and IVM filed a Reply (Paper 28) (“Pet. Reply”). Along with its Patent Owner Response, Xilinx filed a Motion to Amend. Paper 19. The motion was dismissed as defective, and Xilinx filed a Substitute Motion to Amend. See Papers 20, 22. After Xilinx filed its Substitute Motion, the Board entered a decision in *Idle Free Systems, Inc. v. Bergstrom, Inc.*, IPR2012-00027, Paper 26 (June 11, 2013) (“*Idle Free* Decision”) regarding motions to amend. Xilinx requested, and received authorization from the Board, to file a second substitute motion to amend to comply with that decision. Paper 24. Xilinx then filed its Second Substitute Motion to Amend (Paper 26) (“Second Subst. Mot. to Amend”), proposing substitute claims 14-21 if the Board determines claim 1 to be unpatentable, and substitute claims 22-26 if the Board determines claim 9 to be unpatentable. IVM filed an Opposition to the Second Substitute Motion to Amend (Paper 29) (“Opp.”), and Xilinx filed a Reply (Paper 31) (“PO Reply”). The parties did not seek an oral hearing. Paper 34.

The Board has jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine that IVM has shown by a preponderance of the evidence that claims 1-13 of the '960 patent are unpatentable, and we deny Xilinx's Second Substitute Motion to Amend.

A. The '960 Patent

The '960 patent relates to an “interposer disposed inside an integrated circuit package between a die and the package, wherein the interposer provides bypass capacitance, signal redistribution functionality and/or signal termination structures close to the semiconductor die.” Ex. 1001, col. 1, ll. 5-9. The '960 patent explains that it was known in the prior art to add a bypass capacitor to an integrated circuit (IC) device to reduce various power supply problems. *Id.* at col. 1, l. 49-col. 2, l. 30. According to the '960 patent, however, power supply problems often could not be anticipated during the initial design of an integrated circuit, and redesigning an integrated circuit to add bypass capacitance after it already has been designed and built “can be exceedingly expensive and slow.” *Id.* at col. 2, ll. 31-40. Also, the interconnections between the terminals on an integrated circuit and the signal traces on a printed circuit board (PCB) are sometimes incorrect, such that “[i]t would be desirable to be able to correct for this problem without having to redesign and refabricate the printed circuit.” *Id.* at col. 2, ll. 41-50. The '960 patent describes adding an extremely thin “capacitive interposer (caposer),” which provides the necessary bypass capacitance, between an integrated circuit die and an inside surface of an integrated circuit package (connected to a printed circuit board). *Id.* at col. 3, ll. 13-27; Fig. 1. The integrated circuit design then does not need to be

changed to solve power supply and interconnection problems that later arise. *Id.* at col. 3, ll. 41-44; col. 4, ll. 60-67.

The '960 patent describes various exemplary embodiments. Figure 10 is reproduced below.

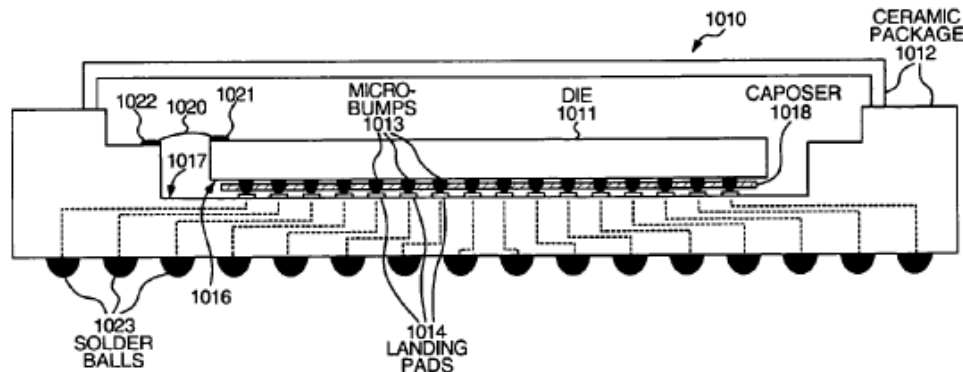


FIG. 10

Figure 10 depicts structure 1010 comprising (1) integrated circuit die 1011 having micro-bumps 1013 on planar surface 1016, (2) ceramic integrated circuit package 1012 having landing pads 1014 on inside upper surface 1017, and (3) through-hole caposer 1018¹ “disposed between inside upper surface 1017 of ceramic package 1012 and surface 1016 of die 1011.” *Id.* at col. 11, ll. 10-31. Integrated circuit package 1012 also has solder balls 1023 on its bottom surface for coupling to a printed circuit board (not shown). *Id.* at col. 11, ll. 33-37.

¹ The '960 patent explains that caposers may be either “through-hole” or “via.” Ex. 1001, col. 10, ll. 47-58. In a through-hole caposer, “an array of through holes passes through the caposer,” whereas in a via caposer, “conductive vias pass substantially orthogonally through the caposer.” *Id.*

Figure 24 depicts another embodiment and is reproduced below.

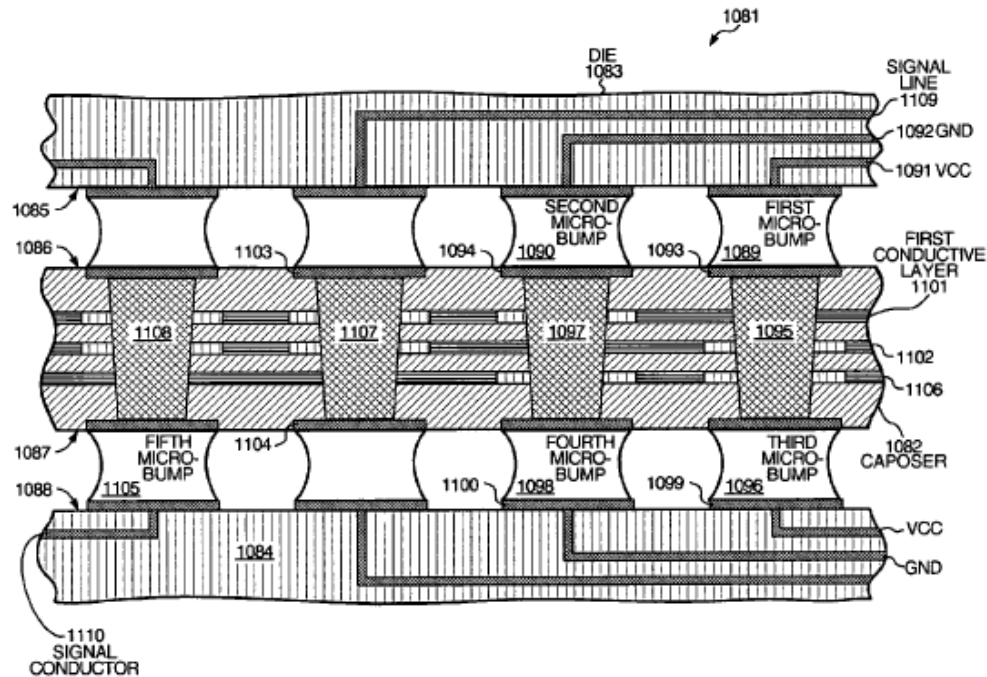


FIG. 24

As shown in Figure 24, caposer 1082 provides bypass capacitance and also “redistributes signals” through the use of multiple conductive layers 1101, 1102, and 1106. *Id.* at col. 18, l. 47-col. 19, l. 3. Signal line 1109 is coupled to landing pad 1103, and third conductive layer 1106 of caposer 1082 is coupled to vias 1107 and 1108. *Id.* This creates an electrically conductive path between the micro-bump above landing pad 1103 and two different landing pads on integrated circuit package 1084: (1) the landing pad below pad 1104 and the corresponding micro-bump, and (2) the landing pad below micro-bump 1105. *Id.* Caposer 1082, therefore, “can be used to redistribute signal inputs and outputs from array positions on die 1083 to different positions on ceramic package 1084.” *Id.* at col. 18, l. 67-col. 19, l. 3.

B. Exemplary Claims

Claims 1 and 9 of the '960 patent are the only independent claims:

1. An assembly, comprising:

an integrated circuit die having an array of micro-bumps disposed on a surface of the integrated circuit die in a first pattern;

an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and an array of solder balls disposed on an outside surface of the integrated circuit package, wherein the first pattern and the second pattern are substantially identical patterns; and

an interposing structure disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer electrically coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite to the first position and to a second landing pad in the array of landing pads.

9. An assembly, comprising:

an integrated circuit die having an array of micro-bumps disposed on a surface of the integrated circuit die in a first pattern;

an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and an array of solder balls disposed on an outside surface of the integrated circuit package, wherein the first pattern and the second pattern are substantially identical patterns; and

means for electrically coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed opposite the first position and to a second landing pad located in a different position in the array of landing pads, the means being disposed inside the integrated circuit package

between the integrated circuit die and the inside surface of the integrated circuit package.

C. Prior Art

The pending grounds of unpatentability in this *inter partes* review are based on the following prior art:

1. U.S. Patent No. 6,423,570 B1, issued July 23, 2002 (Ex. 1008) (“Ma”);
2. U.S. Patent No. 6,469,908 B2, issued Oct. 22, 2002 (Ex. 1005) (“Patel”);
3. U.S. Patent No. 6,730,540 B2, filed Apr. 18, 2002, issued May 4, 2004 (Ex. 1004) (“Siniaguine”); and
4. U.S. Patent No. 6,970,362 B1, filed July 31, 2000, issued Nov. 29, 2005 (Ex. 1007) (“Chakravorty ’362”).

D. Pending Grounds of Unpatentability

This *inter partes* review involves the following grounds of unpatentability:

References	Basis	Claims
Chakravorty ’362 and Siniaguine	35 U.S.C. § 103(a)	1-5, 7-11, and 13
Chakravorty ’362, Siniaguine, and Patel	35 U.S.C. § 103(a)	6 and 12
Siniaguine, Ma, and Chakravorty ’362	35 U.S.C. § 103(a)	1-5, 7-11, and 13
Siniaguine, Ma, Chakravorty ’362, and Patel	35 U.S.C. § 103(a)	6 and 12

II. ANALYSIS

A. Claim Interpretation

Consistent with the statute and legislative history of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), the Board interprets claims using the “broadest reasonable construction in light of the specification of the patent in which [they] appear[.]” 37 C.F.R. § 42.100(b); *see also* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). There is a “heavy presumption” that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). However, a “claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history.” *Id.* “Although an inventor is indeed free to define the specific terms used to describe his or her invention, this must be done with reasonable clarity, deliberateness, and precision.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Also, we must be careful not to read a particular embodiment appearing in the written description into the claim if the claim language is broader than the embodiment. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (“limitations are not to be read into the claims from the specification”).

1. “Inside Surface” and “Inside the Integrated Circuit Package”

Independent claims 1 and 9 recite an integrated circuit package having an array of landing pads disposed on an “inside surface” of the package and an array of solder balls disposed on an “outside surface” of the package. The claims further recite a structure (an “interposing structure” in claim 1

and a “means for electrically coupling” in claim 9) that is disposed “inside the integrated circuit package” between the inside surface of the package and an integrated circuit die.

In the Decision on Institution, based on the arguments presented by IVM in its Petition and by Xilinx in its Preliminary Response, we interpreted the phrase “array of landing pads disposed on an inside surface of the integrated circuit package” in claims 1 and 9 to mean that the integrated circuit package has at least two surfaces (one facing in and one facing out) and that the array of landing pads is located on the surface facing in. Dec. on Inst. 8-11. We did not interpret the claim language as requiring the integrated circuit package to “completely surround” the integrated circuit die and landing pads, as Xilinx had argued in its Preliminary Response. *Id.* Rather, we concluded that, as ordinarily understood, “the fact that a structure has something on its ‘inside surface’ does not mean that the structure completely surrounds that thing (or any other thing).” *Id.* at 9. “For example, a box with its top off has an ‘inside surface’ and may have an object on that surface, even though it does not completely surround the object.” *Id.* IVM agrees with the Board’s interpretation; Xilinx does not.

Xilinx first argues that the term “inside,” and the broader phrases in which it appears in the claims, are understood readily and do not require interpretation. PO Resp. 2-3. We conclude that interpretation is necessary under the circumstances, particularly because there is a disagreement between the parties as to whether the “inside” limitations require complete surrounding or encapsulation by the integrated circuit package, as explained below.

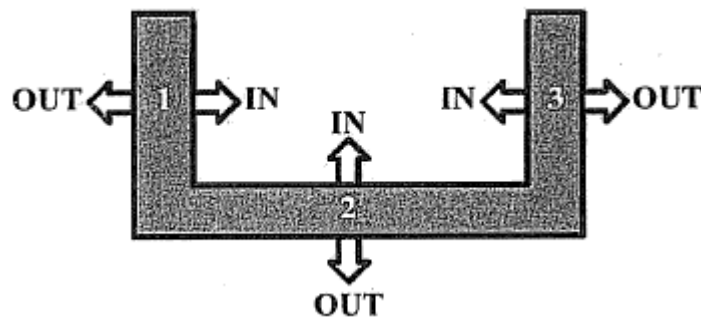
Xilinx further proposes that, if interpretation of the “inside” claim limitations is deemed necessary, the term “inside” should be interpreted to mean “within,” and the term “inside surface” should be interpreted to mean a “surface within.” *Id.* at 2, 6-9. It is evident from Xilinx’s Patent Owner Response, however, that Xilinx imparts a further meaning to the word “within”—namely, that an object “within” another structure is one that is “completely surrounded by” or “encapsulated within” that structure. *See id.* at 4, 6-8 (arguing that the Specification of the ’960 patent “uses ‘inside’ repeatedly to describe components encapsulated within, and completely surrounded by, the integrated circuit package,” and that the applicant “explained [during prosecution] that ‘inside’ means ‘completely surrounded’ or ‘within’”). As such, Xilinx’s position appears to be that the interposing structure in claim 1 and the means for electrically coupling in claim 9, which are disposed “inside” the integrated circuit package, must be completely surrounded by or encapsulated within the integrated circuit package. We do not agree that this is the broadest reasonable interpretation of the claims in light of the Specification.

Ordinary Meaning of “Inside”

“Inside” is used in the claims both as an adjective (“inside surface”) and as a preposition (“inside the integrated circuit package”). One dictionary defines the adjective “inside” as “situated or being on or in the inside; interior; internal: *an inside seat*,” and the preposition “inside” as “on the inner side or part of; within: *inside the circle; inside the envelope*.” RANDOM HOUSE WEBSTER’S UNABRIDGED DICTIONARY 986 (2d ed. 2001) (Ex. 3002). Thus, Xilinx is correct that, at least in some circumstances,

“inside” is synonymous with “within” (and also synonymous with “interior,” “inner,” and “internal”). See PO Resp. 6-9. Xilinx, however, does not point to evidence in the record indicating that “within,” as the term ordinarily is understood, means something that is completely surrounded by or encapsulated within another structure. Indeed, the dictionary examples above suggest just the opposite. A building with its door open may have an “inside seat,” and an unsealed envelope may have a letter “inside the envelope.” See Ex. 3002.

This ordinary understanding is consistent with the box analogy discussed in the Decision on Institution. An object may be “inside” a box, situated on the box’s “inside surface,” even though the box has its top off, and, therefore, does not completely surround the object. See Dec. on Inst. 9. Xilinx contends that the box analogy leads to ambiguity because any surface may be considered “facing in” or “facing out” depending on the perspective from which it is viewed. PO Resp. 4-5. We do not agree. As IVM points out, whether a surface of the integrated circuit package faces in or out is viewed from the perspective of the overall package itself (which may have objects inside it). See Pet. Reply 5-6. IVM provides the following illustrative figure on page 6 of its Reply.



IVM’s figure above shows a box with three sides (1, 2, and 3), each with a surface that faces in from the box (an “inside surface”) and a surface that

faces out from the box (an “outside surface”). Thus, the box analogy is not ambiguous and is consistent with the dictionary definitions of “inside” cited above. The analogy also is consistent with the language of the claims themselves, which recite the integrated circuit package having something disposed “inside” it, and objects on its “inside surface” and “outside surface,” but do not have any limitations that would imply a complete surrounding or encapsulation requirement. Thus, we do not agree with Xilinx that the ordinary and customary meaning of the “inside” claim limitations requires complete surrounding or encapsulation.

Specification of the '960 Patent

Xilinx argues that the Specification of the '960 patent uses the term “inside” to refer to “components encapsulated within, and completely surrounded by, the integrated circuit package.” PO Resp. 6-8. Xilinx cites the following statement in the Specification: “[v]arious embodiments are now disclosed in which caposers are *disposed inside* an IC package *as opposed to being disposed outside* the IC package between the package and a printed circuit board.” *Id.* at 7 (citing Ex. 1001, col. 10, ll. 47-50) (emphasis by Xilinx). We agree with Xilinx that the Specification distinguishes objects “inside” a structure from objects “outside” a structure. That does not mean necessarily, however, that an object must be completely surrounded by the structure to be inside the structure. Again, an object may be inside another structure and still be distinct from something outside that structure.

Xilinx also relies on Figures 10 and 24 of the '960 patent. Xilinx points to statements in the Specification that, in Figure 24, caposer 1082 is

“inside” and “within” integrated circuit package 1084. *Id.* at 7-8 (citing Ex. 1001, col. 17, ll. 45-48, col. 18, ll. 42-43). Figures 10 and 24, however, are merely exemplary embodiments of the invention. *See, e.g.*, Ex. 1001, col. 6, ll. 13-15, 47-48; col. 11, ll. 9-11; col. 17, ll. 44-48. We do not see, and Xilinx does not point to, sufficient language in the Specification indicating that the patentee was defining the term “inside” to mean complete surrounding of one structure by another. For instance, although Figure 10 depicts ceramic package 1012 surrounding caposer 1018, the written description of the ’960 patent does not state explicitly that the caposer in the disclosed embodiments is surrounded by or encapsulated within the integrated circuit package. We also note that Figure 24, unlike Figure 10, does *not* depict caposer 1082 as completely surrounded by integrated circuit package 1084. Rather, caposer 1082 is shown below die 1083 and above an inside surface of integrated circuit package 1084, with nothing shown on the sides of caposer 1082. Thus, we do not view Figures 10 and 24, and their corresponding descriptions, as supportive of Xilinx’s proposed interpretation.

Prosecution History of the ’960 Patent

Both parties rely on the prosecution history of the ’960 patent in their arguments regarding the proper interpretation of the “inside” claim limitations. *See* PO Resp. 8-9; Pet. Reply 2-4.

Xilinx cites the following statement made by the applicant during prosecution of the ’960 patent:

The Applicant refers the Examiner to FIG. 10, which shows a die 1011 inside a package 1012. The package 1012 completely surrounds the die 1011, and hence the die 1011 is

inside the package 1012. Further[,] Applicant's specification states "[a]n integrated circuit die 1011 is mounted within an integrated circuit package 1012." (Applicant's specification, para. 0089).

Ex. 2001 at 31; *see* PO Resp. 8. According to Xilinx, this indicates that the applicant meant "inside" to mean "completely surrounded" or "within." PO Resp. 8-9.

As explained in the Decision on Institution, we do not view the cited statement as an explicit definition of the claim language or an express and clear disclaimer of a broader definition. *See* Dec. on Inst. 10-11; *In re Trans Texas Holdings Corp.*, 498 F.3d 1290, 1298 (Fed. Cir. 2007) (finding "nothing in the specification or the prosecution history that requires" a particular narrower interpretation proposed by a patent owner in a reexamination proceeding); *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004) ("Absent claim language carrying a narrow meaning, the PTO should only limit the claim based on the specification or prosecution history when those sources expressly disclaim the broader definition."). Also, the cited statement refers to the relationship between die 1011 and package 1012, and was made in response to a 35 U.S.C. § 112 rejection to show that the claims are "clear and definite." Ex. 2001 at 31-32. According to the applicant, the statement specifically responds to the Examiner's request that the applicant "explain the claimed structure as it relates to the drawings and specification." *Id.*; *see also id.* at 39 (Office Action with 35 U.S.C. § 112 rejection). The statement, therefore, describes related structure in the "drawings and specification." *See* Ex. 2001 at 31-32, 39. It does not represent a limit on the claims or a disavowal of claim scope. As another example, the applicant vaguely explains that "one skilled in the art would

understand that a die and interposing structure *can be* positioned within or inside [a] surrounding structure, such as an integrated circuit package.” *Id.* at 31 (emphasis added). This statement of what “can be” included within the claim scope can be read as an attempt to maintain a reasonably broad scope that would encompass other (i.e., non-surrounding integrated circuit package) structures.

Moreover, Xilinx’s argument that the prosecution history limits the claims is contradicted by another statement in the prosecution history. During prosecution, the Examiner rejected claim 1 and claim 12 (which became issued claim 9) as anticipated by Chakravorty ’362, citing Figure 2 of Chakravorty ’362. *Id.* at 126-39. Figure 2 of Chakravorty ’362 is reproduced below.

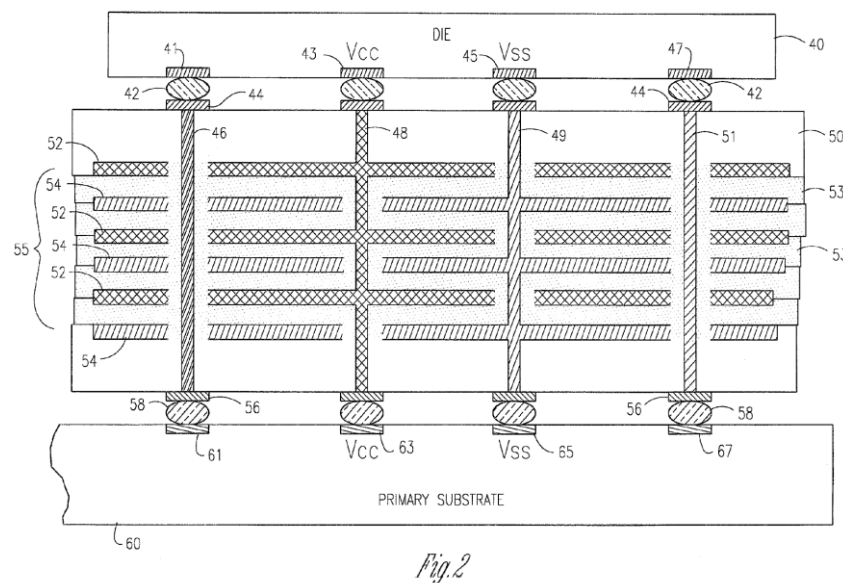


Figure 2 depicts solder bumps 58 on top of primary substrate 60. Ex. 1007, col. 4, ll. 64-66. During prosecution of the ’960 patent, the applicant argued the following as to Chakravorty ’362:

The bumps (58) of the primary substrate in Chakravorty are disposed on the *inside surface* thereof, not the outside

surface. In particular, the Examiner cited the landing pads (61-67) on the primary substrate as being an “array of landing pads disposed on an inside surface of the integrated circuit package.” (Office Action, p. 4). Since these landing pads are coupled to the bumps (58), the bumps (58) of Chakravorty are on the *inside* of the substrate, not the outside.

Ex. 2001 at 121 (emphasis added).² Thus, the applicant took the position during prosecution that solder bumps 58 in Chakravorty ’362 are on an “inside surface” of, and “inside,” primary substrate 60, even though Figure 2 does not depict primary substrate 60 as completely surrounding or encapsulating solder bumps 58. This position is in line with the other statements discussed above showing that the applicant did not intend to limit the claims during prosecution, and contrary to Xilinx’s current position that “inside” requires complete surrounding or encapsulation. See PO Resp. 8-9, 10-11 (arguing that interposer 310 in Figure 3 of Chakravorty ’362 is not “inside” the primary substrate), 11-13 (making a similar argument as to Siniaguine).

We are not persuaded by Xilinx’s arguments regarding the prosecution history of the ’960 patent. At best, the statements cited above are inconsistent, and do not indicate that the applicant was disclaiming a broader definition of the “inside” claim limitations as Xilinx contends.

² Notably, the applicant was able to overcome the Examiner’s rejection based on Chakravorty ’362 by arguing that the reference does not disclose an “array of solder balls disposed on an outside surface of the integrated circuit package.” See Ex. 2001 at 101-10, 121-22. IVM asserts, and Xilinx does not dispute, that this limitation is taught by Siniaguine. See Pet. 29-30, 40-41.

Other Evidence

Xilinx also relies on the declaration of Dean Neikirk, Ph.D. (Exhibit 2007) in support of its proposed interpretation. PO Resp. 9. Dr. Neikirk testifies that the purpose of an integrated circuit package is to “encapsulate and protect the fragile circuitry of an integrated circuit die” from potentially destructive substances and physical damage during manufacturing and use. Ex. 2007 ¶ 25. Therefore, according to Dr. Neikirk, a structure “inside” an integrated circuit package must be “within” the package. *Id.* We give Dr. Neikirk’s testimony little weight as to this point, as it is not supported by evidence in the record and is not tied to the actual language of the claims. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”). Further, the fact that there may be benefits to completely surrounding or encapsulating a structure in an integrated circuit package does not mean necessarily that the “inside” claim limitations should be interpreted to require such a structure. We see no reason why the claimed assemblies would require complete surrounding or encapsulation to function.

Conclusion

Applying the broadest reasonable interpretation of the claims in light of the Specification, we interpret “inside surface” to mean the surface of the integrated circuit package facing in from the package toward the integrated circuit die (as opposed to the “outside surface,” which is the surface of the package facing outward from the package away from the integrated circuit die). We also interpret “inside the integrated circuit package” to mean on the inner part of the integrated circuit package that faces in from the package

toward the integrated circuit die. We do not interpret the claims as requiring the interposing structure (claim 1) or means for electrically coupling (claim 9) to be completely surrounded by or encapsulated within the integrated circuit package.

2. Other Terms

In the Decision on Institution, we interpreted three other claim terms as follows:

Term	Interpretation
micro-bump (claims 1 and 9)	a small bump of electrically conductive material, such as solder
means for electrically coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed opposite the first position and to a second landing pad located in a different position in the array of landing pads (claim 9)	Function: “electrically coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed opposite the first position and to a second landing pad located in a different position in the array of landing pads” Corresponding structure: caposer 1082

Term	Interpretation
means for electrically coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed opposite the first position and to a second landing pad located in a different position in the array of landing pads [and] for providing a bypass current to the integrated circuit die (claim 10)	Functions: “electrically coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed opposite the first position and to a second landing pad located in a different position in the array of landing pads and providing a bypass current to the integrated circuit die” Corresponding structure: caposer 1082

Dec. on Inst. 11-14. Neither party disputes these interpretations, and we apply them in this decision, for the reasons stated in the Decision on Institution.

B. Claims 1-5, 7-11, and 13 are Unpatentable Over Chakravorty '362 and Siniaguine

With respect to the alleged obviousness of claims 1-5, 7-11, and 13 over Chakravorty '362 and Siniaguine, we have reviewed IVM's Petition, Xilinx's Patent Owner Response, and IVM's Reply, as well as the evidence discussed in each of those papers. We are persuaded, by a preponderance of the evidence, that claims 1-5, 7-11, and 13 are unpatentable over Chakravorty '362 and Siniaguine under 35 U.S.C. § 103(a). *See* Pet. 28-36; Ex. 1002 ¶¶ 65-81.

Xilinx's sole argument regarding the asserted ground is that Chakravorty '362 does not teach “an interposing structure disposed inside

the integrated circuit package,” as recited in independent claim 1.³ PO Resp. 9-11. For the reasons explained below, Xilinx’s argument is not persuasive.

Chakravorty ’362 is directed to an “electronic assembly that includes an interposer having one or more embedded capacitors to reduce switching noise in a high-speed integrated circuit, and to manufacturing methods related thereto.” Ex. 1007, col. 1, ll. 17-21. Figure 3 of Chakravorty ’362 is reproduced below.

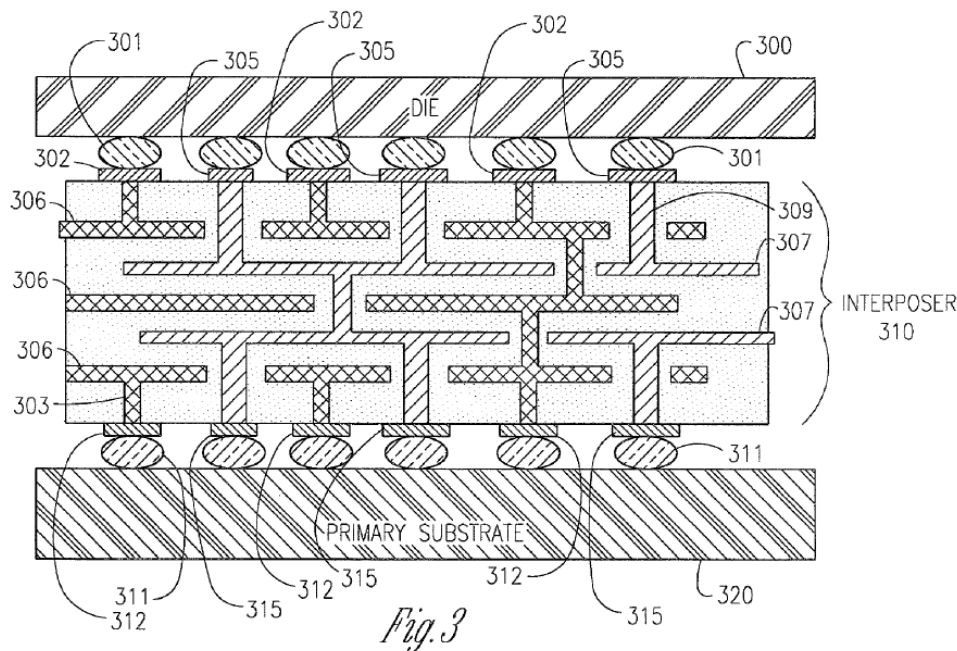


Figure 3 depicts an assembly comprising integrated circuit (IC) die 300, solder balls 301, lands 302, interposer 310 (with embedded capacitors), lands 312, solder balls 311, and primary substrate 320. *Id.* at col. 5, ll. 30-60. IVM identifies IC die 300 as the claimed “integrated circuit die,” primary substrate 320 as the claimed “integrated circuit package,” and

³ Although Xilinx does not address specifically the language of the other independent claim, claim 9, which recites a “means for electrically coupling . . . disposed inside the integrated circuit package,” Xilinx’s argument regarding the “inside” limitation presumably applies to both claims. See PO Resp. 9-12.

interposer 310 as the claimed “interposing structure” of claim 1 and “means for electrically coupling” of claim 9. Pet. 28-30, 33-35. According to IVM, interposer 310 is disposed “inside” primary substrate 320 between the inside surface of the substrate and IC die 300.⁴ *Id*; see Ex. 1002 ¶ 70.

Xilinx argues that interposer 310 is “outside,” not “inside,” primary substrate 320. PO Resp. 9-10. As explained above, however, “inside surface” means the surface of the integrated circuit package facing in from the package toward the integrated circuit die, and “inside the integrated circuit package” means on the inner part of the integrated circuit package that faces in from the package toward the integrated circuit die. *See supra* Section II.A.1. Although interposer 310 is not shown in Figure 3 as completely surrounded by or encapsulated within primary substrate 320, such surrounding or encapsulation is not required by the claims. *See id*. The inside surface of primary substrate 320 is the top of the substrate shown in Figure 3, which has signal terminals/bumps immediately below solder balls 311. *See* Ex. 1007, col. 4, ll. 15-21; col. 5, ll. 20-25; Figs. 2-3. This surface faces in from primary substrate 320 toward IC die 300, in contrast to the bottom of the substrate shown in Figure 3, which faces outward away from IC die 300. Interposer 310 is disposed between the inside surface of primary substrate 320 and IC die 300. The area in which interposer 310 is located is the *inner part* of primary substrate 320. We also note that Figure 3 depicts

⁴ Xilinx contends that IVM is inconsistent in arguing that interposer 310 is “between” primary substrate 320 and IC die 300, and also “inside” primary substrate 320. PO Resp. 10-11 (citing Pet. 30). We do not view IVM’s position as inconsistent. Something (e.g., interposer 310) can be “inside” a structure (e.g., primary substrate 320) and, at the same time, be between the “inside surface” of the structure and another structure (e.g., IC die 300). *See, e.g.*, Ex. 1001, Fig. 10; Ex. 1007, Fig. 3.

interposer 310 with space on either side, such that its length is within the outer bounds of primary substrate 320.

Further, as explained above, Xilinx's position as to what is "inside" an integrated circuit package and what is not is contradicted by arguments the applicant made during prosecution. Specifically, the applicant characterized solder bumps 58 in Figure 2 of Chakravorty '362 as "inside" primary substrate 60, but Xilinx now argues that interposer 310 in Figure 3 is not "inside" primary substrate 320. *See* Ex. 2001 at 121; PO Resp. 9-10. We see no difference between the two. Solder bumps 58 and interposer 310 both are depicted in Chakravorty '362 as above, and within the boundaries of, the substrate. Thus, just as the applicant considered solder balls 58 to be "inside" the substrate, so too is interposer 310. We are persuaded, by a preponderance of the evidence, that Chakravorty '362 teaches "an interposing structure disposed inside the integrated circuit package."

We also are persuaded that, even if the claim term "inside" is interpreted as Xilinx suggests to require complete surrounding or encapsulation of the interposer within the integrated circuit package, the feature would have been obvious based on the teachings of Chakravorty '362 and Siniaguine. *See* PO Resp. 2-9; Pet. Reply 8-9.

Chakravorty '362 discloses that "[i]ntegrated circuits (ICs) are typically assembled into packages by physically and electrically coupling them to a substrate made of organic or ceramic material." Ex. 1007, col. 1, ll. 25-27. The reference further states that the disclosed assemblies may be used in one particular type of package called "controlled collapse chip connect" (C4), or "flip chip," in which the "electrically conductive terminations or lands . . . of an IC component are soldered directly to

corresponding lands on the surface of the substrate using reflowable solder bumps or balls.” *See id.* at col. 2, ll. 3-10; col. 10, ll. 8-11. IVM’s declarant, Morgan T. Johnson, testifies that, based on the disclosure of Chakravorty ’362, interposer 310 and primary substrate 320 would be subject to the effects of high thermal coefficient of expansion (HITCE) manufacturing, and would require an “underfill encapsulant” in the C4 package to mitigate such effects. Ex. 1011 ¶ 22 (citing Ex. 1007, col. 4, ll. 1-3, col. 7, ll. 42-46). As support, Mr. Johnson cites a textbook on chip design, which states that “[o]ne of the major reasons why solder-bumped flip chip on low-cost organic [chip scale package (CSP)] substrates works is because of the underfill epoxy encapsulant,” and describes various advantages of using underfill encapsulants in C4 packages. Ex. 1014 at 19; *see* Ex. 1011 ¶ 22. According to Mr. Johnson, an underfill encapsulant would fill in the areas between solder balls 301 and the areas between solder balls 311 in the assembly shown in Figure 3 of Chakravorty ’362, surrounding interposer 310 inside the C4 package. Ex. 1011 ¶¶ 22-23.

Similarly, Siniaguine discloses a ball grid array (BGA) integrated circuit package with underfill around an interposer. Ex. 1004, col. 7, ll. 61-66. Figure 12 of Siniaguine is reproduced below.

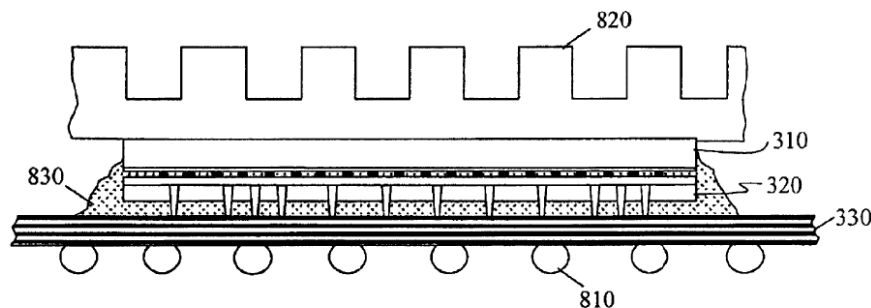


FIG. 12

As shown in Figure 12, underfill 830 surrounds interposer 320 and fills in the area between interposer 320 and wiring substrate 330. *Id.* According to Mr. Johnson, the underfill in Siniaguine serves a similar purpose to the underfill that would be used in Chakravorty '362. Ex. 1011 ¶¶ 25-26.

The disclosures of Chakravorty '362 and Siniaguine, as well as the chip design textbook cited by Mr. Johnson (Exhibit 1014), support Mr. Johnson's testimony. Accordingly, Mr. Johnson's testimony regarding the use of underfill in Chakravorty '362 and Siniaguine is entitled to substantial weight. Based on the teachings of the references, it would have been obvious to a person of ordinary skill in the art to have an integrated circuit package that completely surrounds or encapsulates an interposer, such as interposer 310 in Chakravorty '362, with underfill. Thus, even if the claim term "inside" is given Xilinx's proposed interpretation, independent claims 1 and 9 still would have been obvious over Chakravorty '362 and Siniaguine.

Based on the record evidence, in light of the arguments presented, IVM has shown, by a preponderance of the evidence, that claims 1 and 9, as well as claims 2-5, 7, 8, 10, 11, and 13 depending therefrom, would have been obvious over the combination of Chakravorty '362 and Siniaguine.

*C. Claims 1-5, 7-11, and 13 are Unpatentable Over
Siniaguine, Ma, and Chakravorty '362*

With respect to the alleged obviousness of claims 1-5, 7-11, and 13 over Siniaguine, Ma, and Chakravorty '362, we have reviewed IVM's Petition, Xilinx's Patent Owner Response, and IVM's Reply, as well as the evidence discussed in each of those papers. We are persuaded, by a preponderance of the evidence, that claims 1-5, 7-11, and 13 are

330 as the claimed “integrated circuit package,” and interposer 320 as the “interposing structure” of claim 1 and “means for electrically coupling” of claim 9. Pet. 38-42, 47-48. According to IVM, interposer 320 is disposed “inside” wiring substrate 330 between the inside surface of the substrate (with pads 388) and integrated circuit 310. *Id*; Ex. 1002 ¶ 90; *see* Ex. 1004, col. 3, ll. 39-41 (“integrated circuit 310 mounted on another integrated circuit 320 which in turn is mounted on a wiring substrate 330”).

Similar to its argument regarding Chakravorty ’362, Xilinx contends that the top surface of wiring substrate 330 (shown in Figures 4 and 12 of Siniaguine) with pads 388 is an “outside surface,” not an “inside surface,” of the package, and interposer 320 is not “inside” wiring substrate 330. PO Resp. 11-13; *see* Ex. 2007 ¶¶ 35, 39. We do not agree. The top surface of wiring substrate 330 (with pads 388 for making a connection with interposer 320) faces in from the substrate toward integrated circuit 310, in contrast to the bottom of the substrate (with solder balls 810), which faces out. Like the interposer in Chakravorty ’362, the area in which interposer 320 is located is the *inner part* of wiring substrate 330, and Figures 4 and 12 depict interposer 320 with space on either side, within the outer bounds of wiring substrate 330. This is consistent with an interposer being “inside” a substrate, as the applicant argued during prosecution. *See* Ex. 2001 at 121. Thus, we are persuaded, by a preponderance of the evidence, that Siniaguine teaches “an interposing structure disposed inside the integrated circuit package” and “an array of landing pads disposed on an inside surface of the integrated circuit package.”

Further, as explained above, even if the claim term “inside” is interpreted to require complete surrounding or encapsulation of the

interposer within the integrated circuit package, the feature would have been obvious based on the teachings of Siniaguine and Chakravorty '362. *See supra* Section II.B. In particular, Figure 12 of Siniaguine depicts underfill surrounding interposer 320 in a BGA integrated circuit package. Ex. 1004, col. 7, ll. 61-66; Fig. 12.

Second, Xilinx argues that Ma does not teach an array of micro-bumps on a surface of an integrated circuit die in a first pattern, and an array of landing pads disposed on an inside surface of an integrated circuit package in a second pattern, where the first and second patterns are “substantially identical,” as recited in independent claims 1 and 9. PO Resp. 13-15.

Ma is directed to “packaging technology that encapsulates a microelectronic die with an encapsulation material.” Ex. 1008, col. 1, ll. 10-14. In discussing the prior art, Ma describes a prior art package that has an interposer. *Id.* at col. 1, ll. 31-47. Figure 18 of Ma is reproduced below.

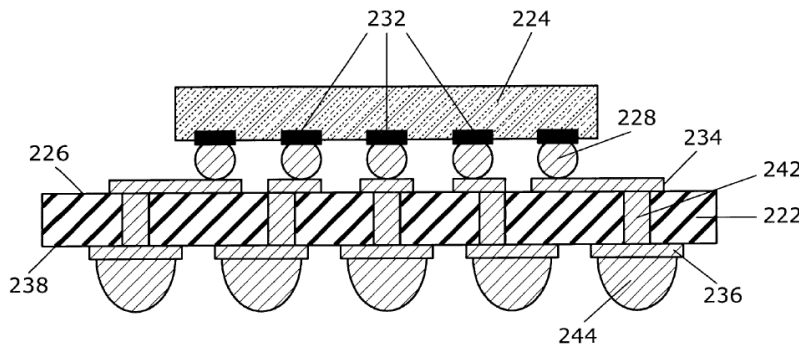


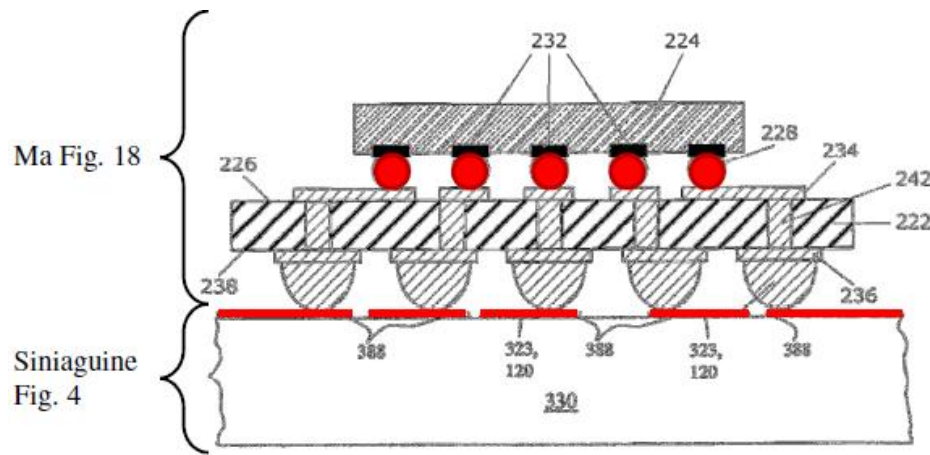
FIG. 18
PRIOR ART

Figure 18 depicts microelectronic die 224, solder balls 228 in a pattern, substrate interposer 222, and external contacts 244 (e.g., solder balls) in a

pattern. *Id.* “[E]xternal contacts 244 are utilized to achieve electrical communication between the microelectronic die 224 and an external electrical system (not shown).” *Id.* at col. 1, ll. 45-47. IVM relies on the teachings of Ma in support of its argument that it would have been a simple modification to Siniaguine to make “the first pattern of micro-bumps disposed on IC 310 in FIG. 4 of Siniaguine . . . have a substantially identical pattern as the second pattern of pads 388 disposed on wiring substrate 330 as taught by Ma.” Pet. 41-42. Further, according to IVM, solder balls 228 in Figure 18 of Ma and pads 388 in Figure 4 of Siniaguine both are in a “1 x N array, where N is an integer greater than 1,” and, therefore, have substantially identical patterns. *Id.*

Xilinx argues that IVM presents no evidence, only attorney argument, as to why a person of ordinary skill in the art would have combined the teachings of Siniaguine and Ma. PO Resp. 13-14. In its Petition, however, IVM relied on Mr. Johnson, who testified that the proposed “substitution can be applied using known packaging techniques and would not change the operation of the semiconductor integrated circuit structure of Siniaguine. Rather, the substitution would provide *flexibility in the signal distribution* between IC 310 and wiring substrate 330 of Siniaguine.” Ex. 1002 ¶ 89 (emphasis added); see Pet. 41-42. Xilinx does not explain why this analysis is incorrect. Mr. Johnson’s testimony is entitled to substantial weight, and we conclude that IVM has shown “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” See *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417-18 (2007) (citation omitted).

Xilinx also asserts that the combination of Siniaguine and Ma does not teach “substantially identical” patterns because the pattern of solder balls 228 in Ma is not substantially identical to the pattern of pads 388 in Siniaguine. PO Resp. 14-15 (citing Ex. 2007 ¶ 46). Xilinx provides, on page 15 of its Patent Owner Response, a figure combining Figure 18 of Ma and Figure 4 of Siniaguine.



Annotated Combination of Ma Fig. 18 and Siniaguine Fig. 4

According to Xilinx, solder balls 228 in Ma are “regularly spaced apart,” whereas pads 388 in Siniaguine are “irregularly spaced apart,” such that the two do not line up together. *Id.* at 15.

We are persuaded, by a preponderance of the evidence, that Siniaguine and Ma teach the “substantially identical” limitation of claims 1 and 9. Xilinx’s argument is based on a physical combination of one portion of an assembly in one reference with that of another reference, which is not a proper method for analyzing obviousness. Rather, we must consider what the references as a whole would have taught to a person of ordinary skill in the art, recognizing that it is often necessary and within the level of ordinary skill to modify the teachings of two references in order to combine them. *See In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (“It is

well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements.”); *In re Keller*, 642 F.2d 413, 425 (CCPA 1981) (“The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.”). Moreover, Xilinx does not point to any indication in the references that the figures are drawn to scale, either individually or together, such that combining them in the manner proposed by Xilinx would make sense. *See Hockerson-Halberstadt, Inc., v. Avia Group Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue”).

Considering the references as a whole, we are persuaded that a person of ordinary skill in the art would have found it obvious to modify the patterns in Siniaguine to be substantially identical. Xilinx does not dispute that the assembly in Figure 18 of Ma has five solder balls 228 in a substantially identical pattern to five external contacts 244, which are designed to contact an “external electrical system” (e.g., a wiring substrate). *See Ex. 1008*, col. 1, ll. 31-47. Siniaguine discloses such a wiring substrate, with pads 388 in a pattern on its inside surface. *See Ex. 1004*, col. 3, l. 39-col. 4, l. 38. Further, the fact that external contacts 244 in Ma and pads 388 in Siniaguine themselves have similar (although not identical) patterns (i.e., 1 x 5 arrays) would have indicated to a person of ordinary skill in the art that the references’ teachings could have been combined to create reliable

connections. We agree with IVM that it would have been a simple modification to Siniaguine, within the skill of an ordinarily skilled artisan, to have the micro-bumps below integrated circuit 310 in Figure 4 of Siniaguine in a “substantially identical” pattern to pads 388, just as the patterns of solder balls 228 and external contacts 244 in Ma are substantially identical.

Finally, we note that, regardless of whether Siniaguine and Ma teach “substantially identical” patterns, Xilinx does not dispute that Chakravorty ’362 teaches such patterns. See Pet. 28-29. Thus, although IVM relies on Chakravorty ’362’s patterns only for its asserted ground based on the combination of Chakravorty ’362 and Siniaguine, *see supra* Section II.B, we see no reason why a person of ordinary skill in the art would not have looked to Chakravorty ’362’s patterns for the proposed combination of Siniaguine, Ma, and Chakravorty ’362 as well.

Third, Xilinx asserts that modifying Siniaguine to use “substantially identical” patterns, as allegedly suggested by Ma, would render the assembly of Siniaguine inoperable for its intended purpose. PO Resp. 16-18. Specifically, Xilinx contends that the purpose of interposer 320 in Siniaguine is to implement a clock distribution network for die 310, where a single clock input signal is distributed to numerous terminals and circuit blocks. *Id.* (citing Ex. 1004, col. 1, ll. 12-16, Fig. 1). According to Xilinx and its declarant, Dr. Neikirk, “[f]or Siniaguine’s clock distribution interposer to work, it necessarily must have . . . more outputs than inputs,” and, therefore, Siniaguine’s assembly would not work if it was modified to use “substantially identical” patterns. *Id.* at 17-18 (citing Ex. 2007 ¶ 44). As support for its argument, Xilinx cites Figures 4 and 15C of Siniaguine, which depict more outputs than inputs. *Id.* at 16-17.

We are not persuaded that Siniaguine would be rendered inoperable for its intended purpose if it was modified to have the micro-bumps below integrated circuit 310 and pads 388 in “substantially identical” patterns. Xilinx does not point to evidence in Siniaguine—and we do not find any—indicating that every interposer in the disclosed clock distribution network must have more clock outputs than inputs. Indeed, an interposer with one input and one output is capable of *distributing* a received clock signal to one other component. Siniaguine also states that the clock distribution network can be of “any type,” and is not limited to the tree-like structure shown in Figure 1. Ex. 1004, col. 3, ll. 47-49.

Further, as IVM points out, the clock distribution network in Siniaguine need not be implemented entirely in interposer 320; some of the network connections may be made via integrated circuit 310. *See id.* at col. 5, ll. 54-58; Pet. Reply 13-14. Thus, if only some of the connections in a tree-like clock distribution network, as shown in Figure 1, are made via interposer 320, the clock inputs and outputs would not be equal necessarily.

We also note that Siniaguine is not limited to the distribution of clock signals. Siniaguine expressly states that “[t]he invention is not limited to any particular signals that can be routed through interposer 320.” Ex. 1004, col. 4, ll. 34-35. For example, in the embodiment depicted in Figure 4, contact pad 323.1 is a power supply input, contact pad 323.3 is a ground input, and contact pad 323.2 may be an input or an output. *Id.* at col. 4, ll. 28-34. Given the fact that pads 388 need not be used solely for clock signaling, and the fact that the Siniaguine interposer is capable of any other signal routing—not just clock inputs and outputs—we see no reason why the

disclosed interposer would not work if it had an equal number of micro-bumps below integrated circuit 310 and pads 388.

Based on the record evidence, in light of the arguments presented, IVM has shown, by a preponderance of the evidence, that claims 1 and 9, as well as claims 2-5, 7, 8, 10, 11, and 13 depending therefrom, would have been obvious over the combination of Siniaguine, Ma, and Chakravorty '362.

D. Claims 6 and 12 are Unpatentable Over Chakravorty '362, Siniaguine, and Patel, and Also Unpatentable Over Siniaguine, Ma, Chakravorty '362, and Patel

In its Patent Owner Response, Xilinx does not argue any additional limitations recited in claims 6 and 12, and instead relies on its arguments as to independent claims 1 and 9. PO Resp. 12, 18. Based on IVM's allegations regarding claims 6 and 12 in its Petition, and the testimony of Mr. Johnson, we are persuaded, by a preponderance of the evidence, that claims 6 and 12 are unpatentable under 35 U.S.C. § 103(a) based on both of the grounds on which a trial was instituted as to these claims: (1) the combination of Chakravorty '362, Siniaguine, and Patel, and (2) the combination of Siniaguine, Ma, Chakravorty '362, and Patel. See Pet. 36-37, 50-51; Ex. 1002 ¶¶ 82-83, 104-105.

E. Xilinx's Second Substitute Motion to Amend

In its Second Substitute Motion to Amend, Xilinx proposes substitute claims 14-21, "contingent upon a Board determination that Claim 1 is unpatentable," and substitute claims 22-26, "contingent upon a Board determination that Claim 9 is unpatentable." Second Subst. Mot. to Amend

1. We determine that claims 1 and 9 are unpatentable and, therefore, reach the merits of Xilinx's motion.

As the moving party, Xilinx bears the burden of proof to establish that it is entitled to the relief requested. 37 C.F.R. § 42.20(c). Entry of the proposed amendments is not automatic, but only upon Xilinx's having demonstrated the patentability of those claims.

Proposed substitute claims 14 and 22 include all of the limitations of claims 1 and 9, respectively, and add new limitations. Second Subst. Mot. to Amend. 2-5. Claim 14 adds the limitations that the interposing structure comprises a "plurality of tiled interposing structures," and the plurality of tiled interposing structures is "held together using an elastomer." *Id.* at 2-3. Claim 22 similarly adds the limitations that the means for electrically coupling comprises a "plurality of tiled interposing structures electrically coupling the array of landing pads and the array of solder balls," and the plurality of tiled interposing structures is "held together using an elastomer." *Id.* at 4-5. Proposed substitute dependent claims 15-21 and 23-26 are identical to dependent claims 2-8 and 10-13, but for a change in dependency to proposed substitute independent claims 14 and 22. *Id.* at 3-6.

1. Compliance with the Idle Free Decision

As an initial matter, IVM argues that Xilinx's motion should be denied because the Board permitted Xilinx to file a second substitute motion to amend for "the sole purpose of complying with the *Idle Free* decision," but Xilinx's motion goes beyond what was needed to comply with that decision. Opp. 1-4; see Paper 24. We need not reach this procedural issue,

however, because we deny Xilinx's motion on the merits for the reasons explained below.

2. Written Description Support

In its motion, Xilinx explains how the subject matter of its proposed substitute claims have written description support in the specification of U.S. Patent Application No. 10/698,704 ("the '704 application"), which issued as the '960 patent, as filed. Second Subst. Mot. to Amend 6-13 (citing Ex. 2001). Regarding the added limitations of a plurality of tiled interposing structures held together using an elastomer, Xilinx relies on Figure 8 of the '704 application and its accompanying description, which disclose "smaller interposers" or "tiles" that are "combined together to form a single interposer device prior to mounting," and an elastomer being used to "hold the tiles together, thus forming the single interposer device." *Id.* at 7-9 (citing Ex. 2001 at 342). We conclude that Xilinx has made a sufficient showing that each of proposed substitute claims 14-26, as a whole, has written description support in the disclosure of the '704 application as filed, and turn to whether Xilinx has shown sufficiently that the claims are patentable.

3. Patentability Over the Prior Art

In its motion, Xilinx states that it is "not aware of any circuit die assembly prior art that discloses an interposer comprising 'a plurality of tiled interposing structures,'" and is not "aware of any circuit die assembly prior art that discloses a 'plurality of tiled interposing structures being held together using an elastomer.'" Second Subst. Mot. to Amend 14. Xilinx

contends that the closest prior art with respect to the proposed substitute claims is Chakravorty '362, Siniaguine, and Ma. *Id.* According to Xilinx and its declarant, Dr. Neikirk, these three references do not disclose the added limitations in proposed substitute claims 14 and 22, and a person of ordinary skill in the art would not have had reason to add such features to the assemblies of Chakravorty '362, Siniaguine, and Ma. *Id.* at 15-19 (citing Ex. 2008).

Xilinx also proposes interpretations for two of the terms in proposed substitute claims 14 and 22. *Id.* at 8-9, 12-13. Xilinx contends that “plurality of tiled interposing structures” means “a regular pattern of side by side interposing structures,” and “elastomer” means “a polymer with elastic properties resembling those of natural rubber.” *Id.* (citing Ex. 2008 ¶ 13, and a dictionary definition of “elastomer,” Ex. 2011). IVM does not dispute these interpretations, and we agree with Xilinx that they are reasonable in light of the Specification of the '960 patent.

We are not persuaded, however, that Xilinx has met its burden to show that proposed substitute claims 14 and 22 would have been nonobvious over the prior art. IVM, in opposing Xilinx's motion, cites the following additional prior art references:

1. U.S. Patent No. 6,002,168, issued Dec. 14, 1999 (Ex. 1018) (“Bellaar”); and
2. U.S. Patent No. 6,319,829 B1, issued Nov. 20, 2001 (Ex. 1017) (“Pasco”).

Opp. 10. IVM asserts that claims 14 and 22 are unpatentable over the following combinations of references: (1) Chakravorty '362, Siniaguine, Pasco, and Bellaar; and (2) Siniaguine, Ma, Chakravorty '362, Pasco, and

Bellaar.⁶ *Id.* at 10-15. IVM argues that Pasco and Bellaar, in combination, teach the added limitations in claims 14 and 22, and a person of ordinary skill in the art would have had reason to modify the assemblies described by the existing combinations of references to include the added limitations. *Id.* IVM's arguments are supported by the testimony of Mr. Johnson. See Ex. 1012 ¶¶ 37-45.

Pasco

Pasco is directed to a “semiconductor chip interposer for increasing fatigue life of interconnections by distributing [the] mismatch of thermal coefficient[s] of expansion between circuit components.” Ex. 1017, col. 1, ll. 62-65. Figure 4 of Pasco is reproduced below.

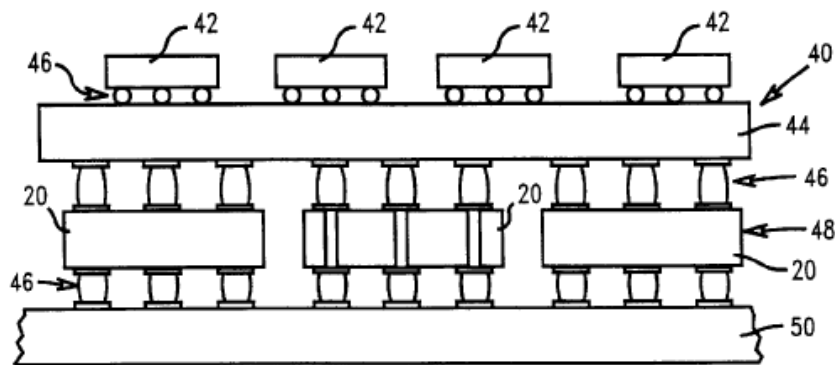


FIG. 4

Figure 4 depicts chips 42, substrate 44, solder balls 46, “segmented interposer 48 compris[ing] plural smaller area interposers 20,” and printed circuit board 50. *Id.* at col. 4, ll. 8-17. Interposers 20 provide for

⁶ IVM also cites a third reference, U.S. Patent No. 6,891,258 B1 (Ex. 1016), as allegedly teaching the added limitations. Opp. 5-6. We need not reach the merits of this argument, as we agree with IVM's arguments regarding Pasco and Bellaar.

interconnection (via solder balls 46) between substrate 44 and printed circuit board 50, and reduce the stress on the solder balls due to different thermal coefficients of expansion. *Id.* at col. 3, l. 56-col. 4, l. 17. Interposers 20 in Pasco are a “plurality of tiled interposing structures” (i.e., a regular pattern of side by side interposing structures).

Bellaar

Bellaar is directed to a “flexible chip carrier” having a chip and rigid and flexible interposers with different thermal coefficients of expansion. Ex. 1018, col. 2, l. 65-col. 3, l. 33. Figure 2 of Bellaar is reproduced below.

FIG. 2

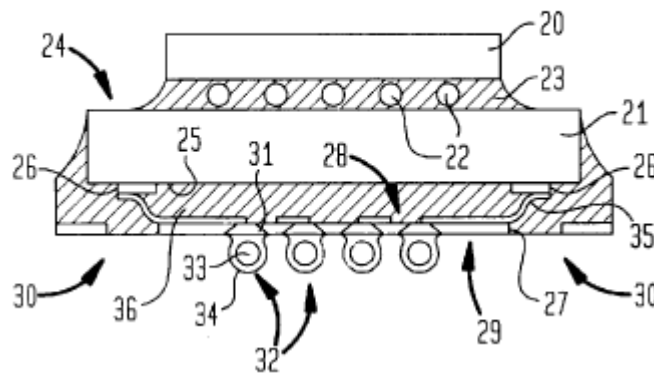


Figure 2 depicts semiconductor chip 20, solder balls 22, rigid interposer 21 with contacts 26, and flexible interposer 27 with flexible leads 35 for making contact with contacts 26. *Id.* at col. 9, ll. 11-45. The assembly also includes “compliant layer 36 formed from an elastomer, gel, adhesive or other compliant material and disposed between the second surface 25 of the rigid interposer 21 and the top surface 28 of the flexible interposer 27, and surrounding flexible leads 35.” *Id.* at col. 9, l. 46-50. Bellaar describes the compliant layer as follows:

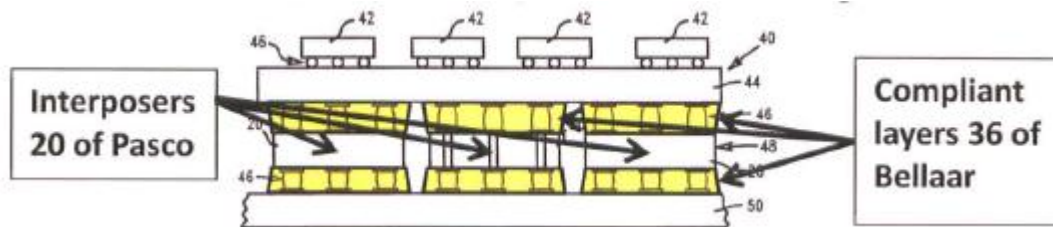
The flexible chip carrier may also include a compliant layer covering the flexible leads in whole or in part. The compliant layer comprises a dielectric material having a low modulus of elasticity, such as an *elastomeric material*. Preferred elastomeric materials include silicones, flexib[i]lized epoxies, and thermoplastics. *Silicone elastomers are particularly preferred.* The dielectric material may be provided in the form of a layer, with holes in the layer aligned with the terminals on the flexible interposer. In preferred embodiments, the compliant layer is formed in at least a two step process. The first step involves dispensing a controlled amount of a thixotropic or non-slumping silicone elastomer on a portion, but not all, of the bottom surface of the rigid interposer and/or a portion, but not all, of the first surface of the flexible interposer, to create a compliant spacer. *The compliant spacer controls the separation between the rigid interposer and the flexible interposer.* The second step involves dispensing a second silicone elastomer over the thixotropic or non-slumping silicone elastomer.

Id. at col. 5, ll. 4-22 (emphasis added). Bellaar, therefore, discloses two stacked interposing structures held together using an elastomer.

Analysis

Xilinx does not dispute that, individually, Pasco teaches a plurality of tiled interposing structures and Bellaar teaches the use of an elastomer with interposers. See PO Reply 4-5. Xilinx's position is that the combination of the two references fails to teach a "plurality of *tiled interposing structures being held together* using an elastomer." *Id.* (emphasis added). According to Xilinx, combining the teachings of Pasco and Bellaar would result in Bellaar's compliant layer only being between stacked substrate 44 and interposers 20, and between stacked interposers 20 and printed circuit board

50. *Id.* Xilinx provides, on page 5 of its Reply, a modified version of Figure 4 of Pasco showing how Xilinx believes the arrangement would work.



In Xilinx’s modified figure, the elastomer holds together substrate 44 and interposers 20, as well as interposers 20 and printed circuit board 50, but does not hold interposers 20 together. *See id.* at 5 (“‘Being held together’ means the tiles must be connected to each other by the elastomer.”). Xilinx further points to Bellaar’s statement that the elastomer is applied to a “portion, but not all,” of the interposer surfaces. *Id.* (citing Ex. 1018, col. 5, ll. 14-18).

We do not find Xilinx’s arguments persuasive. Xilinx does not point to sufficient evidence or testimony in the record to show that Pasco and Bellaar, in combination, would work in the manner described above. Also, Xilinx does not explain sufficiently how an elastomer of the type described in Bellaar could be applied to the tops and bottoms of interposers 20 in Pasco, but would not reach into the spaces between interposers 20. Moreover, as explained above, *see supra* Section II.C, references must be considered for what they would have taught to a person of ordinary skill in the art as a whole. Pasco teaches tiled interposers, and Bellaar teaches an elastomer holding together interposers. The fact that the exemplary interposers in Bellaar are stacked vertically, rather than tiled horizontally, does not mean necessarily that the elastomer could not be applied to

interposers tiled horizontally, or that doing so would not have been beneficial to reduce horizontal stresses on the interconnecting solder balls.

Xilinx has not directed us to sufficient evidence to demonstrate that claims 14 and 22 would not have been obvious over the combinations of references involved in this review (i.e., Chakravorty '362 and Siniaguine, and also Siniaguine, Ma, and Chakravorty '362), as discussed above in connection with claims 1 and 9, in further combination with Pasco and Bellaar. Xilinx contends that a person of ordinary skill in the art would not have been motivated to include a plurality of interposing structures in the assemblies of Chakravorty '362 and Siniaguine because those references do not discuss any need to reduce thermal stresses between components and because using a plurality of tiled interposing structures would require “added manufacturing steps” and “aligning each of the tiled interposing structures.” Second Subst. Mot. to Amend 16.

The record, however, shows that Pasco and Bellaar teach the added limitations of claims 14 and 22, and that a person of ordinary skill in the art would have had reason to modify the existing assemblies to have a plurality of tiled interposing structures held together using an elastomer. In particular, Mr. Johnson’s testimony that a person of ordinary skill in the art would have had reason to incorporate the teachings of Pasco and Bellaar into the interposers of Chakravorty '362 and Siniaguine to mitigate the stresses on connecting structures due to different thermal coefficients of expansion, and that doing so would have been a mere design choice yielding predictable results, is entitled to substantial weight. See Ex. 1012 ¶¶ 39-45. We are persuaded that a person of ordinary skill in the art would have been able to use, and would have recognized the benefits of using, multiple tiled

interposing structures held together using an elastomer, regardless of whether doing so would have required additional manufacturing steps or alignment, as Xilinx suggests.

Finally, we note that Xilinx's motion is deficient in another respect. Xilinx contends that the closest prior art for purposes of its proposed substitute claims is Chakravorty '362, Siniaguine, and Ma. Second Subst. Mot. to Amend 14. Xilinx, however, does not address, in any meaningful way, the level of ordinary skill in the art and what was previously known, or at least within the ordinary creativity and skill set of a person of ordinary skill in the art, regarding interposers and elastomers in general. At least some explanation should have been provided as to why a skilled artisan, applying his or her own knowledge and creativity, would not have found the proposed substitute claims obvious.

Based on the foregoing discussion, Xilinx has not met its burden to demonstrate that claims 14 and 22 would have been nonobvious over (1) the combination of Chakravorty '362, Siniaguine, Pasco, and Bellaar, and (2) the combination of Siniaguine, Ma, Chakravorty '362, Pasco, and Bellaar. Because we agree with IVM regarding the teachings of Pasco and Bellaar, and conclude that Xilinx has not met its burden to demonstrate patentability over these references in combination with the other prior art involved in this *inter partes* review, we need not address IVM's other arguments in its Opposition. See Opp. 4-10.

Also, Xilinx does not present separate patentability arguments for proposed substitute dependent claims 15-21 and 23-26, instead relying only on its arguments regarding claims 14 and 22. See Second Subst. Mot. to Amend 15-19. Because we conclude that Xilinx has not met its burden as to

claims 14 and 22, and Xilinx presents no argument as to the other proposed substitute claims, Xilinx also has not met its burden to demonstrate the patentability of the other claims, and we need not address IVM's arguments pertaining specifically to those claims.

III. ORDER

IVM has demonstrated, by a preponderance of the evidence, that (1) claims 1-5, 7-11, and 13 are unpatentable over Chakravorty '362 and Siniaguine; (2) claims 6 and 12 are unpatentable over Chakravorty '362, Siniaguine, and Patel; (3) claims 1-5, 7-11, and 13 are unpatentable over Siniaguine, Ma, and Chakravorty '362; and (4) claims 6 and 12 are unpatentable over Siniaguine, Ma, Chakravorty '362, and Patel.

In consideration of the foregoing, it is hereby:

ORDERED that claims 1-13 of the '960 patent are *cancelled*; and

FURTHER ORDERED that Xilinx's Second Substitute Motion to Amend is *denied*.

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Patent 7,566,960 B1

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