

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTELLECTUAL VENTURES MANAGEMENT, LLC
Petitioner

v.

XILINX, INC.
Patent Owner

Case IPR2012-00020
Patent 8,058,897

Before SALLY C. MEDLEY, KARL D. EASTHOM, and
JUSTIN T. ARBES, *Administrative Patent Judges*.

MEDLEY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. *Background*

Petitioner, Intellectual Ventures Management, LLC (“IVM”), filed a Petition (Paper 5) (“Pet.”) requesting *inter partes* review of claims 1-9 and 12-14 of U.S. Patent No. 8,058,897 B1 (“the ’897 patent”) pursuant to 35 U.S.C. §§ 311-319. On February 12, 2013, the Board granted the Petition as to all claims challenged, and instituted trial for claims 1-9 and 12-14 on three grounds of unpatentability. Paper 14 (“Dec. on Inst.”).

Subsequent to institution, Patent Owner, Xilinx, Inc. (“Xilinx”) filed a Patent Owner Response (Paper 18; “PO Resp.”) and a Motion to Amend, requesting the cancellation of claim 1 (Paper 20; “Mot. to Amend”). IVM filed a Reply to the Patent Owner Response. Paper 23 (“Pet. Reply”).

Oral hearing was held on November 7, 2013.¹

The Board has jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine that IVM has shown by a preponderance of the evidence that claims 2-9 and 12-14 of the ’897 patent are unpatentable. Xilinx’s Motion to Amend, requesting the cancellation of claim 1, is *granted*.

B. *The ’897 Patent*

The invention of the ’897 patent relates to the configuration of an integrated circuit (IC) that includes multiple dies, such as a master die and a slave die. A master die receives configuration data for both the master die

¹ A transcript of the oral hearing is included in the record. Paper 32.

and the slave die. The master and slave segment of the configuration data is determined, and the slave segment of the configuration data is distributed to the IC's slave die. Ex. 1001, 2:5-15. Configuration data also may be sent from the master die of a first IC to a second IC. *Id.* at 7:45-60.

C. Exemplary Claims

Claim 1 and claim 8 are representative and reproduced here:

1. A method of configuring an integrated circuit (IC), the method comprising:

receiving configuration data within a master die of a first IC, wherein the first IC comprises the master die and a slave die;

determining a master segment and a slave segment of the configuration data, wherein the master segment specifies a master die circuit design to be implemented within the master die and the slave segment specifies a slave die circuit design to be implemented within the slave die;

distributing the slave segment of the configuration data to the slave die of the first IC,

determining, within the master die, whether configuration data comprises a segment of configuration data for a second IC; and

responsive to determining that the configuration data comprises a segment of configuration data for the second IC, sending the segment of the configuration data to the second IC.

8. An integrated circuit (IC) comprising:

an interposer comprising a configuration bus;

a first die on a surface of the interposer;

a second die on the surface of the interposer,

wherein the first die and the second die are coupled by the configuration bus,

wherein the first die is configured, responsive to receiving configuration data, to determine a first segment and a second segment of the configuration data and distribute the second segment of the configuration data to the second die through the configuration bus,

wherein the first die is configured to determine whether the configuration data comprises a segment of configuration data for an additional IC, and

wherein the first die comprises a configuration data output coupled to an output of the IC, and responsive to determining that the configuration data comprises a segment of configuration data for the additional IC, the first die is configured to send the segment of configuration data for the additional IC through the first die configuration data output.

D. The Alleged Grounds of Unpatentability

The prior art references as applied to claims 1-9 and 12-14 are:

Wennekamp	U.S. Patent 7,397,272	July 8, 2008 (Ex. 1009)
Miller	U.S. Patent 7,827,336	Nov. 2, 2010 (Ex. 1010)
Siniaguine	U.S. Patent 6,730,540	May 4, 2004 (Ex. 1013)

The Board instituted trial on the following grounds of unpatentability:

Reference[s]	Basis	Claims challenged
Wennekamp	§ 103	1-7
Wennekamp and Miller	§ 103	1, 8, and 12-14
Wennekamp, Miller, and Siniaguine	§ 103	9

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

If a feature appearing in the specification is not necessary to interpret what the inventor means by a claim term, it would be “extraneous” and should not be read into the claim. *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988).

In the Decision on Institution, the Board determined the broadest reasonable construction for “[f]irst IC comprises the master die and a slave die” (claim 1) and “[a]n integrated circuit (IC) comprising” a “first die on a surface of the interposer” and “a second die on the surface of the interposer” (claim 8). Dec. on Inst. 6-7. For all other claim terms, the Board applied the plain and ordinary meaning that the term would have had to a person of ordinary skill in the art. *Id.* at 7.

Neither party contests the Board's construction or proposes a specific claim construction. We apply the broadest reasonable construction identified above in rendering this final decision.

B. Claims 1-7

The Board instituted trial on the ground that claims 1-7 are unpatentable under 35 U.S.C. § 103 over Wennekamp. Xilinx does not contest the unpatentability of claim 1 in its Patent Owner Response. PO Resp. 3. Rather, Xilinx requests cancellation of claim 1.² Mot. to Amend. Nonetheless, Xilinx argues that dependent claims 2-7 are patentable over Wennekamp based solely on a claim 1 feature. Specifically, Xilinx argues that Wennekamp does not teach or suggest a multi-die IC and that reliance on expert testimony for a teaching or suggestion of a multi-die IC is improper. PO Resp. 7.

Wennekamp describes a system for configuring a plurality of programmable devices that may include an external memory, a master programmable device, and at least one slave programmable device. Ex. 1009, Abstract.

Although Wennekamp does not describe the programmable devices in the context of dies on an integrated circuit, e.g., a “multi-die IC,” Wennekamp describes that the invention is applicable to a variety of systems having programmable or configurable devices, such as programmable logic devices or integrated circuits having some programmable resources. *Id.* at

² As explained herein, we grant Xilinx's motion, which is unopposed, and cancel claim 1. Thus, we need only address the patentability of challenged claims 2-9 and 12-14.

3:15-18. Like the '897 patent, Wennekamp recognizes the field programmable gate array (FPGA) device as a type of programmable logic device. *Id.* at 1:15-18.

Wennekamp describes that a master programmable device (e.g., 320 of Figure 3), can receive configuration data from external memory 310. *Id.* at 5:4-14. Figure 3 further shows a slave device (e.g., 330a) connected to master device 320, and “additional IC” 330B. The external memory contains a master segment and a slave segment of the configuration data (*id.* at 5:12-14, memory 310 “store[s] configuration data, or a configuration bitstream, for configuring the plurality of programmable devices 320 and 330”). Wennekamp also describes that the memory may provide a configuration bitstream in parallel to the master programmable device in response to addresses and that the master programmable device can provide at least a portion of the configuration bitstream in parallel to the slave programmable device. *Id.* at 2:26-31, 5:16-17. The slave device can then, for example, provide configuration data to another slave device from the original data provided to the master device.

Wennekamp describes its parallel daisy chain configuration (*id.* at 5:22-23) as allowing a master device to communicate with other slave devices without first sending configuration data through another device. Based on the description in Wennekamp, a person of ordinary skill in the art would have understood that Wennekamp’s daisy chain configuration minimizes the consumption of board routing resources and avoids long wires, which may degrade signal quality or limit the maximum configuration clock frequency. *See id.* at 4:40-45.

With respect to the embodiment of Figure 4, Wennekamp describes

that certain instructions may indicate that device 400 enables its POUT register 463, which provides data to the P[n:0] output. The enable POUT instruction means that the data being received is not targeted for the current device, but is targeted for a downstream device. *Id.* at 6:21-27. Instructions can be nested in a bitstream to enable multiple devices to ignore the bitstream data and to target a particular device in the chain. *Id.* at 6:31-34. Wennekamp discloses that “by properly arranging the bitstream, a user may enforce the order in which devices in the chain are configured.” *Id.* at 6:40-41.

Wennekamp is not limited to one particular configuration and describes that, although some components are shown directly connected to another, some components are connected through an intermediate component. Wennekamp describes providing interconnection between components to establish electrical communication between components. Wennekamp recognizes that “[s]uch communication [between devices] can often be accomplished using a number of circuit configurations, as will be understood by those of ordinary skill in the art.” *Id.* at 7:35-42.

Wennekamp does not describe explicitly programmable devices in the context of dies on an integrated circuit, e.g., a “multi-die IC.” As explained in the Decision on Institution, IVM accounted for this difference and provided reasons for modifying Wennekamp to arrange its programmable devices as dies on ICs. Dec. on Inst. 10-11.

Xilinx argues that Wennekamp does not teach or suggest a multi-die IC and that reliance on expert testimony for a teaching or suggestion of a multi-die IC is improper, citing 35 U.S.C. § 311(b). PO Resp. 7.

Xilinx’s arguments are not persuasive. It is uncontested that a person

of ordinary skill in the art knew that circuits could be arranged on a die and that an IC could contain more than one die. Multi-die ICs were well known in the art at the time of the invention. Ex. 1002 ¶¶ 20, 21; Ex. 1017 ¶¶ 20-24. Xilinx's expert, Dr. Blanchard, acknowledged, on cross-examination, that multi-die ICs were well known in the art at the time of the invention. Ex. 1016, 27:14-28:9.

A reference need not teach every feature for it to render a claimed invention obvious. “[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). Therefore, an obviousness determination takes into account what a person of ordinary skill in the art would have known at the time of the invention and is not limited to what is contained within the four corners of a patent or printed publication. *See, e.g., Leapfrog Enterprises, Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (court upheld the determination that claims were unpatentable despite the prior art not teaching specifically the claimed reader).

Xilinx's reading of 35 U.S.C. § 311(b) is too narrow. Although section 311(b) states that unpatentability may be determined “only on the basis of prior art consisting of patents or printed publications,” we disagree that this statutory requirement means that each and every limitation must be found explicitly in patents or printed publications. In support of a petition, a petitioner is authorized to submit affidavits or declarations of supporting evidence and opinions. 35 U.S.C. § 312(a)(3)(B). Moreover, 35 U.S.C. §

318(a) requires the Board to issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner. That requirement does not preclude the Board from determining the patentability of a challenged patent claim based on the record before the Board.

Based on the record before the Board, IVM has demonstrated that: (1) multi-die ICs were known at the time of the invention; (2) Wennekamp would have suggested, to a person of ordinary skill in the art, the use of multi-die ICs; and (3) arranging Wennekamp's devices using multi-die ICs was within the skill set of a person of ordinary skill in the art at the time of the invention. In particular, Wennekamp describes that communication between devices may be accomplished using a number of circuit configurations (Ex. 1009, 7:35-42), and IVM has demonstrated that a multi-die configuration is one such compatible configuration. *See* Pet. 6-7; Ex. 1002 ¶ 27; Pet. Reply 7; Ex. 1017 ¶¶ 25-26. Xilinx's expert, Dr. Blanchard, testified that Wennekamp does not suggest using a multi-die configuration. Ex. 2006 ¶ 23-26. That testimony, however, does not outweigh the testimony of IVM's expert, Mr. Johnson, that Wennekamp does suggest using a multi-die configuration. Specifically, Dr. Blanchard's statements are conclusory. For example, Dr. Blanchard does not explain what a person of ordinary skill in the art would have known with respect to multi-die ICs at the time of the invention. Instead, Dr. Blanchard merely concludes that those portions of Wennekamp to which IVM directs attention (e.g., Ex. 1009, 3:15-26, 7:35-42) do not teach or suggest the use of multi-die ICs. Ex. 2006 ¶¶ 24-25. Such conclusory testimony is entitled to little or no weight. 37 C.F.R. § 42.65(a).

Moreover, arranging the master and slave devices of Wennekamp as individual dies on an IC would facilitate Wennekamp's goal of minimizing the consumption of board routing resources and using shorter wires to prevent the degradation of signal quality. See Pet. 7-8; Ex. 1002 ¶ 27; Pet. Reply 8. Indeed, Xilinx's expert, Dr. Blanchard, explained, during cross-examination, that a person of ordinary skill in the art would have recognized the advantages of using multi-die ICs, as opposed to placing multiple ICs on a printed circuit board. Ex. 1016, 33:19-34:7. Making the modification to Wennekamp would not have been beyond the skill of a person of ordinary skill in the art, and therefore, would have been obvious. Ex. 1002 ¶ 27; Ex. 1017 ¶ 26.

In sum, based on the totality of the evidence, multi-die ICs were known at the time of the invention. A person of ordinary skill in the art would have recognized the advantages of arranging programmable devices on multi-die ICs. Such a configuration would have improved the Wennekamp arrangement. Moreover, making such a modification would have been well within the skill of a person of ordinary skill in the art.

C. Claims 8, 9, and 12-14

The Board instituted trial on the ground that independent claim 8 and dependent claims 12-14 are unpatentable under 35 U.S.C. § 103 over Wennekamp and Miller, and dependent claim 9 is unpatentable under 35 U.S.C. § 103 over Wennekamp, Miller, and Siniaguine. Dec. on Inst. 13-16. Xilinx's Patent Owner Response is directed to independent claim 8, as is IVM's Reply.

The ground of unpatentability of claim 8 is based on Wennekamp in

view of Miller. Wennekamp is described in the above section. Miller describes two integrated circuit die where the first die is considered primary and the second die is considered secondary. The two die are connected through an interposer. Ex. 1010, Abs. Miller describes that the two integrated circuit die, each having a processing core and a memory, are interconnected and packaged together to form a multi-chip module. *Id.*

IVM relies on Miller to teach connection of dies through an interposer. *See, e.g.,* Pet. 17. Xilinx does not challenge the teachings of Miller or the combination of Wennekamp and Miller, which the record supports. Therefore, we need to decide only whether Wennekamp teaches or suggests certain claim 8 limitations.

Claim 8 requires a first die configured to “determine whether the configuration data comprises a segment of configuration data for an additional IC.” Xilinx argues that Wennekamp does not teach this limitation. PO Resp. 11.

It is not disputed that Wennekamp describes master device 320, slave device 330A, and “additional IC” 330B. *See, e.g.,* PO Resp. 10. Moreover, IVM accounted for the disputed feature in its Petition, and then again in its Reply, explaining that configuration arrangements described in Wennekamp would have been understood by a person of ordinary skill in the art as describing the disputed feature. Pet. 17-18; Pet. Reply 10-11.

As discussed above, Wennekamp describes that certain instructions may indicate that device 400 (which may be used as device 320 or device 330, *see* Ex. 1009, 5:61-63) enable its POUT register 463, which provides data to the P[n:0] output. The enable POUT instruction means that the data being received is not targeted for the current device, but is targeted for a

downstream device. *Id.* at 6:21-27.

In its Petition, IVM directed attention to the description in Wennekamp regarding the enablement of the POUT register as meeting the limitation of determining whether configuration data comprises a segment of configuration data for an additional IC. Pet. 18-19. Moreover, in support of its Petition, IVM relied on the testimony of Mr. Johnson, who testified that a person of ordinary skill would have understood Wennekamp (at 6:24-28) to describe this determining limitation. Ex. 1002 ¶ 26.

Xilinx did not cross-examine Mr. Johnson. Moreover, in its Patent Owner Response, Xilinx does not address the above discussed portion of Wennekamp or Mr. Johnson's testimony, but focuses attention on other portions of Wennekamp. PO Resp. 11; Ex. 2006 ¶ 29.

In addition, and in response to arguments made in the Patent Owner Response, IVM submitted further testimony by Mr. Johnson as to the disputed feature.

For example, Mr. Johnson testified as follows:

31. Devices downstream of a configuration memory in Wennekamp must be capable of determining whether incoming configuration data is intended for the device itself, or for another device further downstream. In particular, Wennekamp discloses that "certain instructions may indicate that device 400 should enable its POUT register 463, which provides data to the P[n:0] output." (Wennekamp, IVM1009, 6:21-23.) Specifically, "[t]his enable POUT instruction means that the data being received is not targeted for the current device, and is instead targeted to a downstream device," and "[b]y enabling POUT register 463, the input data is passed through to the next device in the chain." (Wennekamp, IVM1009, 6:24-28.)

32. These instructions or other information for determining whether to pass configuration information downstream or to

apply it to the device in question is used by the device 320 (first die) to determine whether the configuration data comprises some segment of configuration data intended for another device, such as device 330A (second die) or device 330B (additional IC). As Wennekamp notes, “programmable device 400 may be used, for example, as master device 320 or slave device 330” (Wennekamp, IVM1009, 5:61-63), and includes configuration control circuitry 450 to enable the POUT register to pass configuration data (including a segment, or number of bytes) “to target a particular device in the chain.” (Wennekamp, IVM1009, 6:21-52.) Absent this ability, it would not be possible for the “enable POUT instruction” of Wennekamp to function.

33. As a result, Wennekamp teaches “determin[ing] whether the configuration data comprises a segment of configuration data for an additional IC” by the first die (e.g., device 320), as device 320 in Wennekamp is capable of determining whether a segment of configuration data is, for example, intended for device 330B, device 330A, or for itself.

Ex. 1017 ¶¶ 31-33.

We give the above testimony substantial weight because the explanation Mr. Johnson provides is consistent with Wennekamp, particularly the description at column 6, lines 21-41. That is, device 400 (which may be master device 320, for example) determines if instructions are for the master device or another device, such as 330A or “additional IC” 330B. As explained above in the cited testimony, if there was no such determining, the POUT enable would not function as described. In contrast, Xilinx’s arguments and evidence do not rebut IVM’s arguments and evidence.

Claim 8 further recites that the first die is configured to (1) “distribute the second segment of the configuration data to the second die through the

configuration bus,” and (2) “send the segment of configuration data for the additional IC through the first die configuration data output.”

Xilinx argues that Wennekamp does not teach or suggest sending some portions of data on one bus for one device and another portion of data on a different bus for a different device. Xilinx argues that all of the data output by device 320 goes through port P[n:0] through the parallel daisy chain to the next device. PO Resp. 11.

Xilinx’s arguments are not commensurate in scope with what is claimed. Claim 8 does not recite sending some portions of data on one bus for one device and another portion of data on a different bus for a different device. Claim 8 requires one bus and one data output, not two buses. Moreover, there is nothing in claim 8 that requires the data intended for the second die and the data intended for the additional IC to go through two separate, non-overlapping outputs or data paths. In other words, Xilinx has not demonstrated that claim 8 requires the distributing and sending to occur over two separate and distinct paths.³ Xilinx’s argument is based on attorney argument and not supported by evidence.

IVM, however, accounted for the disputed features in its Petition. Pet. 17-19. Moreover, IVM demonstrates with supporting evidence that claim 8 does not require the distributing and sending to occur over two separate and distinct paths and that Wennekamp teaches the claim 8 limitations. Pet. Reply 11-14; Ex. 1017 ¶ 37-41. IVM’s arguments and evidence are

³ During the trial hearing, counsel for Xilinx made arguments regarding the interpretation of claim 8 that were not presented previously. *See, e.g.*, Transcript 31:14-24. We need not and do not consider arguments advanced during trial hearing that were not raised prior to the trial hearing. To do otherwise would be prejudicial to IVM.

persuasive. In particular, IVM directs attention to Wennekamp figure 3 in support of showing how the disputed claim 8 features are met.

Figure 3 of Wennekamp is reproduced here:

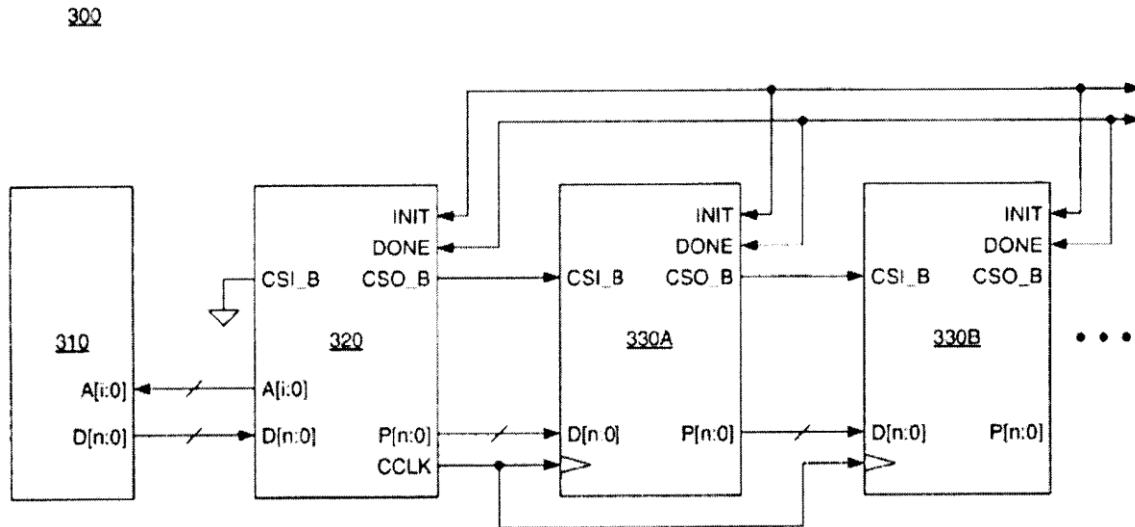


FIG. 3

Figure 3 of Wennekamp shows a system for configuring programmable devices using a parallel daisy chain configuration.

As seen above, Wennekamp shows first device 320, second device 330A (both on the first IC), and “an additional IC” 330B. First device 320 and second device are coupled by a configuration bus (the line between P[n:0] of 320 and D[n:0] of 330A). The first die also comprises a configuration data output P[n:0] of 320 coupled to an output of the second device (output of the first IC) through 330A. The first die is configured to send the segment of configuration data for the additional IC through the output of the first die and distribute the second segment of the configuration data to the second die through the configuration bus. Ex. 1017 ¶¶ 34-41.

Thus, IVM has shown with sufficient evidence that Wennekamp describes that the first die is configured to (1) “distribute the second segment

of the configuration data to the second die through the configuration bus,” and (2) “send the segment of configuration data for the additional IC through the first die configuration data output” as claimed in claim 8. Xilinx has not rebutted that showing.

III. ORDER

IVM has demonstrated, by a preponderance of the evidence, that (1) claims 2-7 are unpatentable over Wennekamp; (2) claims 8 and 12-14 are unpatentable over Wennekamp and Miller; and (3) claim 9 is unpatentable over Wennekamp, Miller, and Siniaguine. Xilinx’s Motion to Amend, cancelling claim 1, is granted.

In consideration of the foregoing, it is

ORDERED that claims 1-9 and 12-14 are CANCELLED; and

FURTHER ORDERED that Xilinx’s Motion to Amend is *granted*.

Case IPR2012-00020

Patent 8,058,897

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