

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTELLECTUAL VENTURES MANAGEMENT, LLC
Petitioner

v.

XILINX, INC.
Patent Owner

Case IPR2012-00023
Patent 7,994,609 B2

Before SALLY C. MEDLEY, KARL D. EASTHOM, and
JUSTIN T. ARBES, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

Petitioner, Intellectual Ventures Management, LLC (“IVM”), filed a Petition to institute an *inter partes* review of claims 1–19 of U.S. Patent No. 7,994,609 B2 (“the ’609 Patent”), owned by Xilinx, Inc. Paper 3 (“Pet.”). See 35 U.S.C. § 311. As set forth in this Final Written Decision, see 35 U.S.C. § 318(a), based on the record presented, IVM has shown “by a preponderance of the evidence,” 35 U.S.C. § 316(e), that claims 1–19 of the ’609 Patent are unpatentable under 35 U.S.C. § 103(a). In addition, Xilinx has failed to show that proposed amended claims are patentable under 35 U.S.C. § 103(a). See Paper 17 (“Mot. to Amend”).

After IVM filed its Petition, Xilinx filed a Preliminary Response opposing the institution of the *inter partes* review. Paper 9 (“Prelim. Resp.”). The Board granted the Petition, concluding that IVM’s Petition demonstrated a reasonable likelihood that claims 1–19 are unpatentable under 35 U.S.C. § 103(a) for obviousness, and instituted trial. Paper 11 (“Inst. Dec.”).

After the Institution Decision, Xilinx filed a Response. Paper 15 (“PO Resp.”). Xilinx also filed a Motion to Amend, contingent upon the Board ultimately determining that challenged claims 1–19 are unpatentable. See Paper 17 (“Mot. to Amend”). IVM then filed a Petitioner Reply to Xilinx’s Response, maintaining that the challenged claims are unpatentable. Paper 22 (“Pet. Reply”). IVM also filed an Opposition to Xilinx’s Motion to Amend, Paper 21 (“Opp.”), and Xilinx filed a Patent Owner Reply to the Opposition, Paper 24 (“PO Reply”). Both parties requested an oral hearing, which occurred on November 7, 2013. A transcript of the oral hearing appears in the record. Paper 33 (“Tr.”).

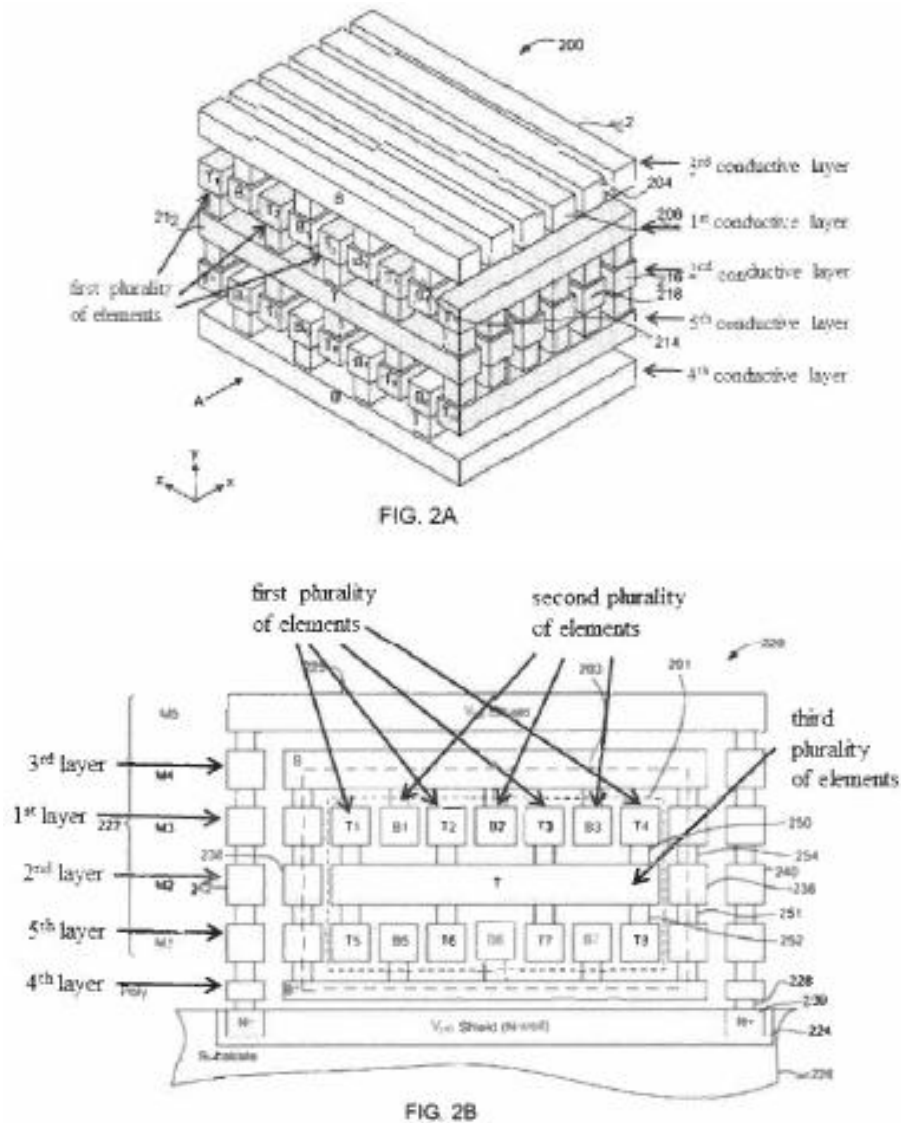
In its Response—i.e., in “response to the [P]etition [and] addressing any ground for unpatentability not already denied,” 37 C.F.R. § 42.120—Xilinx argues that claims 2, 8, 9, 18, and 19, “are valid.” PO Resp. 5. Xilinx does not argue that

claims 1, 3–7, and 10–17 are patentable. Claims 2, 8, and 9 depend from independent claim 1, and claim 19 depends from independent claim 18. Therefore, as Xilinx acknowledged during the oral hearing, Xilinx concedes that claims 1, 3–7, and 10–17 are unpatentable based on the applicable grounds listed in the Institution Decision. Tr. 48, ll. 5–9; *accord* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012) (“The [patent owner] response should identify all the involved claims that are believed to be patentable and state the basis for that belief.”); Inst. Dec. 13 (determining that IVM’s Petition “sufficiently demonstrates a reasonable likelihood that claims 1–19 are unpatentable based on Grounds 1–6”).

A. The '609 Patent

The '609 Patent describes a shielded capacitor in an integrated circuit (IC) having a core capacitor portion that includes multiple layers of conductive elements. Shields, including a shield capacitor portion and a capacitor reference shield, surround the core capacitor portion. The shield capacitor portion includes multiple conductive elements in different metal layers. According to claim 1, the shield capacitor portion forms part of a capacitor node and lies partially between the reference shield and the core capacitor portion. The shields reduce electronic noise. See Ex. 1001, col. 2, l. 40 – col. 3, l. 3; col. 5, ll. 1–4; col. 6, ll. 24–31; Abstract.

To identify disclosed structure that corresponds to certain elements recited in claims 1 and 2, IVM annotates Figures 2A and 2B from the '609 Patent, which are reproduced below:



IVM's annotated figures above show a centrally located core capacitor, including a first (T1, T2) and second (B1, B2) plurality of node elements, numbered conductive layers, one capacitor node (B, B', B1-B5), the other capacitor node (T, T1-T5), and shields. See Pet. 4-5.

With respect to independent claim 1 (which follows), layer T corresponds to a second part of a first capacitor node, layers B and B' correspond to a shield capacitor portion and a second part of a second capacitor node, and the V_{DD} shield corresponds to a reference shield.

B. Exemplary Claims

Claims 1 and 2 are reformatted and annotated with bracketed information added to claim 1 to help illustrate example structure and with limitations at issue in claim 2 emphasized, as follows:

1. A capacitor in an integrated circuit (“IC”) comprising:
 - a core capacitor portion having a first plurality of conductive elements [see T1,T2] electrically connected to and forming a first part of a first node of the capacitor formed in a first conductive layer of the IC and a second plurality of conductive elements [see B1, B2] electrically connected to and forming a first part of a second node of the capacitor formed in the first conductive layer,
 - the first plurality of conductive elements alternating with the second plurality of conductive elements in the first conductive layer, and a third plurality of conductive elements [see T] electrically connected to and forming a second part of the first node formed in a second conductive layer adjacent to the first conductive layer, at least portions of some of the second plurality of conductive elements overlying and vertically coupling to at least portions of some of the third plurality of conductive elements;
 - a shield capacitor portion [see B, B'] having a fourth plurality of conductive elements formed in at least the first conductive layer of the IC, the second conductive layer of the IC, a third conductive layer of the IC, and a fourth conductive layer of the IC, the first conductive layer and the second conductive layer each being between the third conductive layer and the fourth conductive layer, the shield capacitor portion being electrically connected to and forming a second part of the second node of the capacitor and surrounding the first plurality of conductive elements and the third plurality of conductive elements;
 - and
 - a reference shield [see V_{DD} Shield] electrically connected to a reference node of the IC other than the second node of the capacitor,

the shield capacitor portion being disposed between the reference shield and the core capacitor portion.

2. The capacitor of claim 1 wherein the third conductive layer is a metal layer of the IC and the fourth conductive layer is a poly layer of the IC, *the shield capacitor portions* including a first node shield plate formed in the metal layer from a plurality of metal stripes and *a second node shield plate formed in the poly layer*.

See '609 Patent, col. 12, l. 55 – col. 13, l. 25 (emphases added); *see also* PO Resp. 5 (discussing disputed limitations in claim 2).

C. Grounds of the Trial

The prior art references applied to the claims follow:

Paul	U.S. Patent 6,737,698	May 18, 2004	(Ex. 1006)
Anthony	U.S. Patent 7,439,570	Oct. 21, 2008	(Ex. 1007)
Hsueh	U.S. Patent 7,286,071	Oct. 23, 2007	(Ex 1008)
Brennan	U.S. Patent 6,903,918	June 7, 2005	(Ex 1009)
Bi	U.S. Pub. 2008/0128857	June 5, 2008	(Ex 1010)
Marotta	U.S. Patent 7,238,981	July 3, 2007	(Ex. 1011)

The Board instituted trial based upon the following grounds of unpatentability under 35 U.S.C. § 103:

Reference[s]	Basis	Claims challenged
Paul	§ 103	1, 3, 5, 6, and 10–12
Paul and Anthony	§ 103	2 and 13–17
Paul and Hsueh	§ 103	4
Paul and Brennan	§ 103	7–9
Anthony and Marotta	§ 103	18 and 19
Anthony and Bi	§ 103	1 and 13

II. ANALYSIS

A. Claim Interpretation

Consistent with the statute and legislative history of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284, 329 (2011) (“AIA”), the Board interprets claims using the “broadest reasonable construction in light of the specification of the patent in which [they] appear[.]” 37 C.F.R. § 42.100(b); *see also* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

Plate

The parties do not define the term plate, which appears in claims 2 and 18. In addition to capacitor node plates such as B, T, B’, Ex. 1001, col. 5, ll. 58-60, the ’609 Patent also refers to “ground plate 287,” and “shield plate 260,” *id.* at col. 8, l. 25, l. 36, as part of the capacitor, but not necessarily as nodes of a capacitor. *See id.* at Fig. 2C (ground plate 287 and shield plate 260 not electrically connected to capacitor nodes B and T). In other words, according to the ’609 Patent claims and disclosure, a “plate” does not imply necessarily a capacitor node.

In terms of the physical structure of a plate, the ’609 Patent generally discloses that “an arbitrary number of layers may be used in accordance with embodiments of the invention,” *id.* at col. 11, ll. 25–27, and that a “plate layer [can be] made up of strips, rather than a continuous sheet,” *id.* at col. 5, ll. 5–6. The ’609 Patent also refers to “silicide plates or strips,” *id.* at col. 3, l. 59, indicating that a “plate” signifies structure that is distinct from a strip. The ’609 Patent implies that, in addition to being discontinuous, a plate may have multiple layers: “The *bottom plate* conductive matrix [see B, B’ and conductive curtains, Fig. 2C] of the integrated capacitor *loosely surrounds* the top plate conductive matrix [T, T1, T2 . . . T8] of the integrated capacitor *so that the top plate couples with the*

bottom plate on the top, bottom, right side, and left side.” Ex. 1001, col. 6, ll. 3–7 (emphases added), Fig. 2C. This reference to the “bottom plate conductive matrix” that “surrounds” the top plate, and the description that the “top plate couples with the bottom plate on the top, bottom, *right side*, and *left side*,” implies that the “bottom plate” may have multiple layers in order to couple to the top plate on all sides and to surround the top plate.

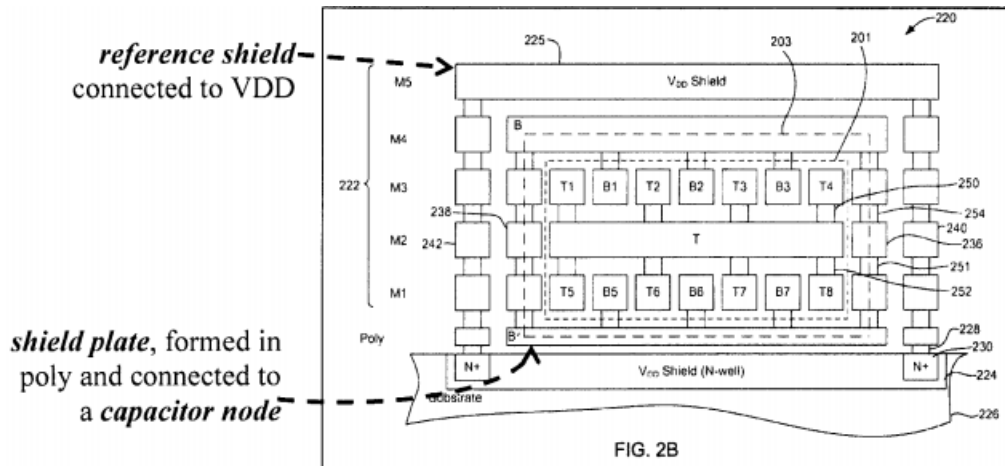
Accordingly, based on the ’609 Patent disclosure, a “plate” is a conductive structure that is part of a capacitor, as either a shield, a node, or a node that also functions as a shield, which may be continuous, as a sheet, or discontinuous, as electrically connected strips, and which may or may not comprise plural electrically connected layers.

B. Claim 2

Poly Node Shield Plate

Xilinx argues that the combination of Paul and Anthony does not render obvious a poly node shield plate as set forth in dependent claim 2. *See* PO Resp. 5–10. According to Xilinx, “neither Paul nor Anthony teach[es] or suggest[s] a ‘shield plate’ that is ‘formed in the poly layer’ and is ‘part of the second node of the capacitor.’” *Id.* at 6.

To illustrate the disputed limitation in claim 2, Xilinx annotates Figure 2B from the '609 Patent, as follows:



Xilinx's annotated Figure 2B from the '609 Patent shows a disclosed poly shield plate, near the bottom, as capacitor node layer B', which connects to capacitor node layer B (the other capacitor node includes layer T). *See id.*

According further to Xilinx's annotated Figure 2B, the capacitor nodes are not connected electrically (i.e., conductively) to the reference shield. Xilinx maintains that claim 2, by virtue of dependency from claim 1, requires "the shield capacitor portion [to be] 'electrically connected to and form a second part of the second node of the capacitor.'" *Id.* (brackets by Xilinx omitted).

IVM and Xilinx agree that Paul does not disclose a poly node shield plate. *See id.*; Pet. 24; Ex. 1002 ¶ 50. The parties also agree that Anthony discloses a poly capacitor bottom shield layer 36 as an alternative to a metal layer. PO Resp. 7; Ex. 1002 ¶ 50 (discussing and quoting Ex. 1007, col. 4, ll. 49–52). However, Xilinx reasons that bottom layer 36 of Anthony "is a reference shield, and is never shown or suggested as being connected to or part of the capacitor node." PO Resp. 9 (footnote omitted). In other words, Xilinx stresses that Anthony only teaches a bottom *reference* poly shield plate 36, as opposed to a bottom *node* poly shield plate. *Id.*

Xilinx's arguments separately attack the references and fail to rebut IVM's obviousness showing that relies on the combination, as IVM states. *See* Pet. Reply 4. IVM asserts, and the record shows, that "Paul's [bottom] shield plate 810 [constitutes] a [metal] shield plate connected to a capacitor node." *See* Pet. Reply 4; Ex. 1006, Fig. 8; Inst. Dec. 11. Both experts agree that Anthony discloses bottom shield layer of poly 36. *See* Pet. Reply 2–5 (discussing testimony by Mr. Johnson and Dr. Blanchard); Ex. 1007, Fig. 3B. Xilinx's arguments imply that Anthony's teaching that poly can be used in place of metal as a capacitor shield does not apply to capacitor nodes or node shields. *See* PO Resp. 9. Xilinx's arguments effectively reduce to the assertion that it would have been unobvious to replace one known type of capacitor conductor layer for another.

To the contrary, Anthony specifically teaches that "[a]s *an alternative to the use of a metal layer* as shown in FIG. 3B (which may be needed for interconnect purposes) *the bottom shield plate 36 can be implemented with a polysilicon or diffusion layer.*" Ex. 1007, col. 4, ll. 49–52 (italics emphases added). As skilled artisans would have recognized, the sentence shows that poly and metal constitute suitable electrical conductors for capacitors. The sentence instructs that metal layers may be "needed for interconnect purposes," which implies or suggests that metal necessarily would not be needed to create nodes or shields. *See id.* It follows that Anthony's teaching is not restricted to metal capacitor shields and applies generally to metal layers, including metal capacitor nodes.

IVM further relies on its expert, Mr. Johnson, and reasons that "one skilled in the art would have been motivated to make this substitution [i.e., to substitute the poly of Anthony for the metal of Paul] to, for example, save a metal layer for another purpose or as a matter of convenience depending on where a signal may be coming from." Pet. Reply 6 (citing Ex. 1013 ¶ 20). IVM also points to the

corroborative testimony of Xilinx's expert, Dr. Blanchard, who reasons that "sometimes you need to get from A to B" and describes

"one of a couple of reasons [for using poly instead of metal], one having to do with layout, because all the other conductive layers were used up, so you need something here, or just out of convenience, a signal might be going to or coming off the poly layer associated with a gate or something else."

Pet. Reply 6 (quoting Ex. 1014, 52, ll. 15–25).

The record shows that choosing a poly layer to replace a metal layer would have amounted to a matter of convenience involved in a circuit layout, where, for example, a poly layer is planned for other circuit components or connections on the same layer, or metal layer constraints exist. Replacing a metal capacitor layer with a poly capacitor layer would have resulted in a predictable result, a capacitor with a similar conductor. "The Court recognized that when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) (citing *United States v. Adams*, 383 U.S. 39 (1966)).

Therefore, based on the record evidence in light of the arguments presented, IVM has shown "by a preponderance of the evidence," 35 U.S.C. § 316(e), that claim 2 would have been obvious over the combination of Paul and Anthony.

C. Claims 8 and 9

Claim 8 depends from claim 7, which depends from claim 1. Claim 8 follows: "The capacitor of claim 7 wherein each of the conductive elements in the third plurality of conductive elements is adjacent to a conductive element electrically connected to and forming a third part of the first node."

Figure 2A from the '609 Patent, annotated by Xilinx, appears below:

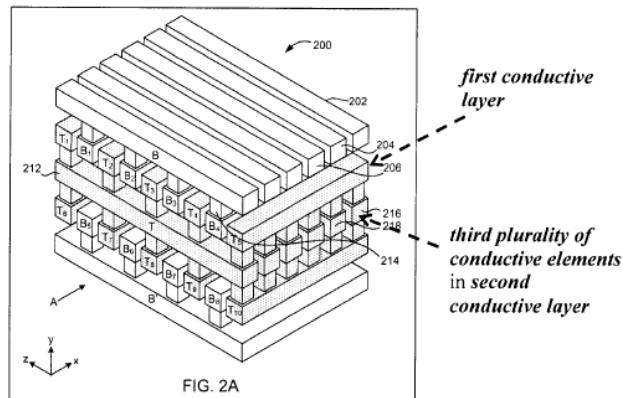


FIG. 2A from '609 patent

Annotated Figure 2A above depicts one view of a third plurality of conductive elements (at node T) corresponding to those elements as recited in claim 8, according to Xilinx. PO Resp. 11.

Adjacent Conductive Elements

Xilinx argues that the prior art combination does not satisfy the limitation that involves “adjacent” conductive elements in claim 8, essentially, according to Xilinx, because “adjacent” conductive elements imply a “plate” layer, and the '609 Patent discloses advantages to having a “plate” layer. See PO Resp. 11–13 (citing Ex. 1001, col. 5, ll. 57–58, as describing a “plate” layer). According to Xilinx, a “plate” layer has non-alternating nodes, which Paul does not disclose, and claim 8 requires “a specific lateral capacitance and vertical capacitance.” *Id.* at 11–12 (citing Ex. 1001, col. 6, ll. 33–38).

In Paul, the outer shield layers, A and B, do include non-alternating conductor strips, while the middle layers do not, because they have alternating nodes, A and B. See, e.g., Ex. 1006, Figs. 4, 8, 12. Paul’s figures also show vertical and horizontal capacitive field coupling that occurs between opposite node strips A and B, see Ex. 1006, Figs. 2, 4. Xilinx does not assert that Paul’s alternating node strip layers fail to produce the unclaimed horizontal and vertical

capacitance.

As discussed in the claim construction section, the '609 Patent refers to “silicide plates or strips,” Ex. 1001, col. 3, l. 59, and indicates that “a plate layer is made up of strips,” *id.* at col. 5, l. 5. Although the '609 Patent indicates that *node plate* layers have non-alternating strips, claim 8 does not recite a “plate” layer. *See id.* at col. 6, ll. 57-60 (“The plate layers B, T, B’ do not have alternating conductive strips, but rather all the conductive strips in these layers are connected to either the top node or bottom node.”) Claim 8 also does not recite “non-alternating” node strips (that may imply or require a “plate” layer). Further, the recited term “adjacent” in claim 8 does not imply a plate layer of non-alternating nodes, as IVM argues. *See* Pet. Reply 8–9. In other words, Xilinx’s arguments fail to show a claim distinction over the prior art, as explained further below.

As noted, IVM asserts obviousness of claim 8 based on the combination of Paul and Brennan. *See* Pet. Reply 8; Pet. 40–41. IVM relies on Paul’s teachings for most of the structure recited in claim 8, and relies on Brennan’s teaching of layers having orthogonal strips, as recited in claim 7, from which claim 8 depends. IVM also relies on Paul’s and Brennan’s teachings that suggest any number of capacitive strips and layers. *See* Pet. 38–43 (discussing dependent claims 7 and 8); *id.* at 40 (quoting Ex. 1009, col. 7, ll. 43–46: “traces . . . may be aligned orthogonal to each other”); *id.* at 42 (quoting Ex. 1006, col. 4, ll. 51–52: “using any number of layers of conductive strips,” and relying on Figure 4 in which “Brennan discloses a multi-layer capacitor”). In light of these and other teachings, IVM reasons that “[a] person of ordinary skill in the art would appreciate that the third plurality of conductive strips of Paul could be arranged to be orthogonal to the first and second pluralities of conductive strips as suggested by Brennan.” Pet. 40.

Annotated Figure G, which represents a modified version of Paul's figures, according to Mr. Johnson's first Declaration and the Petition, appears below:

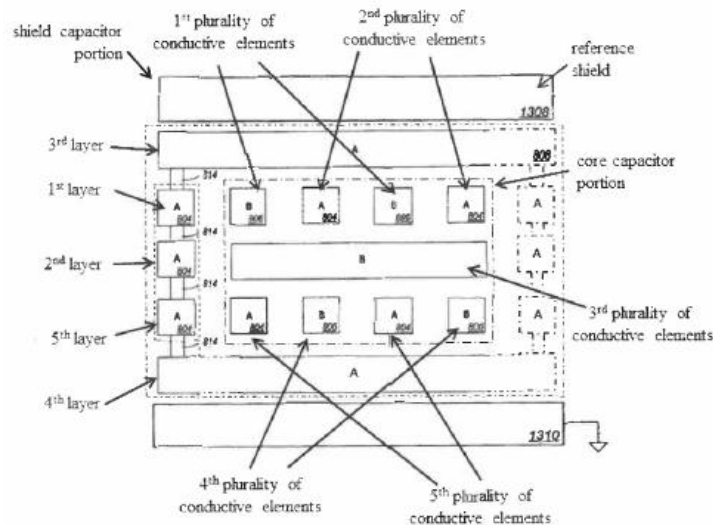


FIG. G of the Johnson Declaration

Annotated Figure G above depicts the third plurality of conductive elements, B, which are orthogonal to adjacent first, second, fourth, and fifth pluralities of conductive elements, generally as recited in claims 7 and 8, according to IVM's Petition. *See* Ex. 1002 ¶ 77; Pet. 43.

IVM points out that the parties' two experts, Dr. Blanchard and Mr. Johnson, agree that the term "adjacent" in claim 8, based on the '609 Patent disclosure, allows conductive elements to be above or below one another. *See* Pet. Reply 8–9 (discussing adjacent capacitor elements B1, B2, B5 as disclosed in the '609 Patent at Fig. 2B, discussing Figure G of the first Johnson Declaration, and citing Ex. 1013 ¶ 21; Ex. 1014, 88, l. 15 – 89, l. 12). Claim 1 corroborates this meaning of "adjacent" by reciting "a second conductive layer adjacent to the first conductive layer." Therefore, claim 8 is broad enough to include "a conductive element . . . forming a third part of a first node" in a layer "adjacent" to, i.e., above or below, the layer having "the third plurality of conductive elements." In other words, contrary to Xilinx's argument, "adjacent" in claim 8 does not signify,

necessarily, a single layer plate or non-alternating node strips in a single plate layer.

Stated differently, although the “third plurality of conductive elements” recited in claim 8 is in a “the second layer” and also forms a “second part of the second node,” according to independent claim 1, the “conductive element electrically connected to and forming a third part of the first node” need not be in that “second layer.” Rather, that conductive element, which forms a third part of the first node, is broad enough to be either in the “second layer” of claim 1, as a “single layer,” or in a layer adjacent to, i.e., above or below, that second layer, as a “double layer.”

As to the former “single layer” situation, conductive elements adjacent to a conductive element and all in the same second layer, Paul suggests non-alternating adjacent conductive strips in the same layer (i.e., a plate layer) as follows: “the conductive strips 404 and 406 *alternate, although other configurations may also be used.*” Ex. 1006, col. 3, ll. 16–17 (italics emphasis added). Such “other configurations” suggest the opposite of alternating nodes—non-alternating nodes, such as Paul depicts in the form of a side shield of node elements A in Figure 8. Ex. 1006. In addition, Brennan explicitly discloses such non-alternating conductive strips in the form of multiple slotted plate layers in a capacitor. See Ex. 1009, Fig. 4. As IVM and Mr. Johnson point out, Paul teaches that a capacitor may have any number of conductive strip layers, further suggesting a modification that employs slotted or non-alternating layers, as Paul and Brennan suggest. See Pet. Reply 7 (citing Ex. 1006, col. 4, ll. 51–52; Ex. 1002 ¶ 77). Employing non-alternating strips in a layer results in more nodes of one type (A) than another (B) and accordingly results in an unequal area, or number, of opposite nodes. This nodal inequality creates an “unbalanced” capacitor that is distinct from a

“balanced” capacitor, according to another of Xilinx’s arguments, as discussed further below. *See* PO Resp. 14–15.

Alternatively, as to the latter “double layer” situation, adjacent conductive strip elements in layers adjacent to the second layer, Paul discloses conductive strip elements B, which IVM annotates in Figure G above as a “1st [or 4th] plurality of conductive elements.” The “1st plurality” in the first layer is depicted as being immediately above, or adjacent to, the “3rd plurality” of conductive node elements B in the second layer. *See supra* annotated Fig. G. Based on this alternative reason, it follows that Paul’s structure, as modified, or not, by Brennan, includes an adjacent “conductive element electrically connected to and forming a third part of the first node,” as set forth in claim 8. *See* Pet. Reply 8–9; Pet. 38–44 (discussing adjacent layers and strip elements).

A subset of the other conductive strips of the “1st [or 4th] plurality of conductive elements” depicted in Figure G correspond to other claim limitations that claim 1 recites and that Xilinx does not challenge. *See supra* annotated Fig. G. Although Figure G does not depict explicitly more than two conductive node strips B in each layer, Paul and Brennan suggest a plurality of such conductive strips—i.e., including a number greater than two.¹

¹ In other words, Paul and Brennan, individually or collectively, suggest any number of conductive strips in a layer. *Compare* Ex. 1006, Figure 7 *with* Figure 8; *see* Ex. 1009, Fig. 4. According to claim 1, “a second part of the first node” must be in the second conductive layer, and “a first part of a first node” must be in a first conductive layer. Claim 8 does not specify the location of the third part of the first node. Accordingly, claim 8 is broad enough to encompass two or more node strips B of Paul (as modified by Brennan), on one side of a layer to form “a first part of a first node”; two or more node strips on one side of an adjacent layer to form “a second part of the first node,” as claim 1 recites; and one or more node strips B on another side of either one of those layers to form “a third part of the first node,” as claim 8 recites. *See* Pet. 42–43 (discussing “adjacent” conductive elements recited

With respect to both “adjacent” alternatives described above (i.e., the single and double layer alternatives), as Xilinx, IVM, and the experts discuss, Brennan’s slotted non-alternating layers provide distinct advantages, such as improving the Q factor and filtering noise in a capacitor by reducing eddy currents that otherwise flow in continuous sheet plate layers. *See* PO Resp. 13–14 (acknowledging Brennan’s benefits); Ex. 1009, col. 6, l. 61 – col. 7, l. 9; Ex. 2006 ¶¶ 23, 26; Ex. 1002 ¶ 75; Pet. 40–41. Brennan’s slotted conductors are similar to Paul’s strip conductors, in comparison to wide continuous sheets that would carry the eddy currents more readily as discussed by Brennan. *See* Ex. 1009, col. 6, l. 61 – col. 7, l. 9. Logically, according to Brennan’s discussion, based on structural similarities, ordinarily skilled artisans would have recognized that Brennan’s described benefits of non-continuous capacitor node layers would flow to non-continuous orthogonal conductor strips in Paul’s modified structure. *See id.*

Balanced versus Unbalanced Capacitors

Turning to Xilinx’s argument, mentioned above, that concerns a distinction between “balanced” and “unbalanced” capacitors, Xilinx asserts that “both Paul and Brennan are directed to balanced capacitors. Paul teaches a capacitor in which the layers of conducting elements are always balanced. . . . Likewise, Brennan teaches a capacitor with equal number of plate layers (balanced).” PO Resp. 14. According to Xilinx, employing one of Brennan’s capacitor layers in Paul’s balanced capacitor structure “is not merely adding another set of nodes to perform their known function, but . . . is changing the functional operation of the resulting capacitor in a way not previously described.” PO Resp. 15. Dr. Blanchard makes the same statement. *See* Ex. 2006 ¶ 35. Citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984), Xilinx implies that IVM’s proposed modification would render Paul’s

in claim 8).

disclosed capacitors unsatisfactory for their intended purpose. *See* PO Resp. 15.

On the other hand, IVM characterizes this dispute about “balanced” capacitors as follows: “Xilinx still does not dispute that the combination of Paul and Brennan disclose[s] all the features of claim 8. Rather, Xilinx relies on an illusory difference between ‘balanced’ and ‘unbalanced’ capacitors to attack the combination of Paul and Brennan.” Pet. Reply 8.

On this record, IVM’s position is more persuasive. Claim 8 does not recite the term “balanced.” IVM responds to Xilinx under the above-discussed assumption that the term “unbalanced” roughly corresponds to a capacitor that has more nodes, or nodal surface area, of one polarity (for example, A) relative to a node of the other polarity (for example, B). *See* Pet. Reply 10; Ex. 1013 ¶ 22; Ex. 1014, 86, 20–24 (discussing unbalanced capacitor in the ’609 Patent at Figure 1 in capacitor 104 due to the greater plate surface area of nodes 112, 120 as compared to the plate surface area of node 108). According to the “BACKGROUND” section of the ’609 Patent, “[p]roviding an equal number of conductive strips in a layer for each node *balances the coupling of each node to the substrate* which is desirable in some applications, but undesirable in others, such as switching applications where it is desirable to have less coupling at one node.” Ex. 1001, col. 1, ll. 63–67 (emphasis added).

In light of this understanding, and addressing Xilinx’s position, Mr. Johnson, IVM’s expert, testifies that Figure 8 of Paul depicts an unbalanced capacitor, with “more conductive elements coupled to Node A than to Node B by virtue of side shield 812.” Ex. 1013 ¶ 22.

Figure 8 of Paul follows:

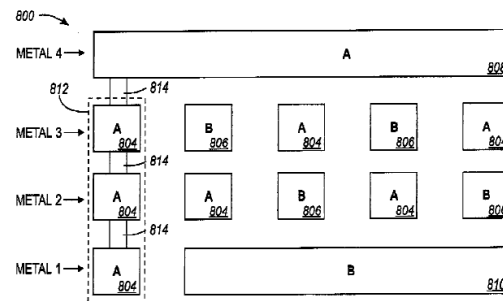


FIG. 8

Figure 8 of Paul, reproduced above, depicts a capacitor having a greater number of node strips A than B. Ex. 1006. According to Mr. Johnson, “[i]f side shield 812 is sufficiently close to elements 804 and 806 located to its right so as to contribute to the total capacitance of the capacitor, then FIG. 8 is an ‘unbalanced capacitor.’” Ex. 1013 ¶ 22.

Temporarily setting aside the question of whether Paul’s Figure 8 represents an unbalanced capacitor, Xilinx’s argument that the proposed combination impermissibly results in an unbalanced capacitor that destroys the function of Paul’s capacitor apparently applies to the single layer alternative—wherein the combined structure results in an unbalanced middle plate layer that only has node strip elements B (thereby forming a large number of node strips B relative to node strips A). See *supra* IVM’s annotated Figure G. The other alternative, the double layer alternative, which results in, according to Brennan’s orthogonal conductor teachings, rotating one of Paul’s balanced layers that has both types of node strip elements A and B, would not result in an unbalanced structure, according to Xilinx’s definition of “balanced” and its characterization of Paul. Therefore, based at least on this latter alternative, Xilinx’s argument is unpersuasive, as it does not account for the full teachings of Paul and Brennan.

Apparently assuming that the obviousness ground only includes the double layer alternative, a balanced middle layer, in related arguments pertaining to

proposed amended claim 20, which Xilinx characterizes as “includ[ing] limitations previously recited in dependent claim 8,” Xilinx maintains that Paul’s Figure 8 capacitor is balanced. PO Reply 2. Xilinx essentially reasons that Paul only teaches balanced capacitors because, in some embodiments, the contribution to capacitance by the wall portion of the shield A, and the longer plate portion A (as compared to plate B), corresponds to what Paul refers to as a ““very small”” “shunt capacitance.”” See PO Reply 3 (discussing and quoting Ex. 1006, Figs. 4, 8; col. 3, ll. 50–56; citing Dr. Blanchard, Ex. 1014, 92, l. 14 – 93, l. 16 (deposition); Ex. 2006 ¶ 26 (declaration)). Xilinx also asserts that its expert, “Dr. Blanchard, has repeatedly asserted that FIG. 8 of Paul is balanced.” PO Reply 3 (citing Ex. 1014, 92, l. 14–93, l. 16).

Xilinx acknowledges that its citation to Paul regarding small shunt capacitance corresponds to a description of Paul’s Figure 4, not Figure 8. See PO Reply 3, n. 1. Contrary to Xilinx’s allegations of similarity, Figure 4 does not depict a side shield, which Figure 8 includes as metal elements 812, 814. Compare annotated Fig. 8 above and Ex. 1006, Fig. 8 with Ex. 1006, Fig. 4. In addition, with respect to Figure 4, Paul states that coupling between underlying node B shield 410 and silicon substrate 402 “is fairly large.” *Id.* at col. 3, ll. 56–57. According to the Background section of the ’609 Patent, as quoted above, this type of single node to substrate coupling, which Paul’s Figure 4 entails, contributes to, or causes, unbalancing. See Ex. 1001, col. 1, ll. 63–67. Further, in his deposition, Dr. Blanchard retreats from his declaration testimony, see Ex. 2006 ¶ 35, and concedes that Paul’s Figure 8 represents an unbalanced capacitor. That is, Dr. Blanchard replies that “[t]he entire capacitor [as represented in Figure 8 of Paul] would be unbalanced,” in response to the following question by IVM’s counsel: “And if you moved what’s labeled 812 to a position where it’s no longer - - it’s not

remote, would that make the capacitor of Figure 8 unbalanced?” Ex. 1014, 95, ll. 18–24.

Still further, Xilinx makes opposite arguments about the strength of the coupling by the outer shield layers, by asserting that “the capacitor of FIG. G now includes *two plates connected to node A, one connected to node B*,” which renders it unbalanced. PO Resp. 15 (emphasis added). If the two plate layers A of annotated Figure G contribute to an unbalanced capacitor, then so must the plate layer A (and wall A) in Figure 8 of Paul. In addition, Paul’s two plate nodes B in Figure 12 similarly would create an unbalanced capacitor, according to Xilinx’s logic. See Ex. 1006. Xilinx’s arguments, which conflict as noted, do not create a claim distinction based on the concept of “balanced,” as IVM argues. See Pet. Reply 8.

The record reflects that the experts, Dr. Blanchard and Mr. Johnson, ultimately agree that Paul discloses or suggests an unbalanced capacitor, depending on the positioning of the shield 812 in Figure 8. In other words, the record reflects the well-known principle that capacitance is related to the distance between the conductors—the closer the conductors, the greater the capacitance or capacitive coupling.²

Xilinx’s arguments, therefore, reduce to a matter of degree that claim 8 does not require—nothing in claim 8 relates to balancing, unbalancing, or the amount of coupling to nodes or shields that might result in unbalancing. Claim 8 also does not specify the relative node numbers and areas. The record also does not support

² “[A] capacitor constructed of two parallel conducting plates of area A, separated by a distance d, has a capacitance $C = \epsilon A/d$, where ϵ is the permittivity, a constant of the insulating material between the plates, and where the linear dimensions of the conducting plates are all very much greater than d.” William H. Hayt, Jr. & Jack E. Kemmerly, 122 ENGINEERING CIRCUIT ANALYSIS (2nd ed. 1971). Ex. 3002.

Xilinx's related argument that modifying Paul's allegedly balanced capacitor to create an unbalanced capacitor would frustrate the purpose of Paul's capacitor. See PO Resp. 15.

As discussed, one modification of Paul, which includes rotating alternating nodes as a middle layer (i.e., a balanced middle layer in the double layer alternative) and loosely coupled shields, according to Xilinx's characterization, does not create an unbalanced capacitor—according to Xilinx's logic. On the other hand, even if claim 8 implicitly requires an unbalanced capacitor, as also discussed, Paul depicts at least three embodiments that disclose or suggest unbalanced capacitors. See Ex. 1006, Fig. 4 (discussing coupling of one node to the underlying substrate); Fig. 8 (large plate shield A and wall shield A) and Fig. 12 (two plate node shields B). Most importantly, IVM points out that the experts agree that “both before and after the modification, Paul's capacitor functions as a capacitor.” Pet. Reply 11, 12 (citing Ex. 1013 ¶ 24; Ex. 1014, 85, l. 7 – 86, l. 12). Therefore, notwithstanding Xilinx's arguments, the record shows that the proposed combination would not render Paul inoperable for its intended purpose of functioning as a capacitor.

Switching, Unbalanced Capacitor

In a related argument that relies on the switching capacitor disclosed in Figure 1 of the '609 Patent, Xilinx argues that “the capacitor of claim 8 is unbalanced . . . and therefore serves as a switching capacitor.” PO Resp. 14. In response, IVM relies again on Xilinx's expert, Dr. Blanchard, who testifies that either a balanced or an unbalanced capacitor “could be used” as a switching capacitor, with possible degradation to noise in unshielded capacitors. See Pet. Reply 11–12 (citing Ex. 1014, 85, l. 7 – 86, l. 12). According to Dr. Blanchard, the unbalanced capacitor depicted in Figure 1 of the '609 Patent has shield 112

connected to a node. The shield to node connection helps to prevent unwanted noise from otherwise coupling to the capacitor, which may occur during switching of voltage in a circuit connected to the capacitor. *See* Ex. 1014, 85, l. 19 – 86, l. 3.

Figure 1 of the '609 Patent follows:

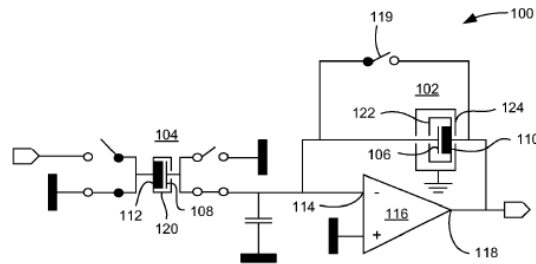


FIG. 1

Figure 1, above, depicts switching capacitor 104 with nodes 108, 112, and shield 120. Ex. 1001, col. 1, ll. 40–54.

Dr. Blanchard also states that because shield 112 connects to node 120 in the capacitor disclosed in Figure 1 of the '609 Patent, he “believe[s]” that the effective surface area of that node renders the capacitor unbalanced. Ex. 1014, 86, ll. 4–24. Figure 1 does not disclose specifically relative areas of nodes, as it shows a general depiction of a capacitor circuit element, without apparent scaling.

In any event, this line of argument and testimony, directed to a switching capacitor, or an unbalanced switching capacitor, which the '609 Patent discloses, does not help to overcome IVM's showing of obviousness. Claim 8 does not recite an unbalanced capacitor, a switch, or a switching capacitor. Dr. Blanchard's testimony relates to shielding and noise in relation to disclosed Figure 1 of the '609 Patent. This testimony about what the '609 Patent discloses fails to show that the shielding recited in claim 8 necessarily requires unbalancing or switching. Further, even if the result of combining Paul and Brennan amounts to an unbalanced capacitor, the experts agree that it would still function as a capacitor, according to the record, as previously discussed.

Even further, the '609 Patent explains, in connection with Figure 1, that “[i]n some embodiments, the bottom node shield contributes to the over-all capacitance of the integrated circuit by coupling to the top node.” Ex. 1001, col. 3, ll. 61–64 (emphasis added). In general, less coupling of one node to a substrate (unbalancing) is desirable for some applications, and not for others that involve switching. *Id.* at col. 1, ll. 63–68. These disclosures imply that claim 8, which does not quantify the top and bottom node coupling or node to substrate coupling, or other balancing or unbalancing features, and does not recite switching, does not implicitly require unbalancing or switching.

It follows that the alleged distinction by Xilinx that rests on balancing or unbalancing amounts to matters of degree that are not quantified on this record. Xilinx does not direct attention to evidence that quantifies the amount of unbalancing (or its effect on noise reduction), as it relates to claim 8 or the disclosed embodiments. Paul’s shield portions 812 and 808 in Figure 8 directly connect together in a fashion similar to that of Figure 1 of the '609 Patent to form one large capacitor node. Both capacitors appear to have relatively larger areas of one node connected together, as compared to the total area of the other node. *Compare* Ex. 1001, Fig. 1 *with* Ex. 1006, Fig. 8.

In any event, claims generally do not incorporate disclosed features of exemplary embodiments described in the specification. Xilinx does not dispute that claim 8 reads on the structural limitations of Paul’s modified capacitor, as IVM asserts.³ Although the record reflects the desirability of employing unbalanced capacitors as switching capacitors, claim 8 does not recite or require implicitly a switch or an unbalanced capacitor, as Mr. Johnson, addressing Dr.

³The Petition describes as obvious further modifications to Paul’s capacitor that include further shielding, a description that Xilinx does not dispute. See Pet. 43.

Blanchard, further points out, and as IVM argues. See Pet. Reply 11–12; Ex. 1013 ¶ 23.

Xilinx does not present separate arguments for claim 9, which depends from claim 8. Instead, Xilinx relies on arguments presented for claim 8 and does not dispute the showing in IVM’s Petition that outlines the obviousness of claim 9. See PO Resp. 15. The record shows that combining Brennan’s and Paul’s shielded capacitors would have resulted in a predictable variation of Paul’s capacitor, including orthogonal conductor elements, as claims 8 and 9 require.

Therefore, based on the record evidence in light of the arguments presented, IVM has shown “by a preponderance of the evidence,” 35 U.S.C. § 316 (e), that claims 8 and 9 would have been obvious over the combination of Paul and Brennan.

D. Claim 18

Independent claim 18 follows:

18. A capacitor in an integrated circuit (“IC”) comprising:
a first plate formed in a first conductive layer of the IC;
a second plate formed in a substrate of the IC;
a gate dielectric layer disposed between the first plate and the second plate;
a shield plate formed in a second conductive layer of the IC having a perimeter electrically connected [to] the second plate so as to form an electrical shield around the first plate; and
a plurality of contacts formed between the shield plate and the second plate;
wherein the shield plate has a gap through which an electrical contact to the first plate extends, and the shield plate, the plurality of contacts, and the second plate provide electrical shielding for the first plate.

In essence, independent claim 18 recites, *inter alia*, “a first plate . . . ; a second plate formed in a substrate of the IC; a gate dielectric . . . between the first plate and the second plate; . . . [and] a shield plate [that] has a gap.”

IVM asserts that the combination of Anthony and Marotta renders claims 18 and 19 obvious. Pet. 45–51. The primary dispute involves the second plate recited in claim 18. IVM relies on shield plates “36/46” in Anthony’s Figures 3A and 4 to suggest the disputed second plate. See PO Resp. 16 (discussing IVM’s reliance, citing Pet. 46).⁴ Xilinx maintains that the shield plate 36/46 in Anthony is “not a plate of the capacitor, but is [a] reference shield.” *Id.*

IVM's annotated Figure 4 of Anthony from the Petition follows:

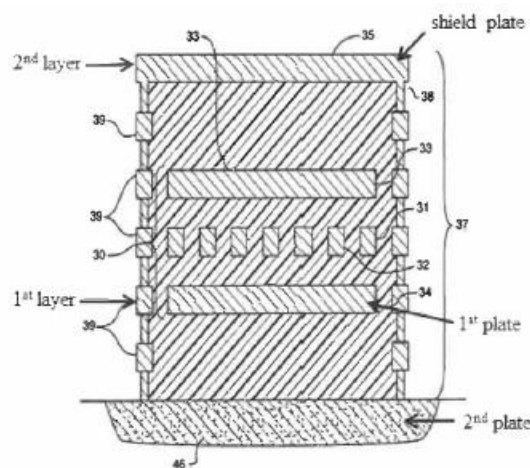


FIG. 4 (annotated)

IVM's annotated Figure 4 of Anthony depicts how IVM reads the claimed first plate, second plate, and shield plate of claim 18 onto Anthony's capacitor layers. *See* Pet. 46.

Xilinx does not explain persuasively why Anthony's shield plate 36/46 does not constitute a second plate of the capacitor structure. Xilinx relies on arguments presented in connection with claim 2. *See* PO Resp. 9, 16. However, claim 2, in contrast to claim 18, explicitly requires the plate to be a node of the capacitor;

⁴ As the quotation “36/46” indicates, the parties typically refer to the two shield plates together, even though each is a bottom plate in similar (i.e., different) embodiments of Anthony. See PO Resp. 16; Pet. 46; Ex. 1007, Fig. 3B (bottom plate 36), Fig. 4 (bottom plate 46).

therefore, the same arguments do not apply here. This claim comparison coalesces with the claim construction of “plate”—a “plate” is not necessarily a capacitor node, according to the disclosure of the ’609 Patent. Xilinx’s arguments discussed in connection with claim 8 above further corroborate the claim construction here and imply that a “plate” signifies a type of structure (for example, multiple connected strips), and not necessarily structure that functions or connects as a node.

During the hearing, tracking arguments made in the Preliminary Response about the “function of a second plate of a capacitor,” Prelim. Resp. 11, Xilinx argued that shield plate 36/46 cannot be a capacitor second plate as recited in claim 18 because it contributes negligible capacitance to the capacitor of Anthony. See Tr. 61, ll. 6–13. Xilinx reasoned that Anthony describes the capacitance between shield plates 36/46 and plate 34 as “nearly eliminated,” or, similarly, that “the capacitance is minimal” or “negligible” because the plates are “far enough apart.” *Id.* This argument is not persuasive for several reasons.

First, the ground of obviousness is based on the combination of Anthony and Marotta. Claim 18 recites “a gate dielectric layer disposed between the first plate and the second plate.” To address the recited gate dielectric, IVM combines Marotta with Anthony to show that such a thin dielectric would have been obvious to employ between Anthony’s first (34) and second (36/46) plates, *inter alia*, “to offer the most area-efficient capacitor design for a specific capacitance value.” See Pet. 48, 46–49; Ex. 1002 ¶¶ 83–85.

Xilinx does not challenge this aspect of IVM’s showing that addresses the obviousness of employing a gate dielectric between the first and second plates. See Tr. 44, ll. 12–19 (IVM making a similar point and discussing Marotta’s gate dielectric layer). Mr. Johnson outlines the basis for the obviousness of the

modification. Ex. 1002 ¶¶ 83–85. Modifying Anthony to form a capacitor with a gate dielectric, based on Marotta’s teachings, as IVM proposes, increases the capacitance between Anthony’s two plates 34 and 36/46. For example, discussing Marotta’s “poly/gate oxide/N-well capacitor,” Mr. Johnson testifies that “[a] gate dielectric, [the gate oxide,] as typically representing the thinnest dielectric layer on-[c]hip, would therefore offer the most area-efficient capacitor design for a specific capacitance value.” See Ex. 1002 ¶ 84 (quoting and discussing Ex. 1011, col. 6, ll. 24–39). Accordingly, because Xilinx does not challenge the proposed gate dielectric combination that results in capacitance between Anthony’s plates 34 and 36/46, Xilinx’s arguments that plate 36/46 is not a capacitor plate, allegedly because the plate 36/46 does not contribute significantly to the capacitance, is unpersuasive. See PO Resp. 9, 16; Prelim. Resp. 11; Tr. 61:1–23.

Second, claim 18 requires the “second plate formed in a substrate” to “provide electrical shielding for the first plate.” As a substrate reference shield, Anthony’s second plate 46 provides electrical shielding for first plate 34, and Xilinx does not argue that it does not. See Ex. 1007, Fig. 4; Pet. 46. In other words, contrary to Xilinx’s arguments in connection with claim 2, claim 18 does not require the second plate to be a node of the capacitor or to contribute significantly to capacitance. In contrast, as explained above, Xilinx’s claim 2 specifically recites such a node connection, and Xilinx emphasizes that connection as a distinction over the prior art. See PO Resp. 6 (discussing claims 1 and 2).

Additional evidence of record supports the first and second reasons: The ’609 Patent corroborates the general understanding that a shield plate typically can be considered to be part of a capacitor, regardless of whether it is a capacitor node or otherwise contributes appreciably to capacitance. For example, the ’609 Patent states that “[t]he integrated *capacitor includes an optional ground shield* 286 . . .

basically forming a Faraday cup.” Ex. 1001, col. 8, ll. 20–22 (emphasis added); Fig. 2C. “The *optional* reference shield *includes* . . . the *shield plate 224*.” *Id.* at col. 7, ll. 18–19 (emphases added).

Third, related to the first and second reasons, as the Institution Decision finds, Xilinx acknowledges that “a capacitor structure simply requires ‘a first plate and a second plate with a dielectric interposing the plates.’” Inst. Dec. 12 (quoting Paper 9 at 8). Based on the understanding of the well-known capacitor structure, the Institution Decision reasons that “IVM’s annotated Figure 4 shows a bottom or second shield plate 46 and a first plate 34 that has a dielectric interposing the two plates and satisfies the claimed capacitor structure, regardless of what Anthony calls the structure.” *Id.* (citing Pet. at 46, IVM’s annotated Fig. 4 of Anthony).

Anthony corroborates this understanding of a capacitor, and describes generic capacitor structure that employs “inter-metal dielectrics which separate metal interconnections” and other “capacitors [that] can be vertical, with horizontal metal plates; lateral, with vertical plates; or mixed, employing capacitance between both vertically-separated and horizontally-separated plates.” Ex. 1007, col. 1, ll. 13–20. Mr. Johnson further corroborates this well-known understanding: “It is further known that areal capacitance density is inversely related to the thickness of the capacitor dielectric layer.” Ex. 1002 ¶ 84.⁵

Therefore, even without Marotta’s thin gate dielectric, contrary to Xilinx’s arguments, Anthony’s shield structure, including second plate 46, does contribute to the capacitance, even though the second plate is not a capacitor node. Anthony generally discloses shielded or unshielded capacitors, situated inside of an outer capacitor shield cage to shield the inner capacitor portion from external circuit

⁵Well-known capacitor properties also corroborate this testimony. *See* note 2 (capacitance is related to the distance between the conductors, *d*, which corresponds to the thickness of the dielectric(s) therebetween).

nodes. The multi-layer external shield includes metal plate 35 and poly/diffused plate 36/46, with shield walls 37 connected by, and made partially of, conductor vias. See Ex. 1007, col. 4, ll. 33–54. According to Anthony, external shield structure 35–37 “*add[s] parasitic capacitance from terminal 31*, and also a slight parasitic capacitance from terminal 32, to the shield, which is usually at ground potential.” *Id.* at col. 4, ll. 55–59 (emphasis added). Outer terminal 31 connects to, and includes, self-shielding plates 33 and 34. *Id.* at col. 4, ll. 4–9, 33–40 (embodiment of Figure 2B is inside shield of Figures 3A, 3B, 4). Anthony also explains that this “outer terminal [31, 34] is either unshielded or may have explicit added shielding [35, 36/46, 37], *which adds parasitic capacitance.*” *Id.* at col. 5, ll. 9–10 (emphasis added).⁶ This parasitic capacitance from the shield creates a trade-off, as a “side-effect” or “compromise.” *Id.* at col. 4, ll. 54–63. That is, external shield plates add parasitic capacitance, but also provide shielding from external circuit nodes. See *id.* at col. 4, l. 49 – col. 5, l. 12.

Xilinx’s arguments apparently rely on Anthony’s description of negligible capacitance contributed by an irrelevant innermost terminal of the capacitor structure. Describing that negligible capacitance, Anthony states that “[t]hese capacitors are inherently asymmetrical: the inner terminal is fully shielded by the outer terminal and has negligible parasitic capacitance.” Ex. 1007, col. 5, ll. 6–8. Contrary to Xilinx’s assertions, that “negligible” parasitic capacitance between the inner shielded terminal 22 or 32, and the outer shields 35, 36/46, is not related to a claim feature at issue here. As discussed above, the relevant parasitic capacitance

⁶ The “outer terminal” 21, 24, explicitly referenced in the quotation, Ex. 1007, col. 5, ll. 5–6, corresponds to the outer terminal 31, 34. In other words, both outer terminals connect to capacitor shield plates 23, 24, and 33, 34, thereby forming self-shielded capacitors. These capacitor node/shield plates 33, 34, part of the outer terminal, contribute parasitic capacitance to the external shield 35–37, as explained. See Ex. 1007, Figs. 2B, 3B, col. 4, ll. 20–69.

between plate 34 and outer shield structure 35, 36/46, 37, creates a trade-off based on the side-effect (i.e., parasitic capacitance) of the shield. *See id.* Figs. 2A, 2B, 3A, 3B.

Therefore, Xilinx's arguments are based on an implicit (unclaimed) capacitance that is not quantified on this record. Xilinx does not quantify any implicit amount of capacitance involved in the "gate dielectric layer disposed between the first plate and the second plate," as claim 18 recites. (Claim 18 also does not preclude other dielectrics, in addition to the thin gate dielectric, between the first and second plates.) Therefore, any implicit contribution to capacitance by the second plate, which, as set forth in claim 18, is not a capacitor node, may range from insignificant to significant, depending on the (unclaimed) distance between the first and second plates, and the (unclaimed) properties of the dielectric(s) therebetween.

Hence, even if claim 18 requires more than negligible capacitance between the first and second plate in order for the second capacitor plate to read on Anthony's second plate, the record shows that Anthony's two plates, with or without Marotta's gate dielectric touching both plates, contribute a parasitic capacitance between the two plates, which Anthony describes as more than negligible.⁷ *See* Pet. Reply 13 (arguing that Anthony satisfies the structure recited in claim 18); Tr. 73–74 (similar argument). Claim 18 does require explicitly the second plate to "provide electrical shielding," and Xilinx does not argue that the prior art structure of Anthony, as modified by Marotta, fails to provide such

⁷ As noted, Xilinx does not respond to IVM's reliance on Marotta's gate dielectric. On this record, claim 18 is reasonably broad enough to be satisfied by modifying Anthony so as to place Marotta's gate dielectric somewhere between the first and second plates, with or without touching the two plates, as another capacitor dielectric, for example, within Anthony's shield structure to provide shielding thereto.

shielding.

Therefore, based on the record evidence in light of the arguments presented, Petitioner has shown “by a preponderance of the evidence,” 35 U.S.C. § 316(e), that claim 18 would have been obvious over the combination of Anthony and Marotta.

E. Claim 19

Claim 19 depends from claim 18 and recites the following: “The capacitor of claim 18 wherein the first conductive layer is a first poly layer, the substrate comprises silicon and [the] second plate is formed in an N-well of the substrate and the shield plate is formed in a second poly layer of the IC.”

Figure 4B of the '609 Patent, annotated by Xilinx, follows:

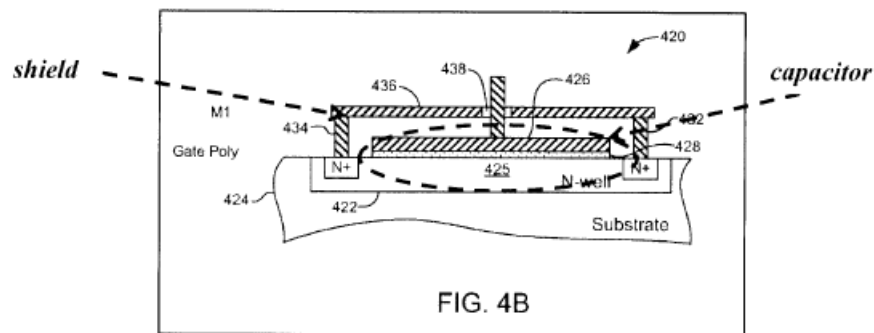


Figure 4B above depicts exemplary structure representing the following elements recited in dependent claim 19: first plate 426 formed in a first conductive poly layer (see independent claim 18), a second plate formed in conductive N-well 422, and shield plate layer 436 having gap 438 therein formed in a second poly layer. See Prelim. Resp. 9; Ex. 1001, col. 10, l. 62 – col. 11, l. 5.

IVM asserts that the combination of Anthony and Marotta renders dependent claim 19 obvious. Pet. 50–52. Xilinx does not challenge explicitly IVM’s assertion that the combination of Anthony and Marotta renders obvious certain recited limitations, including, *inter alia*, a shield plate gap, and a second plate

formed in an N-well of the substrate, as claim 19 requires.⁸ Rather, Xilinx asserts that the combination fails to render obvious “one poly layer used for a [first] plate of the capacitor and the other poly layer used for a shield plate.” See PO Resp. 17 (citing Ex. 2006 ¶¶ 20, 25).

Two Poly Plate Layers

Xilinx focuses its arguments on the “poly” elements recited and contends that it would not have been obvious to replace two metal plate layers in Anthony with two poly layers: “Neither of the references teaches an IC with two poly layers, one poly layer used for a [first] plate of the capacitor and the other poly layer used for a shield plate.” PO Resp. 17. Accordingly, the central issue presented by Xilinx’s arguments is the obviousness of substituting two poly layers for two metal capacitor layers in Anthony.

As to the claimed first plate formed in a first poly layer, IVM points out that Marotta discloses top capacitor plate layer 302 of poly, and that Anthony discloses capacitor shield plate 36 of poly, and reasons that the combined teachings render it obvious to form plate 34 of Anthony in a first poly layer. See annotated Fig. 4 from Anthony (first plate 34); Pet. 50–51 (citing Ex. 1011, col. 5, ll. 30–34, Fig. 3; Ex. 1007, col. 4, ll. 49–53). Xilinx does not dispute the underlying facts that support the contention. See PO Resp. 17.

As to the claimed shield plate formed in a second poly layer, based on similar teachings, including Marotta’s upper poly capacitor plate 302 and Anthony’s poly shield plate 36, IVM also reasons that skilled artisans would have found it obvious to combine the teachings and replace upper metal shield layer 35

⁸ As to the latter limitation, IVM relies on the combination of teachings: Anthony’s capacitor shield plate 46 is in a well, and Marotta discloses a substrate having an N-well capacitor, thereby rendering obvious “a second plate formed in an N-well of the substrate,” as claim 19 requires. See Pet. 51–52.

of Anthony's capacitor with a second poly layer. See Pet. 51. IVM relies partially on Mr. Johnson's testimony that a known semiconductor fabrication process termed "double poly," employed to form gate level capacitance, "supports the combination." *Id.* at 51 (quoting Ex. 1002 ¶ 88).

For reasons similar to those expressed above with respect to claim 2, the record shows that replacing two metal layers with two poly layers would have been obvious to a person of ordinary skill in the art. As noted, Anthony specifically teaches that "[a]s an alternative to the use of a metal layer as shown in FIG. 3B (which may be needed for interconnect purposes)[,] the bottom shield plate 36 can be implemented with a poly-silicon or diffusion layer." Ex. 1007, col. 4, ll. 49–52. In sum, Anthony teaches replacing a metal capacitor shield layer with a poly layer, and Marotta discloses a poly layer as a top plate of a capacitor.

The record shows that poly and metal have similar qualities of conductivity for capacitor plate or shield purposes, because they were employed in the prior art as capacitor shields and plates. Replacing one type of conductor for another would have resulted in a predictable result, conductive capacitor layers functioning to provide capacitance, shielding, or both. As noted with respect to claim 2 above, IVM presents other persuasive reasons for using poly in place of metal, such as making convenient connections and saving metal for other purposes. As explained with respect to claim 2, "when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result." *KSR*, 550 U.S. at 416 (citation omitted).⁹

⁹ The Board recognizes Dr. Blanchard's deposition testimony that, typically, a double poly process involves two poly layers with one directly above the other, because low cost metal layers, such as aluminum, therebetween otherwise would not survive the high temperatures associated with poly (although more expensive

Shield Plate Gap

The parties agree that Anthony discloses first plate 34, shield plate 35, and multi-layer wall 39 as metal conductors, instead of poly conductors as claim 19 requires. *See* Ex. 2006 ¶ 19; Pet. Reply 13–14; PO Resp. 17. In addition to the poly shield plate limitation, claim 19, by its dependence from claim 18, also requires the shield plate to have a gap therein: Claim 18 recites “the shield plate has a gap through which an electrical contact to the first plate extends.”

Xilinx does not discuss the gap limitation. IVM addresses it by reading the “shield plate formed in a second poly layer” of claim 19 as allowing the shield plate to be formed in a poly layer and in other layers. Simply put, IVM contends that the shield plate is a multi-layered plate that includes one poly layer and at least one metal layer, which has the claimed gap therein. Specifically, IVM asserts that the claimed shield plate reads on Anthony’s shield plate 35 and multi-layer wall 39, which includes a “gap.” IVM points to the gap in multi-layer wall 39 through which terminal 31 extends. *See* Pet. 49–50 (discussing shield plate limitations, Ex. 1007, Fig. 3A); Ex. 1007, Figure 3B, col. 4, ll. 42–48.

Although the embodiment represented by Figure 4B of the ’609 Patent, above, appears to depict a single layer poly shield plate that has a gap therein, claim 19 does not recite that the shield plate consists of a single layer. As discussed in the claim construction section, according to the ’609 Patent, a plate may be discontinuous, and also have a top layer, a bottom layer, and multi-layered

noble metal layers may survive the poly process). *See* Ex. 1014, 61–62. However, Xilinx does not rely on this testimony, or point the Board to its significance, in attempting to overcome IVM’s obviousness showing. Moreover, claim 18 recites “a plurality of contacts” that essentially would be between or under the two poly layers associated with claim 19, although the ’609 Patent indicates that those contact layers would be metal in one embodiment, but would be eliminated in a double poly embodiment. *See* Ex. 1001, col. 10, ll. 51–61.

sides. In addition, a term such as “a . . . layer,” which appears in the open-ended claim 19 phrase, “a shield plate formed in *a* second poly layer of the IC” (emphases added), normally signifies formation (of the plate, in this case) in one or more layers. See *TiVo, Inc. v. EchoStar Commc’ns Corp.*, 516 F.3d 1290, 1303 (Fed.Cir.2008). (“As a general rule, the words ‘a’ or ‘an’ in a patent claim carry the meaning of ‘one or more.’”) “The exceptions to this rule are extremely limited: a patentee must ‘evinced a clear intent’ to limit ‘a’ or ‘an’ to ‘one.’” *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed.Cir.2008) (citation omitted). Therefore, claim 19 reasonably allows “the shield plate [to be] formed in a poly layer” and other conductive layers.

Significantly, as noted, Xilinx fails to discuss the gap. In other words, Xilinx does not challenge IVM’s showing in the Petition that Anthony discloses or renders obvious the claimed gap in the shield plate, and otherwise fails to assert in a clear fashion that claim 19 restricts the shield plate to a single layer poly shield plate. See Pet. 49–50; PO Resp. 17. Based on the arguments and evidence of record, the claimed shield plate and gap structure reasonably is broad enough to read on Anthony’s modified multi-layer shield plate 35, 39 and gap, as set forth in the Petition. See Pet. 50; Ex. 1007, Figs. 2A, 2B 3A, 3B, Fig. 4 (terminal 32 of first plate 34 extends through a gap in the intermediate layer of wall 39, which has a perimeter surrounding first plate 34).

Therefore, based on the record evidence in light of the arguments presented, IVM has shown “by a preponderance of the evidence,” 35 U.S.C. § 316(e), that claim 19 would have been obvious over the combination of Anthony and Marotta.

F. Declaration Evidence

Xilinx also argues that the proposed grounds of obviousness, with respect to claims 2, 8, 18 and 19, are improper under 35 U.S.C. § 311(b), because IVM relies

partially on declaratory evidence, instead of patents or printed publications. *See* PO Resp. 9–10, 16–17. IVM contends otherwise. *See* Pet. Reply 12–14.

Xilinx’s arguments are not persuasive. Xilinx’s allegations in connection with claims 2, 8, 18, and 19 are similar. However, Xilinx does not explain specifically why the declarations are improper with respect to claims 2, 8, and 18. *See* PO Resp. 9–10, 16. With respect to claim 19, Xilinx argues that “a double-poly layer is not disclosed in the prior art,” thereby implying that it is improper to rely on Mr. Johnson’s declarations that discuss this technique in terms of its status as a known prior art procedure. *See* PO Resp. 17. In contrast to claim 19, claim 2 requires only one poly layer, and claims 8 and 18 do not recite a poly layer. Therefore, Xilinx’s claim 19 arguments, premised on Mr. Johnson’s testimony about two poly layers, do not apply to claims 2, 8, and 18. The ensuing discussion applies to claim 19.

Section § 311(b) states that “[a] petitioner . . . may request to cancel as unpatentable 1 or more claims only on a ground raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.” However, 35 U.S.C. § 312 (a)(3) states that a petition may include “(A) copies of patents and printed publications . . . ; and (B) affidavits or declarations of supporting evidence and opinions, if the petitioner relies on expert opinions.” Xilinx fails to explain adequately why the declaration evidence here is improper as “supporting evidence” under 35 U.S.C. § 312(a)(3)(B).

During the oral hearing, Xilinx explained that the two statutory provisions can be reconciled by prohibiting declaration evidence if it supplies “missing [claim] elements that are not shown in a printed publication.” Tr. 63, ll. 11–12. Xilinx argued that the claim element missing from the prior art references is a “double poly process . . . and that is a specific element of claim 19.” *See* Tr. 62, ll.

15–16; *accord* PO Resp. 17. Xilinx acknowledges that a single prior art reference may establish obviousness, when, for example, an expert provides motivation for making a modification, but argues that, generally, it would be improper to allow an expert to opine on the obviousness of a missing claim element in an *inter partes* review. *See* Tr. 65, ll. 18–24. IVM counters that its expert declaration “was provided to explain how one skilled in the art would view Anthony and Marotta.” Pet. Reply 14.

IVM’s declaration evidence is proper pursuant to the AIA statutory scheme and according to Federal Circuit precedent involving reexamination proceedings under an analogous statutory scheme. Generally, the Federal Circuit has endorsed the use of declaration evidence in reexamination proceedings, which have the same statutory requirement as *inter partes* review proceedings—“prior art consisting of patents or printed publications.” 35 U.S.C. § 305 (*ex parte* reexamination); 35 U.S.C. § 311(b) (*inter partes* review); *see In re Baxter Travenol Labs*, 952 F.2d 388, 390 (Fed. Cir. 1991) (in a reexamination proceeding, “extrinsic evidence may be considered when it is used to explain, but not expand, the meaning of a reference” for anticipation); *Randall Mfg. v. Rea*, 733 F.3d 1355 (Fed. Cir. 2013) (discussed next).

In Randall Manufacturing, an appeal of a reexamination proceeding, the Federal Circuit reminded the Board to consider the following evidentiary approach:

In *KSR*, the Supreme Court criticized a rigid approach to determining obviousness based on the disclosures of individual prior-art references, with little recourse to the knowledge, creativity, and common sense that an ordinarily skilled artisan would have brought to bear when considering combinations or modifications. *KSR*, 550 U.S. at 415–22 Rejecting a blinkered focus on individual documents, the Court required an analysis that reads the prior art in context, taking account of “demands known to the design community,” “the

background knowledge possessed by a person having ordinary skill in the art,” and “the inferences and creative steps that a person of ordinary skill in the art would employ.” *Id.* at 418 This “expansive and flexible approach,” *id.* at 415 . . . , is consistent with our own pre-KSR decisions acknowledging that the inquiry “not only permits, but *requires*, consideration of common knowledge and common sense.” *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed.Cir.2006).

Randall Mfg., 733 F.3d at 1362.

Although *Randall Manufacturing*, 733 F.3d at 1362, highlights prior art documentary evidence as “[o]ne form of evidence . . . [that is] perhaps the most reliable,” the court endorses other types of evidence, including declaration evidence, as signaled by its citation to *Perfect Web Technologies, Inc. v. InfoUSA, Inc.*, 587 F.3d 1324 (Fed. Cir. 2009). *Perfect Web* involves declaration evidence about common sense and general knowledge surrounding a claim element that was not disclosed in the references—i.e., “step (D) merely involves repeating earlier steps” and such “repetition would have been known to a person of ordinary skill.” *Id.* at 1330.

Pursuant to a long thread of obviousness precedent, including *Baxter*, *KSR* and *Randall Manufacturing*, the Board must consider, *inter alia*, background knowledge, common knowledge, and common sense in a proper obviousness determination. IVM’s declaration evidence falls within these required review categories under the “expansive and flexible approach” of *KSR*. The evidence shows that double-poly layers were background or common knowledge in the art, at the time of the invention, as corroborated by Xilinx’s expert, who essentially agrees with IVM’s evidence. See Pet. Reply 14 (discussing the experts, citing Ex. 1002 ¶¶ 86–88; Ex. 1014, 60, ll. 4–12); see also discussion *supra* of claim 2. The testimony about double-poly layers also points to the level of skill involved. Further, it rebuts Xilinx’s initial argument that double poly processes were not

known in the prior art, *see* PO Resp. 17—although Xilinx later admitted during the oral hearing that double poly processes were known in the prior art, Tr. 63, ll. 17–19.

Similar to the situation in *Perfect Web*, 587 F.3d at 1330, where the expert evidence was “not necessary” to support obviousness, the declaration evidence here is not necessary, but it supports the Board’s obviousness determination. The prior art references, by themselves, suggest that replacing one type of conductor for another, for at least one or two layers, would have resulted in a predictable result, a conductive capacitor layer functioning to provide capacitance, shielding, or both.

G. Xilinx’s Motion to Amend Claims

In its Motion to Amend, Xilinx cancels claims 1–17, maintains original claims 18 and 19, and adds substitute claims 20–34. *See* Mot. to Amend. IVM’s Opposition contests the Motion to Amend on procedural and substantive grounds. *See* Opp. Xilinx’s Patent Owner Reply responds to IVM’s Opposition. *See* PO Reply.

Issued claims 18 and 19, and Proposed Substitute Claims 20–29

Xilinx presents issued claims 18 and 19 and proposed substitute claims 20–29 as amendments. Under 37 C.F.R. § 42.121(a)(2)(i), “[a] motion to amend may be denied where . . . [t]he amendment does not respond to a ground of unpatentability involved in the trial.” The moving party, in this case Xilinx, carries the burden to support its motion and show that the amended claims are patentable. *See* 37 C.F.R. §§ 42.20 (c) (burden on moving party), 42.121(a) (motion to amend). Presenting the same claim, the same claim in an independent form, or a broader version of the same claim, as Xilinx does in its Motion to Amend, fails, under the rule, to respond to the grounds of unpatentability asserted against those

claims.

Specifically, this Final Written Decision and the Institution Decision address the merits of claims 18 and 19. Presenting issued claims 18 and 19, and designating them as proposed amendments, does not address the merits in a responsive manner, fails to alter the outcome, and is improper.

Proposed independent claim 20 combines the limitations recited in issued claims 1 and 8, but omits limitations from issued dependent claim 7, from which claim 8 depends. In other words, proposed claim 20 is broader than claim 8 but narrower than claim 1. The Board considers claim 20 to be a proposed substitute for issued claim 1. *See* Mot. to Amend 12; PO Resp. 15; Opp. 3 (noting that “newly presented claim 20 fails to incorporate the subject matter of claim 7 and is therefore broader than claim 8”). Claim 21 is the same as issued claim 2, albeit written in independent form. Mot. to Amend 12–13. Claim 27 is the same as issued claim 9, except for the new dependency from claim 20. *Id.* at 13.

Xilinx relies on arguments presented for claims 2 and 8 to allege patentability for claims 20–29. PO Resp. 18–19. Xilinx’s arguments directed to claims 20–29 are improper procedurally, because a patent owner may not include arguments for proposed amended claims in a patent owner response. *See* 37 C.F.R. § 42.120 (“patent owner may file a response *to the petition*”) (emphasis added). Rather, these arguments should have appeared in the Motion to Amend in order to support that motion. *See Idle Free Sys., Inc. v. Bergstrom, Inc.*, IPR2012-00027, Paper 26 (PTAB June 11, 2013). Also, Xilinx’s incorporation of arguments directed to claims 2 and 8 by reference to its Patent Owner Response is improper procedurally under 37 C.F.R. § 42.6(a)(3).

In any event, even if Xilinx’s arguments are considered, Xilinx has not met its burden of showing that the claims are patentable. In summary, Xilinx relies on

the arguments presented in connection with issued claims 2, 8, 18, and 19, arguments addressed above in this Final Written Decision. Setting aside that the failure to further limit claims 18–29 renders the proposed amendments nonresponsive to the grounds of unpatentability, presenting the same or broader claims fails to overcome the merits addressed above in connection with the issued claims. Simply put, presenting the same or broader claims as amended claims fails to satisfy Xilinx’s burden to show patentability.

In its Patent Owner Reply, Xilinx, in response to IVM’s Opposition, presents arguments directed to claims 20, 21, and 30. These arguments, procedurally, do not reply properly to IVM’s Opposition, and, substantively, they are not persuasive. Xilinx’s arguments directed to claims 20 and 30 essentially repeat arguments made previously in connection with issued claims 2, 8, 18, and 19, focusing on the concepts of “double poly” and “balancing.” See PO Reply 2–3, 5. For the reasons discussed above, the arguments are not persuasive.

With respect to claim 21, Xilinx presents arguments, slightly different in form only, that are not persuasive, because they track the thrust of the arguments presented in Xilinx’s Response in connection with issued claim 2. For example, Xilinx presents a new “Graphical representation of claim 21,” mischaracterizes the required basis for the ground of unpatentability (by conflating a connection between the reference shield and capacitor shield that the obviousness ground does not propose or require), and argues the references separately. See PO Reply 4–5 (emphasis omitted).

Procedurally, IVM states correctly in its Opposition that Xilinx relied upon arguments in connection with issued claim 2 to urge the patentability of claim 21. See Opp. 6 (pointing out and responding to the reliance on claim 2 arguments); *accord* Mot. to Amend 15 (asserting that “patentably distinct features” flow from

“the claims as originally issued” and that “[p]roposed claim 21 is the same as original claim 2”). A proper responsive reply to IVM’s assertion that Xilinx presented arguments in connection with claim 2 does not include a presentation of new arguments by Xilinx in its Reply. On the other hand, if the arguments directed to claim 21 are not new, then the discussion of claim 2 above applies. In either case, Xilinx fails to satisfy the burden of showing patentability of claim 21 in its Motion to Amend. *See* 37 C.F.R. § 42.121(a).

Proposed Substitute Claims 30–34

With respect to claims 30–34, Xilinx presents arguments for claim 30. According to Xilinx,

claim 30 is the same as original claim 13, except that it further limits the claimed fourth conductive layer to be a ‘poly’ layer. This is patentably distinct from the prior art because the fourth conductive layer is part of the shield capacitor portion, which is connected to and part of the second node of the capacitor and the second plurality of conductive elements.

Mot. to Amend 15.

In its Opposition, IVM asserts that claim 30 would have been obvious over the combination of Paul and Anthony, or the combination of Anthony and Bi. Opp. 6. IVM notes that Xilinx does not dispute the obviousness of issued claim 13 over those combinations. Opp. 6; *accord* Inst. Dec. 10–11 (instituting on the applicable grounds involving the noted combinations). In other words, Xilinx and IVM focus on the asserted obviousness of further limiting the claimed fourth conductive layer, as recited in issued claim 13, to a poly layer. Xilinx does not dispute that the prior art combinations suggest all the limitations of claim 13, including a fourth conductive layer.

With respect to the first prior art combination, Paul and Anthony, IVM cites Mr. Johnson’s testimony and asserts that changing the fourth layer of Paul to a

poly layer, where Anthony teaches a poly shield layer 36, amounts to a predictable variation, and would have allowed circuit designers to employ a metal layer for another purpose. *See* Opp. 7–8 (citing Ex. 1002 ¶ 88; Ex. 1013 ¶ 29); Ex. 1013 ¶28 (indicating Paul’s modified bottom shield layer A as a fourth layer in original claim 13, referring to annotated Fig. D2 in Ex. 1002 ¶ 56—annotated Fig. D2 includes Paul’s modified poly capacitor structure inside Anthony’s shield); Pet. 22–25 (discussing claim 13). As explained above in connection with issued claims 2 and 19, using poly in place of metal amounts to substituting one known capacitor conductive material for another with predictable results. Mr. Johnson testifies that double poly processes were well known at the time of the invention, and that skilled artisans, armed with Anthony’s teachings, would have employed known design tools available at the time of the invention to form both of the lower metal layers in Paul’s capacitor structure out of poly with predictable results, including the result of using metal conductive layers for another required purpose—forming circuit element connections. *See* Ex. 1002 ¶ 88; Ex. 1013 ¶ 29.

Similar remarks apply to the combination of Anthony and Bi. Again, as discussed in connection with claims 2 and 19, the dispute centers on whether it would have been obvious to substitute poly, a known material for a capacitor, for metal, another known material for a capacitor. *See* Opp. 8–9; PO Resp. 19 (relying on arguments for original claim 2). As IVM notes, Xilinx does not dispute IVM’s factual assertions and rationale underlying the Institution Decision with respect to the obviousness of claim 13. *See, e.g.*, Inst. Dec. 12–13 (“IVM sets forth supporting rationale for employing Bi’s first and second layers in the core of Anthony’s shielded capacitor – for example, to increase the capacitance.”)

Addressing the proposed limitation of requiring a “fourth layer” of poly, as recited in claim 30, IVM produces the following annotated Figure 2B from

Anthony:

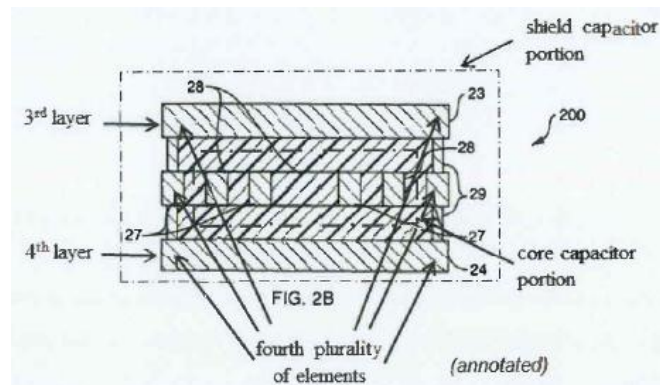


Figure 2B from Anthony above, as annotated by IVM, shows the fourth (4th) layer 24 in dispute that corresponds to the “fourth poly conductive layer” as recited in claim 30. See Opp. 8.

Annotated Figure 2B represents Anthony’s self-shielded capacitor of Figure 2B, inside of Anthony’s outer shield 35, 37 (annotated above as “shield capacitor portion”) of Figures 3B and 4, according to Anthony’s disclosure. See Ex. 1007, col. 4, ll. 33–38; Figs. 3A, 3B. See Pet. 53–57.

As discussed, Xilinx does not dispute that Anthony discloses a fourth conductive layer. See annotated Fig. 2B. As IVM explains, Anthony discloses bottom shield capacitor layer 36 of poly as a metal capacitor layer substitute. See Opp. 9 (citing Ex. 1007, Fig. 3B, col. 4, ll. 49–52). IVM explains that forming Anthony’s capacitor layer 24 out of poly, which corresponds to the claimed fourth poly layer, would have been obvious for the same or similar reasons essentially outlined in the discussion of claims 2 and 19. See Opp. 8–9.

As also discussed, the record shows that Anthony teaches that poly is a known conductor substitute for metal in capacitors. Substituting one or two poly layers for one or two metal layers would have led to predictable results. Ex. 1013 ¶ 29. The record also shows that the substitution involves employing known design tools to arrive predictably at a similar capacitor having conductive layers

and a desired capacitance, while conveniently employing metal layers for circuit connection purposes. *See id.*; Opp. 9.

Xilinx does not present separate patentability arguments for claims 31–34. *See* PO Resp. 19; Opp. 9–10. Based on the foregoing discussion, Xilinx has not met the burden of showing, in its Motion to Amend, that claims 30–34 would have been unobvious over the combination of Paul and Anthony or of Anthony and Bi. *See* 37 C.F.R. §§ 42.20(c), 42.121(a).

H. Summary

Based on the record evidence in light of the arguments presented, including Xilinx’s concession as to the unpatentability of claims 1, 3–7, and 10–17, IVM has demonstrated that claims 1–19 would have been obvious, and Xilinx has not demonstrated that proposed amended claims 20–34 would have been unobvious.

III. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1–19 of the ’609 Patent are *cancelled*; and

FURTHER ORDERED that Xilinx’s Motion to Amend claims is *denied*.

Case IPR2012-00023

Patent 7,994,609

For Petitioner:

Lori Gordon

Robert Sterne

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

lgordon@skgf.com

RSTERNE@skgf.com

For Patent Owner:

David M. O'Dell

Thomas B. King

HAYNES AND BOONE, LLP

david.odell@haynesboone.com

thomas.king@haynesboone.com