

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MACRONIX INTERNATIONAL CO., LTD.,  
MACRONIX ASIA LIMITED, MACRONIX (HONG KONG) CO., LTD.,  
and MACRONIX AMERICA, INC.  
Petitioner

v.

SPANSION LLC  
Patent Owner

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Case IPR2014-00107  
Patent 7,018,922 B1

Before HOWARD B. BLANKENSHIP, KRISTEN L. DROESCH, and  
JUSTIN T. ARBES, *Administrative Patent Judges*.

DROESCH, *Administrative Patent Judge*.

DECISION  
Denying Institution of *Inter Partes* Review  
37 C.F.R. § 42.108

## I. INTRODUCTION

### A. Background

Macronix International Co. Ltd., Macronix Asia Limited, Macronix (Hong Kong) Co., Ltd., and Macronix America, Inc. (collectively “Petitioner”) filed a petition (Paper 3) (“Pet.”) to institute an *inter partes* review of claims 1–7 of U.S. Patent No. 7,018,922 B1 (“the ’922 Patent”). See 35 U.S.C. § 311. Spansion LLC (“Patent Owner”) filed a Preliminary Response (Paper 12) (“Prelim. Resp.”) to the Petition. We conclude that, under 35 U.S.C. § 314(a), Petitioner does not demonstrate a reasonable likelihood of prevailing with respect to at least one of the challenged claims.

### B. Related Proceedings

Petitioner indicates the ’922 Patent is at issue in the following actions: (1) *Spansion LLC v. Macronix International Co.*, No. 3:13-cv-03566, filed August 1, 2013, in the United States District Court for the Northern District of California; and (2) *In re Flash Memory Chips and Products Containing Same*, Inv. No. 337-TA-893, filed August 1, 2013, before the U.S. International Trade Commission. Pet. 1. Petitioner concurrently filed petitions for *inter partes* review of the following claims of the following Patents:

claims 1–4 of U.S. Patent No. 6,369,416 B1 (IPR2014-00103);  
claims 1–14 of U.S. Patent No. 6,459,625 B1 (IPR2014-00104);  
claims 1–28 of U.S. Patent No. 6,731,536 B1 (IPR2014-00105);  
claims 1–10 of U.S. Patent No. 6,900,124 B1 (IPR2014-00106);  
and  
claims 1–14 of U.S. Patent No. 7,151,027 B1 (IPR2014-00108).

The '922 Patent issued from a continuation of the application that issued as U.S. Patent No. 6,900,124 B1 (IPR2014-00106).

*C. The '922 Patent (Ex. 1001)*

The '922 Patent relates to manufacturing of integrated circuits, in particular to a method of improving the depth of focus and overlay margin within the stacked gate layer of a flash memory device. Ex. 1001, Abs.; col. 1, ll. 11–14.

Figure 2 of the '922 Patent, reproduced below, depicts a schematic top view of stacked gate pattern 50. *Id.* at col. 3, ll. 16–19.

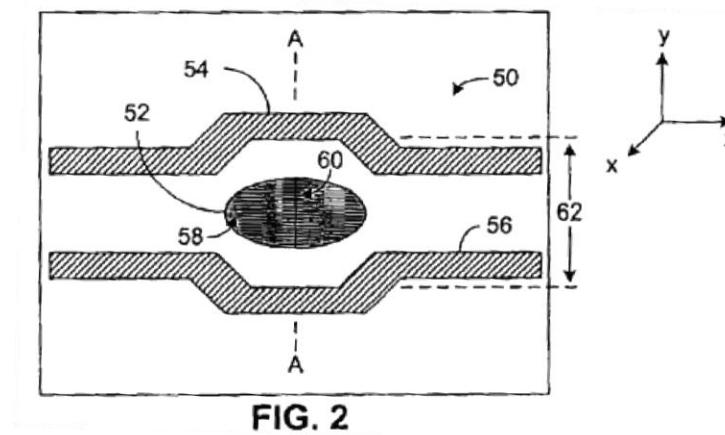


Figure 2 illustrates stacked gate pattern 50, including elliptical  $V_{ss}$  contact 52 formed between first and second stacked gate layers 54, 56. *Id.* at col. 3, ll. 54–57; col. 4, ll. 5–6.  $V_{ss}$  contact 52 is formed in an elongated shape, such as an ellipse, wherein major axis 58 of the ellipse is parallel substantially to stacked gate layers 54, 56, and minor axis 60 of the ellipse is perpendicular substantially to stacked gate layers 54, 56. *Id.* at col. 4, ll. 6–14.

Figure 4H of the '922 Patent, reproduced below, depicts a sectional view of  $V_{ss}$  contact 52 formed between stacked gate layers 54, 56. *Id.* at col. 3, ll. 38–39.

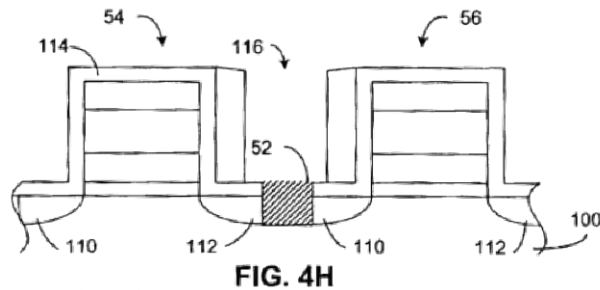


Figure 4H illustrates semiconductor substrate 100, stacked gate layers 54, 56, source region 110, drain region 112, interlayer insulating layer 114,  $V_{ss}$  contact hole 116, including conductive material forming  $V_{ss}$  contact 52. *Id.* at col. 5, ll. 20–27, 51–56, 64–67; col. 6, ll. 6–16. Stacked gate layers 54, 56 include a gate oxide layer deposited on semiconductor substrate 100, a floating gate layer deposited on the gate oxide layer, an inter-gate dielectric layer deposited on the floating gate layer, and a control gate layer deposited on the inter-gate dielectric layer. *Id.* at col. 5, ll. 26–50.

Figure 5 of the '922 Patent, reproduced below, depicts a schematic top view of stacked gate pattern 50 of another embodiment. *Id.* at col. 3, ll. 40–43; col. 6, ll. 21–23.

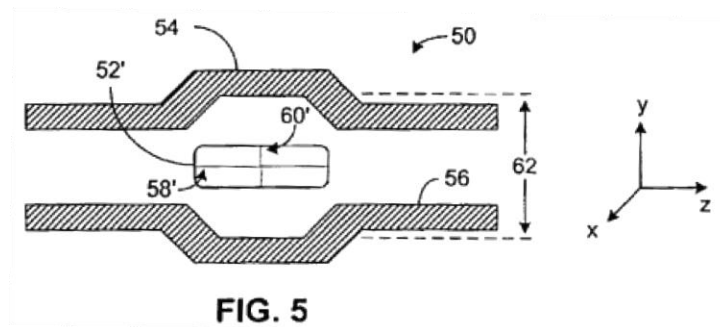


Figure 5 illustrates stacked gate pattern 50, including rectangular  $V_{ss}$  contact 52' formed between first and second stacked gate layers 54, 56. *Id.* at col. 6, ll. 23–26.  $V_{ss}$  contact 52' is formed in the shape of a rectangle with a first pair of sides longer than a second pair of sides. *Id.* at col. 6, ll. 26–29. Major axis 58' is defined as an axis parallel to the first pair of sides, and intersecting a midpoint of the second pair of sides, and minor axis 60' is defined as an axis parallel to the second pair of sides and intersecting a midpoint of the first pair of sides. *Id.* at col. 6, ll. 34–39. Figure 5 further depicts the corners of  $V_{ss}$  contact 52' as rounded.

#### *D. Illustrative Claim*

Claim 1, reproduced below, is the only independent claim and is illustrative of the claims at issue (*emphases added*):

1. A method of forming a contact in a flash memory device that improves the depth of focus (DOF) margin and the overlay margin between a plurality of stacked gate layers and the respective contact, comprising the steps of:  
forming a plurality of stacked gate layers on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers;  
depositing an interlayer insulating layer over the plurality of stacked gate layers;  
*patterning a contact hole between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact hole is an elongated shape having a major axis and a minor axis, and the contact hole is dimensioned along the major axis so as to maintain focus of an image of the contact hole as the minor axis is reduced in size towards a DOF limit; and*  
depositing a conductive layer in the contact hole.

## II. ANALYSIS

### A. *Claim Construction*

Consistent with the statute and legislative history of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284, 329 (2011), the Board interprets claims using the broadest reasonable construction in light of the specification. *See* 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). There is a “‘heavy presumption’ that a claim term carries its ordinary and customary meaning.” *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). However, a “claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history.” *Id.* “Although an inventor is indeed free to define the specific terms used to describe his or her invention, this must be done with reasonable clarity, deliberateness, and precision.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

#### 1. “*Depth of Focus*” or “*DOF*”

Independent claim 1 recites “depth of focus (DOF)” in the context of a DOF margin and a DOF limit. Petitioner asserts that “depth of focus” or “DOF” is defined expressly in the ’922 Patent Specification as “the range of lens-wafer distances over which line widths are maintained within specifications and resist profiles are adequate.” Pet. 5 (citing Ex. 1001, col. 2, ll. 20–22; Fig. 4C). Petitioner further asserts that this construction is consistent with the plain and ordinary meaning of “depth of focus,” as well as the understanding of a person of ordinary skill in the art. Pet. 5–6 (citing Ex. 1010; Ex. 1002 ¶ 32).

Patent Owner acknowledges that Petitioner correctly quotes one passage of the Specification, but asserts that Petitioner omits additional portions of the Specification pertinent to a proper construction of the term. Prelim. Resp. 8–11 (citing Ex. 1001, col. 1, ll. 50–56; col. 2, ll. 17–32; col. 7, ll. 11–14; Figs. 2, 4E, 4F). Patent Owner contends that “[i]n lithography, the depth of focus (‘DOF’) must be sufficient to ensure that the shape to be created in the photoresist layer is in focus throughout the entire depth of the photoresist.” Prelim. Resp. 9 (citing Ex. 1001, col. 1, ll. 52–56; col. 2, ll. 20–22). Patent Owner further contends that the Specification emphasizes the importance of three dimensional patterning and maintaining focus through the depth dimension of the photoresist. Prelim. Resp. 9–10 (citing Ex. 1001, col. 1, ll. 50–56); *see* Prelim. Resp. 8–9, n.8 (citing Ex. 1001, col. 2, ll. 17–32); Prelim. Resp. 10–11 (citing Ex. 1001, Figs. 4E, 4F). On the foregoing bases, Patent Owner asserts that the broadest reasonable interpretation of “Depth of Focus” or “DOF” is “the range of lens-wafer distances over which exposed photoresist will generate line widths within specifications and adequate resist profiles.” Prelim. Resp. 8.

We are not persuaded by Patent Owner’s assertions that the broadest reasonable interpretation of “depth of focus” or “DOF” requires the exposed photoresist to generate line widths within specifications and adequate profiles, or otherwise requires maintaining focus throughout the entire depth of the photoresist. The ’922 Patent does not provide a sufficient factual basis to support Patent Owner’s assertions, because the ’922 Patent is silent regarding exposed photoresist and maintaining focus throughout the entire depth of the photoresist. We are persuaded that the definition in the Specification cited by Petitioner applies.

Accordingly, applying the broadest reasonable interpretation, “depth of focus” and “DOF” means “the range of lens-wafer distances over which line widths are maintained within specifications and resist profiles are adequate.” Ex. 1001, col. 2, ll. 20–22.

## 2. “*DOF Limit*”

Petitioner and Patent Owner do not provide a proposed construction for “DOF limit,” as recited in claim 1. Consistent with the broadest reasonable interpretation of “depth of focus” and “DOF,” “DOF limit” means “a limit associated with the range of lens-wafer distances over which line widths are maintained within specifications and resist profiles are adequate.” *See id.*

## 3. *Remaining Claim Terms or Phrases*

All other terms in the challenged claims need not be construed expressly for purposes of this Decision.

*B. Asserted Grounds of Unpatentability*

Petitioner contends the challenged claims are unpatentable under 35 U.S.C. §§ 102(b) and 103(a) on the following specific grounds (Pet. 3–4):

| <b>Reference[s]<sup>1</sup></b>                                    | <b>Basis</b> | <b>Claims Challenged</b> |
|--------------------------------------------------------------------|--------------|--------------------------|
| Goda                                                               | § 102        | 1, 6, and 7              |
| Goda and An                                                        | § 103        | 1–7                      |
| Goda, An, and/or Kim                                               | § 103        | 1–7                      |
| Goda and Toshiba                                                   | § 103        | 1–7                      |
| (1) Goda, An and/or Kim, and Lee, or<br>(2) Goda, Toshiba, and Lee | § 103        | 1–7                      |

*1. 35 U.S.C. § 102 Ground of Unpatentability over Goda*

Petitioner contends claims 1, 6, and 7 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Goda.<sup>2</sup> Pet. 16–29.

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<sup>1</sup> The Petition relies on the following references: U.S. Patent No. 6,611,010 B2 (Ex. 1003) (“Goda”); U.S. Patent No. 5,536,668 (Ex. 1004) (“An”); Dong-Chan Kim et al., *A 2Gb NAND Flash Memory with 0.044  $\mu\text{m}^2$  Cell Size using 90nm Flash Technology*, IEEE 2002 (Ex. 1005) (“Kim”); Kevin Gibb, *A Structural Analysis of the Toshiba TC58256DC-CT0501 256M NAND Flash*, SEMICONDUCTOR INSIGHTS 2000 (Ex. 1006) (“Toshiba”) (citations to original pagination); and U.S. Patent No. 6,515,329 B2 (Ex. 1009) (“Lee”). The Petition also relies on the Declaration of Chris A. Mack (Ex. 1002).

<sup>2</sup> Petitioner asserts that Goda is prior art to the claims of the ’922 Patent under 35 U.S.C. § 102(b). Pet. 18. The ’922 Patent has an effective filing date of September 3, 2003. Goda issued as U.S. Patent No. 6,611,010 B2 on August 26, 2003, with an application date of December 1, 2000. Goda is not prior art under 35 U.S.C. § 102(b), because Goda did not issue as a patent more than one year prior to the September 3, 2003 effective filing date of the ’922 Patent. Nevertheless, based on the current record, Goda is prior art under 35 U.S.C. §§ 102(a) and (e), and we address Petitioner’s contentions of anticipation by Goda under those provisions of 35 U.S.C. § 102.

## a. Goda

Goda provides the following description:

[a] non-volatile semiconductor memory device . . . includ[ing] element areas and element isolation areas repeatedly arranged in one direction at a regular period, memory cells arranged in the element areas, first contact holes arranged in the one direction generally at the same period as the regular period; a bit line arranged in the first contact holes and connected to one end of a current path of each memory cell through at least one transistor, second contact holes arranged in the one direction generally at the same period as the regular period, and a source line arranged in the second contact holes and connected to the other end of the current path of each memory cell through at least one transistor, wherein both the first and second contact holes have a width in a second direction orthogonal to the first direction larger than a width in the first direction.

Ex. 1003, col. 10, ll. 35–49.

Figure 109 of Goda, reproduced below, depicts a top plan view of NAND cell type non-volatile semiconductor memory device according to an embodiment. *Id.* at col. 15, ll. 4–6.

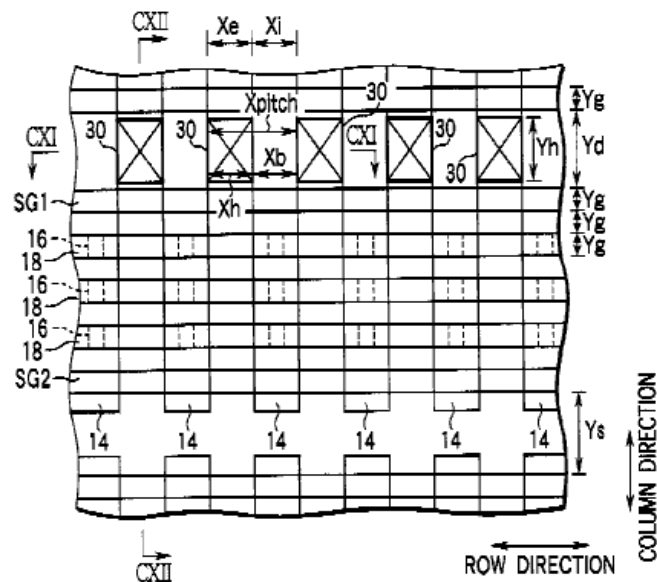


Figure 109 illustrates “contact holes 30 [] formed in the shape of rectangle[s] instead of square[s].” *Id.* at col. 37, ll. 64–65; *see id.* at Figs. 103, 115, 121, 127; col. 35, ll. 1–2; col. 41, ll. 17–18, 60–61; col. 44, ll. 43–44; col. 45, ll. 16–17; col. 47, ll. 26–27; col. 48, ll. 25–26. The width  $Y_h$  of contact holes 30 in the column direction is larger than a width  $X_h$  of contact holes 30 in a row direction. *Id.* at col. 37, l. 65–col. 38, l. 2; col. 38, ll. 57–61; *see id.* at Figs. 103, 115, 121, 127; col. 35, ll. 2–6, 59–63; col. 41, ll. 18–22; col. 41, l. 62–col. 42, l. 6; col. 42, ll. 44–48; col. 44, ll. 44–48; col. 45, ll. 17–21; col. 47, ll. 27–31; col. 48, ll. 26–30.

Figure 112 of Goda, reproduced below, is a cross-sectional view taken along the line CXII-CXII in Figure 109. *Id.* at col. 15, ll. 11–12.

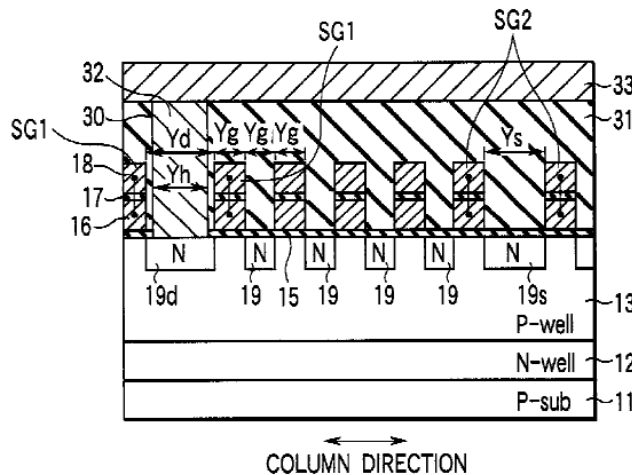


Figure 112 illustrates N-well region 12 and P-well region 13 formed in P-type silicon substrate 11, with memory cells and select transistors formed in P-type well region 13. *Id.* at col. 37, ll. 12–15; *see id.* at Figs. 106, 118, 124, 130; col. 34, ll. 24–26; col. 40, ll. 7–9; col. 43, ll. 59–61; col. 46, ll. 29–31. Control gate layer 18 is formed on charge transfer layer 16 through intergate insulating layer 17. *Id.* at col. 37, ll. 31–32; *see id.* at col. 34, ll. 42–43; col. 40, ll. 48–49; col. 46, ll. 54–55. A surface area of silicon substrate 11

beneath charge transfer layer 16 serves as a channel region, with N-type diffusion layers 19 (a source region or drain region) formed on both sides of the channel region. *Id.* at col. 37, ll. 46–50; *see id.* at col. 34, ll. 56–60; col. 40, ll. 63–67; col. 47, ll. 1–5. Control gate layer 18 and select gate lines SG1, SG2 of memory cells extend in a row direction. *Id.* at col. 37, ll. 57–58, *see id.* at col. 34, ll. 61–62; col. 41, ll. 7–9; col. 44, ll. 32–33. Interlayer insulating layer 31 overlying memory cells is formed with contact holes 30, which reach drain diffusion layer 19d of the NAND strings. *Id.* at col. 37, ll. 59–63; *see id.* at col. 34, ll. 62–67; col. 41, ll. 9–13; col. 44, ll. 34–39; col. 47, ll. 18–22. Contact plug 32 made of conductive material is buried in each contact hole 30. *Id.* at col. 38, ll. 10–11; *see id.* at col. 35, ll. 14–15; col. 41, ll. 44–45; col. 45, ll. 3–4; col. 48, ll. 11–14. Bit lines 33 are formed on interlayer insulating layer 31 and are connected electrically to drain diffusion layers 19d of associated memory cells through contact plugs 32, and extend in a column direction. *Id.* at col. 38, ll. 11–16; *see id.* at col. 35, ll. 15–19.

Figure 113 of Goda, reproduced below, shows the shape of contact holes 30 when the device of Figs. 109 and 112 is manufactured. *Id.* at col. 15, ll. 14–16.

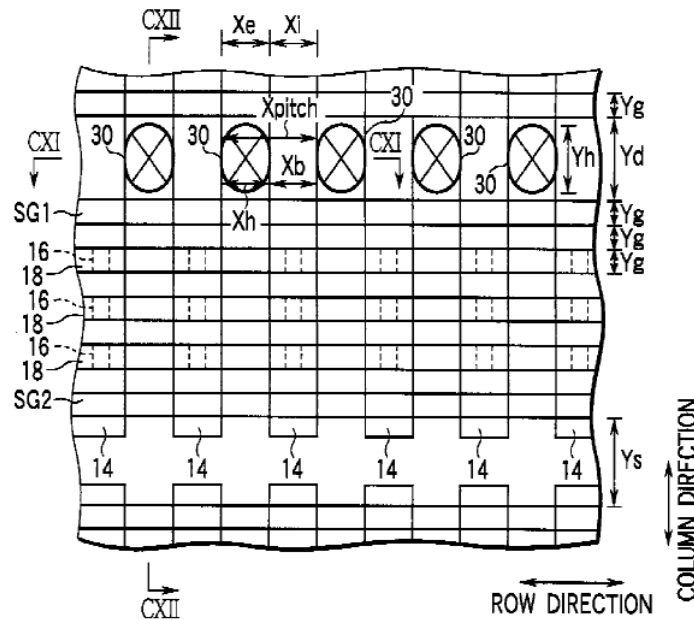


Figure 113 illustrates resulting contact holes 30 in the shape of “rectangle[s] with rounded corners.” *Id.* at col. 38, ll. 42–56; *see id.* at Figs. 107, 108, 114, 119, 120, 125, 126, 131, 132; col. 35, ll. 42–56; col. 42, ll. 27–43; col. 45, ll. 52–67; col. 48, ll. 49–64. Goda provides the following explanation:

as memory cells are miniaturized and contact holes (bit line contacts) are also miniaturized, even if the contact holes are laid out in the shape of rectangle[s], a resist film serving as a mask is in the shape of rectangle[s] with rounded corners (a shape resembling an ellipse), resulting in contact holes likewise in the shape of rectangle[s] with rounded corners, which are formed by etching with the circular resist film used as a mask.

*Id.* at col. 38, ll. 45–52; *see id.* at col. 35, ll. 45–52; col. 42, ll. 31–39; col. 45, ll. 55–64; col. 48, ll. 52–60. Goda further explains that contact holes 30 are “formed in the shape of rectangle[s] (or rectangle[s] with rounded corners) so as to accomplish the feature of the line and space pattern, i.e., an

improved processing margin resulting from the proximity effect.” *Id.* at col. 38, ll. 61–66; *see id.* at col. 42, ll. 48–54.

Goda still further explains that because contact holes 30 are arranged in a line in the row direction (in the direction in which word lines 18 extend), width  $X_h$  of contact holes 30 in the row direction is reduced, while width  $Y_h$  of contact holes 30 in the column direction is made longer than width  $X_h$  in the row direction. *Id.* at col. 39, ll. 1–6; *see id.* at col. 42, ll. 55–60. In addition, Goda explains that this enables pitch  $X_{pitch}$  of contact holes 30 (equal to the width  $X_h$  of contact holes 30 in the row direction plus a spacing  $X_b$  between adjacent contact holes 30) to be reduced and simultaneously width  $X_e$  of the element areas and width  $X_i$  of the element isolation areas to be reduced to approximately the minimum processing dimension available for the line and space pattern. *Id.* at col. 39, ll. 6–11; *see id.* at col. 42, ll. 60–65.

*b. Claims 1, 6, and 7*

Independent claim 1 recites “the contact hole is an elongated shape having a major axis and a minor axis, and the contact hole is dimensioned along the major axis so as to maintain focus of an image of the contact hole as the minor axis is reduced in size towards a DOF limit.” Petitioner asserts that the aforementioned limitation is found in the following description in Goda:

as the memory cells are miniaturized and the contact holes (bit line contacts) 30 and the contact holes (source line contacts) 40 are also miniaturized, even if the contact holes 30, 40 are laid out in the shape of rectangle[s], a resist film serving as a mask is in the shape of rectangle[s] with rounded corners (a shape resembling an ellipse), resulting in the contact holes 30, 40 likewise in the shape of rectangle[s] with rounded corners,

which are formed by etching with the circular resist film used as a mask.

It should be noted that this embodiment is intended to explain that the contact holes 30, 40 may be formed not only in the shape of rectangle[s] but also in the shape of rectangle[s] with rounded corners.

Pet. 22 (quoting Ex. 1003, col. 48, ll. 52–64); *see* Pet. 22–24 (quoting Ex. 1003, col. 36, ll. 17–22; col. 38, ll. 57–67; col. 41, ll. 7–8; col. 42, ll. 44–65; col. 47, ll. 60–67; reproducing Ex. 1003, Fig. 131). Petitioner does not explain sufficiently how the quoted portions of Goda describe that the contact hole is dimensioned along the major axis so as to maintain focus of an image of the contact hole as the minor axis is reduced in size towards a DOF limit (i.e., a limit associated with the range of lens-wafer distances over which line widths are maintained within specifications and resist profiles are adequate). At best, Petitioner asserts that Goda discusses elongating contact holes to improve the processing margin (Pet. 18 (citing Ex. 1003, col. 42, ll. 44–65)), and contends that “[o]ne of ordinary skill in the art would understand that the DOF margin discussed in the ’922 Patent is simply a type of processing margin as discussed in Goda” (Pet. 18 (citing Ex. 1002 ¶ 48)).

Patent Owner asserts that none of the passages in Goda cited by Petitioner addresses or discloses dimensioning a contact hole to maintain image focus as the minor axis is reduced towards a DOF limit. Prelim. Resp. 24. Patent Owner further argues that Petitioner’s declarant, Dr. Chris A. Mack, does not state that Goda teaches dimensioning the major axis of a contact hole to maintain focus of an image of the contact hole as the minor axis is reduced in size toward a DOF limit. *Id.* at 28 (citing Ex. 1002 ¶¶ 48–50). Instead of addressing the disputed claim limitation, Dr. Mack’s

testimony discusses the DOF margin by providing the following assertions:

(1) one with ordinary skill in the art would understand that DOF margin in one type of processing margin as the term is used in the Goda reference; (2) one with ordinary skill in the art would understand the importance of processing margin during manufacturing to ensure acceptable results; and (3) DOF is referred to sometimes as “focus margin.” Ex. 1002 ¶¶ 48–50.

We are persuaded that Petitioner’s arguments and supporting evidence do not demonstrate sufficiently that Goda describes a contact hole dimensioned along the major axis so as to maintain focus of an image of the contact hole as the minor axis is reduced in size towards a DOF limit. To the extent that Petitioner asserts that a “DOF margin” is synonymous with a “DOF limit,” Petitioner’s arguments remain unavailing. Petitioner’s assertion that the DOF margin discussed in the ’922 Patent is a type of processing margin discussed in Goda (Pet. 18) (i.e., Goda’s processing margin describes a DOF margin) is not supported by a sufficient underlying factual basis. Ex. 1002 ¶ 48; 37 C.F.R. § 42.65(a).

Thus, on the record before us, Petitioner does not demonstrate a reasonable likelihood of prevailing on its assertion that Goda anticipates independent claim 1, and claims 6 and 7 dependent therefrom.

*2. 35 U.S.C. § 103 Grounds of Unpatentability for Claims 1–7*

We are persuaded that, as applied by Petitioner, none of the An, Kim, Toshiba, or Lee references remedies Goda’s deficiency in teaching “the contact hole is dimensioned along the major axis so as to maintain focus of an image of the contact hole as the minor axis is reduced in size towards a DOF limit.” Prelim. Resp. 30–31; see Pet. 30–58. Petitioner does not rely on any reference other than Goda for this limitation. Therefore, Petitioner

does not establish a reasonable likelihood of prevailing on its assertions that claim 1, and claims 2–7, dependent therefrom, would have been obvious over the following combinations of references: (1) Goda and An; (2) Goda, An, and/or Kim; (3) Goda, An, and/or Kim, and Lee; (4) Goda and Toshiba; and (5) Goda, Toshiba, and Lee.

Because we agree with Patent Owner’s arguments regarding the limitation of claim 1 that “the contact hole is an elongated shape having a major axis and a minor axis, and the contact hole is dimensioned along the major axis so as to maintain focus of an image of the contact hole as the minor axis is reduced in size towards a DOF limit,” we need not address Patent Owner’s other arguments directed to the asserted grounds.

### III. CONCLUSION

We conclude, based on the record before us, there is not a reasonable likelihood that Petitioner would prevail in showing that claims 1–7 are unpatentable.

### IV. ORDER

Accordingly, it is ORDERED that the Petition for *inter partes* review is denied.

Case IPR2014-00107

Patent 7,018,922 B1

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