

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GSi TECHNOLOGY, INC.,
Petitioner,

v.

CYPRESS SEMICONDUCTOR CORPORATION,
Patent Owner.

Case IPR2014-00121
Patent 6,292,403 B1

Before MIRIAM L. QUINN, WILLIAM V. SAINDON, and
KEVIN W. CHERRY, *Administrative Patent Judges*.

CHERRY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, GSI Technology, Inc. (“Petitioner”) has failed to show by a preponderance of the evidence that claims 1–7, 12, 13, 15–17, 19, and 20 of U.S. Patent No. 6,292,403 B1 (Ex. 1001, “the ’403 patent”) are unpatentable.

A. Procedural History

Petitioner filed a Petition requesting an *inter partes* review of claims 1–7, 12–17, 19, and 20 of the ’403 patent. Paper 1 (“Pet.”). Cypress Semiconductor Corp. (“Patent Owner”) filed a Preliminary Response. Paper 9. On April 16, 2014, pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review of all but one of the claims challenged in the Petition on the following grounds of unpatentability:

Reference(s)	Basis	Challenged Claim(s)
Sharp ¹	§ 102(b)	1–6, 16, 19, and 20
Sharp and Chappell ²	§ 103(a)	7
Sharp and Lee ³	§ 103(a)	12
Sharp, Takayanagi ⁴ , and Proebsting ⁵	§ 103(a)	13

¹ US 5,257,236, iss. Oct. 26, 1993 (Ex. 1002).

² US 5,204,841, iss. Apr. 20, 1993 (Ex. 1007).

³ US 5,493,530, iss. Feb. 20, 1996 (Ex. 1008).

⁴ JP H4-163784, pub. June 9, 1992 (Ex. 1004); English Translation (Ex. 1005).

Reference(s)	Basis	Challenged Claim(s)
Sharp and Suzuki ⁶	§ 103(a)	17
Takayanagi	§ 102(b)	1 and 15

Paper 13 (“Decision” or “Dec. on Inst.”), 22.⁷

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 21, “PO Resp.”). Petitioner filed a Reply (Paper 38, “Pet. Reply”). Oral hearing was held on January 12, 2014.⁸

Petitioner submitted the Declaration of Mr. Robert Murphy, dated November 4, 2013, Ex. 1011 (“Murphy Declaration”), in support of its Petition. Petitioner also submitted the Supplemental Declaration of Robert Murphy, dated November 23, 2014, Ex. 1016 (“Supplemental Murphy Declaration”), in support of its Reply.

Patent Owner submitted the Affidavit of Vivek Subramanian, dated August 8, 2014, Ex. 2015. Patent Owner also submitted other affidavits in support of its contentions of secondary considerations of non-obviousness. See Ex. 2039, Ex. 2040.

B. Related Proceedings

The ’403 patent is involved in an ongoing district court lawsuit, *Cypress Semiconductor Corp. v. GSI Technology, Inc.*, C.A. 13-2013-JST,

⁵ US 5,546,569, iss. Aug. 13, 1996 (Ex. 1009).

⁶ US 5,717,653, iss. Feb. 10, 1998 (Ex. 1010).

⁷ In our Decision, we found that Petitioner had not demonstrated a reasonable likelihood of prevailing on claim 14. Dec. on Inst. 18–19.

⁸ A transcript of the oral hearing (“Tr.”) is included in the record as Paper 45.

consolidated with *Cypress Semiconductor Corp. v. GSI Technology, Inc.*,
C.A. 13-3757-JST, currently pending in the Northern District of California.
Paper 5.

C. The '403 Patent

The '403 patent relates to a circuit that enables reading from and writing to a random access memory ("RAM") in the same clock cycle. Ex. 1001, col. 1, ll. 38–40. Specifically, the patent discloses using the rising and falling edges of the clock cycle to trigger read and write operations. *Id.* at col. 5, ll. 65–66. The relevant operational details of the circuit may be understood from Figure 4, reproduced below.

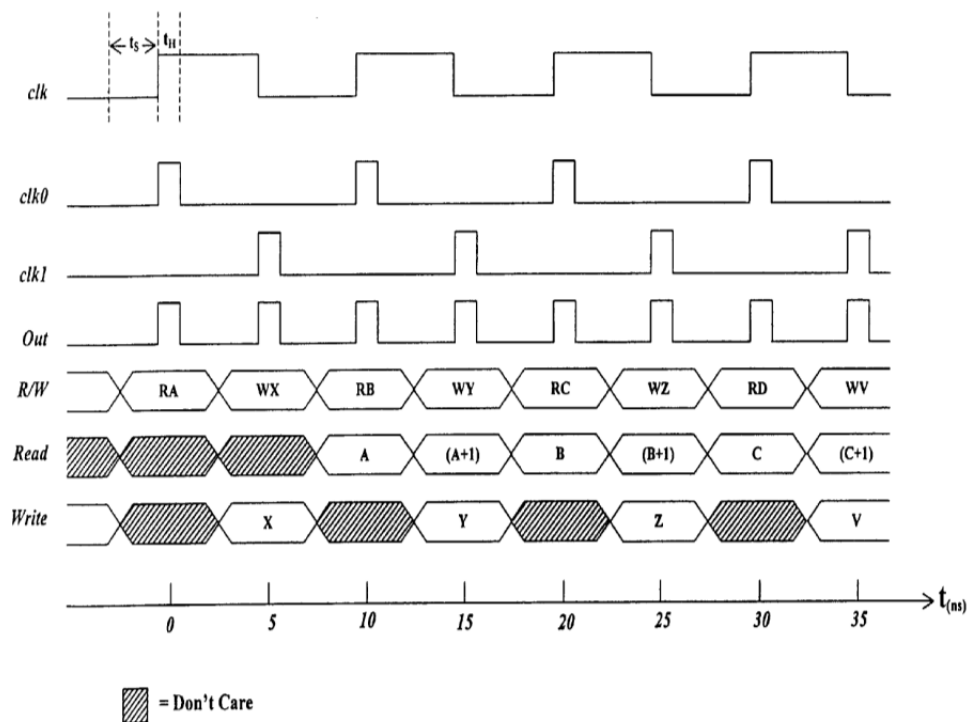


Figure 4 of the '403 patent.

Figure 4 provides a timing diagram showing the various signal transitions in a set of exemplary read and write operations. *Id.* at col. 2, ll. 41–44. At time 0, the *clk* signal is rising and control pulse *clk0* is

triggered, causing address A to be latched into the address register. *Id.* at col. 7, ll. 10–15. At time 5, the *clk* signal is falling and control pulse *clk1* is triggered, causing address X to be latched into the address register, which in turns causes the data held in data register 220 or 222 (shown in Figure 7B, not reproduced here) to be written into the memory array. *Id.* at col. 7, ll. 52–60. At time 10, the *clk* signal is rising and control pulse *clk0* is triggered, causing the data to be latched from address A into output register 202 or 204 (shown in Figure 7A, not reproduced here). *Id.* at col. 7, ll. 22–28. As depicted in Figure 4, this cycle continues, such that, during one cycle of the *clk* signal, data is read into either output register 202 or 204, and data is written into the memory array from either data register 220 or 222. *Id.* at col. 7, ll. 43–60.

The timing diagram of Figure 4 corresponds to a register comprised of two sub-registers, such as depicted in Figure 1 (not shown). *Id.* at col. 6, ll. 63–65. Multiple registers also may be used and each register further may be comprised of multiple sub-registers. *See e.g., id.* at col. 6, ll. 29–50. In such an arrangement, it may be possible to have several read and write operations carried out in a single clock cycle. *Id.*

D. Illustrative Claim

Claims 1, 19, and 20 are the independent claims of the '403 patent. Claim 1 is illustrative of the claims and recites:

1. A circuit comprising:
a register configured to store (i) a first address in response to a first periodic signal transition and (ii) a second address in response to a second periodic signal transition, wherein the first and second periodic signal transitions both occur within a single periodic signal cycle.

Claim 19 is similar to claim 1, but recites the elements of claim 1 using means-plus-function limitations. Claim 20 also is similar to claim 1, but is written as a method claim.

II. ANALYSIS

A. Claim Construction

In the Decision on Institution, we applied the broadest reasonable claim interpretation and interpreted certain claim terms as follows:

Claim Term	Construction
“periodic signal”	“any signal that has an oscillating waveform, the frequency of which may be predicted and/or controlled in accordance with techniques known in the art, and that can be configured to control one or more circuit functions performed as part of a read operation or a write operation in a memory”
“signal transition”	“that portion or edge of the signal that is rising or falling between its low and high values”
“complementary transition”	“either the same transition of complementary signals (e.g., the rising edges of both CLK and CLK*), or opposite transitions of the same signal (i.e., the rising and falling edges of CLK)”
“register”	“a circuit that holds information to be processed or transferred”

Claim Term	Construction
“means for storing a first address in response to a first periodic signal transition” and “means for storing a second address in response to a second periodic signal transition”	Construed as means-plus-function limitations. The structures disclosed for carrying out the recited functions of “storing a first/second address in response to a first/second periodic signal transition” are one [or] more registers, each of which may comprise a plurality of sub-registers. The registers may be D-type registers, T-type registers, master-slave registers, or latches. The sub-registers may be a D-type or master-slave-type registers.

Dec. on Inst. 7–12.

Neither party has expressed disagreement with these constructions, and we see no reason to modify these constructions based on the evidence introduced during trial. We maintain these constructions for this Final Written Decision.

B. Legal Principles Related to Unpatentability

To prevail in challenging Patent Owner’s claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A claim is anticipated if a single prior art reference either expressly or inherently discloses every limitation of the claim. *Orion IP, LLC v. Hyundai Motor Am.*, 605 F.3d 967, 975 (Fed. Cir. 2010).

[U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the

claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.

Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1371 (Fed. Cir. 2008).

C. Asserted Anticipation of Claims 1–6, 16, 19, and 20 Based on Sharp (Ex. 1002)

1. Overview of Sharp

Sharp, titled “Static RAM,” discloses a static memory, which when used in a dual port cache memory simplifies write cycles by providing latching of decoded address signals, which are used in a subsequent memory cycle for writing. Ex. 1002, Abstract. Sharp also discloses logic that allows the propagation of data at the rate f with timing signals of frequency $\frac{1}{2} f$. *Id.*

Figure 1 of Sharp is reproduced below.

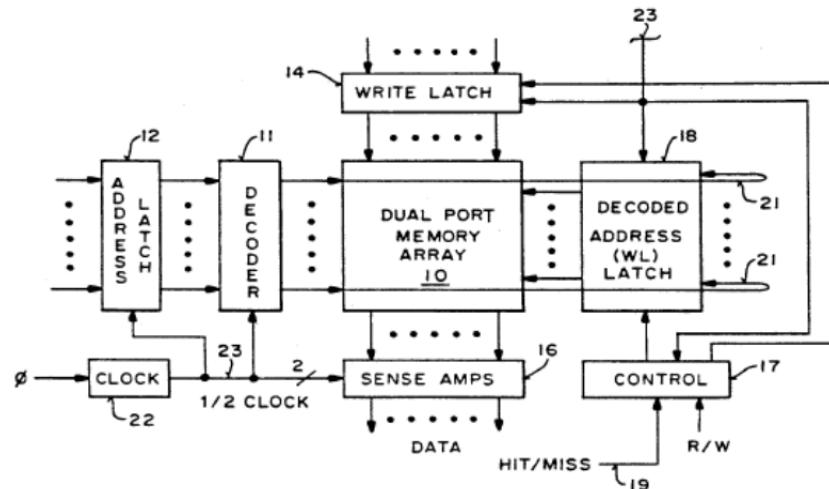


Figure 1 is a block diagram of a memory described in Sharp.

Figure 1 shows memory array 10, which may comprise a plurality of dual port static memory cells, decoder 11, address latch 12, write latch 14, sense amps 16, control 17, decoded address latch 18, and clock 22. *Id.* at col. 2, l. 48–col. 3, l. 13.

Figure 2 of Sharp is reproduced below.

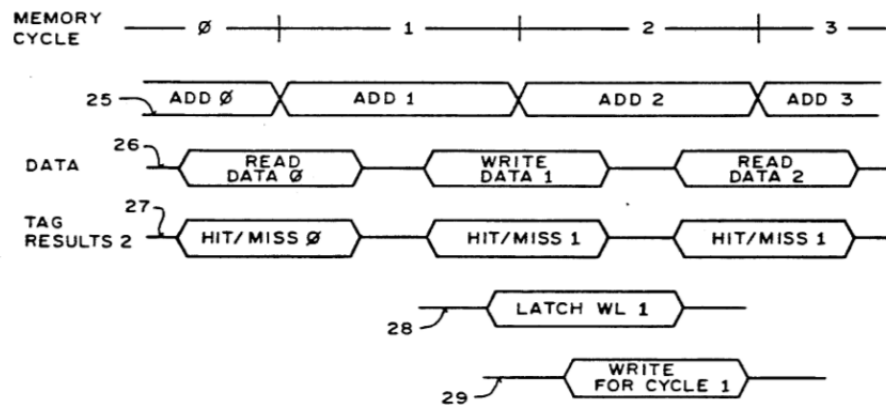


Figure 2 is a timing diagram illustrating the operation of the memory of Figure 1. *Id.* at col. 2, ll. 19–20.

In Figure 2, line 25 illustrates sequential memory addresses for read and write cycles for memory cycles 0, 1, 2, and 3. *Id.* at col. 3, ll. 34–36. These addresses are coupled to address latch 12. *Id.* at col. 3, ll. 36–37. Line 26 illustrates data on the data bus. For memory cycle 0, data are read from memory array 10 onto the data bus as the address signals are decoded and then used to select cells for the first port. *Id.* at col. 3, ll. 38–39. Line 26 shows the read data. *Id.* at col. 3, ll. 40–41. Memory cycle 1 is a write cycle and the write data are shown on line 26. *Id.* at col. 3, ll. 41–42. These data are coupled into write latch 14. *Id.* at col. 3, ll. 42–43.

Figure 3 of Sharp is reproduced below.

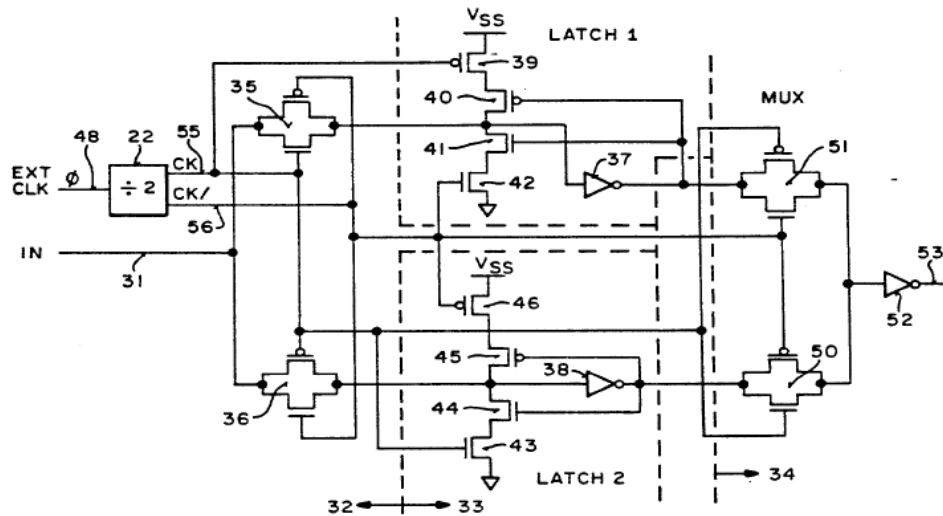


Figure 3 of Sharp is a diagram of a circuit for use for latches or other logic circuits. *Id.* at col. 4, ll. 22–23. The memory of Figure 1 may be realized without this circuit, and conversely, the circuit may be used in circuits other than the memory of Figure 1. *Id.* at col. 4, ll. 23–26. An externally applied clock signal ϕ is shown on line 48 coupled to clock circuit 22, which can be a divide-by-two circuit, with outputs of complementary clocking signals on lines 55 and 56. *Id.* at col. 4, ll. 27–31. The circuit of Figure 3 includes latch 1, which comprises inverter 37 and a second inverter comprising transistors 39, 40, 41, and 42, and latch 2, which includes inverter 38 and a second inverter comprising transistors 43, 44, 45, and 46. *Id.* at col. 4, ll. 63–68. The circuit of Figure 3 permits the data to be moved from line 31 to line 53 at a frequency f assuming that f is the frequency of the externally applied clocking signal. *Id.* at col. 4, ll. 40–43. The internal clocking signal on lines 55 and 56 is $\frac{1}{2}f$, which provides the advantage of clocking data at the frequency f with a frequency of $\frac{1}{2}f$. *Id.* at col. 4, ll. 43–46.

Figure 4 of Sharp, is reproduced below.

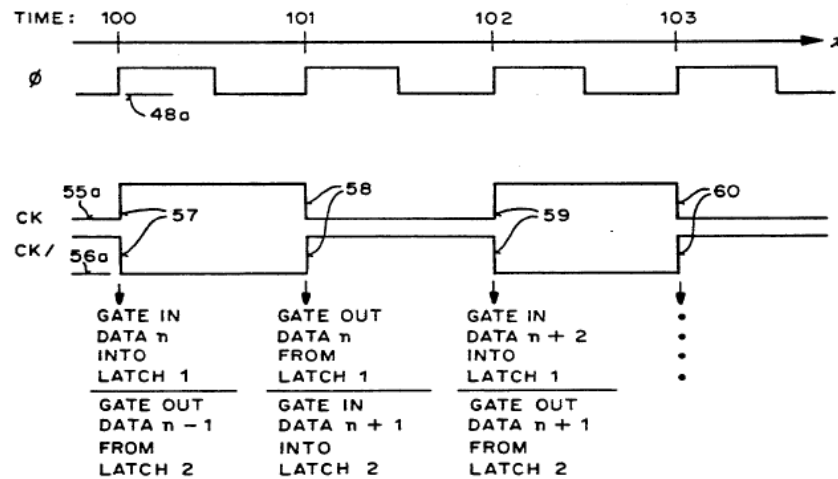


Figure 4 of Sharp.

Figure 4 of Sharp is a timing diagram for the circuit shown in Figure 3. *Id.* at col. 3, ll. 20–22. Figure 4 shows DATA n being read into LATCH 1 at time 100, which corresponds to rising transition edge 57 of periodic signal 55a (designated as CK). *Id.* at col. 5, ll. 31–37. Simultaneously, LATCH 2 writes DATA $n - 1$ into RAM memory. At time 101, which corresponds to falling transition edge 58 of periodic signal 55a, DATA n is read out of LATCH 1 and DATA $n + 1$ is coupled to LATCH 2. *Id.* at col. 5, ll. 42–43.

2. Analysis

Petitioner contends that Sharp anticipates claims 1–6, 16, 19, and 20. Pet. 14–21. Petitioner’s challenges based on Sharp are premised on using the circuitry shown in Figure 3 as address latch 12 in Figure 1. *Id.* at 15. It was on this basis—that Sharp discloses that the circuit of Figure 3 can be address latch 12—that we instituted trial on this ground. Dec. on Inst. 13–15. Patent Owner argues that Petitioner has failed to prove sufficiently that

the circuitry of Figure 3 is address latch 12 in Figure 1, and thus, Petitioner's contention that Sharp anticipates claims 1–6, 16, 19, and 20 must fail. PO Resp. 4–19.

Patent Owner offers testimony and argument why Figure 3 could not be used as address latch 12. PO Resp. 4–19; Ex. 2015 ¶¶ 17–37. In particular, Patent Owner argues and offers evidence that if the circuit of Figure 3 were used as address latch 12, without any modification, it would not be able to read an address because there is no address to be read when the circuit of Figure 3 reads data. PO Resp. 4–10. Patent Owner further argues that the circuit of Figure 3 is for storing “data,” not “addresses.” PO Resp. 10–13. Finally, Patent Owner argues that even if the circuit of Figure 3 could read and store addresses, it cannot be address latch 12 because it would cause the memory of Sharp to operate in a manner inconsistent with the disclosure of Sharp. PO Resp. 14–19.

We are persuaded that Petitioner has failed to establish that Sharp anticipates claims 1–6, 16, 19, and 20 of the '403 patent, because Petitioner has failed to show by a preponderance of the evidence Sharp discloses the elements of claims 1–6, 16, 19, and 20 as arranged in those claims.

As we mentioned above, Petitioner asserts that Sharp discloses that address latch 12 in Figure 1 may include the circuitry shown in Figure 3. Pet. 15 (citing Ex. 1002, Fig. 3, col. 4, ll. 22–26; Ex. 1011 ¶ 29). Yet we do not agree that Sharp's disclosure regarding the use of the circuit of Figure 3 as address latch 12 is clear on its face or unambiguous. The cited portion of Sharp actually states that “[i]n Fig. 3 a circuit is illustrated which may be used for latches or other logic circuits. The memory of Fig. 1 may be realized without this circuit and conversely, the circuit may be used in other

than the memory of Fig. 1.” Ex. 1002, col. 4, ll. 22–26. At best, this statement suggests that the circuit of Figure 3 could be used somewhere in the memory of Figure 1. The statement also could be read as saying that Figure 3 represents an independent disclosure, and that a skilled artisan could modify the circuit of Figure 3 to create the memory of Figure 1. Indeed, the statement establishes that the memory of Figure 1 does not need to use the circuitry of Figure 3. *Id.* The Petition points us to nothing in Sharp that expressly discloses, nor does the Petition provide an analysis as to why a skilled artisan would understand, that Figure 3 is used as address latch 12, or even could be used as address latch 12—without modification—as Petitioner contends. *See* Pet. 14–21.

The only other evidence that Petitioner cites on this point in its Petition, the Murphy Declaration (Ex. 1011), is not persuasive because the Murphy Declaration contains the same conclusory statement as the Petition, and cites the same statement from Sharp without any additional analysis or explanation. *See* Ex. 1011 ¶ 29. But as we explained above, these statements are insufficient, and are no more persuasive coming from an expert witness, rather than the Petition, without some additional reasoning and explanation. *See Perreira v. Dep’t of Health and Human Serv.*, 33 F.3d 1375, 1377 n.6 (Fed. Cir. 1994) (“An expert opinion is no better than the soundness of the reasons supporting it.”).

In the Supplemental Murphy Declaration (Ex. 1016), Mr. Murphy testifies that he has been “asked to provide additional thoughts as to whether the circuitry of Figure 3 can be used as the address latch 12 in Figure 1.” Ex. 1016 ¶ 19. Mr. Murphy testifies that address latch 12 is a latch depicted in Figure 1 that can embody the circuitry depicted in Figure 3. *Id.* ¶ 19.

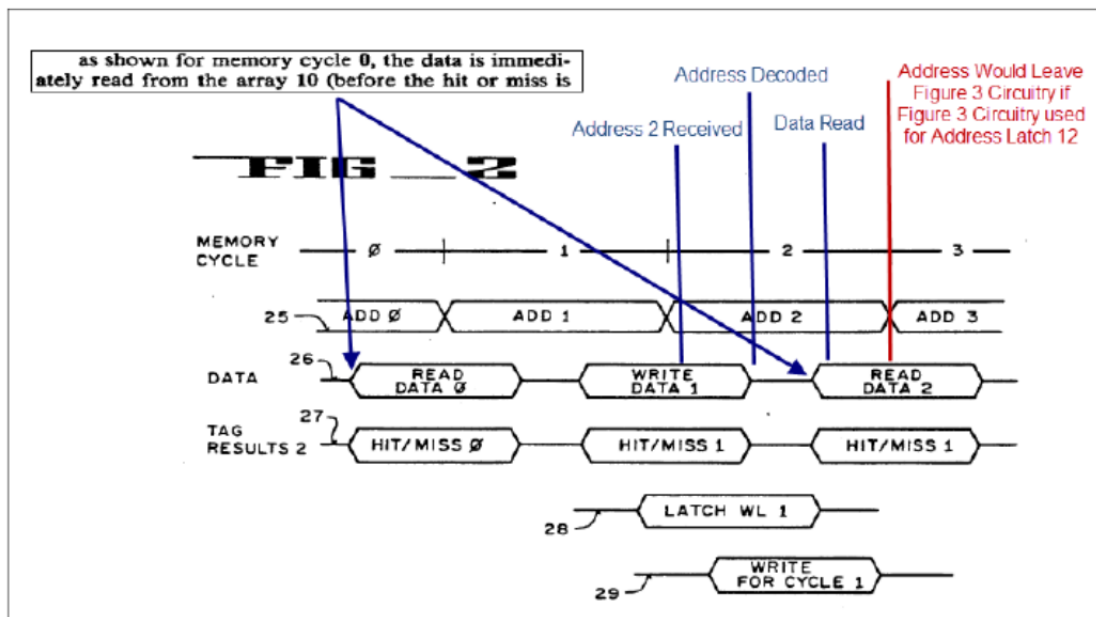
Mr. Murphy goes on to testify that the other two possible structures depicted in Figure 1, write latch 14 and decoded address latch 18, cannot be implemented with the circuitry of Figure 3. *Id.* ¶¶ 19–20. Mr. Murphy bases this conclusion on the fact that write latch 14 and decoded address latch 18 require an additional input, a control signal from control block 17, and that the control signal is not present in Figure 3. *Id.* ¶ 20.

This testimony and its conclusion could be significant, but only if we assume that Figure 3 must be capable of being used, without modification, somewhere in Figure 1. Mr. Murphy appears to start with that assumption and then eliminates possible candidate structures in Figure 1 until only one is left. *Id.* ¶¶ 19–20. Mr. Murphy does not provide a reason why a person of ordinary skill would understand Sharp as disclosing the use of Figure 3, without any modifications, in Figure 1, so we are left to speculate on this critical connection between Sharp’s explicit disclosure and Petitioner’s contentions. This conspicuous gap in the provided analysis undermines the persuasive weight of his testimony.

We also find Mr. Murphy’s testimony unpersuasive because the testimony is inconsistent with the disclosure of Sharp. If Petitioner’s contention were correct, then Figure 3 can be used only as address latch 12. Sharp, however, does not describe Figure 3 to be as limited as Petitioner argues, and, instead, states that Figure 3 shows circuitry “which may be used for latches or other logic circuits.” Ex. 1002, col. 4, ll. 22–26. Thus, we find Mr. Murphy’s new testimony that Figure 3 can be used only as address latch 12 to be inconsistent with the open-ended description in Sharp. Without an explanation that reconciles Sharp’s description of Figure 3 with Mr. Murphy’s new analysis, we are persuaded that Mr. Murphy’s testimony

is entitled to little or no weight. See *Network Commerce, Inc. v. Microsoft Corp.*, 422 F.3d 1353, 1361 (Fed. Cir. 2005) (“[E]xpert testimony at odds with the intrinsic evidence must be disregarded.”).

In addition to the gaps in Mr. Murphy’s reasoning and the tension between Mr. Murphy’s testimony and the disclosure of Sharp, the probative value of Mr. Murphy’s testimony is diminished further in light of certain evidence presented by Patent Owner. Patent Owner has presented evidence that—even if we assume that the other arguments Patent Owner raises in its Response are incorrect—simply inserting the circuitry of Figure 3 into Figure 1 yields a device that would operate in a manner that is inconsistent with the disclosure of Sharp. PO Resp. 14–19. In particular, Patent Owner’s expert testifies that Sharp discloses that data in Sharp must be read before the receipt of the hit/miss signal. Ex. 2015 ¶ 35 (citing Ex. 1002, col. 3, ll. 48–57). This is illustrated in the annotated version of Figure 2 below:



This is Figure 2 of Sharp, annotated by Patent Owner’s expert. *Id.* ¶ 36. Patent Owner’s expert’s interpretation of Sharp’s disclosure of the sequence

of address read, address decoding, and data read, in the circuit of Figure 1 are shown in blue on the annotated Figure 2. *Id.* ¶ 35. The time when the address would be available in the circuit resulting from using the circuit of Figure 3 as address latch 12 is shown in red. *Id.* ¶ 36. Patent Owner's expert testified that, as illustrated above, Petitioner's proposed circuit would not deliver the address to decoder 11 until well after the hit or miss signal could be detected. *Id.* ¶¶ 36, 37. Patent Owner's expert testifies this timing would be inconsistent with Sharp's disclosure and would result in a circuit that does not work as described. *Id.*

Petitioner's response to this argument is that Figure 3 does not introduce delay. Pet. Reply 3–4. This response does not address, however, Patent Owner's argument. Patent Owner agrees with Petitioner's description of the speed of Figure 3. *See* PO Resp. 15; Tr. 30:20–31:9. The question is whether Patent Owner's expert's testimony correctly states the timing of the “read” operation. On that point, Petitioner fails to refute this contention with objective evidence, and instead resorts to attorney argument. *See* Tr. 58:7–62:23. But mere attorney argument cannot carry Petitioner's burden. *See Meitzner v. Mindick*, 549 F.2d 775, 782 (CCPA 1977). Thus, Patent Owner's expert's testimony stands un rebutted. Our review of that testimony shows that it is reasoned, and supported by the citations to Sharp. Thus, we decide that Patent Owner's evidence is entitled to significant weight. *See, e.g., Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another “unless no reasonable trier of fact could have done so”); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) (“[T]he Board is entitled to weigh the declarations and conclude that the lack of factual

corroboration warrants discounting the opinions expressed in the declarations.”).

Taking Patent Owner’s evidence and weighing it against the evidence Petitioner has offered that Figure 3 is, without modification, the address latch of Figure 1, we find that Petitioner has failed to show that Sharp unambiguously discloses such a circuit. *In re Arkley*, 455 F.2d 586, 587 (CCPA 1972) (“[T]he [prior art] reference must clearly and unequivocally disclose the claimed [invention] or direct those skilled in the art to the [invention] without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference.”). Instead, we conclude that Petitioner picks and chooses among the components disclosed in Sharp to assemble the claimed subject matter. This cannot establish anticipation. *See Lindemann Maschinenfabrik GMBH v. Am. Hoist & Derrick Co.*, 730 F.2d 1452, 1459 (Fed. Cir. 1984) (“The requirement that the prior art elements themselves be ‘arranged as in the claim’ means that claims cannot be ‘treated . . . as mere catalogs of separate parts, in disregard of the part-to-part relationships set forth in the claims and that give the claims their meaning.’”).

Even if a skilled artisan would have been able to modify the circuit of Figure 1 of Sharp and its timing such that the circuit of Figure 3 could be used as address latch 12, our reviewing court has held that “differences between the prior art reference and a claimed invention, however slight, invoke the question of obviousness, not anticipation.” *Net MoneyIN, Inc.*, 545 F.3d at 1371. Here, Petitioner has failed to establish by a preponderance of the evidence that Sharp unambiguously discloses the use of the circuit of Figure 3 as address latch 12 in Figure 1, without requiring modification of

the circuit. Thus, we find that Petitioner has failed to show that Sharp anticipates claims 1–6, 16, 19, and 20. *See Arkley*, 455 F.2d at 587 (“[R]ejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art.”).

D. Asserted Anticipation of Claims 1 and 15 Based on Takayanagi (Ex. 1005)

1. Overview of Takayanagi

Takayanagi is titled “Semiconductor Memory.” Ex. 1005, 1.⁹ Takayanagi is directed to a multi-port memory cell array. *Id.* Figure 4 of Takayanagi (as translated) is reproduced below.

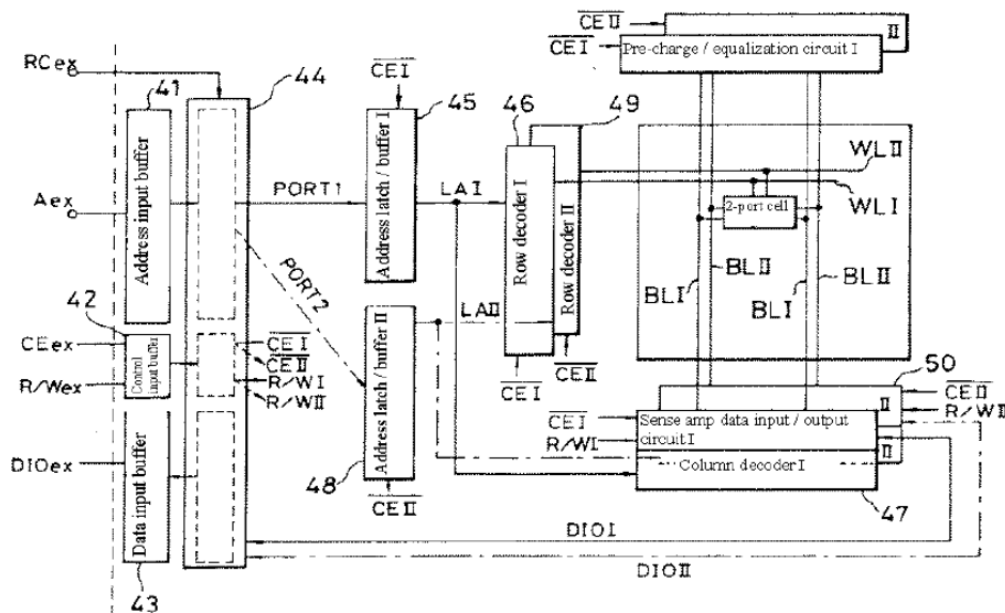


Fig. 4

⁹ All of our citations are to the English translation of Takayanagi and to the page numbers Petitioner included on the bottom, right corner of the exhibit.

Figure 4 shows an example of the memory circuit disclosed in Takayanagi. *Id.* at 3, left col., ll. 40–52.

Figure 4 of Takayanagi discloses a two-port memory circuit having address latch 45 that takes an address on the rising edge of PC_{ex} in front of decoder I (46 and 47) and address latch 48 that takes an address on the falling edge of PC_{ex} in front of decoder I (49 and 50). *Id.* at 3, right col., ll. 5–13. The port switching control circuit operates with port switching signals PC_{ex} . *Id.* at 3, left col., ll. 50–52. Each address latch is preceded by a buffer that receives the address information from an address bus and provides the address information to the address latch. *Id.* at 3, left col., l. 46–right col., l. 13, Fig. 4. The input data and control signals for each port are created similarly. *Id.* at 3, left col., ll. 1–5.

2. Analysis

We instituted trial on the ground of whether Takayanagi anticipates claim 1 and 15 under 35 U.S.C. § 102(b). Dec. on Inst. 20. In view of the entire record, we find that Petitioner has failed to show that Takayanagi discloses storing addresses in response to a “first periodic signal transition” and a “second periodic signal transition,” as recited in claims 1 and 15.

In its Petition, Petitioner advanced the contention that Takayanagi disclosed a register configured to store “(i) a first address in response to a first periodic signal transition and (ii) a second address in response to a second periodic signal transition,” as recited in claim 1. Pet. 29–30. Specifically, Petitioner argues that Takayanagi’s disclosure that addresses are stored in the address latch by

inputting a port switching control signal PC_{ex} with the same cycle as the cycle of the address, and providing a latching means

45 that takes in an address on the rising edge of PC_{ex} in front of decoder I (46 and 47 in the figures), and providing a latching means 48 that takes in an address on the falling edge of PC_{ex} in front of decoder I (49 and 50 in the figures).

Pet. 31 (quoting Ex. 1005, 3, right col., ll. 5–13). Petitioner illustrates this analysis through Figure 5 of Takayanagi, annotated by Petitioner, as shown below:

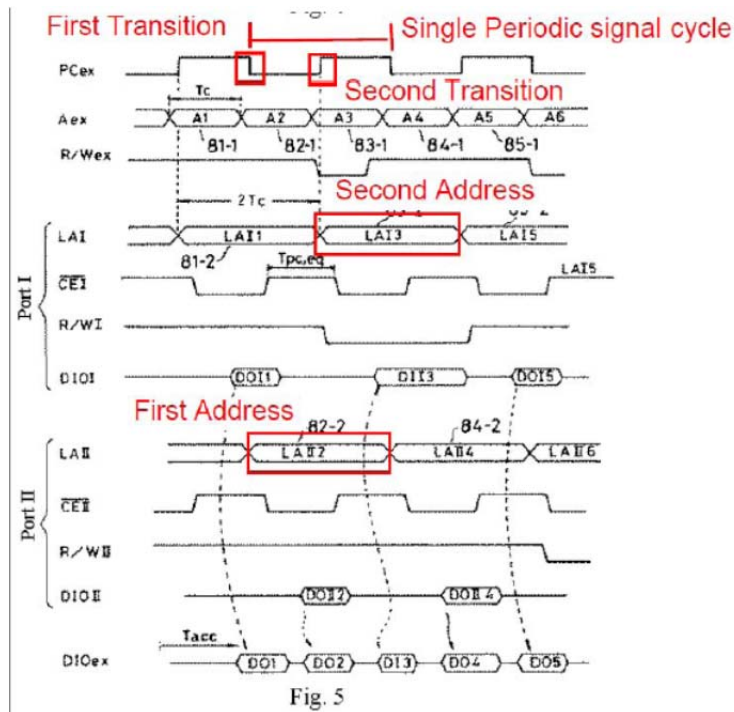


Figure 5, as annotated by Petitioner, shows Petitioner's contentions that Takayanagi discloses storing a first address (LAII2) in response to a first signal transition of PC_{ex} and a second address (LAI3) in response to a second signal transition of PC_{ex}. Pet. 31–32. Petitioner's declarant, Mr. Murphy, agreed and offered a similar analysis. Ex. 1011 ¶¶ 56–57. Based on this evidence and analysis, we instituted trial as to whether Takayanagi anticipates claims 1 and 15. Dec. on Inst. 20.

With a full record, we agree, however, with Patent Owner that this analysis is flawed. PO Resp. 26–31. As Patent Owner and its expert note, the circuit depicted in Figure 4 of Takayanagi, on which Petitioner relies, does not show address latches 45 and 48 or even buffer 41, which receives addresses for Port 1, connected to the PC_{ex} signal. PO Resp. 27–28; Ex. 2015 ¶¶ 39–40. Petitioner concedes this. Tr. 14:19–24 (“They argue there’s no direct connection between PC_{ex} and the address latches There is no direct connection, we admit that.”). Instead, Petitioner now advances a theory that the PC_{ex} signal indirectly causes the addresses to be stored “according to the complementary signals $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ (which were generated from PC_{ex}), as illustrated in Figure 4.” Pet. Reply 7–8.

We are not persuaded by Petitioner’s new theory because the evidence in the record weighs against it. Petitioner strings together several alleged admissions by Patent Owner into the conclusion that the latches operate in response to $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$. *Id.* at 8. In particular, Petitioner argues that Patent Owner “admits” that latching means 45 and 48 operate on the rising and falling edges of PC_{ex}, that $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ are the only control or timing signals shown as connected to latching means 45 and 48, and that $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ are made from PC_{ex}. *Id.* Thus, Petitioner concludes that PC_{ex} indirectly causes the addresses to be stored “according to the complementary signals $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$.” *Id.* Yet even if we followed this logical chain, there is one key factual gap—there is no disclosure in Takayanagi or evidence in the record that $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ are involved in latching the address. Petitioner provides no citation for this conclusion. *Id.* Takayanagi’s only discussion of $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ is that they are “chip enable” signals and that they are

made from PC_{ex}. Ex. 1005, 561, right col, ll. 26–29. The only evidence in the record on this point, the testimony of Patent Owner’s expert, is directly contrary to Petitioner’s assertion that $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ are involved in latching the address. Ex. 2015 ¶¶ 41–44. Petitioner’s attorney argument cannot make up for this factual gap. See *In re Pearson*, 494 F.2d 1399, 1405 (CCPA 1974) (“Attorney’s argument in a brief cannot take the place of evidence.”).

Further, Petitioner provides insufficient reasoning or explanation to support the inferences it seeks to have us draw from the few bits of evidence that it does cite. Pet. Reply 8. The statements presented merely state a series of facts and then state a conclusion. But the conclusion presented—that $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ control latching—does not flow necessarily from the evidence that allegedly supports it. It requires inferences that because the address latching happens at the same time as a transition in PC_{ex}, PC_{ex} necessarily causes the address to be latched, and that because $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ are related to PC_{ex}, they must be controlling latching. We decline to make these inferences without some reasoning or evidence. Therefore, we are not persuaded by the evidence and arguments presented by Petitioner.

In contrast, Patent Owner offers an analysis supported by the testimony of its expert and citations to Takayanagi that explains why it contends that $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ are not involved in latching the addresses. Petitioner has not explained how this explanation is wrong or pointed us to any place in the cross examination of Patent Owner’s expert where it impeached Patent Owner’s expert on this point. This evidence, therefore, stands un rebutted. Given the significant failings in Petitioner’s proof, the

lack of objective evidence to support its contentions, and the un rebutted evidence of Patent Owner, we determine that Petitioner cannot meet its burden of showing unpatentability by a preponderance of the evidence.

Moreover, even if Petitioner did cite some evidence and provide an explanation to support its contentions, it would establish, at best, only that it was possible that Takayanagi discloses $\overline{\text{CE I}}$ and $\overline{\text{CE II}}$ are involved in latching the addresses. Merely establishing a possibility that a reference discloses a claim element is insufficient to establish anticipation. *See In re Oerlich*, 666 F.2d 578, 581 (CCPA 1981) (“Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.”).

Thus, we find that Petitioner has failed to show by a preponderance of the evidence that Takayanagi anticipates claims 1 and 15.

E. Remaining Grounds

We also instituted trial on several obviousness grounds based on Sharp or Takayangi, including (1) that claim 7 was unpatentable as obvious over the combination of Sharp and Chappell, (2) that claim 12 was unpatentable as obvious over the combination of Sharp and Lee, (3) that claim 13 was unpatentable as obvious over the combination of Sharp, Takayanagi, and Proebsting, and (4) that claim 17 was unpatentable as obvious over the combination of Sharp and Suzuki. Petitioner offers no reasoning or rationale to justify using Figure 3 of Sharp as address latch 12 or PC_{ex} to control the latches of Takayanagi based on an obviousness analysis. Instead, Petitioner relies on the same analysis of Sharp and Takayanagi that we have found unpersuasive, as discussed above. Pet. 22–

28, 38–40. Petitioner does not contend that Chappell, Lee, Proebsting, or Suzuki would compensate for any of the deficiencies we have identified in Sharp and Takayanagi. Accordingly, we find that Petitioner also has failed to show, by a preponderance of the evidence, that claims 7, 12, 13, or 17 are unpatentable under 35 U.S.C. § 103(a) based on the combinations identified above.

III. CONCLUSION

Petitioner has failed to prove, by a preponderance of the evidence, that claims 1–7, 12, 13, 15–17, 19, and 20 of the '403 patent are unpatentable.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that it is determined that claims 1–7, 12, 13, 15–17, 19, and 20 of U.S. Patent No. 6,292,403 B1 have not been shown, by a preponderance of the evidence, to be unpatentable;

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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