

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANON INC.,
Petitioner,

v.

INTELLECTUAL VENTURES I LLC,
Patent Owner.

Case IPR2014-00757
Patent 8,300,285 B2

Before THOMAS L. GIANNETTI, JAMES A. TARTAL, and
PATRICK M. BOUCHER, *Administrative Patent Judges*.

BOUCHER, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Canon Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1–20 of U.S. Patent No. 8,300,285 B2 (“the ’285 patent”). After consideration of a

Preliminary Response (Paper 6, “Prelim. Resp.”) filed by Intellectual Ventures I LLC (“Patent Owner”), the Board instituted trial on November 21, 2014. Paper 8 (“Dec.”).

During the trial, Patent Owner timely filed a Patent Owner Response (Paper 14, “PO Resp.”), and Petitioner timely filed a Reply to the Patent Owner Response (Paper 20, “Reply”). An oral hearing was held on June 24, 2015 (Paper 34, “Tr.”).

We have jurisdiction under 35 U.S.C. § 6(c). This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the record before us, Petitioner has not demonstrated, by a preponderance of the evidence, that any claim of the ’285 patent is unpatentable.

B. Related Proceedings

The ’285 patent has been asserted against Petitioner in *Intellectual Ventures I LLC v. Canon Inc.*, 13-cv-473-SLR (D. Del.). Pet. 1.

C. The ’285 Patent

The ’285 patent is a continuation of U.S. Patent No. 7,315,406 (“the ’406 patent”), which is the subject of *Canon Inc. v. Intellectual Ventures I LLC*, Case IPR2014-00535 (PTAB) (“the related proceeding”). The ’285 patent describes scanning circuit structures for scanners capable of reducing distortion during high-speed image signal transmission. Ex. 1001, col. 2, ll. 9–14. Figure 2 of the ’285 patent is reproduced below.

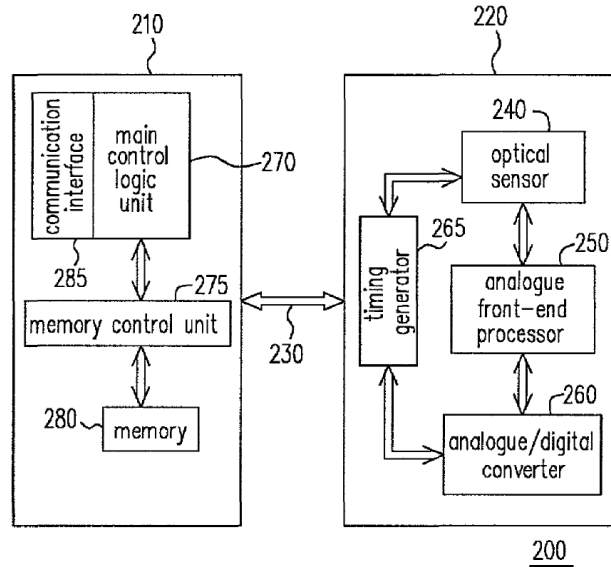


Figure 2 illustrates a circuit structure for a scanner, including main circuit module 210 and optical sensor circuit module 220 linked together with flat cable 230. *Id.* at col. 3, ll. 39–43. Communication interface 285 of the main circuit module allows interfacing with a human being, such as over a universal serial bus (“USB”) interface. *Id.* at col. 3, ll. 50–59. The communication interface receives scanning instructions regarding image resolution, brightness level, and scanning range, and converts such scanning instructions into scanning control signals that are conveyed to the optical sensor circuit module over the flat cable. *Id.* Timing generator 265 produces timing control signals for extracting an analog signal image from optical sensor 240, which may be a charge-coupled device (“CCD”) or complementary metal-oxide-semiconductor (“CMOS”) image sensor. *Id.* at col. 3, ll. 60–66. After preprocessing of a collected image by analog front-end preprocessor 250, analog/digital converter 260 (“A/D converter”) converts the preprocessed image to digital data, which are transmitted to the main circuit module over the flat cable. *Id.* at col. 3, l. 65 – col. 4, l. 4.

The '285 patent identifies two specific advantages of this arrangement. First, a clearer image can be obtained at higher scanning speeds because the flat cable transmits digital data instead of easily distorted analog image signals. *Id.* at col. 4, ll. 25–27. Second, electromagnetic-interference effects are mitigated because the flat cable transmits scanning control signals rather than timing control signals. *Id.* at col. 4, ll. 28–31.

D. Illustrative Claim

Claim 7 of the '285 patent is illustrative of the claims at issue:

7. An apparatus, comprising:
 a main circuit module;
 a connection cable; and
 an optical sensor circuit module coupled to the main circuit module through the connection cable, wherein the optical sensor circuit module is configured to:
 receive scan control signals from the main circuit module; and
 generate timing control signals for extracting an analog image signal in response to the received scan control signals, wherein the received scan control signals do not comprise any timing control signals.

E. Grounds of Unpatentability

Petitioner relies on the following references.

Hayashi	JP H11-041389	Feb. 12, 1999	Ex. 1004
Tsuboi	JP H11-046302	Feb. 16, 1999	Ex. 1005
Wada	JP 2000-244716	Sept. 8, 2000	Ex. 1006
Shiraishi	JP H11-205556	July 30, 1999	Ex. 1007
Kono	US 6,958,830 B2	Oct. 25, 2005	Ex. 1008
Ochiai	US 5,457,544	Oct. 10, 1995	Ex. 1009

We instituted this proceeding based on the following grounds.

Reference(s)	Basis	Claim(s) Challenged
Hayashi	§ 102(b)	1, 5, 7, 11, 13, 17, and 18
Hayashi and Kono	§ 103(a)	6, 12, 19, and 20
Hayashi and Shiraishi	§ 103(a)	2–4, 8, and 14–16
Hayashi, Shiraishi, and Ochiai	§ 103(a)	9 and 10
Tsuboi and Wada	§ 103(a)	1–7, 11–14, and 16–20
Tsuboi, Wada, and Shiraishi	§ 103(a)	8 and 15
Tsuboi, Wada, Shiraishi, and Ochiai	§ 103(a)	9 and 10

II. ANALYSIS

A. *Claim Construction*

The Board interprets claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, at 1277–79 (Fed. Cir. 2015); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

1. “*scanning instruction*”

In the Institution Decision, we construed “scanning instruction” as an instruction for scanning. Dec. 5. We see no reason to alter that construction based on the positions of the parties as developed during the trial, and adopt it herein.

2. “*scan control signals*” and “*timing control signals*”

In the Institution Decision, we construed “scan control signals” as signals for scan control, and construed “timing control signals” as signals

generated by a timing generator and used to control the timing of extraction of an analog image signal. Dec. 5–7. After considering the submissions of the parties and their respective positions regarding the prior art, discussed *infra*, we revisit our constructions of these terms. In particular, our preliminary construction of “timing control signals” was “mindful that the phrase appears in the claims as part of a negative limitation, namely that ‘received scan control signals *do not* comprise any timing control signals.’” *Id.* at 6. But Patent Owner points out that “timing control signals” also is recited positively in the claims, such as in claim 7’s recitation that the optical sensor circuit module is configured to “generate timing control signals for extracting an analog image signal in response to the received scan control signals.” PO Resp. 8. In light of the tension between positive and negative recitations of “timing control signals,” it is not apparent that a relatively narrow construction of “timing control signals” corresponds to the broadest reasonable interpretation of the claims as a whole.

Petitioner proposes that “scan control signals” be construed as intermediary signals based on the scanning instruction and that “timing control signals” be construed as signals generated by a timing generator and used to control the timing of extraction of an analog image signal. Pet. 6–7. Patent Owner proposes that “scan control signals” be construed as signals for scan control and that “timing control signals” be construed as signals for timing control. Prelim. Resp. 5–7. We agree with Patent Owner that Petitioner’s proposed construction for “scan control signals” improperly introduces extraneous terms. *Id.* at 5; see Dec. 5–6.

With respect to construing “timing control signals,” several considerations are relevant. First, the Specification of the ’285 patent explains that the “flat cable transmits scanning control signals . . . *instead of* timing control signals.” Ex. 1001, col. 4, ll. 26–28 (emphasis added). In the related proceeding, we observed that this portion of the Specification “suggests a distinction between scanning control signals and timing control signals,” but “does not support unambiguously Patent Owner’s position of complete independence between scan control signals and timing control signals.” *Canon Inc. v. Intellectual Ventures I LLC*, Case IPR2014-00535, slip op. at 8 (PTAB Sept. 23, 2015) (Paper 37). We note that a construction of “scan control signals” and “timing control signals” that effected such complete independence would render the negative limitation that “the received scan control signals do not comprise any timing control signals” superfluous in the claims of the ’285 patent. “A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.” *Merck & Co., Inc. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) (citing *Elekta Instrument S.A. v. O.U.R. Sci. Int’l, Inc.*, 214 F.3d 1302, 1307 (Fed. Cir. 2000)); see *Gen. Am. Transp. Corp. v. Cryo-Trans, Inc.*, 93 F.3d 766, 770 (Fed. Cir. 1996) (rejecting district-court claim construction that rendered claim requirement superfluous).

Second, we disagree with Petitioner’s contention that Patent Owner’s proposed constructions are “inconsistent with the claim language itself” and “would *per se* violate the negative limitation.” Reply 3–4. We agree, instead, with Patent Owner that Petitioner’s proposed construction is deficient because it would give no patentable weight to the negative

limitation. PO Resp. 12–13. Petitioner contends that “under [Patent Owner’s] theory, the very scan control signals used in the sole embodiment of the ’285 patent would violate the negative limitation,” and that it is legally untenable to adopt a claim construction that excludes the sole embodiment of the Specification. *Id.* at 4–5. Although the Specification does not support unambiguously a position of complete independence between scan control signals and timing control signals, the Specification also is not unambiguously inconsistent with such a position. In particular, Petitioner’s argument overstates the impact of the claims’ requirement of generating timing control signals “in response to” the received scan control signals. *See id.* at 3–4. This language is meaningfully different than the requirement of the claims in the related proceeding of “*converting* the scan control signals to timing control signals.” *See Canon*, Paper 37, at 6–7 (emphasis added). Specifically, generation of timing control signals “in response to” received scan control signals does not require any change of form of the received scan control signals as part of that generation.

Third, during prosecution, the Examiner found that Kono’s primary clock signal corresponds to the recited scan control signals and that the secondary control signals correspond to the recited timing control signals. Ex. 1010 at 4, 7, 9. As the Federal Circuit recently emphasized, “‘claims should always be read in light of the specification and teachings in the underlying patent’ [and the Board] should also consult the patent’s prosecution history in proceedings in which the patent has been brought back to the agency for a second review.” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (quoting *In re Suitco Surface*

Inc., 603 F.3d 1255, 1260 (Fed. Cir. 2010), citing *Tempo Lighting Inc. v. Tivoli LLC*, 742 F.3d 973, 977 (Fed. Cir. 2014)). To distinguish Kono, the applicant amended the claims by adding the negative limitation, arguing that “Kono fails to disclose communication means for receiving scan control signals from a main circuit module . . . wherein the received scan control signals do not comprise any timing control signals.” PO Resp. at 9. In allowing the application, the Examiner indicated that the independent claims “define[] over Kono . . . since the scan control signals of Kono include[] timing control signals.” Ex. 2005 at 224. Petitioner’s proposed construction of “timing control signals” would exclude the same signals determined to be timing control signals during prosecution.

In light of these considerations, and applying the broadest reasonable interpretation in light of the Specification and prosecution history, we construe “timing control signals” as signals that affect timing control, and we construe “scan control signals” as signals that affect scan control. We note that these constructions are the same as the constructions we adopted in the related proceeding. *Canon*, Paper 37, at 9–10.

3. *Means-Plus-Function Limitations*

Claims 1–6 include several terms recited as “means for” performing identified functions. In the Institution Decision, we construed these recitations under 35 U.S.C. § 112, ¶ 6, as follows. Dec. 7–8. We see no reason to alter those constructions based on the positions of the parties as developed during the trial, and accordingly adopt them herein.

“means for . . .”	Corresponding structure
“communication means for receiving scan control signals”	connection cable 230
“. . . generating timing control signals”	timing signal generator 265
“. . . receiving a scanning instruction from a communication interface”	main circuit module 210, main control logic unit 270, or communication interface 285
“. . . producing the scan control signals”	main control logic unit 270, main circuit module 210, or communication interface 285
“. . . converting the analog image signal into digital image data”	analog/digital converter 260
“. . . extracting the analog image signal”	optical sensor circuit module 220 and optical sensor 240
“. . . generating the analog image signal”	optical sensor 240
“. . . pre-processing the analog image signal”	analog front-end processor 250
“. . . converting the . . . analog image signal into the digital image data”	analog/digital converter 260

B. Hayashi-Based Grounds

Petitioner challenges claims 1, 5, 7, 11, 13, 17, and 18 as anticipated under 35 U.S.C. § 102(b) by Hayashi; challenges claims 6, 12, 19, and 20 as unpatentable under 35 U.S.C. § 103(a) over Hayashi and Kono; challenges claims 2–4, 8, and 14–16 as unpatentable under 35 U.S.C. § 103(a) over Hayashi and Shiraishi; and challenges claims 9 and 10 as unpatentable under 35 U.S.C. § 103(a) over Hayashi, Shiraishi, and Ochiai. Pet. 17–41.

Hayashi describes an image-processing device. Ex. 1004 ¶ 1. Figure 1 of Hayashi is reproduced below.

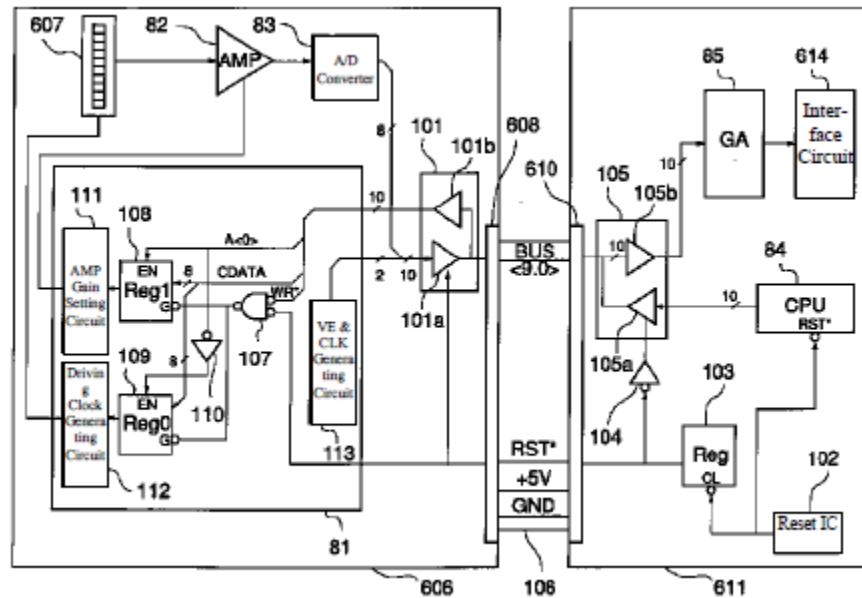


Figure 1 illustrates a structure for a scanner separated into two components joined by scanning cable 106: image processing substrate 611 and reading substrate 606 that includes an image sensor. *Id.* ¶ 3. Image processing substrate 611 includes a CPU that provides overall control of the scanner. *Id.* ¶ 8. When an operator initiates a scanning operation, the CPU outputs a set of signals identified by Hayashi as WR*, A<0>, and CDATA<7, . . . ,0>.¹ *Id.* ¶ 13. The set of signals collectively include ten bits: signal CDATA<7, . . . ,0> is an eight-bit data bus, *id.* ¶ 13; signal A<0> is the least significant bit of a 16-bit address bus, *id.* ¶ 13; and signal WR* is a one-bit writing signal, *id.* ¶ 35.

After originating at CPU 84, the set of signals passes into bidirectional buffer 105 of image processing substrate 611, through connector 610, across

¹ Reference in ¶ 13 of Petitioner's English translation of Hayashi to "CDATA<7, . . . , 60>" (emphasis added) appears to be an error, as evident from a comparison with the original Japanese version of the same paragraph.

scanning cable 106, through connector 608, and into bidirectional buffer 101. The signals then pass to different circuitry components. Of particular relevance, signal A<0> passes to register 109 through inverter 110 so that the inverted digital value of A<0> is input to enable terminal EN of register 109. *Id.* ¶ 37. In addition, signal CDATA<7, . . . ,0> provides 8-bit operating-mode data that are written to register 109. *Id.* ¶ 13. The output of register 109, which depends on values of A<0> and CDATA<7, . . . ,0>, is input into driving clock generating circuit 112 to set the driving mode of the image sensor. *Id.* ¶ 39. Signals generated by driving clock generating circuit 112 drive image sensor 607 and extract analog image data. *Id.* ¶ 40.

Each of independent claims 1, 7, and 13 of the '285 patent recites generation of timing control signals in response to receipt of scan control signals, “wherein the [received] scan control signals do not comprise any timing control signals.” Petitioner contends that all limitations of the independent claims, including this recitation, are disclosed by Hayashi. Pet. 17–25. Specifically, Petitioner contends that the set of signals WR*, A<0>, and CDATA<7, . . . ,0> are “scan control signals” and that the signals output by driving clock generating circuit 112 are “timing control signals.” *Id.* at 17–19. Petitioner identifies a distinction in the functionality of signals WR*, A<0>, and CDATA<7, . . . ,0>, and the functionality of signals output by driving clock generating circuit 112. Because the signals output by the driving clock generating circuit are produced in response to a data value carried by CDATA<7, . . . ,0>, Petitioner contends that CDATA<7, . . . ,0> is not itself a timing control signal. *Id.* at 19. According to Petitioner, only signals output by Hayashi’s driving clock generating circuit are timing

control signals, not signals traveling to the driving clock generating circuit.

Id. Petitioner supports its argument with testimony by Richard Carley, Ph.D. Ex. 1002 ¶¶ 52–60, 121–128, 196–203.

Patent Owner responds that “[a]t least some of the identified scan control signals, such as the operating mode data of CDATA<7, . . . ,0>[,] are timing control signals.” PO Resp. 43–44; *see id.* at 42. Patent Owner observes that CPU 84 of Hayashi generates signals A<0> and the operating mode data of CDATA<7, . . . ,0>, and Patent Owner’s declarant, Richard G. Zech, Ph.D., testifies that “CPUs are understood by one of ordinary skill in the art to control timing generators.” *Id.* at 42; Ex. 2004 ¶ 110. The operating mode data of CDATA<7, . . . ,0> ultimately “cause the image sensor [607] to be driven.” Ex. 1004 ¶ 40. Because the operating mode data of CDATA<7, . . . ,0> control the driving clock, they are used to control the timing of extraction of an analog image signal for timing control. Ex. 2004 ¶ 110. Patent Owner reasons that at least CDATA<7, . . . ,0> is a “scan control signal” that comprises a “timing control signal.” PO Resp. 43.

Under the claim construction we have adopted, we are persuaded by Patent Owner’s analysis. Based on the evidence before us, we find that Petitioner has not demonstrated that Hayashi discloses “wherein the received scan control signals do not comprise any timing control signals,” as recited in each of the independent claims. Patent Owner’s analysis thus applies to all claims of the ’285 patent. Accordingly, we conclude that Petitioner has not established, by a preponderance of the evidence, that any claim of the ’285 patent is unpatentable over Hayashi alone or in combination with other art.

C. Tsuboi-Wada-Based Grounds

Petitioner challenges claims 1–7, 11–14, and 16–20 as unpatentable under 35 U.S.C. § 103(a) over Tsuboi and Wada; challenges claims 8 and 15 as unpatentable under 35 U.S.C. § 103(a) over Tsuboi, Wada, and Shiraishi; and challenges claims 9 and 10 as unpatentable under 35 U.S.C. § 103(a) over Tsuboi, Wada, Shiraishi, and Ochiai. Pet. 41–59.

Tsuboi describes an image-reading device that uses a CCD to collect image data. Ex. 1005 ¶ 1. Figure 4 of Tsuboi is reproduced below.

[FIG. 4]

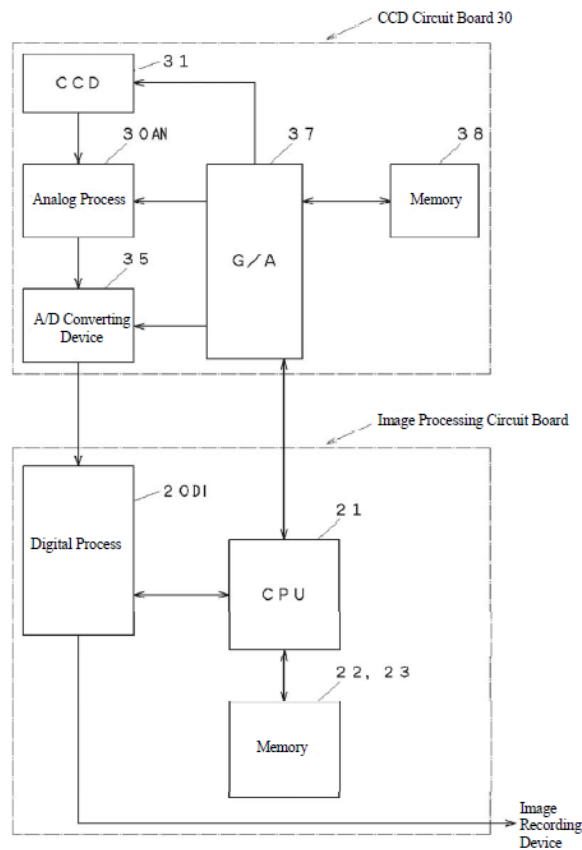


Figure 4 provides a schematic illustration of the image-reading device with components distributed between an image processing circuit board and a CCD circuit board. *Id.* ¶ 36. Petitioner draws a correspondence between (1) the image processing circuit board of Tsuboi and the optical sensor circuit module recited in the claims of the '285 patent, and (2) the CCD circuit board of Tsuboi and the main circuit module recited in the claims. Pet. 42. The image processing circuit board and the optical sensor circuit module are connected by a flexible cable. Ex. 1005 ¶ 25. Similar to the configuration shown in Figure 2 of the '285 patent, Tsuboi discloses that the CCD circuit board includes CCD image sensor 31, analog processing circuit 30AN, analog-digital converter 35, and “signal processing circuit 37 for controlling the timing with which the CCD 31 is driven and for generating a clock.” *Id.* ¶ 36; *see id.* ¶ 3. Signals used to generate that timing information are received from the image processing circuit board. *Id.* ¶ 39. Specifically, in response to a scanning instruction supplied by a user, CPU 21 on main circuit module 20 generates a primary scanning synchronization signal that is transmitted via the flexible cable to signal processing circuit 37, which generates signals that control the timing with which CCD 31 generates and extracts analog image signals. *Id.* ¶¶ 39, 25.

Petitioner acknowledges that “Tsuboi does not explain in detail how [signal processing] circuit 37 generates the timing control signals in response to the scan control signals,” but contends that “one of ordinary skill in the art would have appreciated that the scan control signals would have been processed to generate the timing control signals.” Pet. 43. Petitioner supports its contention with declaration testimony by Dr. Carley that it was

known at that time to generate timing control signals at an optical sensor circuit module in response to a synchronization signal like the primary synchronization signal in Tsuboi. *Id.* (citing Ex. 1002 ¶¶ 64–67).

Wada describes an image-reading device that uses an image sensor to read a document. Ex. 1006 ¶ 1. Figure 5 of Wada is reproduced below.

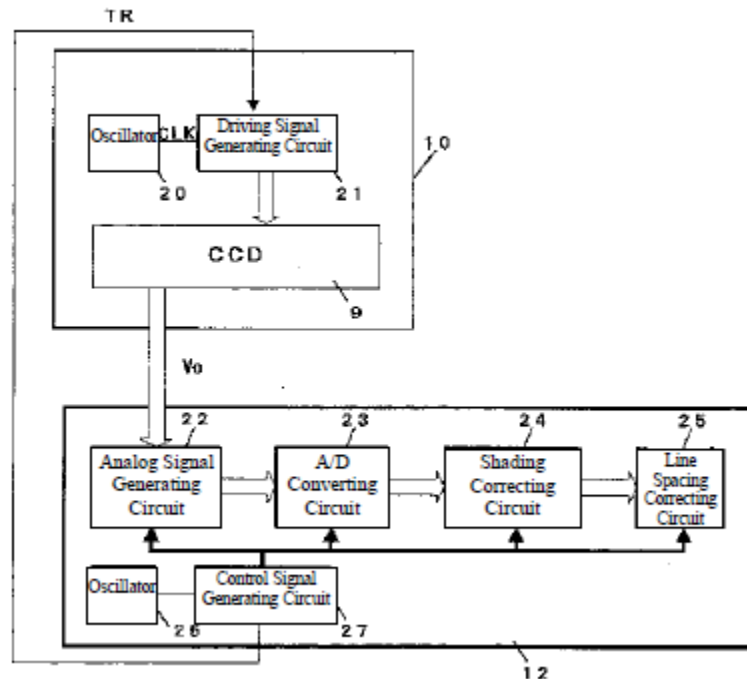


Figure 5 is a block diagram illustrating a structure for the image-reading device, including sensor substrate 10 and processing substrate 12. *Id.* ¶ 15. The sensor substrate includes image sensor (CCD) 9, oscillator 20, and driving signal generating circuit 21. *Id.* The processing substrate includes analog signal generating circuit 22, A/D converting circuit 23, shading correcting circuit 24, line spacing correcting circuit 26, oscillator 26, and control signal generating circuit 27. *Id.* ¶ 17. In response to transmission of a synchronization signal TR from the signal processing substrate to the sensor substrate, the driving signal generating circuit

generates signals shift pulse SH, transmission clocks $\phi 1$ and $\phi 2$, reset signal ϕRS , and clamp signal ϕCLP for outputting an image signal to the image sensor. *Id.* ¶ 15. Petitioner identifies such signals as “timing control signals.” Pet. 44.

Petitioner thus contends that all limitations of the independent claims, including the requirement that “the [received] scan control signals do not comprise any timing control signals,” are disclosed by Tsuboi and Wada. Pet. 41–54.

Patent Owner responds that “[p]eople of ordinary skill in the art would readily recognize Tsuboi’s primary scanning synchronization signal and Wada’s synchronization signal TR are timing control signals.” PO Resp. 25. Similar to its argument directed at the Hayashi-based grounds, Patent Owner relies on testimony by Dr. Zech that a “CPU is understood by one of ordinary skill in the art to control a timing generator.” *Id.* at 25–26 (citing Ex. 2004 ¶ 69). Patent Owner observes that “Tsuboi’s primary scanning synchronization signal is generated . . . by CPU 21” and that “Wada’s synchronization signal TR is also generated by a timing generator, namely control signal generating circuit 27.” *Id.* (citing Ex. 1005 ¶ 39; Ex. 1006 ¶ 18). Patent Owner further notes that Petitioner’s expert, Dr. Carley, acknowledged during his deposition that the primary scanning synchronization signal “is used to ***align the reading out of the CCD in time***, meaning it starts it up.” *Id.* at 26 (citing Ex. 2006, 72:14–16).

Under the claim construction we have adopted, we are persuaded by Patent Owner’s analysis. Based on the evidence before us, we find that Petitioner has not demonstrated that Tsuboi or Wada discloses “wherein the

received scan control signals do not comprise any timing control signals,” as recited in each independent claim. Patent Owner’s analysis thus applies to all claims of the ’285 patent. Accordingly, we conclude that Petitioner has not established, by a preponderance of the evidence, that any claim of the ’285 patent is unpatentable over Tsuboi and Wada together or in combination with other art.

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, based on a preponderance of the evidence, claims 1–20 of U.S. Patent No. 8,300,285 B2 have not been shown to be unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2014-00757
Patent 8,300,285 B2

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