

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORPORATION,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00971
Patent 8,359,501 B1

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and
GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

GAUDETTE, *Administrative Patent Judge*.

DECISION
Petitioner's Request for Rehearing
37 C.F.R. § 42.71(d)

I. BACKGROUND

Sandisk Corporation (“Petitioner”) filed a Request for Rehearing (Paper 35, “Req. Reh’g” or “Request”) of our Final Decision (Paper 34, “Final Dec.”).

In our Final Decision, we concluded Petitioner demonstrated, by a preponderance of the evidence, unpatentability of claims 1–3, 5–8, and 11–20, but not claims 4, 9, 10, and 15 of U.S. Patent No. 8,359,501 B1 (Ex. 1001, “the ’501 patent”). More specifically, we determined Petitioner had shown, by a preponderance of the evidence, unpatentability of:

(a) claims 1–3, 5–8, 11–14, and 16–20 under 35 U.S.C. § 102(b) based on U.S. Patent Application Publication No. 2005/0257109 A1 (Ex. 1003, “Averbuj”); and

(b) claims 1–3, 5, and 14–16 under 35 U.S.C. § 103(a) based on Huang et. al., *An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers*, Fourteenth International Conference on VLSI Design 379–384 (IEEE 2001) (Ex. 1004, “Huang”).

We determined Petitioner had not met its burden to establish unpatentability of:

- (c) claim 15 under 35 U.S.C. § 102(b) based on Averbuj;
- (d) claim 4 under 35 U.S.C. § 103(a) based on Huang;
- (e) claims 6–8, 11, and 17–20 under 35 U.S.C. § 103(a) based on Huang and Averbuj; and
- (f) claims 9 and 10 under 35 U.S.C. § 103(a) based on Huang, Averbuj, and JEDEC Standard, Fully Buffered DIMM (FBDIMM): DFX Design for Validation and Test, JESD82–28 (Ex. 1006).

Petitioner requests rehearing of our holding as to above-listed challenges (c), (d), and (f). For the reasons discussed below, we *grant* Petitioner’s Request for Rehearing of challenge (f) and modify our Institution Decision and our Final Decision as outlined in our Order, below. Petitioner’s Request for Rehearing of challenges (c) and (d) is *denied*.

II. STANDARD OF REVIEW

The party requesting rehearing has the burden of showing the decision should be modified, and “[t]he request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply.” 37 C.F.R. § 42.71(d).

III. UNPATENTABILITY OF CLAIM 4 UNDER 35 U.S.C. § 103(a) BASED ON HUANG

Claim 4 depends from independent claim 1, and recites: “wherein the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers.”

A. Background

In its Petition (Paper 1, “Pet.”), Petitioner challenged the patentability of claim 4 under 35 U.S.C. § 103(a) based on Huang in view of U.S. Patent Application Publication No. 2007/0070669 (Ex. 1005, “Tsern”). *See* Pet. 41–42. Petitioner did not identify explicitly a challenge as to any claim based solely on Huang, but also challenged the patentability of claims 1–3, 5, and 14–16 based on the combination of Huang and Tsern. *See id.* at 6. In support of a motivation to combine Huang and Tsern, Petitioner relied on the declaration testimony of its expert, Dr. Donald Alpert (Ex. 1007). *See id.* at

42 (citing Ex. 1007 ¶ 157). In concluding Petitioner had not demonstrated a reasonable likelihood it would prevail in showing that claim 4 would have been obvious over Huang in view of Tsern, we explained that it was unclear on the record whether the disclosure in the '501 patent relied on by Dr. Alpert was a description of the prior art, and that Dr. Alpert's opinions "lack[ed] sufficient articulated reasoning with rational underpinning as to why an ordinary artisan at the time of the invention would have had a reason to combine the prior art elements in the manner required by the challenged claims. Institution Decision (Paper 12, "Dec. on Inst."), 16, 19–20. We determined, however, that Petitioner had demonstrated a reasonable likelihood that it would prevail in showing claim 4 would have been obvious over Huang, alone (*id.* at 18), and instituted an *inter partes* review of the '501 patent on this ground (*id.* at 22).

B. Argument

Petitioner acknowledges that we had authority to institute trial based on obviousness over Huang, alone, even though Petitioner did not identify this ground explicitly in the Petition. Req. Reh'g 2–3 (citing *SightSound Techs., LLC v. Apple Inc.*, No. 2015-1159, 2015 WL 8770164, at *3 (Fed. Cir. Dec. 15, 2015); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1274 (Fed. Cir. 2015), *cert. granted, sub nom. Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 890 (mem.) (2016)). Petitioner argues, however, that we erred in our interpretation of the law in requiring it to identify evidence in the Petition to support this ground of unpatentability, because the Board relied not only on evidence cited in the Petition, but also on its own findings with respect to the teachings of Huang. *See id.* at 3–4; *see also id.* at 9 ("The Board [itself] expanded the scope of trial beyond the four corners of the

Petition by instituting on a new ground – Huang alone.”). Petitioner contends we should have adopted, at the trial phase, our finding of “sufficient evidence in the Petition and Huang to institute review on the grounds that Huang alone discloses or renders claim 4 obvious” (*id.* at 5) thereby shifting the burden of production to Patent Owner to rebut this finding. *See id.* at 5–7. Petitioner contends the Board, instead, improperly placed the burden on Petitioner at trial to identify evidence in the Petition alone to support a prima facie case of unpatentability based on Huang. *See id.* at 3–7. Petitioner argues that if we had adopted and/or allowed Petitioner to rely on our findings made in the Institution Decision with respect to the teachings of Huang, we would not have found the arguments and evidence in the Reply (Paper 25) to be “outside the scope of a proper reply.” *Id.* at 9 (quoting Final Dec. 52). Petitioner contends we erred in failing to consider the arguments in the Reply and evidence presented in Dr. Alpert’s second declaration in support thereof that “directly reinforce[] **the Board’s finding** that Huang alone teaches or suggests two physically separate integrated circuit packages[,] . . . and **directly counter[]** Patent Owner’s assertion to the contrary” (*id.* at 10). *See id.* at 9–11.

C. Analysis

Petitioner’s arguments are based on an underlying contention that, because the Board *sua sponte* raised a patentability challenge based on Huang alone, whereas Petitioner’s challenge was based on a combination of Huang and Tsern, the Board relied on evidence that was not cited in the Petition. Petitioner has not identified, nor do we find, however, any indication in our Institution Decision that we relied on evidence other than that expressly cited by Petitioner, e.g., Dr. Alpert’s statement that “[t]o the

extent th[e] additional claim [4] element may not be disclosed by Huang alone, it is disclosed by Tsern” (Dr. Alpert’s first declaration (Ex. 1007) ¶ 156, *cited in* Pet. 42). *See* Dec. on Inst. 17–18. Petitioner has not explained, moreover, why it delayed more than a year to bring to our attention the alleged error in our finding that the Petition “identifies where Huang discloses or suggests every element of challenged claim[2].” (Dec. on Inst. 18). For example, Petitioner did not file a request for rehearing of our decision denying institution of trial on Petitioner’s challenge based on Huang and Tsern and/or instituting trial based on unpatentability in view of Huang alone. *See* 37 C.F.R. § 42.71(d) (“A party dissatisfied with a decision may file a single request for rehearing without prior authorization from the Board.”). Nor did Petitioner seek our authorization to withdraw the instituted challenge of claim 4 based on Huang alone. *Cf. Ericsson Inc. v. Intellectual Ventures I LLC*, 2015 WL 8651563, at *9–10 (PTAB 2015) (denying Petitioner’s motion to withdraw its challenge as to some of the claims where Petitioner delayed in seeking to correct its petition: “[O]ur Decision to Institute should have apprised Ericsson of the problem with its challenge to claim 55.”).

Petitioner contends that, because we found sufficient evidence in the Petition and Huang to institute review of claim 4 based on Huang alone, we were required to provide adequate reasoning before reversing our position in our Final Decision. Req. Reh’g 5. In a decision issued subsequent to the filing of Petitioner’s Request, our reviewing court rejected a similar argument, and explicitly stated that the Board is not bound by any findings made in its Institution Decision. *See Trivascular, Inc. v. Samuels*, No. 2015-1631, 2016 WL 463539, at *9 (Fed. Cir. Feb. 5, 2016) (addressing

TriVascular’s argument that the Board’s conclusion of nonobviousness in its Final Written Decision was “inconsistent with the Board’s findings in its Institution Decision, since the Board found that TriVascular had initially demonstrated a reasonable expectation of success in demonstrating obviousness” and “that the Board should not have changed its view of the patent’s validity without clearly explaining why it had done so”). The court reasoned:

[a]t that point [of institution of a trial], the Board is considering the matter preliminarily without the benefit of a full record. The Board is free to change its view of the merits after further development of the record, and *should do so* if convinced its initial inclinations were wrong. To conclude otherwise would collapse these two very different analyses into one, which we decline to do. If those determinations were somehow binding with respect to the Board’s final decision, . . . the patentee’s appeal rights as to that second determination would be close to illusory. . . . [T]here is a significant difference between a petitioner’s burden to establish a “reasonable likelihood of success” at institution, and actually proving invalidity by a preponderance of the evidence at trial. *Compare* 35 U.S.C. § 314(a) (standard for institution of inter partes review), *with* 35 U.S.C. § 316(e) (burden of proving invalidity during inter partes review). The Board’s findings in its Final Written Decision were thus not inconsistent with those in its Institution Decision; they were made under a qualitatively different standard.

Id.; see also *Achates Reference Publishing, Inc. v. Apple Inc.*, 803 F.3d 652, 658 (Fed. Cir. 2015) (“[T]he board is always entitled to reconsider its own decisions.” (citing *GTNX, Inc. v. INTTRA, Inc.*, 789 F.3d 1309, 1313 (Fed. Cir. 2015))).

Petitioner’s argument that we erred in declining to consider the arguments and evidence in the Reply are based on its contention that it

should have been allowed to rely, during the merits phase, on findings made by the Board during the institution phase. *See* Req. Reh’g 9–11. We did not find this latter argument persuasive for the reasons discussed above.

Accordingly, we are not persuaded of error in our determination that “Petitioner’s arguments and evidence in the Reply are outside the scope of a proper reply because they do more than merely address Patent Owner’s argument that Huang teaches away; rather, they attempt to provide a new theory for modifying Huang that was not set forth clearly in the Petition.” Final Dec. 52.

In sum, for the above reasons, we are not persuaded of error in our determination that Petitioner did not meet its burden to establish unpatentability of claim 4 under 35 U.S.C. § 103(a) based on Huang.

IV. UNPATENTABILITY OF CLAIM 15 UNDER 35 U.S.C. § 102(b) BASED ON AVERBUJ

Claim 15 depends from claim 1 and recites: “wherein the control circuit is further configured to selectively input to the address and control ports of the one or more memory chips either the address and control signals from the memory controller of the computer system or the address and control signals from the control circuit.”

A. Background

In its Petition, Petitioner asserted that the claim 15 limitations are met by Averbuj’s multiplexer 46 that selectively inputs “BIST_ADDR/CTRL (*i.e.*, address and control signals from the control circuit) to the address and control port of the associated memory device.” Pet 24–25 (citing Averbuj ¶ 0048, Fig. 6; Ex. 1007 ¶¶ 86–88). In our Final Decision, we agreed with Patent Owner that multiplexer 46, as illustrated and described in Averbuj, is part of memory interface 41 (the alleged data handler), not sequencer 8 (the

alleged control circuit). *See* Final Dec. 43–44. We determined, therefore, that “Petitioner ha[d] not explained adequately how Averbuj’s sequencer 8 (the alleged control circuit) is ‘configured to’ (i.e., designed, adapted, or arranged to) ‘selectively input . . . address and control signals’ (claim 15) to memory modules 12.” *Id.* at 43.

B. Argument

Petitioner contends “the Board overlooked evidence cited in the Petition and provided in the supporting Alpert Declaration that explains how the **sequencer** performs the selectively input claim limitation.” Req. Reh’g 13. Petitioner argues, more specifically, that Dr. Alpert explained in both his first declaration in support of the Petition and his second declaration (Ex. 1009) in support of the Reply that Averbuj’s sequencer is configured to selectively input address and control signals to the memory modules by sending a BIST_EN signal to control multiplexer 46 to perform the selective input of address and control signals. *Id.* at 13–14. Petitioner directs us, for example, to the following testimony in Dr. Alpert’s first declaration:

Fig. 6 shows that a sequencer is configured to selectively input address and control signals (ADDR/CTRL OUT at right top) to the address and control ports using multiplexer (46) under control of signal BIST_EN (left middle) ... Thus, by generating BIST_EN the sequencer is configured to selectively input to the address and control ports. If such configuration is determined to require the structure that performs the selection itself, then the disclosed control module also includes multiplexer 46 of memory interface 41.

Id. (quoting Ex. 1007 ¶ 87). Petitioner also directs us to the following testimony in the Dr. Alpert’s second declaration (*id.* at 14): “the address and control signals generated by the sequencer of Averbuj, are selectively input to the address and control ports of the memory, as controlled by the signal

BIST_EN output by the sequencer” (Ex. 1009 ¶ 47).

C. Analysis

In its Petition, Petitioner identified multiplexer 46, exclusively, as meeting the claim 15 limitations. *See* Pet. 24–25. The Petition is devoid of any discussion of BIST_EN in connection with the claim 15 limitations. *See id.* Likewise, the Reply fails to contain any discussion of how the claim limitations are met by Averbuj’s use of the BIST_EN signal. *See* Reply 14–15.

37 C.F.R. § 42.22(a)(2) requires each petition to include “[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent.” Our discussion in the Final Decision of the patentability challenge as to claim 15 based on anticipation by Averbuj addresses Petitioner’s arguments in the Petition and Reply, which are limited to a contention that Averbuj’s multiplexer 46 is required to meet the “configured to selectively input” limitation. *See* Final Dec. 43–44 (citing Pet. 24–25; Reply 14–15).

In arguing that we should have considered Dr. Alpert’s testimony that Averbuj’s sequencer, by generating a BIST_EN signal, is “configured to selectively input” address and control signals to memory modules 12, Petitioner attempts to improperly incorporate arguments into its Petition and Reply by reference to Dr. Alpert’s declaration testimony. *See* 37 C.F.R. § 42.6(a)(3) (“Arguments must not be incorporated by reference from one document into another document.”).

In any event, we find the declaration testimony relied on by Petitioner in support of this Request (*see* Req. Reh’g 13–14) supports our

determination that Petitioner failed to show, by a preponderance of the evidence, that Averbuj anticipates claim 15. Dr. Alpert testified that if the “configuration [to selectively input to the address and control ports] is determined to require the structure that performs the selection itself, then *the disclosed control module also includes multiplexer 46 of memory interface 41.*” Ex. 1007 ¶ 87 (emphasis added). Petitioner did not explain (see Pet. 24–25; Reply 14–15) how Averbuj describes multiplexer 46 as being part of sequencer 8 (the alleged control circuit). See Final Dec. 43–44 (explaining that Petitioner has not addressed Patent Owner’s argument that the device that selectively inputs address and control signals to memory modules 12 is multiplexer 46 of memory interface 41 (the alleged data handler), not sequencer 8 (the alleged control circuit)).

In sum, for the above reasons, we are not persuaded of error in our determination that Petitioner did not meet its burden to establish unpatentability of claim 15 under 35 U.S.C. § 102(b) based on Averbuj.

V. UNPATENTABILITY OF CLAIMS 9 AND 10

Claims 9 and 10 are reproduced below:

9. The memory system of claim 5, wherein the control circuit is further configured to store memory addresses associated with failures in the operation of the one or more memory locations of the one or more memory chips.

10. The memory system of claim 5, wherein the memory system is further configured to store data associated with failures in the operation of the one or more memory locations of the one or more memory chips.

A. Petitioner’s Argument

In our Final Decision, we determined Petitioner had not met its burden to show unpatentability of claims 9 and 10, because Petitioner’s arguments

and evidence with respect to these claims did not “cure the deficiencies in its challenge with respect to claim 5.” Final Dec. 58. We agree with Petitioner that we erred in our decision with respect to claims 9 and 10, because we overlooked our holding that claim 5 is unpatentable under 35 U.S.C. § 103(a) based on Huang (*see id.* at 53) and under 35 U.S.C. § 102(b) based on Averbuj (*see id.* at 44). Req. Reh’g 11–12; *see* Final Dec. 58. Having determined that Petitioner had met its burden to establish unpatentability of claim 5, we further erred in our Final Decision in failing to address the merits of Petitioner’s and Patent Owner’s arguments and evidence with respect to claims 9 and 10.

B. Discussion of Error in the Institution and Final Decisions

In considering Petitioner’s Request, we also discovered an ambiguity in our statement of the instituted ground(s) of unpatentability as to claims 9 and 10. In our Institution Decision and our Final Decision we identified the instituted “ground” (singular) of unpatentability as to claims 9 and 10 as based on “Huang, Averbuj, and JEDEC Standard.” Dec. on Inst. 23; Final Dec. 57. Patent Owner indicates in its Response that it understood the instituted ground of unpatentability as to claims 9 and 10 as based on “Huang *in view of* Averbuj and the JEDEC Standard.” P.O. Resp. 59 (emphasis added)). It was our intention, however, to institute an *inter partes* review of claims 9 and 10 based on two grounds of unpatentability: (1) obviousness over Averbuj and JEDEC Standard and (2) obviousness over Huang and JEDEC Standard.

In our view, it would be unfair to Petitioner if, in reconsidering patentability of claims 9 and 10, we required a showing of sufficient argument and evidence in the Petition to support a conclusion of

obviousness over Huang *in view of* Averbuj and the JEDEC Standard. Petitioner did not challenge patentability of claims 9 and 10 based on a combination of Huang and Averbuj, and we did not provide any discussion in our Institution Decision to justify institution of an *inter partes* review of claims 9 and 10 based on a ground not advanced explicitly by Petitioner. *See* Dec. on Inst. 21–22. We are mindful that Patent Owner’s Response presents arguments in support of patentability of claims 9 and 10 over a combination of three references. We discern no prejudice to Patent Owner, however, in our reconsideration of the patentability of claims 9 and 10 based on two separate grounds under 35 U.S.C. § 103(a) (i.e., unpatentability over (1) Averbuj and JEDEC Standard and (2) Huang and JEDEC standard), because Patent Owner’s arguments in support of patentability of claims 9 and 10 are directed solely to alleged error in Petitioner’s contentions with respect to the teachings of JEDEC Standard. *See* PO Resp. 59–60.

*C. Alleged unpatentability of claims 9 and 10 under
35 U.S.C. § 103(a) based on (1) Huang and JEDEC Standard,
and (2) Averbuj and JEDEC Standard*

JEDEC Standard “covers Design for Test, Design for Manufacturing and Design for Validation (‘DFx’) requirements and implementation guidelines for Fully Buffered DIMM technology.” Ex. 1006, 1. In its Petition, Petitioner relies on JEDEC Standard for a teaching that “failing data and [the] corresponding address should be recorded in an error register.” Pet. 30, 51 (citing Ex. 1006 § 8.2.4.5). Petitioner argues it would have been obvious to combine the teachings of JEDEC Standard with the BIST architectures disclosed in Averbuj and Huang “for many reasons, including the well known benefit of recording memory errors in a BIST system to enable a failure analysis and determine where the errors are

located.” *Id.* at 31, 52. Petitioner relies on Dr. Alpert’s first Declaration to support its contention that it would have been obvious to modify the respective memory systems of Averbuj and Huang to store addresses and data as taught by JEDEC Standard. Pet. 30–31, 51–52 (citing Ex. 1007 ¶¶ 123–127, 206–209). Dr. Alpert cites column 3, lines 46–49 of the ’501 patent in support of his testimony that “the ’501 patent acknowledges the relevancy of the JEDEC standard to self-testing memory modules.” Ex. 1007 ¶ 124; *see* Ex. 1001, 3:46–49 (“Certain embodiments described herein present a self-testing memory module that includes a control module and a data module which can generate memory addresses and data according to the JEDEC standard memory protocol.”).

In its Response, Patent Owner argues that claims 9 and 10 require a system configured to record “failures,” but in the system described in JEDEC Standard, testing stops after only one failure is recorded. Resp. 59–60. Patent Owner further argues claims 9 and 10 require an internal tester, but the tester in JEDEC Standard is external to the memory system being tested. *Id.* at 60. In support of these arguments, Patent Owner relies on the declaration testimony of its witness, Dr. Sechen (Exhibit 2012). *Id.* at 59–60 (citing Ex. 2012 ¶¶ 229–32).

Petitioner, in its Reply, argues “[t]he claims are not limited to recording failures during a single test. Instead, the cla[i]ms only require that the data and addresses associated with the failures be stored.” Reply 22. Petitioner directs us to the section of JEDEC Standard relied on its Petition, noting there is a subsection on “Multiple Failures” and a description of “a procedure to generate ‘a complete data log of all failures’ including the address and data associated with the failure.” *Id.* (citing Ex. 1006 § 8.2.4.5).

In response to Patent Owner's argument that the system in JEDEC Standard uses an external tester, Petitioner, relies on testimony in Dr. Alpert's second Declaration (Ex. 1009). *See* Reply 22–23. Petitioner argues Dr. Sechen's testimony is based on disclosure in JEDEC Standard relating to transparent mode testing (Ex. 1006 § 8.1), which differs from Memory BIST, described in the section of JEDEC Standard cited in the Petition (*id.* at § 8.2). *See id.*; Ex. 1009 ¶ 79 (asserting that the sections of JEDEC Standard relied on by Dr. Sechen, e.g., sections 5.1 and 5.5, relate to transparent mode). Dr. Alpert explains that "Transparent Mode is used during FB-DIMM manufacturing to detect defects in the memory devices, interface, and board assembly using data patterns supplied by an external tester. Memory BIST is used for testing a FB-DIMM in a system at power-on initialization without using test equipment external to the system." Ex. 1009 ¶ 78. During the oral hearing, Patent Owner did not dispute these assertions. *See generally*, Paper 33 (transcript of the oral hearing).

We find that Dr. Sechen's testimony is related to JEDEC Standard's description of testing in transparent mode and does not address adequately JEDEC Standard's discussion of Memory BIST, i.e., the section of JEDEC Standard relied on by Petitioner in support of its patentability challenges as to claims 9 and 10. We also agree with Petitioner that Patent Owner's arguments are not commensurate in scope with claims 9 and 10. We find Petitioner's contentions with respect to the teachings of JEDEC Standard and motivation for modifying the respective systems of Averbuj and Huang are supported by JEDEC Standard, and conclude Petitioner has met its burden to show, by a preponderance of the evidence that claims 9 and 10 are

unpatentable over (1) Averbuj and JEDEC Standard, and (2) Huang and JEDEC Standard.

VI. CONCLUSION

For the reasons discussed above, we are not persuaded that we erred in our Final Decision with respect to claim 4 by:

(1) faulting Petitioner for not identifying support **in the Petition** for unpatentability based on Huang alone even though this was a **new ground identified by the Board** in its Institution Decision; (2) ignoring the evidence presented by Petitioner in the record that supports the Board's Institution Decision finding that Huang alone teaches or suggests mounting two physically separate components on a printed circuit board; and (3) concluding that Petitioner's Reply exceeded proper scope even though it properly supports the ground of unpatentability instituted by the Board and is directly responsive to arguments made by Patent Owner.

Req. Reh'g 1–2.

Nor are we persuaded that we overlooked arguments or evidence in support of Petitioner's challenge as to claim 15 based on anticipation by Averbuj. *See id.* at 12.

Petitioner has persuaded us that we erred in our Final Decision with respect to unpatentability of claims 9 and 10. We determine Petitioner has met its burden show that claims 9 and 10 are unpatentable under 35 U.S.C. § 103(a) over (1) Averbuj and JEDEC Standard, and (2) Huang and JEDEC Standard.

VII. ORDER

Petitioner's Request for Rehearing is *granted* with respect to its patentability challenges as to claims 9 and 10 under 35 U.S.C. § 103(a), but is *denied* with respect to its patentability challenges of claim 15 under 35

U.S.C. § 102(b) based on Averbuj and claim 4 under 35 U.S.C. § 103(a) based on Huang. It is hereby:

ORDERED that a new Final Written Decision holding claims 9 and 10 unpatentable is entered concurrently with this Order;

FURTHER ORDERED that the original Final Written Decision (Paper 34) is expunged; and

FURTHER ORDERED that Section VI of our Institution Decision (Dec. on Inst. 23) is modified to replace instituted ground 4) and add ground 5) as follows:

“4) claims 9 and 10 on the ground that these claims would have been obvious over Averbuj and JEDEC Standard; and

5) claims 9 and 10 on the ground that these claims would have been obvious over Huang and JEDEC Standard.”

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