

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ATOPTECH, INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

Case IPR2014-01145
Patent 6,237,127 B1

Before TRENTON A. WARD, MATTHEW R. CLEMENTS, and
PETER P. CHEN, Administrative Patent Judges.

WARD, *Administrative Patent Judge.*

DECISION
FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have statutory authority under 35 U.S.C. § 6(c). This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

With respect to the grounds instituted in this trial, we have considered the papers submitted by the parties and the evidence cited therein. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–4 and 7–11 of U.S. Patent No. 6,237,127 B1 (Ex. 1001, “the ’127 patent”) are unpatentable.

A. BACKGROUND

ATopTech, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–13 of the ’127 patent. Paper 2 (“Pet.”). Synopsys, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). On January 21, 2015, we instituted an *inter partes* review for claims 1–4 and 7–11 on certain grounds of unpatentability alleged in the Petition. Paper 7 (“Dec. on Inst.”).

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 15, “PO Resp.”), to which Petitioner filed a Reply (Paper 18, “Pet. Reply”). An oral hearing was held on November 13, 2015, consolidated with the hearings in IPR2014-01150 and IPR2014-01159. The transcript of the consolidated hearing has been entered into the record. Paper 23 (“Tr.”).

B. RELATED PROCEEDINGS

The ’127 patent is involved in a district court proceeding in the U.S. District Court of the Northern District of California, captioned *Synopsys, Inc. v. ATopTech, Inc.*, Case No. 3:13-cv-02965-MMC (N.D. Cal. 2013). Pet. 1. In a related proceeding before the Board, we instituted an *inter*

partes review of claims 1, 4, 8, 9, 12, 16, 19–22, and 32–36 of U.S. Patent No. 6,567,967 B2, in *ATopTech, Inc. v Synopsys, Inc.*, Case IPR2014-01150, slip. op. 22–23 (PTAB January 21, 2015) (Paper 11). Additionally, we instituted an *inter partes* review of claims 5, 23, 24, 26, 27, and 31 of U.S. Patent No. 6,567,967 B2, in *ATopTech, Inc. v Synopsys, Inc.*, Case IPR2014-01159, slip. op. 25–26 (PTAB January 21, 2015) (Paper 11).

C. THE '127 PATENT

The '127 patent relates generally to the static timing analysis of digital electronic circuits, and in particular applies static timing analysis to synthesis of circuits by analyzing certain paths of a circuit using “non-default timing constraints known as exceptions.” Ex. 1001, Title, 1:8–11. Exceptions allow a circuit designer, working with a circuit synthesis system, to specify certain paths through the circuit to be synthesized as being subject to non-default timing constraints. *Id.*, Abstract. The '127 patent discloses that static timing analysis had been used to verify that the design of a digital electronic circuit would perform correctly at the target clock speeds, and “[f]or similar reasons, it would be useful to apply, as efficiently as possible, static timing analysis to the synthesis process.” *Id.* at 1:40–42. Specifically, the '127 patent discloses performing static timing analysis on units of a circuit, referred to as “sections,” which comprise a set of “launch” flip flops, non-cyclic combinational circuitry, and a set of “capture” flip flops. *Id.* at 2:1–4.

The static timing analysis described in the '127 patent is accomplished in two main phases: (1) propagation of tagged rise-fall (RF) timing tables and (2) relative constraint analysis. Ex. 1001, 8:37–41. In the first phase of the timing analysis, delays between inputs and outputs of circuit devices are

represented by “timing arcs.” Ex. 1001, 8:44–45. Using the timing arcs for the circuit devices, maximum and minimum delay values for the rise time and the fall time are determined and stored in RF timing tables. *Id.* at 9:54–67. The timing tables are propagated through the circuit and the delays at each circuit node are added to the minimum and maximum values of the timing table from the previous node. *Id.* at 9:58–13:2, Fig. 5. Additionally, each timing table is associated with a “tag” that may include a clock identifier and a variety of “labels.” Ex. 1001, 3:11–15, 10:21–25. The labels of a “tag” also may identify points in the circuit referenced by an exception. Ex. 1001, 3:29–32.

After the propagation of the timing tables through the circuit, the second phase of the timing analysis, relative constraint analysis, is performed. Ex. 1001, 13:3–4. Relative constraint analysis involves the comparison of the delay values included in the timing tables with the timing constraints of the circuit. *Id.* at 13:66–14:27. The ’127 patent describes maximum allowable path delays (“MAPD”s) and shortest allowable path delays (“SAPD”s), which are default timing constraints alterable by exceptions. *Id.* at 13:34–63, 14:30–38. The delay values stored in the timing tables are compared to the MAPD and SAPD values, and if the MAPD and SAPD timing constraints are satisfied, the circuit has passed the static timing analysis. *Id.* at 13:56–14:26.

Additionally, with respect to exceptions, the ’127 patent instructs “[e]xceptions are specified by the circuit designer as individual syntactic units called ‘exception statements’ which are comprised of a ‘timing alteration’ and a ‘path specification.’” Ex. 1001, 1:58–61. The timing alteration instructs the timing analyzer how to alter the default timing

constraints for paths through the circuit to be analyzed which satisfy the path specification. *Id.* at 1:61–63. For example, a “set_false_path” exception indicates that for paths satisfying the path specification, the relevant MAPD value is set to infinity and the relevant SAPD value is set to zero for the relative constraint analysis. *Id.* at 14:47–54.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A method performed in a circuit analysis process, comprising the steps performed by a data processing system of:
 - marking certain points in a circuit description according to their being referenced by at least a first exception;
 - propagating a plurality of timing tables through the circuit description; and
 - wherein at least a first timing table, of the plurality of timing tables, refers to a tag comprising at least a first label indicating a marked point in the circuit description, through which the table has been propagated.

Id. at 31:47–32:5.

D. LEVEL OF ORDINARY SKILL IN THE ART

Patent Owner’s declarant, Dr. Martin G. Walker, states that in view of the ’127 patent, a person of ordinary skill in the art would have a minimum of a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or a closely related field and would have a minimum of one to two years of professional experience in the development and analysis of digital electronic circuits.

Ex. 2004, Declaration of Dr. Martin G. Walker ¶ 22. Petitioner does not disagree with Dr. Walker’s opinion as to the proper level of ordinary skill in the art. Pet. Reply 17.

Based on our review of the '127 patent and the testimony of Patent Owner's Declarant, we adopt Patent Owner's definition of a person of ordinary skill in the art at the time of the claimed invention. Furthermore, as noted in the Decision on Institution, the applied prior art also reflects the appropriate level of skill at the time of the claimed invention. See Dec. on Inst. 23 (citing *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) ("the absence of specific findings on the level of skill in the art does not give rise to reversible error where the prior art itself reflects an appropriate level and a need for testimony is not shown.") (internal quotations omitted); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995)).

E. INSTITUTED GROUNDS AND PRIOR ART

We instituted an *inter partes* review on the following grounds (Dec. on Inst. 25):

Reference(s)	Basis	Claims
Belkhale ¹	§ 103	1–4 and 7–11
Belkhale and Tom ²	§ 103	1–4 and 7–11

¹ Krishna Belkhale, *Timing Analysis with known False Sub Graphs*, in IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN, DIGEST OF TECHNICAL PAPERS 736–740 (Nov. 5–9, 1995) (Ex. 1005, "Belkhale").

² U.S. Patent No. 5,210,700, issued May 11, 1993 (Ex. 1006, "Tom").

II. ANALYSIS

A. CLAIM CONSTRUCTION

The Board will interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent. *See* 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1275–79 (Fed. Cir. 2015). Under the broadest reasonable interpretation standard, claim terms are given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). An inventor may rebut that presumption by providing a definition of the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In the absence of such a definition, limitations are not to be read from the specification into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

1. “exception”

Petitioner asserts one of ordinary skill in the art would understand that an “exception” is a “non-default timing constraint.” Pet. 19–20 (citing Ex. 1007, ¶¶ 99–100). Specifically, Petitioner’s declarant Dr. Ghiasi states that the ’127 patent defines an “exception statement” as altering the default timing constraints; thus, Dr. Ghiasi states that a person having ordinary skill in the art would understand that an “exception” is a “non-default timing constraint.” Ex. 1007 ¶ 100 (quoting Ex. 1001, 14:30–33) (emphasis removed).

With respect to the term “exception,” the Specification expressly states that “the present invention relates to analyzing certain paths of a

circuit under non-default timing constraints known as exceptions.”
Ex. 1001, 1:8–11; *see id.* at Title, Abstract. The Specification adds “[e]xceptions are specified by the circuit designer as individual syntactic units called ‘exception statements’ which are comprised of a ‘timing alteration’ and a ‘path specification.’” Ex. 1001, 1:58–61. The timing alteration instructs the timing analyzer how to alter the default timing constraints for paths through the circuit to be analyzed which satisfy the path specification. *Id.* at 1:61–63. The Specification further states, “[t]he path specification consists of one or more ‘path specifiers,’ with each path specifier taking an ‘argument.’ In order for a path specification to be satisfied, each argument of each of its path specifiers must be satisfied.” *Id.* at 1:64–67.

In view of the foregoing, we maintain the construction provided in the Decision on Institution (Dec. on Inst. 7) and construe the term “exception” as “non-default timing constraints.”

2. “*timing table*”

Petitioner submits that the term “timing table” is not limited to the four values³ disclosed as an “RF timing table” in the ’127 patent but refers to the propagation of any delay value. Pet. 23–24. Patent Owner asserts that Petitioner’s construction contradicts the plain meaning of the term “table,” which must include a *set* of data, instead of just a single data item. PO Resp. 10. In support of its proposal, Patent Owner offers the definition of “table” from the Microsoft Computer Dictionary (Third Edition 1997) as a

³ “The RF timing tables propagated are comprised of the following four values: minimum rise time (minRT), maximum rise time (maxRT), minimum fall time (minFT) and maximum fall time (maxFT).” Ex. 1001, 3:8–11.

“data structure usually consisting of a list of entries.” PO Resp. 10–11 (quoting Ex. 2006 at 459).

Petitioner counters that Patent Owner’s arguments fail to provide any evidence that a “set” must include more than a single data item. Pet. Reply. 3. Petitioner argues that both the ’127 patent and Belkhale refer to a “null set,” which is a set having *no* data items. *Id.* (citing Ex. 1001, Fig. 9A, 9E; Ex. 1005 at 737). We agree with Petitioner that the term “table” does not require multiple data items and, likewise, that the term “timing table” does not require multiple delay values. Although the Specification discloses an exemplary “RF timing table” as having four RF values (Ex. 1001, 9:54–57), the claim language is broader and not restricted to a specific type of table or number of data items in the table. To require otherwise would improperly import a limitation from the Specification into the claim. *See, e.g., SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (“Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim.”). In view of the foregoing, we maintain the construction provided in the Decision on Institution (Dec. on Inst. 7) and determine the broadest reasonable interpretation of “timing table” is a “table having a timing value.”

B. ASSERTED OBVIOUSNESS IN VIEW OF BELKHALE

1. *Belkhale (Ex. 1005)*

Belkhale, titled “Timing Analysis with known False Sub Graphs,” discloses that a static timing analysis, widely used at that time, determined timing violations in circuits by computing the difference of slack (SLK) between an arrival time (AT) and required time (RAT) at each vertex in a timing graph. Ex. 1005, 736. Belkhale adds that while SLK “gives a good local measure of the magnitude of a timing violation,” the analysis does not take logic into account and results in the algorithm considering paths that may not be “logically realizable.” *Id.* Belkhale uses the term “false path” to refer to paths that are not logically realizable. *Id.* Belkhale teaches that false paths “must be detected and eliminated from consideration from the timing analysis.” *Id.* Additionally, Belkhale describes the use of false sub graphs as a way to eliminate multiple false paths from the timing analysis. *Id.* Specifically, “the ability to remove entire sub graphs from consideration from timing is a powerful feature.” *Id.*

Belkhale further provides examples of false paths and false sub graphs. Figure 2 is reproduced below as an example of a false path.

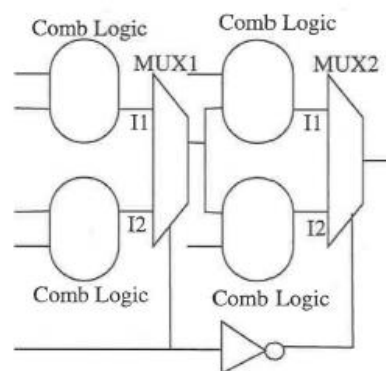


Figure 2 depicts two multiplexers MUX₁ and MUX₂ each having a

first pin I_1 . *Id.* at 740. Each multiplexer receives input from a control signal, which is inverted when input into MUX_2 . *Id.* Belkhale teaches that all paths between pin I_1 of MUX_1 to pin I_1 of MUX_2 are false because a control signal allowing propagation of I_1 at the first MUX_1 will block propagation at the second pin I_1 at MUX_2 due to the inverted control signal. *Id.* at 7, Fig. 2. Belkhale discloses these false paths can be represented by a false sub graph with an ordered pair specifying $\{(MUX_1/ I_1, MUX_2/ I_1)\}$. *Id.* at 7.

Belkhale further describes false sub graphs as “in general, equivalent to many individual paths.” Ex. 1005, 739. Figure 1 is reproduced below.

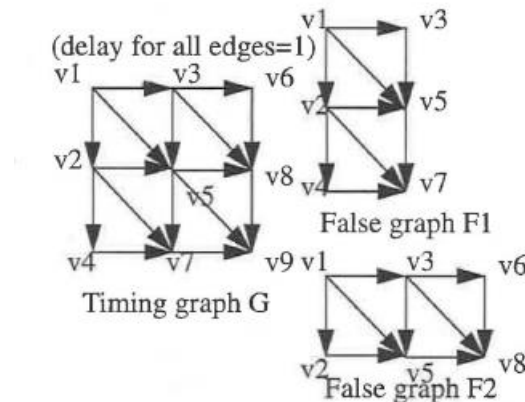


Fig. 1. Timing graph and false sub graphs.

Figure 1 depicts false sub graphs, identified as F1 and F2, for timing graph G. Ex. 1005, Fig. 1. False graph F1 represents the false paths from v1 to v7 and false graph F2 represents the false paths from v1 to v8, within timing graph G. *Id.*

Additionally, Belkhale discloses “Algorithm 1,” which computes multiple arrival and required times at a node, and distinguishes the different times based on a set attribute. Ex. 1005, 737. The set attribute is a subset of the set of false sub graphs $\{1, \dots, k\}$ where k is the number of input false

sub graphs. For the example shown in Figure 1, k is 2 and the possible values of the set attribute are $\{\}$, $\{1\}$, $\{2\}$, and $\{1, 2\}$. *Id.* The set attribute value provides the “set of false sub graphs that a signal has come through.” *Id.*

2. *Asserted Obviousness in View of Belkhale*

Petitioner contends that claims 1–4 and 7–11 of the ’127 patent would have been obvious in view of Belkhale. Pet. 18–39.

a. *Claim 1*

Claim 1 recites the step of “marking certain points in a circuit description according to their being referenced by at least a first exception.” To satisfy this limitation, Petitioner asserts that Belkhale teaches that a user can specify false sub graphs using an ordered pair of vertices. Pet. 20–21. Referring to the multiplexer example in Figure 2, Petitioner explains Belkhale shows marking points by defining a false path with ordered pair $\{(MUX1/I1, MUX2/I1)\}$. Pet. 21 (citing Ex. 1005, 737). Petitioner asserts the ’127 patent discloses false paths as an exception and, therefore, a person of ordinary skill would appreciate the false paths and false sub graphs disclosed in Belkhale to be exceptions. Pet. 21 (citing Ex. 1001, 14:44–54; Ex. 1007 ¶¶ 103–106).

Separate from the argument above, Petitioner also asserts that Belkhale’s Algorithm 1 satisfies the marking step recited in claim 1. Pet. 21. Specifically, Petitioner argues that Belkhale teaches an alternative embodiment for marking points within a circuit where the marking takes place within the timing analysis software. *Id.* Petitioner asserts Algorithm 1 uses three data sets $BG(v)$, $EG(v)$, and $IN(e)$ to reference points or edges in circuit modeled by graph G based on false sub graphs. Pet. 21–22 (citing

Ex. 1005, 737; Ex. 1007 ¶¶ 110–111). Petitioner argues that the false sub graphs are exceptions. *Id.* at 21.

We are persuaded that Belkhale’s false paths and false sub graphs teach or suggest the claimed “exception.” As Petitioner observes, Belkhale describes false paths as paths that are not logically realizable and must be detected and eliminated from the timing analysis. Pet. 13 (citing Ex. 1005, 736). Likewise, Belkhale explains that removing an entire false sub graph from timing consideration is advantageous because multiple paths may be simultaneously removed from consideration. See Pet. 13–14 (citing Ex. 1005, 736; Ex. 1007 ¶ 78). Accordingly, we are persuaded by Petitioner’s argument that Belkhale’s false path and false sub graph are each a non-default timing constraint (i.e., an exception) because they represent circuit pathways that are not logically realizable and must be eliminated from the timing analysis. *Id.*

Second, we also are persuaded Petitioner has established sufficiently how Belkhale’s ordered pair vertices or Algorithm 1 disclose “marking certain points in a circuit description according to their being referenced by,” recited in claim 1, a false path or false sub graph. As Petitioner points out, Belkhale defines false paths in a multiplexer circuit with ordered pair vertices. Additionally, Petitioner separately equates Belkhale’s use of “three separate data structures” BG(v), EG(v), and IN(e) to associate points in the circuit description with the false sub graph. Pet. 21–22; see Pet. 16–18 (explaining Algorithm 1 in operation). We understand Petitioner’s latter argument to be that Belkhale’s timing graph “G” discloses a circuit description, the false sub graphs disclose exceptions, and the three data sets define vertices and edges according to a relationship to the false sub graphs.

Claim 1 further recites “propagating a plurality of timing tables through the circuit description.” For this limitation, Petitioner asserts “Belkhale calculates multiple delay values – arrival times (AT) – at each point of the circuit and propagates those delay values through the circuit.” Pet. 22 (citing Ex. 1005, 736). Petitioner further argues the propagated delay values are shown in timing tables in Belkhale’s Figure 3. Pet. 23. Figure 3 depicts vertices v1–v9 with delay value(s) and set attribute(s) for each vertex. Pet. 23 (showing annotated Figure 3).

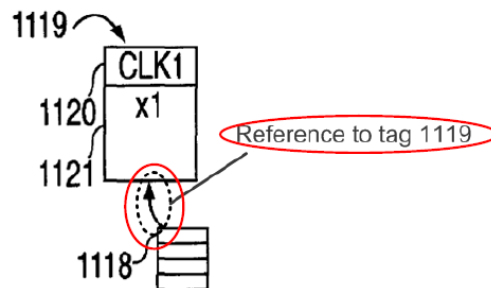
Claim 1 further recites “wherein at least a first timing table, of the plurality of timing tables, refers to a tag comprising at least a first label indicating a marked point in the circuit description, through which the table has been propagated.” Petitioner asserts that Figure 3 described in Belkhale discloses the plurality of timing tables with “set attributes,” i.e. tags. Pet. 25. Petitioner further asserts “Belkhale teaches that when the timing table passes through a false path, a ‘set attribute’ is appended to the timing table.” *Id.* at 26 (citing Ex. 1005, 737). “The set attribute value gives the set of false sub graphs the signal has come through.” *Id.* (emphasis omitted). Essentially, Petitioner takes the position that the false sub graphs or false paths disclose “a marked point in the circuit description,” recited in claim 1, and the set attribute shown in Belkhale’s Figure 3 is a tag with a label indicating that a signal arriving at a particular vertex has passed through a false sub graph. *Id.*

Patent Owner argues that Belkhale does not disclose “propagating a plurality of timing tables through the circuit description” because this limitation cannot be met by propagating only delay values through a circuit description, as at least one of the propagated timing tables must include a

reference to a tag. PO Resp. 17. Specifically, Patent Owner argues that the recitation in claim 1 that “at least a first timing table . . . *refers to a tag*” requires propagating “a *refer[ence] to a tag*.” *Id.* (quoting claim 1) (emphasis added). We are not persuaded by Patent Owner that the language of claim 1 requires propagating “a *refer[ence] to a tag*.” .

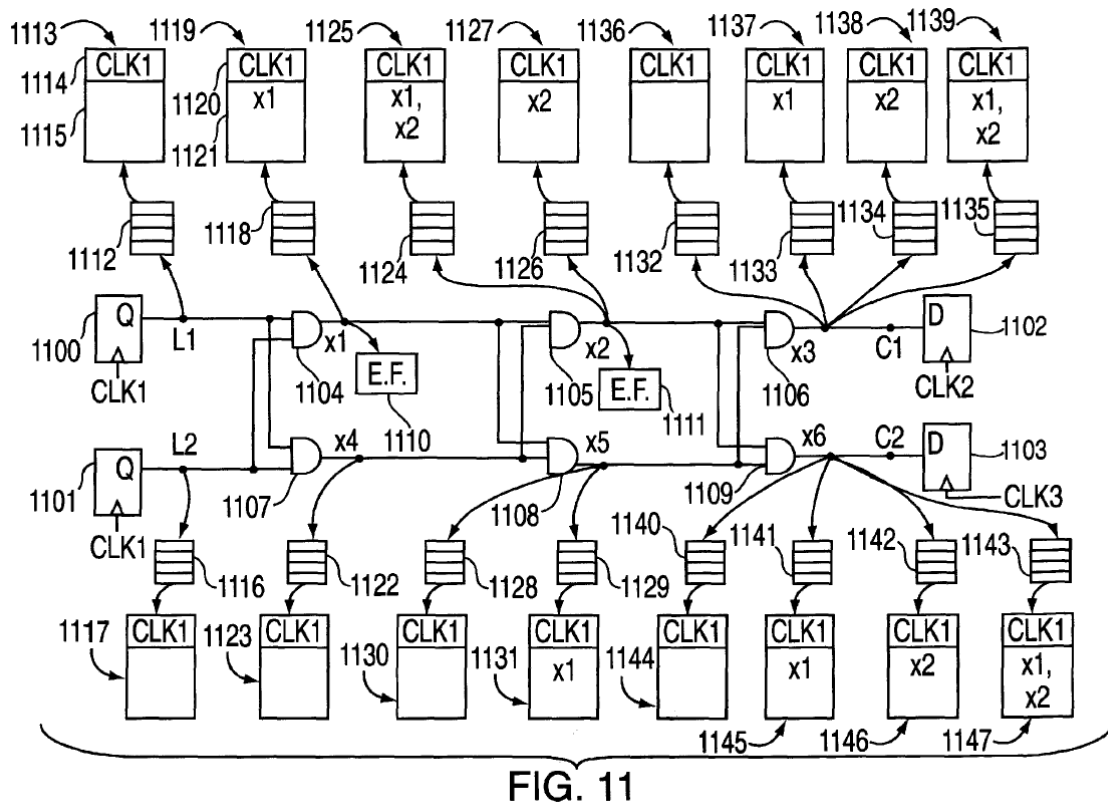
As indicated by Patent Owner’s use of brackets, claim 1 does not recite a “*reference to a tag*” but instead recites “wherein at least a first timing table, of the plurality of timing tables, *refers to a tag*.” Accordingly, Petitioner argues that the claims do not require a thing (i.e., a noun) called a “reference,” but only a first timing table that *refers to tag*. Pet. Reply. 5–6. Furthermore, Petitioner argues that the term “refer” can simply mean “to concern.” Pet. Reply 4–5 (citing Ex. 1008, 1517).

We note that the ’127 patent fails to explicitly disclose a “reference to a tag.” In view of this deficiency, Patent Owner argues that the ’127 patent illustrates the “reference to a tag” in Figure 11, as provided in Patent Owner’s annotated excerpt from Figure 11 below.



PO Resp. 3 (excerpt of Ex. 1001, Fig. 11 (annotated)). Patent Owner annotates this excerpt of Figure 11 of the ’127 patent above by adding the items circled in red; namely, the dashed circle around the arrow from 1118 to 1119, and the text “reference to tag 1119.” *Compare* Ex. 1001, Fig. 11 with PO Resp. 3, annotated Fig. 11.

Contrary to Patent Owner's arguments, the '127 patent fails to disclose this "reference to tag 1119," but rather states, in describing Figure 11, that "RF timing table 1118 is shown, *along with its tag 1119.*" Ex. 1001, 23:57 (emphasis added). Figure 11 is reproduced below without annotation.



As shown in Figure 11 above, the '127 patent discloses numerous RF timing tables, such as 1112, 1116, 1118, 1122, 1124, and numerous tags, such as 1113, 1119, and 1125, but the '127 patent does not disclose that any of these timing tables contains a "reference to a tag." See Ex. 1001, Fig. 11; 23:53–24:28. Instead, the '127 patent discloses the following: "RF timing table 1112 is given at tag 1113" (Ex. 1001, 23:18) (emphasis added); "RF timing table 1122' gets a tag" (Ex. 1001, 24:3–4) (emphasis added); "RF timing table 1118' gets a tag comprising tag 1119" (Ex. 1001, 24:7–8) (emphasis added); "RF timing table 1128 has the same tag as RF timing table 1122,

and RF timing table 1129 *has the same tag* as RF timing table 1118” (Ex. 1001, 24:15–17) (emphasis added). Accordingly, we are unpersuaded by Patent Owner that the ’127 patent discloses a “reference to a tag.”

Furthermore, we do not construe the recitation in claim 1 that “at least a first timing table . . . *refers to a tag*” to require “a *reference to a tag*,” but construe the claim phrase according to its plain and ordinary meaning in view of the specification that at least the first timing table must simply refer to a tag.

Patent Owner also argues that Petitioner’s challenge of claim 1 based on Belkhale fails because, at most, Petitioner argues that it is the set attribute (i.e., the tag itself) that is propagated in Belkhale and not a *reference to a tag*. PO Resp. 21. As stated above, we are not persuaded by Patent Owner’s argument that claim 1 requires a reference to a tag. Furthermore, as conceded by Patent Owner,⁴ claim 1 does not prohibit the tag itself from being included in the timing table.

Petitioner provides the following annotated Figure 3 of Belkhale in support of its contentions regarding the “first timing table” and “tag” recited in claim 1:

⁴ “Judge Ward: So you agree that claim 1 does not exclude the ability for the first timing table to include, to also include the tag itself? Mr. Sauer: So long as there is a reference. So long as the timing table refers to the tag.” Tr. 38:13–17.

	V1	V2	V3	V4	V5	V6	V7	V8	V9
Arrival Time (AT) Delays	(0, {})	(1, {1,2})	(1, {1,2})	(2, {1})	(1, {}) (2, {1,2})	(2, {2})	(2, {})	(2, {})	(3, {})
Required Arrival Time (RAT)	(2, {})	(3, {1,2})	(3, {1,2})	(N, {1})	(3, {}) (4, {1,2})	(N, {2})	(4, {})	(4, {})	(5, {})

Fig. 3: Arrival Time and Required Time propagation (N = No RAT)

Pet. 15, 23, 26 (citing Belkhale, Fig. 3). As discussed above, Petitioner takes the position that Figure 3 of Belkhale teaches the “plurality of timing tables” recited in claim 1, and that the set attribute shown in Belkhale’s Figure 3 is a tag with a label indicating that a signal arriving at a particular vertex has passed through a false sub graph. Pet. 23 (citing Ex. 1007 ¶¶ 117–118), 26. For example, at node v4, the timing table of Belkhale is (2, {1}), where 2 is the delay value and {1} designates the false sub graph the signal has propagated through. Pet. 15–18 (citing Ex. 1005, Fig. 3; Ex. 1007 ¶¶ 89–90). In an additional example, at node v5, the timing tables of Belkhale are (1, {}) and (2, {1,2}): (1, {}) indicating a delay value of 1 and a set attribute of {} indicating that the signal did not propagate through a false sub graph; and (2, {1,2}), indicating a delay value of 2 and a set attribute {1,2}, indicating that the signal propagated through false sub graphs 1 and/or 2. Ex. 1007 ¶¶ 90–91 (citing Ex. 1005, Fig. 3). Given this relationship in Belkhale between the timing table and the set attribute (i.e., the “tag” in claim 1), we are sufficiently persuaded by Petitioner that this disclosure in Belkhale teaches or suggests “wherein at least a first timing table, of the plurality of timing tables, refers to a tag,” recited in claim 1.

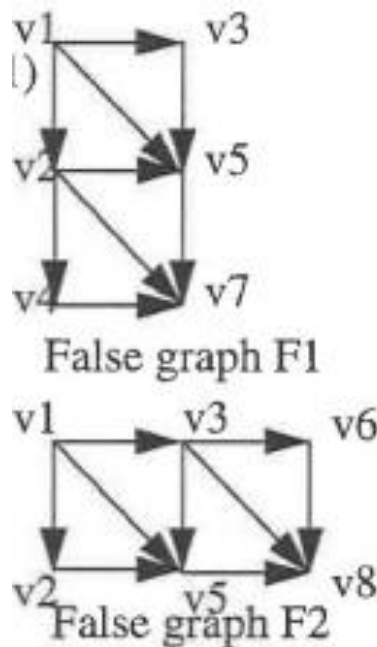
Additionally, Patent Owner argues that Petitioner’s challenge based on Belkhale fails because the set attribute disclosed in Belkhale does not

teach or suggest “a tag comprising at least a first label indicating a marked point in the circuit description, through which the table has been propagated,” as recited in claim 1. PO Resp. 24. Specifically, Patent Owner argues that Belkhale’s set attribute indicates a false sub graph, but a false sub graph is not “a marked point in [a] circuit description.” *Id.* at 26. As an example, Patent Owner cites to the timing table (2, {1,2}) for node v5 in Figure 3 of Belkhale as evidence that, given a set attribute of {1, 2}, a timing table could propagate from node v1 to node v5 via multiple different routes, given the many paths of false sub graphs F1 and F2 in Belkhale. PO Resp. 28–29. Thus, Patent Owner argues that, given the set attribute of {1, 2}, it is not possible to determine a marked point through which a time table has propagated. PO Resp. 30. Petitioner counters Patent Owner’s arguments on two grounds.

First, Petitioner argues that claim 1 does not preclude that a label indicates multiple points in the circuit description. Pet. Reply 14. Namely, the claim 1 recitation that “a first label indicating a marked point in the circuit description,” does not prohibit the label from indicating multiple marked points in the circuit description. *Id.* We agree. In fact, claim 2, which depends from claim 1, recites that “first label represents a boolean relationship amongst several marked circuit points.” Thus, claim 2 requires that the “label” recited in claim 1 be broad enough to represent a relationship among several marked circuit points. Furthermore, we note that the recitation of the indefinite article “a” in a claim, as used in the claimed “a marked point,” is construed as meaning “one or more” in open-ended claims like claim 1. See *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008) (the Federal Circuit “has repeatedly emphasized that

an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’”)

Second, Petitioner argues that, contrary to Patent Owner’s assertions, many of the timing tables described in Belkhale have a tag with a label indicating a *single marked point* in the circuit description. As an example, Petitioner identifies the timing table of (1, {1,2}) for node v2 in Figure 3, indicating that the set attribute for v2 includes false sub graphs F1 and F2. Pet. Reply 16 (citing Ex. 1005, Fig. 3). Furthermore, Petitioner relies upon Figure 1 of Belkhale, of which an excerpt is reproduced below, illustrating false sub graphs F1 and F2.



Ex. 1005, Fig. 1. Petitioner argues that for node v2, because there is only one possible path from v1 to v2 (as shown above), the false graph F1 is a first label that indicates a single marked circuit point v1 through which the table has been propagated, and false graph F2 is a second label that also

indicates a single marked circuit point v1 through which the table has been propagated. Pet. Reply 16 (citing Ex. 1005, Figure 1; Ex. 1009, 50:16–19). Petitioner therefore argues that Belkhale discloses a tag having a label indicating a particular marked point in the circuit description. *Id.* (citing Ex. 1009, 42:13–43:2). In view of the teachings of Belkhale cited by Petitioner, we are persuaded that Belkhale teaches or suggests “a tag comprising at least a first label indicating a marked point in the circuit description, through which the table has been propagated,” recited in claim 1.

Patent Owner further argues that Petitioner’s challenge based on Belkhale fails because the Petition does not articulate the differences between the prior art and the claims at issue. PO Resp. 34 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)). Contrary to Patent Owner’s assertion, Petitioner argues that it has pointed out when there are differences between the ’127 patent and Belkhale, and has argued in those instances that it would have been obvious for a person of ordinary skill in the art to modify the Belkhale reference. Pet. Reply 18. For example, Petitioner stated in the Petition that Belkhale discloses timing tables with only a single value, but Petitioner argued that it was well known to one skilled in the art at the time of the ’127 Patent to propagate timing tables with multiple values. Pet. 24 (citing Ex. 1007 ¶ 124). Additionally, Patent Owner argues that Petitioner provides no evidence to establish the level of ordinary skill in the art. PO Resp. 35. As we identified in the Decision on Institution, however, it is not necessary to present separate and independent evidence of the level of skill in the art if the prior art adequately reflects an appropriate level of skill. Dec. on. Inst. 23–24 (citing *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) and *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755

F.2d 158, 163 (Fed. Circ. 1985)). Patent Owner argues that these cases are not applicable to the instant proceeding because Patent Owner and Petitioner have not agreed on a level of ordinary skill in the art. PO Resp. 37.

Contrary to Patent Owner's arguments, as discussed above, Petitioner does not disagree with Patent Owner's proposal for the level of ordinary skill in the art. Pet. Reply 17; Tr. 16:21–17:2. Accordingly, we are not persuaded by Patent Owner's argument that Petitioner's challenge based on Belkhale fails to address the *Graham* factors.

b. Claims 2–4 and 7–11

Claim 2 depends from claim 1 and requires that “the first label represents a boolean relationship amongst several marked circuit points.” Patent Owner argues that Belkhale does not disclose this limitation because Belkhale's set attribute represents a Boolean relationship amongst *false paths*, not a Boolean relationship amongst several *marked circuit points*. PO Resp. 46–47.

With respect to claim 2, Petitioner argues that the set attribute in Belkhale, such as {1}, represents a Boolean “OR” relationship between several marked circuit points, because the single set attribute {1} may represent multiple points. Pet. 29–30 (citing Ex. 1007 ¶¶ 145–147); Pet. Reply. 24. For example, as shown in Belkhale's Figure 1 reproduced above, in arriving at node v5, the false sub graph F1 may be through node v2 or node v3, yet only the single entry in the set attribute {1} is required. Pet. Reply 24. Thus, Petitioner argues that the set attribute {1} represents the Boolean OR relationship between marked points in the circuit. *Id.*

Additionally, Patent Owner argues that Belkhale's set attribute does not teach the claim 2 limitation because Belkhale's false paths have an

associated directionality. PO Resp. 47. Patent Owner fails to identify, however, how claim 2 or claim 1 prohibits the inclusion of additional information, such as directionality, in the claimed “first label.” Accordingly, we are persuaded by Petitioner that Belkhale teaches or suggests the limitation of claim 2.

Claim 3 depends from claim 2 and requires that “the first label represents a Boolean OR relationship amongst several marked circuit points.” Patent Owner argues that, even assuming Belkhale’s set attribute could be understood to represent a Boolean relationship amongst marked circuit points, the Boolean relationship would be an AND relationship, not an OR relationship. PO Resp. 48. Contrary to Patent Owner’s argument, Petitioner’s Declarant Dr. Ghiasi identifies that the set attribute represents an exception such that if a signal propagates through either node, it may be subject to the false path timing constraint; thus, “Belkhale’s ‘set attribute’ is a label representing a [b]oolean ‘OR’ relationship amongst several marked circuit points.” Ex. 1007 ¶¶ 143–146. For example, in the embodiment addressed above with respect to claim 2, and shown in Belkhale’s Figure 1 reproduced above, in arriving at node v5, the false sub graph F1 may be through node v2 OR node v3. See Ex. 1005, Fig. 1. Accordingly, we are persuaded by Petitioner that Belkhale teaches or suggests the limitation of claim 3 regarding “a boolean OR relationship amongst several marked circuit points.”

Patent Owner argues that dependent claims 10 and 11, which provide similar recitations to claims 2 and 3, are not obvious over Belkhale for at least the same reasons as claims 2 and 3. Similar to claims 2 and 3, we are unpersuaded by Patent Owner’s arguments against claims 10 and 11. We

also are persuaded by Petitioner's evidence regarding dependent claims 4, 7, 8, and 9. Pet. 30–31, 34–36.

3. Conclusion Regarding Claims 1–4 and 7–11

With respect to the Petitioner's challenge that claims 1–4 and 7–11 of the '127 patent would have been obvious in view of Belkhale, we have considered the papers submitted by the parties and the evidence cited therein. For the foregoing reasons, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1–4 and 7–11 of the '127 patent would have been obvious in view of Belkhale.

C. ASSERTED OBVIOUSNESS IN VIEW OF BELKHALE AND TOM

1. *Tom (Ex. 1006)*

Tom, titled, "Automatic Delay Adjustment for Static Timing Analysis," discloses an automatic delay adjustment for static timing analysis. Ex. 1006, Title. Tom teaches that timing adjustment problems can be resolved by (1) associating clock information with the delay values which are propagated through the logic design, (2) propagating multiple delay values downstream in the logic design, and (3) using clock information associated with a delay to automatically adjust as needed. *Id.* at 4:65–5:6. Referring to Figure 3, Tom further discloses clock tags (T0, T2) associated with each delay values in a logic network. In Figure 3, the clock tag is the name of the clock signal which operates the clocked element generating the signal with which the clock tag is associated. Ex. 1006, 5:9–16. Referring to Figure 8, Tom discloses path delay table 38 containing multi-field data elements representing the cumulative path delays for each input or output pin of every block included in the logic design. *Id.* at 7:17–20. Figure 8

includes clock tags that identify clocking information associated with the path delay value of the entry. *Id.* at 7:31–34.

2. *Analysis of Asserted Obviousness in View of Belkhale and Tom*

Petitioner contends that Belkhale teaches or suggests all the limitations of claims 1–4 and 7–11. Pet. 40–60. Petitioner primarily relies on the same disclosure in Belkhale, discussed above, to demonstrate claim 1 would have been obvious in view of Belkhale and Tom. Pet. 45–46. Additionally, Petitioner points to features in Tom that disclose a clock tag and a timing table with more than one delay value. *Id.* at 46, 47 (citing Ex. 1006, 4:68–5:3, 5:9–10, 7:28–33, 7:61–68). For the clock tag, Petitioner asserts Tom teaches that a “clock tag field of any entry in the path delay table 38 identifies the clocking information associated with the path delay value of the entry.” *Id.* at 46 (quoting Ex. 1006, 7:31–33). Petitioner argues Belkhale and Tom both disclose tagging propagated delay values, where Belkhale does so to eliminate false paths, and Tom does so to handle multi-cycle clocking. *Id.* at 43. For the timing table, Petitioner asserts each entry in Tom’s path delay table (shown in Figure 8) includes a *pair* of delay values. Pet. 47 (citing Ex. 1006, 7:61–68) (emphasis added).

Patent Owner argues that Petitioner’s challenge based on Belkhale and Tom fails because Tom does not cure the deficiencies in Belkhale regarding the claimed limitations of “propagating a plurality of timing tables through the circuit description” or “a tag comprising at least a first label indicating a marked point in the description through which the table has been propagated.” PO Resp. 40. As discussed above with respect to the challenge based on Belkhale, we are not persuaded by Patent Owner that Belkhale fails to teach or suggest these claim limitations; thus, we are

similarly not persuaded in the arguments against the combination of Belkhale and Tom.

Patent Owner also argues that a person of ordinary skill in the art would not have been motivated to combine Belkhale and Tom, because Belkhale is directed to a method to perform a static timing analysis that takes into account false paths of a circuit description that are not logically realizable but Tom is directed to performing static timing analysis in circuits having multiple clock signals. PO Resp. 42–43 (Ex. 1005, 736; Ex. 1006, 1:6–10). Thus, Patent Owner argues Belkhale and Tom are “directed to entirely different subject matter.” PO Resp. 42. We are not persuaded by this argument, as even Patent Owner agrees that both references are “related to the broad concept of static timing analysis.” *Id.* Petitioner’s Declarant, Dr. Ghiasi, states that a person of ordinary skill in the art would have been motivated to combine Tom with Belkhale to construct a system for static timing analysis that would allow both false paths and multi-cycle timing adjustments as it would provide a more accurate timing analysis that could uncover hidden timing errors and be less error prone. Ex. 1007 ¶¶ 211–213 (citing Ex. 1006, 3:62–68, 4:2-7).

Petitioner further argues that it is because Belkhale and Tom are “looking to improve the same thing” (static timing analysis) in different ways that they are combinable. Pet. Reply 20 (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007) (“if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill.”)). More particularly, Petitioner asserts the combined references would “not only

produce a system that could handle both multi-cycle and false path non-default timing adjustments, it would produce an accurate system that takes the logic of the circuit into account and enables optimization by removing false paths.” Pet. 45. Accordingly, we are persuaded that Petitioner has presented sufficiently an “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)) (internal quotation marks omitted).

As to dependent claims 2, 3, 10, and 11, Patent Owner argues that the combination of Belkhale and Tom fails for the same reasons addressed above regarding the challenge of Belkhale alone. PO Resp. 45–50. Similar to above, we are equally unpersuaded by these arguments against the combination of Belkhale and Tom. We also are persuaded by Petitioner’s evidence regarding dependent claims 4, 7, 8, and 9. Pet. 53, 55–56.

3. *Conclusion Regarding Claims 1–4 and 7–11*

With respect to the Petitioner’s challenge that claims 1–4 and 7–11 of the ’127 patent would have been obvious in view of Belkhale and Tom, we have considered the papers submitted by the parties and the evidence cited therein. For the foregoing reasons, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1–4 and 7–11 of the ’127 patent would have been obvious in view of Belkhale and Tom.

III. CONCLUSION

Petitioner has shown by a preponderance of the evidence that:

(1) claims 1–4 and 7–11 of the '127 patent would have been obvious in view of Belkhale, and (2) claims 1–4 and 7–11 of the '127 patent would have been obvious in view of Belkhale and Tom.

IV. ORDER

For the reasons given, it is

ORDERED that, based on Petitioner's showing by a preponderance of the evidence, claims 1–4 and 7–11 of the '127 patent are unpatentable; and

FURTHER ORDERED that this is a final written decision and that parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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