

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ATOPTECH, INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

Case IPR2014-01150
Patent 6,567,967 B2

Before TRENTON A. WARD, MATTHEW R. CLEMENTS, and
PETER P. CHEN, *Administrative Patent Judges*.

CHEN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

ATopTech, Inc. (“Petitioner”) filed a Corrected Petition requesting an *inter partes* review of claims 1–4, 7–22, and 32–36 of U.S. Patent No. 6,567,967 B2 (Ex. 1001, “the ’967 patent”). Paper 7 (“Pet.”). Synopsys, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 10 (“Prelim. Resp.”). On January 21, 2015, we instituted an *inter partes* review for claims on certain grounds of unpatentability alleged in the Petition. Paper 11 (“Dec. to Inst.”).

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 23, “PO Resp.”), to which Petitioner filed a Reply (Paper 28, “Pet. Reply”). An oral hearing was held on November 13, 2015, consolidated with the hearings in IPR2014-01145 and IPR2014-01159. The transcript of the consolidated hearing has been entered into the record. Paper 33 (“Tr.”).

The Board has statutory authority under 35 U.S.C. § 6(c). In this Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, we determine Petitioner has shown by a preponderance of the evidence that claims 1, 4, 8, 9, 12, 16, 19–22, and 32–36 of the ’967 patent are unpatentable.

A. *Related Proceedings*

On June 26, 2013, Patent Owner filed a Complaint against Petitioner in the U.S. District Court for the Northern District of California, alleging infringement of the ’967 patent. *Synopsys, Inc. v ATopTech, Inc.*, No. cv-13-02965-MMC (N.D. Cal. 2013). We also instituted an *inter partes* review of claims 5, 23, 24, 26, 27, and 31 of the ’967 patent, in *ATopTech, Inc. v Synopsys, Inc.*, Case IPR2014-01159, slip. op. 25 (PTAB January 21, 2015) (Paper 11). Additionally, we instituted an *inter partes* review of claims 1–4

and 7–11 of Patent Owner’s U.S. Patent No. 6,237,127, in *ATopTech, Inc. v Synopsys, Inc.*, Case IPR2014-01145, slip. op. 25 (PTAB January 21, 2015) (Paper 7).

B. The ’967 Patent

The ’967 patent is titled, “Method for Designing Large, Standard-Cell Base Integrated Circuits.” The subject matter of the challenged claims of the ’967 patent relates generally to automated methods for physically designing large integrated circuits (ICs). Ex. 1001, 1:18–20. There are two basic techniques for physically designing ICs, called standard-cell and full-custom. *Id.* at 1:24–25. As the complexity of such integrated circuits increases, automated standard-cell design techniques are inadequate in development time, chip size, or operating speed. *Id.* at 2:22–25. In most cases, a full-custom design technique, in which layout occurs manually by hand, is impractical due to the long and expensive development process. *Id.* at 2:27–29. The ’967 patent describes an automated design method for large ICs that partitions areas of the design, where each section can be designed independently in the desired design time, and creates connections between blocks to maximize operating speed while minimizing the area of the IC. *Id.* at Abstract, 2:44–49.

Figure 1 of the '967 patent is reproduced below.

Fig. 1

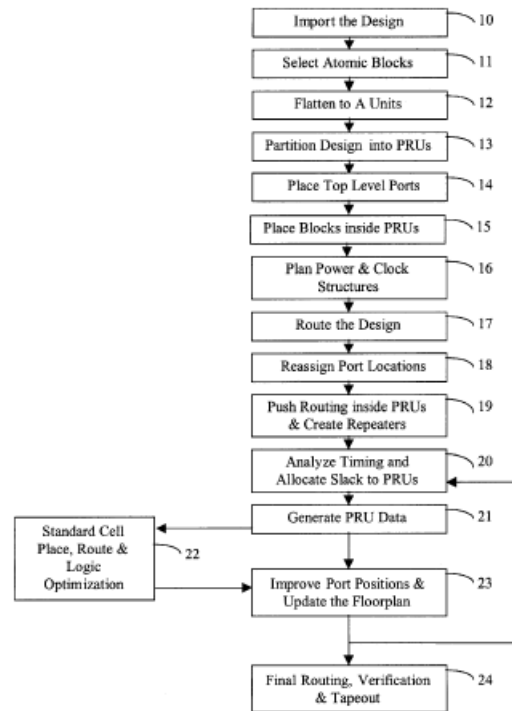


Figure 1 is a flowchart of a method for designing large ICs as claimed in the '967 patent. *Id.* at 3:6–8. At step 10, design data consisting of a netlist and other information is imported, or read. *Id.* at 3:66–4:6, 5:29–6:19. At step 11, atomic or “A” blocks, or units, are selected from the imported design data. *Id.* at 4:7–13. These “A” blocks are indivisible. *Id.* at 4:12. At step 12, the design is flattened to remove levels of hierarchy above the A blocks. *Id.* at 4:13–14. At step 13, the design is partitioned, into place and route units (“PRUs”), so as to minimize the total length of wire interconnect between blocks and to minimize the total area of the IC. *Id.* at 4:15–25. At step 14, ports, which allow interconnections between PRUs and other circuit elements, are placed temporarily into the physical design. *Id.* at 4:26–28. At

step 15, blocks are positioned within PRUs. *Id.* at 4:29–31. “[G]ood hard block placement within each PRU is the primary goal of this step,” *id.* at 9:58–59, and by “allowing the soft blocks to assume rectilinear shapes,” empty wasted space can be eliminated. *Id.* at 10:11–18. Steps 16–24 complete the design process. *Id.* at 4:32–5:27.

Figure 3 of the ’967 patent is reproduced below.

Fig. 3

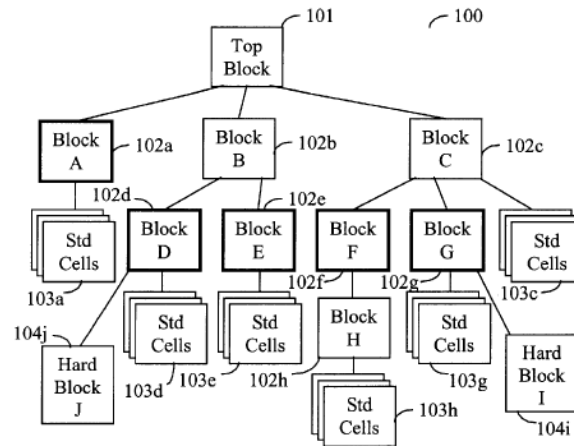


Figure 3 is a block diagram of exemplary design 100 for an IC, having a hierarchical structure including pre-designed hard blocks 104i and 104j, groups of standard cells 103a, 103c, 103d, 103e, 103g, and 103h, and blocks 102a, 102d, 102e, 102f, and 102g designated as “A” or atomic blocks. *Id.* at 6:20–25, 36–38, 49–50. “A” blocks generally are selected to be one or more hierarchy levels above the bottom (or “leaf” level) of the design. *Id.* at 6:36–39.

Figure 5 of the '967 patent is reproduced below.

Fig. 5

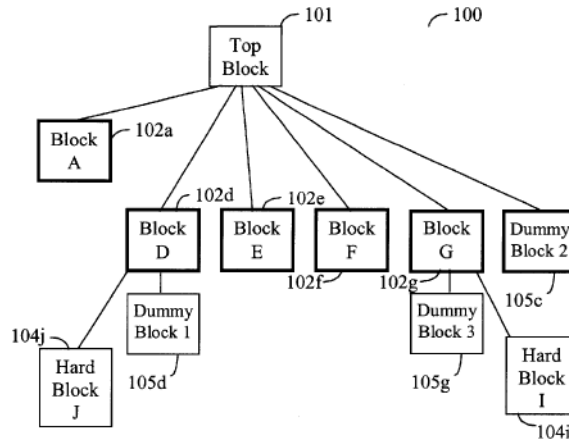


Figure 5 shows the hierarchy resulting after design 100 is flattened to the “A” block level by removing high level blocks 102b and 102c.

Ex. 1001, 7:25–29. The flat group of “A” blocks is then partitioned to form place and route units (“PRUs”). *Id.* at 7:35–37, 54–57.

Figure 6 of the '967 patent is reproduced below.

Fig. 6

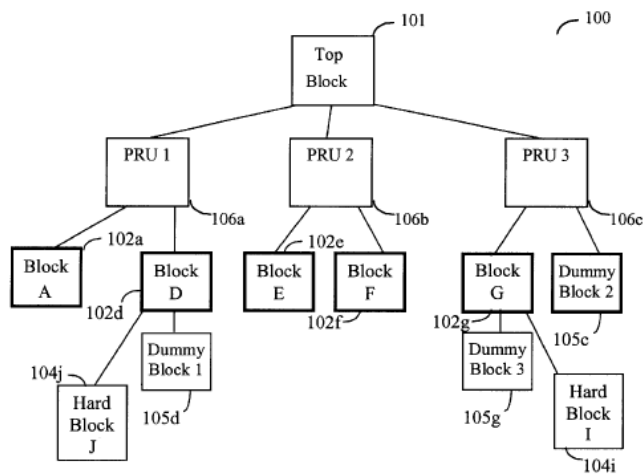


Figure 6 shows design 100 with a new level of hierarchy of PRU blocks 106a, 106b, and 106c formed by grouping sets of “A” blocks together “to minimize overall wirelength, chip area, and/or the worst case timing paths of the design.” Ex. 1001, 7:49–62.

C. Illustrative Claims

Claims 1, 4, 8, 9, 12, 16, 19–22, and 32–36 of the ’967 patent are the subject of the trial. Claims 1, 32, and 33 are independent. Claims 2, 8, 9, 12, 16, and 19–22 directly or indirectly depend from claim 1, and claims 34–36 directly or indirectly depend from claim 33. Independent claims 1, 32, and 33 are illustrative and are reproduced as follows.

1. A method for physically designing an integrated circuit comprising:

importing a netlist description of an integrated circuit design, said netlist description comprising a plurality of hierarchically arranged branches;

selecting atomic blocks for each of said plurality of hierarchically arranged branches, each of said atomic blocks selected to be one or more hierarchy levels above the bottom of a corresponding one of said hierarchically arranged branches, each of said atomic blocks being either an atomic hard block, an atomic soft block or an atomic hierarchical block;

flattening each of said plurality of hierarchically arranged branches by eliminating superfluous levels of hierarchy above said atomic blocks;

partitioning each of said atomic blocks into one of a plurality of place and route units ("PRUs"); and

positioning said atomic blocks within each of said plurality of PRUs.

32. A method of fitting an integrated circuit design within a predefined area, the integrated circuit design comprising one or more of hard blocks, hierarchical blocks and soft blocks, the hard blocks having a fixed shape, comprising:

determining optimal placement of each of the hard blocks, if any, within the predefined area; and

selecting a rectilinear shape for each of the soft blocks, if any, and hierarchical blocks, if any, so that the soft blocks, if any, and hierarchical blocks, if any, fit within spaces of the predefined area left unoccupied by the hard blocks.

33. A method of fitting an integrated circuit design within a predefined area, said method comprising:

determining placement of at least one hard block within the predefined area, wherein said at least one hard block has a predefined shape; and

selecting a rectilinear shape for at least one block within the predefined area, such that said at least one block fits within space in said predefined area left unoccupied by said at least one hard block.

Id. at 17:19–37, 20:20–40.

D. Prior Art Supporting the Instituted Challenges

The following references were asserted in the instituted grounds.

Reference	Title	Ex. No.
Fields	<i>Creating Hierarchy in HDL-Based High Density FGPA Design</i> , Euro-DAC '95, 594–99 (Sept. 18-22, 1995)	Ex. 1005
Su	<i>Performance-Driven Soft-Macro Clustering and Placement by Preserving HDL Design Hierarchy</i> , Proceedings, 1998 International Symposium on Physical Design: ISPD-98, 12–17 (Apr. 8, 1998)	Ex. 1006

E. The Instituted Challenges of Unpatentability

The following table summarizes the challenges to patentability on which we instituted *inter partes* review.

Reference(s)	Basis	Claims Challenged
Fields and Su	§ 103	1, 4, 8, 9, 12, 16, and 19–22
Su	§ 102	32–36

II. ANALYSIS

A. *Claim Construction*

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1275–79 (Fed. Cir. 2015). The claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). Claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). On the other hand, a “claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer” and clearly set forth a definition of the claim term in the specification. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). Finally, only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy.

Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999).

In our Decision to Institute, we construed “place and route unit (PRU).” We determined that the broadest reasonable interpretation of that term is, “a section of the IC design created to represent the physical partitioning of the IC design.” Dec. to Inst., 10. Neither party disputes that construction in their post-institution filings.

Petitioner has not proposed any additional terms for construction. Patent Owner has proposed that “atomic block” be construed as “a netlist block that is indivisible for the purpose of partitioning the circuit design into place and route units (PRUs).” PO Resp. 8–10. Petitioner appears to disagree with Patent Owner’s proposal. Pet. Reply 8–9.

Our interpretation of the disputed term begins with the language of the claim. See *Microsoft Corporation v. Proxyconn Inc.*, 789 F.3d 1292, 1299 (Fed. Cir. 2015). Claim 1 does not define an atomic block, but recites that “each of said atomic blocks [is] selected to be one or more hierarchy levels above the bottom of a corresponding one of said hierarchically arranged branches, each of said atomic blocks being either an atomic hard block, an atomic soft block or an atomic hierarchical block.”

Claims should also be read in light of the specification and teachings in the underlying patent. *In re Cuozzo*, 793 F.3d at 1280; *Microsoft Corporation v. Proxyconn Inc.*, 789 F.3d at 1298. Here, the specification expressly defines atomic blocks:

Defining Atomic ("A") blocks (sometimes called units) – “A” blocks are the netlist blocks that will be physically partitioned to create place and route units (PRUs). “A” blocks may contain only standard cells or they may contain additional levels of

hierarchy. For the purpose of partitioning the circuit design into PRUs, the "A" blocks are indivisible.

Ex. 1001, 4:8–12. Consistent with the patentee’s express definition of atomic block, we determine the broadest reasonable interpretation of atomic block to be, “a netlist block that is indivisible for the purpose of physically partitioning the circuit design into place and route units (PRUs).”

B. Principles of Law

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). “A reference anticipates a claim if it discloses the claimed invention such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.” *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) (quoting *In re LeGrice*, 301 F.2d 929, 936 (CCPA 1962)) (internal quotation marks and emphasis omitted). In the context of anticipation, “it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826 (CCPA 1968).

Similarly, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). A prima facie case of obviousness is established when the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. *In re Rinehart*, 531 F.2d 1048, 1051 (CCPA 1976).

C. Level of Ordinary Skill in the Art

Petitioner has not proposed a level of ordinary skill in the art. Patent Owner proposes that one of ordinary skill in the art would possess a “Bachelor of Science degree in Electrical Engineering, Computer Engineering, or a closely related field,” as well as “a minimum of one to two years of professional experience in the engineering development of integrated circuit technology.” Ex. 2004 (Declaration of Daniel Foty, Ph.D.), ¶ 15. At the oral hearing, Petitioner stated it had no dispute with Patent Owner’s proposal. Tr. 16:21–17:2.

We determine that an express definition of the level of ordinary skill is not required. The level of ordinary skill in the art can be reflected in the cited prior art references. See *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (“the absence of specific findings on the level of skill in the art does not give rise to reversible error where the prior art itself reflects an appropriate level and a need for testimony is not shown.”) (internal quotations omitted); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Therefore, we find the level of ordinary skill in the art to be reflected in the cited references.

*D. Claims 1,4, 8, 9, 12, 16, and 19–22:
Asserted Obviousness over Fields and Su*

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). Petitioner contends claims 1, 4, 8, 9, 12, 16, and 19–22 are unpatentable under 35 U.S.C. § 103 as obvious over Fields and Su. Pet. 15–50.

Fields (Exhibit 1005)

Fields was published in a 1995 digest of technical papers and is titled, “Creating Hierarchy in HDL-Based High Density FGPA(sic) Design.” Fields states that “[c]urrent design methodologies tend to target ASIC devices” and, for field-programmable gate array (“FPGA”) devices, Fields states that “proper use of hierarchy in high density FPGA designing is critical in achieving desired device utilization.” Ex. 1005, 594. Fields describes “partitioning a large design into modules” and states, “employing floorplanning techniques to govern the relative placement of those modules, results in the most-effective combination of FPGA device capacity and performance.” *Id.*

Figure 1 of Fields is reproduced below.

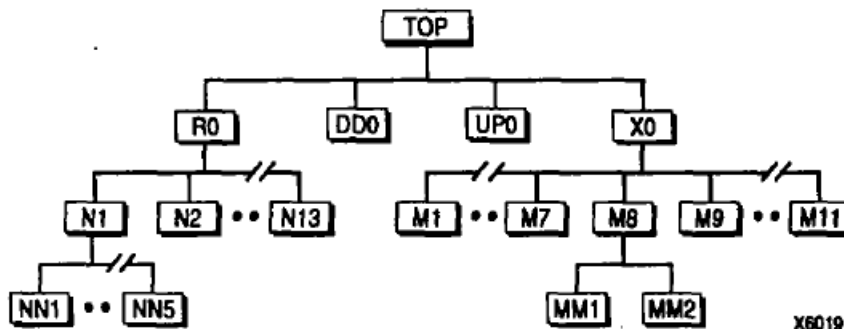


Figure 1 Original Hierarchy of Top Design

In Figure 1, the original multi-level hierarchy of the design has a level below “Top” including modules DD0, UP0, X0 and R0, ranging in size from four configurable logic blocks (“CLBs”) to 591 CLBs, and sub-hierarchical modules M1–M11 and N1–N13. Ex. 1005, 595. Fields also describes “[t]he recommended methodology for a large HDL design is to re-group the design’s hierarchy into mid-size modules.” *Id.* at 596.

Figure 4 of Fields is reproduced below.

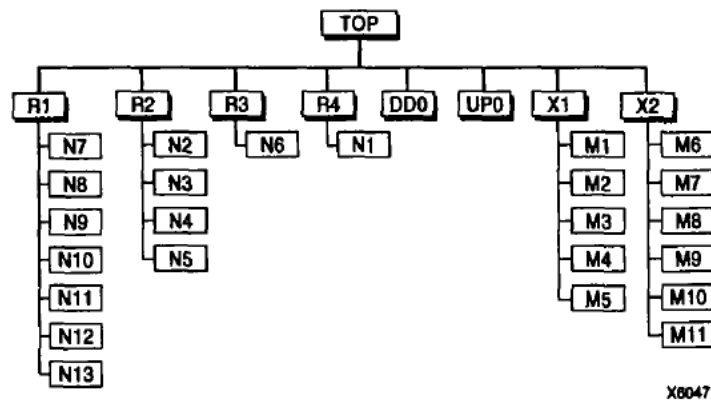


Figure 4 New Design Hierarchy

In Figure 4, the design is “re-grouped” into mid-size modules based on “the sizes of the modules and the modules’ interconnections with surrounding modules.” *Id.* at 596. Module R0 “was separated into 4 modules” (R1–R4) and module X0 into modules X1–X2, as shown in Figure 4. *Id.* New module X1 contains sub-hierarchical modules M1 through M5, and new module X2 contains M6 through M11. *Id.* Fields also describes how the modules were “constrained into regions of the device.” *Id.* at 597.

Figure 5 of Fields is reproduced below.

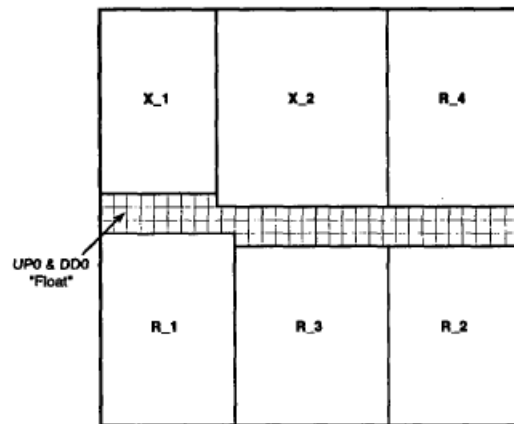


Figure 5 Floorplanning Modules into Areas

In Figure 5, the newly re-grouped modules are “constrained into regions of the device,” where “[e]ach region must be large enough to fit the module and provides the placement and routing tools room to route the module.” *Id.* at 597.

Su (Exhibit 1006)

Su was published in a 1998 digest of technical papers and is titled, “*Performance-Driven Soft-Macro Clustering and Placement by Preserving HDL Design Hierarchy.*” Su describes a design methodology to implement hierarchical circuit designs physically, in particular, a soft macro clustering and placement technique which preserves the HDL design hierarchy. Ex. 1006, 12. Su’s described methodology is “performance driven” and seeks to “improve the quality of soft macro placement.” *Id.* at 12, 13.

Figures 2(a) and (b) of Su are reproduced below.

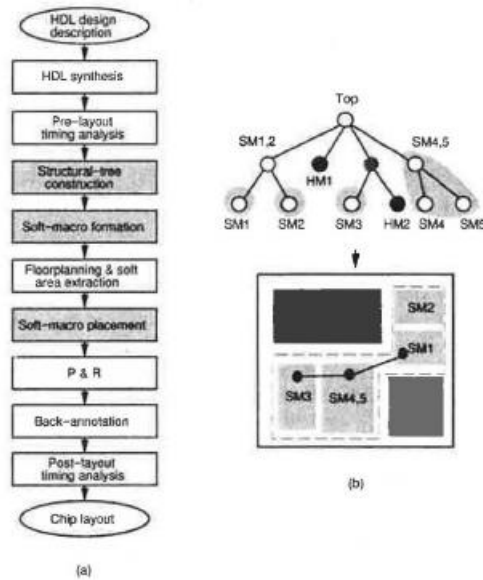


Figure 2: The proposed method: (a) the design flow, (b) an example.

Figure 2(a) is a flowchart of Su's proposed design flow. "In the first step, an HDL-based synthesizer converts the Verilog design description into a hierarchical gate-level netlist by performing HDL compilation and a series of [Register-Transfer Level] RTL and logic synthesis tasks." Ex. 1006, 13. In the second step, timing analysis is performed. "In the third step, an HDL structural tree of the design is constructed to preserve the design hierarchy." *Id.* "In the fourth step, the system groups small subcircuits to form large macros and decomposes extremely large macros into smaller ones." *Id.*

Figure 2(b) illustrates the soft macro formation of four soft macros SM1, SM2, SM3, and SM4,5, from "a structural tree which contains two hard macros HM1 and HM2, and five soft leaf-macros SM1-SM5." *Id.* After soft macro formation and a floorplanning process, a rectilinear area is extracted for soft macros (dotted line area in Figure 2(b)). *Id.* at 13–14.

Figure 3 of Su is reproduced below.

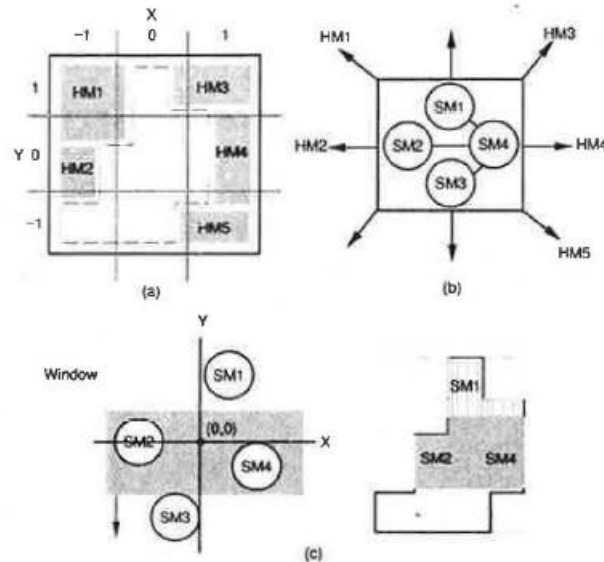


Figure 3(a) shows nine regions of the layout plane for soft macro placement, including HM1 and HM2. *Id.* at 14–15. Figure 3(b) shows the relative location of each soft macro SM1–SM4. *Id.* Figure 3(c) shows the assignment of soft macros in their allocated region. *Id.* at 15.

Analysis -- Claim 1

Petitioner explains how the subject matter of independent claim 1 is taught or suggested by Fields and Su. Pet. 20–29. In particular, Petitioner explains that Fields inherently discloses an imported netlist, as Fields Figure 1 “reflects the hierarchical netlist for an IC design.” *Id.* at 21, 27; Ex. 1005, 596 and Fig. 1. Petitioner further contends Fields discloses the selection of atomic blocks and that “Su discloses ‘hard macros,’ ‘soft macros,’ and ‘hierarchical modules,’ which correspond to” the recited ‘an atomic hard block, an atomic soft block or an atomic hierarchical block’ of claim 1, respectively.” Pet. 22–23, 27–28; Ex. 1005, 595–96, 599, Fig. 1; Ex. 1006, 13. Petitioner further contends Fields and Su disclose flattening of the hierarchy by eliminating levels of hierarchy above the atomic blocks

(Pet. 22–25, 28; Ex. 1005, 596, Figs. 1, 4; Ex. 1006, 13 and Fig. 2(b)), that Fields discloses partitioning the atomic blocks into PRUs (Pet. 25–26, 28–29; Ex. 1005, 597 and Fig. 5), and finally, that Su “expressly teaches positioning atomic blocks within a single PRU.” Pet. 26, 29; Ex. 1006, 14 and Fig. 3.

Patent Owner’s Response makes several arguments against the Fields and Su combination. Patent Owner first argues that one of ordinary skill in the art would not combine Fields and Su “because they address completely different problems in completely different technologies using completely different design tools.” PO Resp. 19. Patent Owner does concede Su describes a “design flow for the physical layout” of an IC (*id.* at 20), but argues that Fields is not relevant to physical IC design. *Id.* at 18.

In reply, Petitioner contends Fields is analogous art to the ’967 patent because “an FPGA is indisputably a type of integrated circuit . . . and Fields relates to a method for physical design as the size of the circuit increases.” Pet. Reply 2. Petitioner cites a textbook entitled “VLSI Physical Design Automation” (Ex. 1022, the “VLSI textbook”), relied upon by Petitioner’s declarant Dr. Ghiasi, which expressly describes FPGA as one of a series of “layout approaches used to generate physical representations of circuits,” along with full custom and standard cell techniques (described in the ’967 patent, *see* Section I.B.), and others. Pet. Reply 3–5 (citing Ex. 1022); *see also* Ex. 1022, § 1.3, Table 1.1.

Petitioner further contends Fields is reasonably pertinent to the problem to be solved, namely, the increasing density and complexity of circuit designs (Pet. Reply 6–7), and that it would have been obvious to combine Fields and Su (Pet. Reply 7–8 (citing Ex. 1009 (Ghiasi Decl.)

¶¶ 72–76); *see also* Pet. 20)). At the oral hearing, Petitioner stated, “[a]ll of the purposes of constraining the CLBs into the areas of the FPGA are relevant to dividing a silicon-based IC into PRUs.” Tr. 114:14–16; *see also id.* at 69:21–71:4, 112:18–114:13.

We agree with Petitioner that the ’967 patent, Fields, and Su are all directed at efficient circuit design involving large and complex circuits, and determine that, as set forth in the VLSI textbook, FPGA is indeed a type of layout for physical design. We also credit the testimony of Dr. Ghiasi, who opines that:

While Fields presents this logical approach to IC floorplanning in the context of FPGA design, one of ordinary skill as of September 2000 would have understood that the general teachings of Fields could be applied to the design of an ASIC chip as well as an FPGA chip and would have been motivated to apply the teaching of Fields to solve the problem of very large IC chip design. . . . One of ordinary skill in the field of EDA design would be familiar with IC design for both ASIC and FPGA formats and would rely on teachings in the context of FPGA chip design, especially in the front end of an EDA design flow, through floorplanning and partitioning of the physical design in addressing problems in ASIC chip design, and vice versa.

Ex. 1009 ¶¶ 72–73. Even assuming *arguendo* the Board were to accept Patent Owner’s assertion that design of an FPGA is “completely different” from design of an integrated circuit, the Supreme Court’s decision in *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) stated, “[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.” Thus, under KSR, such purportedly “different” teachings of Fields about FPGA design could be applicable to the physical design of an integrated

circuit as described in the '967 patent and in Su. We are persuaded by Petitioner's evidence, including the VLSI textbook and the Ghiasi declaration, and find that one of ordinary skill in the art would have understood the applicability of Fields' FPGA teachings to physical design of an integrated circuit as recited in claim 1 of the '967 patent.

Second, Patent Owner argues the combination of Fields and Su does not "disclose"¹ claim 1's recited selection of atomic blocks. PO Resp. 22–26. We have construed atomic block as "a netlist block that is indivisible for the purpose of physically partitioning the circuit design into place and route units (PRUs)." Patent Owner argues Fields "never states whether the program modules being regrouped are divisible or indivisible" (PO Resp. 22–24) and argues Su's soft macros "are not indivisible for the purpose of placement; instead they are divided into smaller modules for placement" (PO Resp. 24–26).

In reply, Petitioner asserts "both Fields and Su disclose 'selecting atomic blocks,' because both disclose that certain blocks in the hierarchy are partitioned without being divided." Pet. Reply 8–11. In particular, Petitioner asserts Figures 1 and 2 of Fields disclose that blocks N1–N13 and M1–M11 were selected as atomic blocks because they were partitioned into PRUs without being divided. Pet. Reply 10; Ex. 1005, Figs. 1, 2. Furthermore, Dr. Ghiasi states that by re-grouping sub-hierarchical modules N1–N13 and M1–M11 of the hierarchy's branches into new modules, Fields discloses that the sub-hierarchical modules N1–N13 and M1–M11 are

¹ Both parties use the term "disclose" throughout their arguments on the Fields and Su combination. For obviousness combinations, however, a reference need only "teach or suggest."

selected. Ex. 1009 ¶ 79. In Su, soft macros SM1, SM2, SM3, and SM4,5 were “formed,” i.e., selected as atomic blocks, because they were selected as indivisible units. Pet. Reply 10–11; Ex. 1006, 13, Fig. 2. We are persuaded by Petitioner’s reasoning and find that one of ordinary skill in the art would have understood Fields and Su to teach or suggest the selection of atomic blocks that are indivisible for purposes of a partitioning process.

Third, Patent Owner argues the combination of Fields and Su does not disclose claim 1’s recited flattening of hierarchically arranged branches by eliminating superfluous layers of hierarchy above the atomic blocks. PO Resp. 26–30. In particular, Patent Owner argues Fields does not eliminate levels of hierarchy, but rather, merely regroups modules by dividing them into smaller modules. *Id.* Patent Owner also argues Su’s soft macros SM1 and SM2 are not atomic blocks, but are “leaf-macros” at the bottom level of Su’s hierarchy. PO Resp. 29–30.

In reply, Petitioner asserts that in Fields, modules R0 and X0 were removed, and in Su, node SM1,2 is eliminated. Pet. Reply 11–14; Ex. 1005, Figs. 1, 4; Ex. 1006, Fig. 2(b). In addition, Petitioner asserts Su’s leaf macros contain standard cells and therefore are different from the ’967 patent’s leaf, or bottom, level. Pet. Reply 13–14. At the oral hearing, Petitioner added that Su “is taking the two hard blocks that are at different levels of the hierarchy to start with and it is moving them both up under the single layout plane level.” Tr. at 82:9–20.

As testified to by Dr. Ghiasi, in Fields, the level of hierarchy containing modules R0 and X0 (and UP0 and X0) as depicted in Figure 1 is eliminated from Figure 4 in that it does not appear in the same form, having been replaced with the R0 and X0 modules being divided and renamed as

R1–R4 and X1–X2, respectively. Ex. 1009 ¶ 83. Fields describes the process as a re-grouping, or new grouping. Ex. 1005, 596, Figs. 1, 4. In Figure 2(b) of Su, the two hard macros HM1 and HM2 are first shown at two different levels of the “structural tree of the design,” and then are depicted after soft macro formation in the same layout plane, where “each hard macro is assigned into its corresponding region.” Ex. 1006, 13–14, Figs. 2(b) and 3. See Ex. 1009 ¶ 84. While neither Fields nor Su explicitly describes the elimination of a level of hierarchy, we are persuaded based on the figures and accompanying text in both references, that one of ordinary skill in the art would have understood Fields and Su to teach or suggest the elimination of a level of hierarchy above the atomic blocks.

Lastly, Patent Owner argues Fields does not teach or suggest claim 1’s recited partitioning of atomic blocks into PRUs, because Fields does not describe physical partitioning of an IC design. PO Resp. 30–32. The Petition cited Figure 5 of Fields, which illustrates a floorplan with regions, “each of which corresponds to one of the recited a plurality of PRUs.” Pet. 25. In its reply, Petitioner reiterates Figures 5 (and 6) of Fields depict floorplanning of circuit modules into areas of the device, quoting Fields’ description of “partitioning a large design into modules in the 3,000 to 5,000 gate range” and “constraining” configurable logic blocks into regions of the device. Pet. Reply 14–15; Ex. 1005, 594, 597, Figs 2, 3, 7; Ex. 1009 (Ghiasi Decl.) ¶ 85.

We agree with Petitioner. We have construed PRU as “a section of the IC design created to represent the physical partitioning of the IC design.” Section II.A. Fields expressly and repeatedly describes “partitioning” a large design of an FPGA device. Ex. 1005, Abstract, 594, 595, 599. We

find that one of ordinary skill in the art would have understood that Fields' modules (i.e., the recited "atomic blocks") are partitioned into regions, which correspond to the recited "PRUs." We also find that one of ordinary skill in the art would have read Fields, including its reference to ASICs (*id.* at 594) and understood that Fields' teachings could be applied not only to FPGAs, but also to physical design of ICs in general.

We find the other elements of claim 1 to be taught or suggested by Fields and Su. Pet. 20–22, 26–27, 29. Based on our review of the entirety of the evidence in this trial, we determine that Petitioner has shown by a preponderance of evidence that the combination of Fields and Su teaches or suggests the limitations of claim 1, and that Petitioner has provided articulated reasoning supported by rational underpinnings for combining the references.

Analysis -- Claims 4, 8, 9, 12, 16, and 19–22

Dependent claims 4, 8, 9, 12, 16, and 19–22 all depend directly or indirectly from claim 1. Petitioner explains how Fields (claim 16), Su (claims 4, 8, 9, 19–22), and Fields and Su (claim 12) teach or suggest the limitations of these claims. Pet. 34–39, 46–49.

Claim 4 narrows claim 1's step of positioning atomic blocks within PRUs by moving atomic hard blocks within PRUs to a level of hierarchy below the PRU, determining optimal placement of the atomic blocks, and selecting a rectilinear shape for soft atomic blocks and hierarchical atomic blocks. Ex. 1001, 17:64–18:10. Petitioner contends Su discloses the limitations of claim 4. Pet. 34–37; Ex. 1006, 13–14, Figs. 2(b), 3.

Patent Owner argues Su does not disclose atomic hard blocks or placement of hard blocks within a PRU. PO Resp. 33. In reply, Petitioner

asserts Su's hard macros correspond to the recited hard blocks, and are atomic because they are "placed in the layout plane without being divided." Pet. Reply 15–16. Petitioner further asserts one of ordinary skill would understand that Su's layout plane is "logically equivalent to a PRU because the purpose of a PRU is to split up a chip into sections" for individual design. *Id.* We agree that Figures 2 and 3, and accompanying text, of Su teach or suggest that its hard macros are atomic and are placed within a PRU. Ex. 1006, 13-14, Figs. 2(b), 3.

Patent Owner also argues that neither Fields nor Su teaches or suggests "selecting a rectilinear shape for each of" the soft blocks. PO Resp. 33–33. Patent Owner asserts the claim language requires the selection of a particular, specific rectilinear shape among more than one such shape. *Id.* at 34; Tr. 106:18–20, 107:23–108:1. In reply, Petitioner states:

Like the specification, the claims require only that a rectilinear shape be selected so that the blocks "fit within spaces of the predefined area left unoccupied by the hard blocks," not that a selection be made between various rectilinear shapes.

Pet. Reply 16, 25. We agree with Petitioner. The claim does not recite that a selection occur among various rectilinear shapes, but rather states only that "a rectilinear shape" is selected for each soft block. Ex. 1001, 18:5. The '967 specification also describes soft block placement in terms of "using more general ('rectilinear') shapes to fit around the hard blocks." Ex. 1001, 10:39–40. We find that the claim language and the specification do not require the selection of specific rectilinear shapes argued for by Patent Owner.

Claim 8 recites designating at least one of the atomic blocks as “stopped,” in that it does not contain a hard block. Ex. 1001, 6:50–55, 18:27–28. Petitioner contends Figure 2(b) of Su shows stopped atomic blocks. Pet. 38; Ex. 1006, Fig. 2(b).

Claim 9 recites at least one of the atomic blocks contains no hard blocks. Ex. 1001, 18:29–30. Petitioner contends Figure 2(b) of Su renders this claim obvious by showing soft macros without hard macros in them. Pet. 38; Ex. 1006, Fig. 2(b).

Claim 12 recites that the superfluous levels of hierarchy in claim 1 include “all levels of hierarchy between the atomic blocks and a top level block.” Ex. 1001, 18:35–37. Petitioner contends Fields and Su both teach the elimination of superfluous levels of hierarchy above the atomic blocks and below the top level. Pet. 40–41; Ex. 1005, 595 and Figs. 1, 4; Ex. 1006, 13 and Fig 2(b).

Claim 16 recites that the partitioning step of claim 1 results in each PRU “abutting at least one other PRU.” Ex. 1001, 18:54–56. Petitioner contends Figure 5 of Fields shows regions abutting others. Pet. 44; Ex. 1005, Fig. 5.

Claims 19–22 recite the use of rectilinear shapes for soft blocks in PRUs. Ex. 1001, 18:63–19:17. Petitioner explains how Su describes and illustrates the use of rectilinear soft macros that correspond to the recited rectilinear shapes in the PRUs. Pet. 46–50; Ex. 1006, 13–14 and Figs. 2–3.

Based on our review of the Petition and the entirety of the evidence in the trial, we are persuaded Petitioner sufficiently demonstrates that Fields and/or Su teach or suggest the respective limitations of these dependent claims.

Accordingly, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 4, 8, 9, 12, 16, and 19–22 would have been obvious over Fields and Su.

E. Claims 32–36: Asserted Anticipation by Su

Petitioner contends claims 32–36 are unpatentable under 35 U.S.C. §§ 102 as anticipated by Su. Pet. 50–55. Independent claims 32 and 33 and dependent claims 34–36 recite methods for fitting integrated circuit design within predefined areas by selecting rectilinear shapes for blocks within the predefined areas. Ex. 1001, 20:20–46.

Analysis -- Claim 32

Petitioner explains how Su discloses the recited limitations of independent claim 32. Pet. 50–52. Petitioner contends that (1) Figure 2(b) of Su discloses the recited “method of fitting an integrated circuit design within a predefined area, the integrated circuit design comprising one or more of hard blocks, hierarchical blocks and soft blocks” (Pet. 50; Ex. 1006, 13, and Fig. 2(b)); (2) Figures 2(b) and 3(a) disclose the recited “determining optimal placement of each of the hard blocks, if any, within the predefined area” (Pet. 51; Ex. 1006, 13–14); and (3) Figs. 2(b), 3(a), and 3(c) disclose “selecting a rectilinear shape for each of the soft blocks, if any, and hierarchical blocks, if any” so that the blocks fit in unoccupied space in the predefined area (Pet. 51–52; Ex. 1006, 13–14, and Figs. 2(b) and 3). Claim 32 requires “one or more” of “hard blocks, hierarchical blocks, and soft blocks,” and Petitioner asserts Su discloses all three types of blocks. Pet. 50.

Patent Owner argues Su does not expressly disclose “determining optimal placement” of hard blocks present in the design, and that the Petition

has not provided evidence to support an argument of anticipation by inherency. PO Resp. 35–38. In reply, Petitioner contends Su “discloses ‘optimal’ placement of the hard blocks” by describing a “performance-driven” method using a commercial floorplanning tool that was provided with “most critical paths” for timing constraints. Pet. Reply 17–18 (citing Ex. 1009 (Ghiasi decl.) ¶ 135); *see also* Ex. 1006, Abstract 13, 16.²

We credit the testimony of Dr. Ghiasi and agree with Petitioner that while Su does not expressly use the term “optimal,” its performance-driven method is optimized. As explained above in Section II.B., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009). Here, Su plainly discloses the placement of hard blocks, in its description of a “commercial floorplanner to perform macro floorplanning to determine the locations of hard macros” (Ex. 1006, 13, 14). In addition, we are persuaded there is a preponderance of evidence that Su discloses “determining optimal placement” of hard blocks (along with the remainder of Su’s method), because Su repeatedly discloses its “performance-driven” method, including in its title and abstract (*id.* at 12, 13, 16), the “effectiveness of the proposed method” (*id.* at 12, 15–16; *see also* Abstract), and the “quality of soft macro placement” (*id.* at 13). Optimal hard block placement is consistent with the explicitly stated goals of Su’s methodology.

² Petitioner also argues briefly that Su at least inherently discloses optimal placement, or renders the limitation obvious. Pet. Reply at 21. We note that we instituted trial only on an anticipation ground, and any argument as to obviousness therefore is not relevant. We also agree with Patent Owner that Petitioner’s arguments are insufficient to support a showing of anticipation by inherency. PO Resp. 37.

Patent Owner also argues that Su fails to disclose “selecting a rectilinear shape.” PO Resp. 38–42. Patent Owner asserts the claim language requires the selection of a particular rectilinear shape among more than one such shape. *Id.* at 39; Tr. 106:18–20, 107:23–108:1 (selecting limitation requires that a specific rectilinear shape be chosen for each of the soft blocks). In reply, Petitioner states:

Like the specification, the claims require only that a rectilinear shape be selected so that the blocks “fit within spaces of the predefined area left unoccupied by the hard blocks,” not that a selection be made between various rectilinear shapes.

Pet. Reply 25. We agree with Petitioner. The claim language does not recite that a selection occurs among various rectilinear shapes, and instead recites only that “a rectilinear shape” is selected for each soft block. Ex. 1001, 18:5. The ’967 specification also describes soft block placement in terms of “using more general (‘rectilinear’) shapes to fit around the hard blocks.” Ex. 1001, 10:39–40. Such language undermines the selection of specific rectilinear shapes argued for by Patent Owner. Based on the entirety of the evidence in this trial, we are persuaded Petitioner has established, by a preponderance of the evidence, that Su discloses the selecting limitation, and further that Su discloses the other limitations of claim 32.

Analysis -- Claims 33–36

Independent claim 33 lacks claim 32’s recitation of “optimal” placement of hard blocks, and instead recites only “determining placement of at least one hard block.” Ex. 1001, 20:33–34. Claim 33 does recite, similarly to claim 32, “selecting a rectilinear shape for at least one block within the predefined area” for the IC design. *Id.* at 20:26–27, 20:31–40. Petitioner explains how Su discloses the recited limitations of independent

claim 33. Pet. 52–54. In particular, Petitioner contends Su discloses the block placement and rectilinear shape limitations of claim 33. Pet. 53–54; Ex. 1006, 13–14, Figs. 2(b), 3. Petitioner also contends Su discloses the limitations of dependent claims 34–36, which recite further details of the blocks. Pet. 54–55; Ex. 1001, 20:41–46.

Patent Owner argues only that Su fails to disclose selecting a rectilinear shape (PO Resp. 38–42), which we find no more persuasive for claim 33 than the same argument was for claim 32, as discussed above. Based on the entirety of the evidence in this trial, we are persuaded Petitioner has established, by a preponderance of evidence, that Su discloses the limitations of claims 33–36.

III. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence the unpatentability of claims 1, 4, 8, 9, 12, 16, and 19–22 of the '967 patent as obvious over Fields and Su, and of claims 32–36 of the '967 patent as anticipated by Su.

IV. ORDER

Accordingly, it is

ORDERED that, based on Petitioner's showing by a preponderance of the evidence, claims 1, 4, 8, 9, 12, 16, 19–22, and 32–36 of the '967 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of this decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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