

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ATOPTECH, INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

Case IPR2014-01159
Patent 6,567,967 B2

Before TRENTON A. WARD, MATTHEW R. CLEMENTS, and
PETER P. CHEN, *Administrative Patent Judges*.

CHEN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

ATopTech, Inc. (“Petitioner”) filed a Corrected Petition requesting an *inter partes* review of claims 5, 6, and 23–31 of U.S. Patent No. 6,567,967 B2 (Ex. 1001, “the ’967 patent”). Paper 7 (“Pet.”). Synopsys, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 10 (“Prelim. Resp.”). On January 21, 2015, we instituted an *inter partes* review for claims on certain grounds of unpatentability alleged in the Petition. Paper 11 (“Dec. to Inst.”).

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 21, “PO Resp.”), to which Petitioner filed a Reply (Paper 26, “Pet. Reply”). An oral hearing was held on November 13, 2015, consolidated with the hearings in IPR2014-01145 and IPR2014-01150. The transcript of the consolidated hearing has been entered into the record. Paper 31 (“Tr.”).

The Board has statutory authority under 35 U.S.C. § 6(c). In this Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, we determine Petitioner has shown by a preponderance of the evidence that claims 5, 23, 26, and 27 of the ’967 patent are unpatentable.

A. *Related Proceedings*

On June 26, 2013, Patent Owner filed a Complaint against Petitioner in the U.S. District Court for the Northern District of California, alleging infringement of the ’967 patent. *Synopsys, Inc. v ATopTech, Inc.*, No. cv-13-02965-MMC (N.D. Cal. 2013). In a related matter before the Board, we instituted an *inter partes* review of claims 1, 4, 8, 9, 12, 16, 19–22, and 32–36 of the ’967 patent, in *ATopTech, Inc. v Synopsys, Inc.*, Case IPR2014-01150, slip. op. 23 (PTAB January 21, 2015) (Paper 11). Additionally, we instituted an *inter partes* review of claims 1–4 and 7–11 of Patent Owner’s

U.S. Patent No. 6,237,127, in *ATopTech, Inc. v Synopsys, Inc.*, Case IPR2014-01145, slip. op. 25 (PTAB January 21, 2015) (Paper 7).

B. The '967 Patent

The '967 patent is titled, “Method for Designing Large Standard-Cell Base Integrated Circuits.” The subject matter of the challenged claims of the '967 patent relates generally to automated methods for physically designing large integrated circuits (ICs). Ex. 1001, 1:18–20. There are two basic techniques for physically designing ICs, called standard-cell and full-custom. *Id.* at 1:24–25. As the complexity of such integrated circuits increases, automated standard-cell design techniques are inadequate in development time, chip size, or operating speed. *Id.* at 2:22–25. In most cases, a full-custom design technique, in which layout occurs manually by hand, is impractical due to the long and expensive development process. *Id.* at 2:27–29. The '967 patent describes an automated design method for large ICs that partitions areas of the design, where each section can be designed independently in the desired design time, and creates connections between blocks to maximize operating speed while minimizing the area of the IC. *Id.* at Abstract, 2:44–49.

Figure 1 of the '967 patent is reproduced below.

Fig. 1

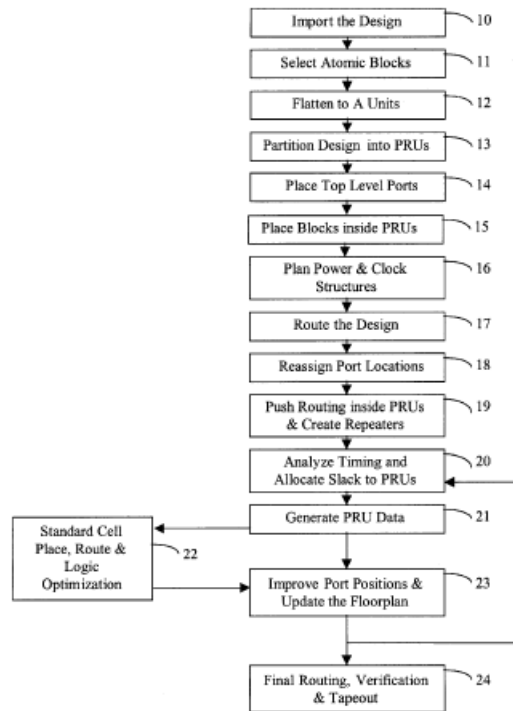


Figure 1 is a flowchart of a method for designing large ICs as claimed in the '967 patent. *Id.* at 3:6–8. At step 10, design data consisting of a netlist and other information is imported, or read. *Id.* at 3:66–4:6, 5:29–6:19. At step 11, atomic or “A” blocks, or units, are selected from the imported design data. *Id.* at 4:7–13. These “A” blocks are indivisible. *Id.* at 4:12. At step 12, the design is flattened to remove levels of hierarchy above the A blocks. *Id.* at 4:13–14. At step 13, the design is partitioned, into place and route units (“PRUs”), so as to minimize the total length of wire interconnect between blocks and to minimize the total area of the IC. *Id.* at 4:15–25. At step 14, ports, which allow interconnections between PRUs and other circuit elements, are placed temporarily into the physical design. *Id.* at 4:26–28, 4:41–43. These temporary, or dummy, ports, are placed within the area of

the PRUs. *Id.* at 9:40–56, 13:3–7. At step 15, blocks are positioned within PRUs. *Id.* at 4:29–31. “[G]ood hard block placement within each PRU is the primary goal of this step,” *id.* at 9:58–59, and by “allowing the soft blocks to assume rectilinear shapes,” empty wasted space can be eliminated. *Id.* at 10:11–18. At step 16, power and clock structures are generated. *Id.* at 11:55–56. At step 17, after the dummy ports are placed on all PRU blocks, the design is routed using a global router, and exact locations are determined for where nets cross the edges of PRU blocks. *Id.* at 12:52–55, 13:35–52. At step 18, the dummy ports are deleted, and the global router is run again to generate real ports at the edges of the PRU blocks. *Id.* at 13:55–60. Steps 16–24 complete the design process. *Id.* at 4:32–5:27.

Figure 3 of the '967 patent is reproduced below.

Fig. 3

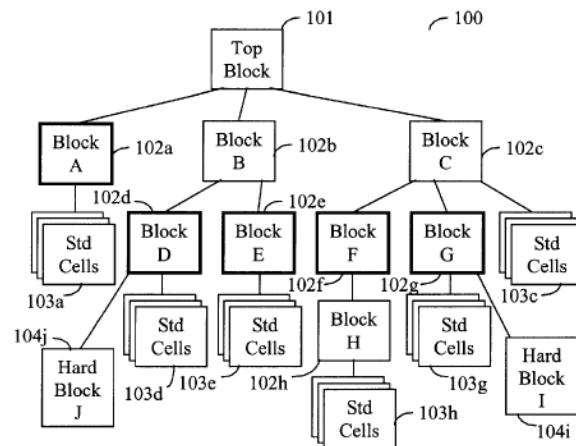


Figure 3 is a block diagram of exemplary design 100 for an IC, having a hierarchical structure including pre-designed hard blocks 104i and 104j, groups of standard cells 103a, 103c, 103d, 103e, 103g, and 103h, and blocks 102a, 102d, 102e, 102f, and 102g, designated as “A” or atomic blocks. *Id.* at 6:20–25, 36–38, 49–50. “A” blocks generally are selected to be one or more

hierarchy levels above the bottom (or “leaf” level) of the design. *Id.* at 6:36–39.

Figure 5 of the '967 patent is reproduced below.

Fig. 5

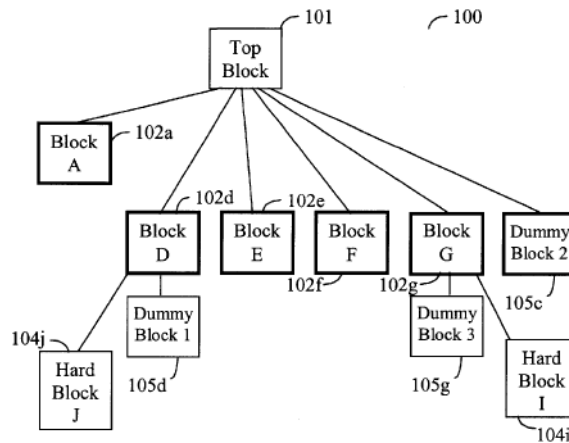


Figure 5 shows the hierarchy resulting after design 100 is flattened to the “A” block level by removing high level blocks 102b and 102c. *Id.* at 7:25–29. The flat group of “A” blocks is then partitioned to form place and route units (“PRUs”). *Id.* at 7:35–37, 54–57.

Figure 6 of the '967 patent is reproduced below.

Fig. 6

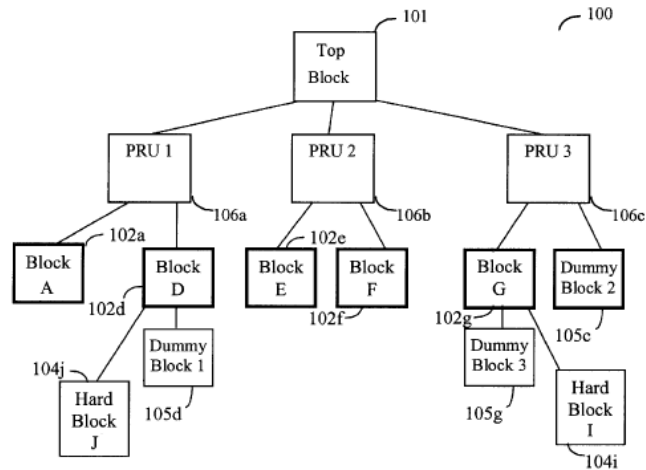


Figure 6 shows design 100 with a new level of hierarchy of PRU blocks 106a, 106b, and 106c formed by grouping sets of “A” blocks together “to minimize overall wirelength, chip area, and/or the worst case timing paths of the design.” *Id.* at 7:49–62.

C. Illustrative Claims

Claims 5, 23, 24, 26, 27, and 31 of the '967 patent are the subject of the trial. Claims 1 and 31 are independent. Claims 5, 23, 24, 26, and 27 directly or indirectly depend from claim 1. Independent claim 1 is reproduced for reference, and claim 31 is illustrative and is also reproduced as follows.

1. A method for physically designing an integrated circuit comprising:
importing a netlist description of an integrated circuit design, said netlist description comprising a plurality of hierarchical arranged branches;
selecting atomic blocks for each of said plurality of hierarchically arranged branches, each of said atomic blocks

selected to be one or more hierarchy levels above the bottom of a corresponding one of said hierarchically arranged branches, each of said atomic blocks being either an atomic hard block, an atomic soft block or an atomic hierarchical block;

flattening each of said plurality of hierarchically arranged branches by eliminating superfluous levels of hierarchy above said atomic blocks;

partitioning each of said atomic blocks into one of a plurality of place and route units ("PRUs"); and

positioning said atomic blocks within each of said plurality of PRUs.

31. A method of routing an integrated circuit design comprised of a plurality of place and route units ("PRUs"), comprising:

creating dummy ports on each of said PRUs, said dummy ports allowing a net to traverse from a first of said plurality of PRUs to a second of said plurality of PRUs;

connecting said dummy ports on said PRUs by routing nets between them;

determining where said routing nets cross edges of said plurality of PRUs;

deleting said dummy ports; and

generating real ports where said routing nets cross edges of said plurality of PRUs.

Id. at 17:19–37, 20:5–19.

D. Prior Art Supporting the Instituted Challenges

The following references were asserted in the instituted grounds.

Reference	Title	Ex. No.
Fields	<i>Creating Hierarchy in HDL-Based High Density FGPA Design</i> , Euro-DAC '95, 594–99 (Sept. 18-22,	Ex. 1005

Reference	Title	Ex. No.
	1995)	
Su	<i>Performance-Driven Soft-Macro Clustering and Placement by Preserving HDL Design Hierarchy</i> , Proceedings, 1998 International Symposium on Physical Design: ISPD-98, 12–17 (Apr. 8, 1998)	Ex. 1006
Ling	US 6,223,329 (issued Apr. 24, 2001, filed June 17, 1998)	Ex. 1007
Venkatesh	US 5,778,216 (issued July 7, 1998, filed June 30, 1995)	Ex. 1008

E. The Instituted Challenges of Unpatentability

The following table summarizes the challenges to patentability on which we instituted *inter partes* review.

Reference(s)	Basis	Claims Challenged
Ling	§ 102	31
Fields, Su, and Ling	§ 103	5, 23, 24, and 26
Fields, Su, and Venkatesh	§ 103	27

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1275–79 (Fed. Cir. 2015). The claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech.*

Ctr., 367 F.3d 1359, 1364 (Fed. Cir. 2004). Claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). On the other hand, a “claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer” and clearly set forth a definition of the claim term in the specification. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). Finally, only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

In our Decision to Institute, we construed “place and route unit (PRU).” We determined that the broadest reasonable interpretation of that term is, “a section of the IC design created to represent the physical partitioning of the IC design.” Dec. to Inst., 10. Neither party disputes that construction in their post-institution filings.

Petitioner has not proposed any additional terms for construction. Patent Owner has proposed that “atomic block” be construed as “a netlist block that is indivisible for the purpose of partitioning the circuit design into place and route units (PRUs).” PO Resp. 8–10. Petitioner appears to disagree with Patent Owner’s proposal. Pet. Reply 8–9.

Our interpretation of the disputed term begins with the language of the claim. *See Microsoft Corp. v. Proxyconn Inc.*, 789 F.3d 1292, 1299 (Fed. Cir. 2015). Claim 1 does not define an atomic block, but recites that “each of said atomic blocks [is] selected to be one or more hierarchy levels above the bottom of a corresponding one of said hierarchically arranged branches,

each of said atomic blocks being either an atomic hard block, an atomic soft block or an atomic hierarchical block.”

Claims should also be read in light of the specification and teachings in the underlying patent. *In re Cuozzo*, 793 F.3d at 1280; *Microsoft Corporation v. Proxyconn Inc.*, 789 F.3d at 1298. Here, the specification expressly defines atomic blocks:

Defining Atomic ("A") blocks (sometimes called units) – “A” blocks are the netlist blocks that will be physically partitioned to create place and route units (PRUs). "A" blocks may contain only standard cells or they may contain additional levels of hierarchy. For the purpose of partitioning the circuit design into PRUs, the "A" blocks are indivisible.

Ex. 1001, 4:8–12. Consistent with the patentee’s express definition of atomic block, we determine the broadest reasonable interpretation of atomic block to be, “a netlist block that is indivisible for the purpose of physically partitioning the circuit design into place and route units (PRUs).”

B. Principles of Law

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). “A reference anticipates a claim if it discloses the claimed invention such that a

skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.” *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) (quoting *In re LeGrice*, 301 F.2d 929, 936 (CCPA 1962)) (internal quotation marks and emphasis omitted). In the context of anticipation, “it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826 (CCPA 1968).

Similarly, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). A prima facie case of obviousness is established when the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. *In re Rinehart*, 531 F.2d 1048, 1051 (CCPA 1976).

C. Level of Ordinary Skill in the Art

Petitioner has not proposed a level of ordinary skill in the art. Patent Owner proposes that one of ordinary skill in the art would possess a “Bachelor of Science degree in Electrical Engineering, Computer Engineering, or a closely related field,” as well as “a minimum of one to two years of professional experience in the engineering development of integrated circuit technology.” Ex. 2004 (Declaration of Daniel Foty, Ph.D.), ¶ 15. At the oral hearing, Petitioner stated it had no dispute with Patent Owner’s proposal. Tr. 16:21–17:2.

We determine that an express definition of the level of ordinary skill is not required. The level of ordinary skill in the art can be reflected in the cited prior art references. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (“the absence of specific findings on the level of skill in the art does not give rise to reversible error where the prior art itself reflects an appropriate level and a need for testimony is not shown.”) (internal quotations omitted); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Therefore, we find the level of ordinary skill in the art to be reflected in the cited references.

D. Claim 31: Asserted Anticipation by Ling

Petitioner contends claim 31 is unpatentable under 35 U.S.C. § 102 as anticipated by Ling. Pet. 16–28.

Ling (Exhibit 1007)

To prevail in its challenges to the patentability of claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). Ling is titled, “Hybrid Design Method and Apparatus for Computer-Aided Circuit Design,” and discloses hierarchical circuit design where the design is divided into individual components that can be processed independently of one another. Ex. 1007, 2:53–58. Figure 3 of Ling is reproduced below.

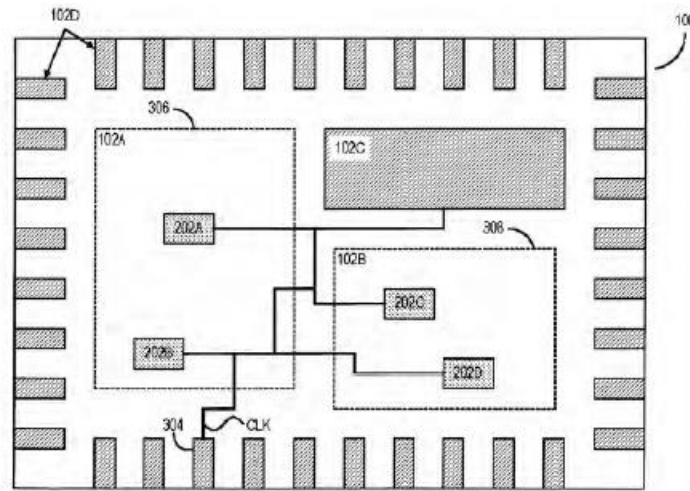


FIGURE 3

Figure 3 is a block diagram of circuit design 100, including hard block 102C, which generally cannot be modified during circuit design, soft blocks 102A and B, which “can be modified relatively easily by human circuit design engineers,” sub-blocks 202A–D, clock signal CLK, and pin 304. Ex. 1007, 4:11–14, 4:49–51, 4:62–67, 6:30–36. Clock signal CLK travels between soft blocks 102A and B, creating a global network. *Id.* at 6:34–36. Figure 4 of Ling is reproduced below.

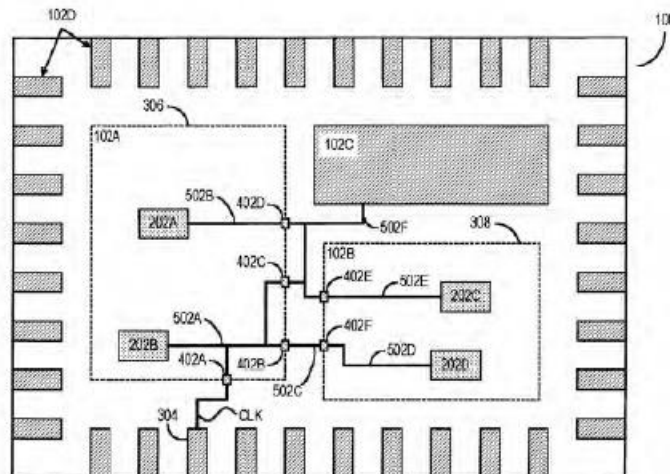


FIGURE 4

Figure 4 is a block diagram of design 100 in which pins 402A–F have been inserted at the edges of soft blocks 102A and B. Ex. 1007, 6:55–65. In

particular, a router “determines the relative positions at which a global network intersects a soft block boundary and creates a pin at each such intersection.” *Id.* at 6:60–62. Wire fragments 502A–F are formed by dividing global network CLK at locations of pins 402A–F. *Id.* at 6:65–67. Wire fragments 502C and 502F and a portion of CLK between pins 304 and 402A are outside the boundaries of soft blocks 102A and 102B and are fixed in place in the floor plan of circuit design 100. *Id.* at 7:4–12. Figure 5 of Ling is reproduced below.

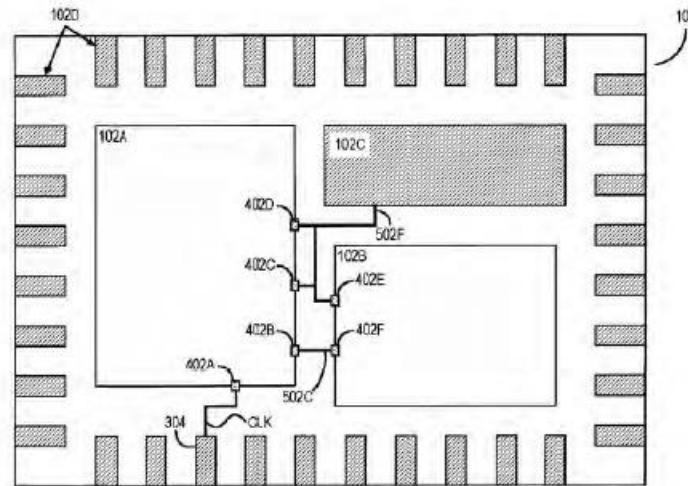


FIGURE 5

Figure 5 is a block diagram of design 100 showing that soft blocks 102A–B and other components of circuit design 10 are “fully de-coupled,” i.e., share no blocks, elements, or lines. Ex. 1001, 8:23–26. Pins 402A–F remain in design 100, and wire fragments 502A, B, D, and E have been removed, while wire fragments CLK, 502C, and 502F are fixed. *Id.* at Fig. 5, 10:7–8. Each de-coupled component of circuit design 100 can be processed independently. *Id.* at 8:32–34, 9:4–6. For example, soft block 102A “can be modified, flattened, simulated, reconstructed, modified, and

flattened again while the remainder of circuit design 100 remains unchanged.” *Id.* at 9:6–9.

Analysis

Independent claim 31 recites the creation, connection, and deletion of dummy ports on PRUs and the generation of real ports in place of dummy ports. *Id.* at 20:56–19. Petitioner contends claim 31 is unpatentable under 35 U.S.C. § 102 as anticipated by Ling. Pet. 16–28. Ling does not explicitly refer to ports, dummy ports, or real ports, or the “creation” or “deletion” of any of the aspects of its design. Petitioner asserts Ling discloses the creation of dummy ports because each of Ling’s sub-blocks 202A–D are shown in Figure 3 to be starting or ending points of the CLK net routed between PRUs, and therefore each sub-block “contains a dummy port” (Pet. 20–22, 25; Ex. 1007, Fig. 3, 5:30–41, 6:27–36, 13:35–42). Petitioner asserts Ling discloses the deletion of dummy ports because “each sub-block contains a dummy port and both the sub-block and dummy port location are temporary and may change upon final place and route.” Pet. 23–24, 27; Ex. 1007, Fig. 5, 5:30–41, 9:9–18.

Patent Owner argues that Ling fails to disclose creation of dummy ports because sub-blocks 202A–D are placed into “relatively optimal positions” in blocks 102A–C. PO Resp. 40–41; Ex. 1007, 5:23–26. Patent Owner asserts “relatively optimal” means the sub-blocks are “permanently” placed. *Id.* at 41. We disagree because Ling nowhere uses the term “permanent” or otherwise describes placement of sub-blocks as fixed. In addition, the use of the modifying adjective “relatively” can also suggest the possibility of modification or revision.

Patent Owner further argues that Ling fails to disclose the deletion of dummy ports because Ling's sub-blocks, which allegedly contain the dummy ports, are global components preserved for the final circuit design. PO Resp. 44–46. In particular, Patent Owner argues that sub-blocks 202A–D are not deleted after Ling's hierarchy is reconstructed, but rather are added to the hierarchy. *Id.* at 44, citing Ex. 1007, 7:43–8:7.

In its Reply, Petitioner cites to Figure 5 of Ling in which the sub-blocks are not depicted, and makes the conclusory assertion that the original ports on the sub-blocks therefore were deleted. Pet. Reply 20–21. At the oral hearing, Petitioner conceded, “Ling does not specifically call out the – it doesn't say, you know, in this step you create it, in this step you delete it.” Tr. 86:3–5. Petitioner further admitted:

So regardless of which stage, what we see is that the creating and deleting of the dummy ports is not tied to an actual creation of a port and a deletion of a port. It is essentially a construct that is used for the global routing and then, once you do that step to identify where it crosses the boundaries, then you can omit those dummy ports from the global route.

Tr. 119:14–20. Patent Owner stated at the oral hearing:

[F]igure 5 in Ling is showing an abstraction of the physical design such that after you have routed the PRUs together, you then decouple them and you are then able to perform the local routing inside of each of those blocks. That's why they are blank. They are not blank in this figure because anything was deleted.

Tr. 110:4–9. We agree with Patent Owner that Ling does not disclose deletion of dummy ports for several reasons. First, there is no explicit description in Ling of deletion of dummy ports, or of any structure corresponding to the recited dummy ports. Petitioner admits there is no

“actual” deletion of a dummy port, rather, “[i]t is essentially a construct.” Tr. 119:17. Second, while Ling describes that its soft blocks may be modified, flattened, simulated, or reconstructed, none of those actions is a deletion, and even so, there is no such disclosure of such actions as to the sub-blocks that Petitioner alleges contain the recited dummy ports.

Third, Petitioner’s conclusory assertions about Ling are also undermined by its concessions that Ling “at a minimum inherently” discloses both the creating and deleting of dummy ports (Pet. Reply 22) and that “one of ordinary skill in the art would recognize that after the blocks are decoupled . . . dummy ports are no longer necessary and may be deleted.” Pet. 23–24; Pet. Reply 21. Petitioner does not elaborate further on its glancing reference to anticipation by inherency, which we find to be insufficient. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (inherency may not be established by probabilities or possibilities.). In addition, Petitioner’s citation to what one of ordinary skill might recognize suggests that Ling at most renders claim 31 obvious, by itself or in combination with other references, a consideration not relevant to Petitioner’s challenge of anticipation by Ling.

Based on our review of the entire record in the trial, we are not persuaded that Petitioner has shown by a preponderance of the evidence that Ling anticipates claim 31 because Ling fails to disclose the recited deletion of dummy ports.

*E. Claims 5, 23, 24, and 26:
Asserted Obviousness over Fields, Su and Ling*

Dependent claims 5, 23, 24, and 26 all depend directly or indirectly from claim 1, which is not challenged in this trial. Petitioner contends

claims 5, 23, 24, and 26 are unpatentable under 35 U.S.C. § 103 as obvious over Fields, Su, and Ling. Pet. 28–54. We first analyze independent claim 1 in light of the Fields and Su references.

Fields (Exhibit 1005)

Fields was published in a 1995 digest of technical papers and is titled, “Creating Hierarchy in HDL-Based High Density FGPA(sic) Design.” Fields states that “[c]urrent design methodologies tend to target ASIC devices” and, for field-programmable gate array (“FPGA”) devices, Fields states that “[p]roper use of hierarchy in high density FPGA designing is critical in achieving desired device utilization.” Ex. 1005, 594. Fields describes “partitioning a large design into modules” and states, “employing floorplanning techniques to govern the relative placement of those modules, results in the most-effective combination of FPGA device capacity and performance.” *Id.*

Figure 1 of Fields is reproduced below.

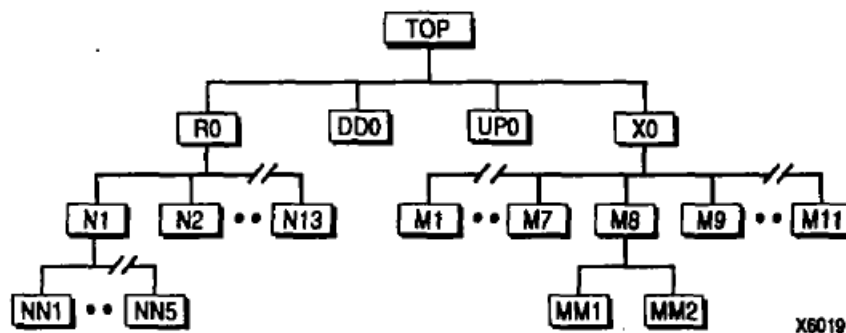


Figure 1 Original Hierarchy of Top Design

In Figure 1, the original multi-level hierarchy of the design has a level below “Top” including modules DD0, UP0, X0 and R0, ranging in size from four configurable logic blocks (“CLBs”) to 591 CLBs, and sub-hierarchical modules M1–M11 and N1–N13. Ex. 1005, 595. Fields also describes “[t]he

recommended methodology for a large HDL design is to re-group the design's hierarchy into mid-size modules.” *Id.* at 596.

Figure 4 of Fields is reproduced below.

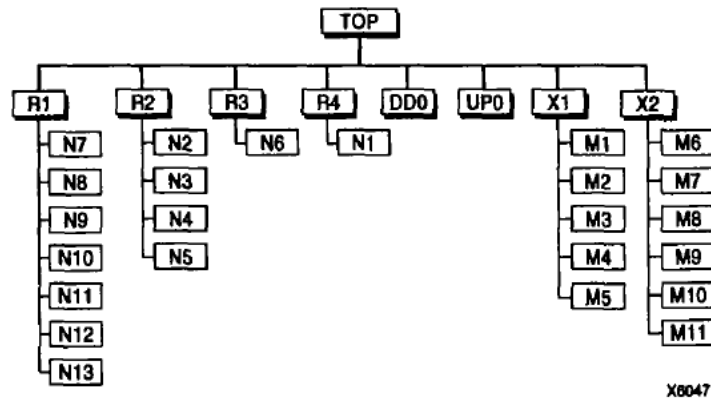


Figure 4 New Design Hierarchy

In Figure 4, the design is “re-grouped” into mid-size modules based on “the sizes of the modules and the modules’ interconnections with surrounding modules.” *Id.* at 596. Module R0 “was separated into 4 modules” (R1–R4) and module X0 into modules X1–X2, as shown in Figure 4. *Id.* New module X1 contains sub-hierarchical modules M1 through M5, and new module X2 contains M6 through M11. *Id.* Fields also describes how the modules were “constrained into regions of the device.” *Id.* at 597.

Figure 5 of Fields is reproduced below.

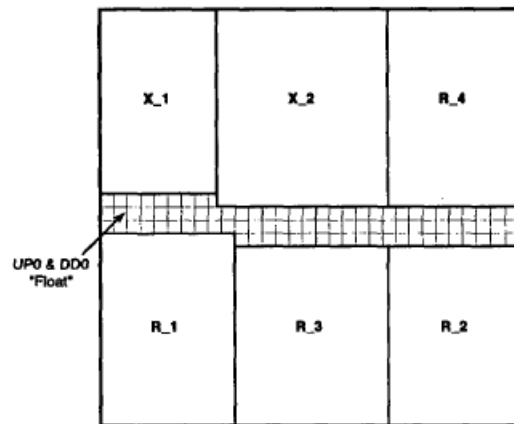


Figure 5 Floorplanning Modules into Areas

In Figure 5, the newly re-grouped modules are “constrained into regions of the device,” where “[e]ach region must be large enough to fit the module and provides the placement and routing tools room to route the module.” *Id.* at 597.

Su (Exhibit 1006)

Su was published in a 1998 digest of technical papers and is titled, “*Performance-Driven Soft-Macro Clustering and Placement by Preserving HDL Design Hierarchy.*” Su describes a design methodology to implement hierarchical circuit designs physically, in particular, a soft macro clustering and placement technique which preserves the HDL design hierarchy. Ex. 1006, 12. Su’s described methodology is “performance driven” and seeks to “improve the quality of soft macro placement.” *Id.* at 12, 13.

Figures 2(a) and (b) of Su are reproduced below.

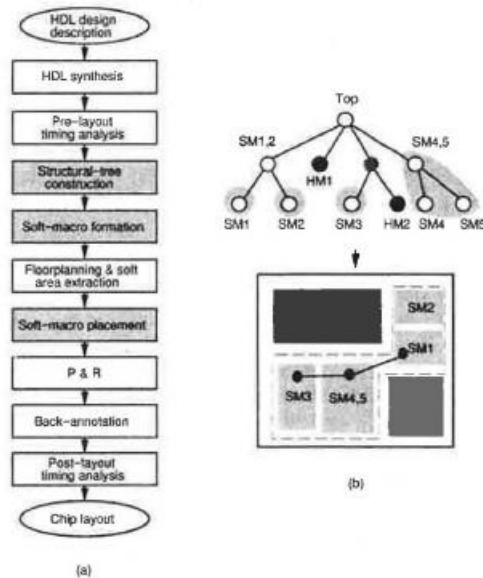


Figure 2: The proposed method: (a) the design flow, (b) an example.

Figure 2(a) is a flowchart of Su’s proposed design flow. “In the first step, an HDL-based synthesizer converts the Verilog design description into a hierarchical gate-level netlist by performing HDL compilation and a series of [Register-Transfer Level] RTL and logic synthesis tasks.” Ex. 1006, 13. In the second step, timing analysis is performed. “In the third step, an HDL structural tree of the design is constructed to preserve the design hierarchy.” *Id.* “In the fourth step, the system groups small subcircuits to form large macros and decomposes extremely large macros into smaller ones.” *Id.*

Figure 2(b) illustrates the soft macro formation of four soft macros SM1, SM2, SM3, and SM4,5, from “a structural tree which contains two hard macros HM1 and HM2, and five soft leaf-macros SM1-SM5.” *Id.* After soft macro formation and a floorplanning process, a rectilinear area is extracted for soft macros (dotted line area in Figure 2(b)). *Id.* at 13–14.

Figure 3 of Su is reproduced below.

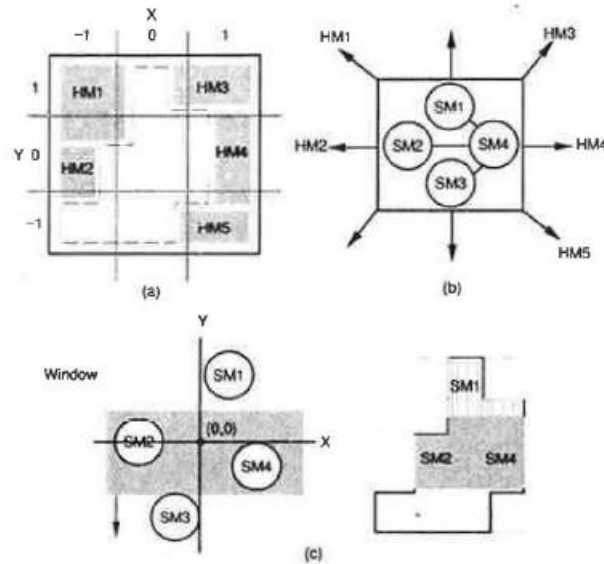


Figure 3(a) shows nine regions of the layout plane for soft macro placement, including HM1 and HM2. *Id.* at 14–15. Figure 3(b) shows the relative location of each soft macro SM1–SM4. *Id.* Figure 3(c) shows the assignment of soft macros in their allocated region. *Id.* at 15.

Analysis -- Claim 1

Before analyzing the challenged dependent claims in light of the asserted references, we must first determine whether independent claim 1 would have been obvious over those references. Petitioner explains how the subject matter of independent claim 1 is taught or suggested by Fields and Su. Pet. 34–43. In particular, Petitioner explains that Fields inherently discloses an imported netlist, as Fields' Figure 1 reflects the hierarchical netlist for an IC design. *Id.* at 35, 41; Ex. 1005, 596 and Fig. 1. Petitioner further contends Fields discloses the selection of atomic blocks and that "Su discloses 'hard macros,' 'soft macros,' and 'hierarchical modules,' which correspond" to the recited 'an atomic hard block, an atomic soft block or an atomic hierarchical block' of claim 1." Pet. 36–37, 41–42; Ex. 1005, 595–

96, 599, Fig. 1; Ex. 1006, 13. Petitioner further contends Fields and Su disclose flattening of the hierarchy by eliminating levels of hierarchy above the atomic blocks (Pet. 37–39, 42; Ex. 1005, 596, Figs. 1, 4; Ex. 1006, 13 and Fig. 2(b)), that Fields discloses partitioning the atomic blocks into PRUs (Pet. 39, 42–43; Ex. 1005, 597 and Fig. 5), and finally, that Su “expressly teaches positioning atomic blocks within a single PRU.” Pet. 40, 43; Ex. 1006, 14 and Fig. 3.

Patent Owner’s Response makes several arguments against the Fields and Su combination. Patent Owner first argues that one of ordinary skill in the art would not combine Fields and Su “because they address completely different problems in completely different technologies using completely different design tools.” PO Resp. 26. Patent Owner does concede Su describes a “design flow for the physical layout” of an IC (*id.* at 26–27), but argues that Fields is not relevant to physical IC design. *Id.* at 25.

In reply, Petitioner contends Fields is analogous art to the ’967 patent because “an FPGA is indisputably a type of integrated circuit . . . and Fields relates to a method for physical design as the size of the circuit increases.” Pet. Reply 2. Petitioner cites a textbook entitled “VLSI Physical Design Automation” (Ex. 1022, the “VLSI textbook”), relied upon by Petitioner’s declarant Dr. Ghiasi, which expressly describes FPGA as one of a series of “layout approaches used to generate physical representations of circuits,” along with full custom and standard cell techniques (described in the ’967 patent, see Section I.B.), and others. Pet. Reply 3–5 (citing Ex. 1022); see also Ex. 1022, § 1.3, Table 1.1.

Petitioner further contends Fields is reasonably pertinent to the problem to be solved, namely, the increasing density and complexity of

circuit designs (Pet. Reply 6–7), and that it would have been obvious to combine Fields and Su (Pet. Reply 7–8 (citing Ex. 1009 (Ghiasi Decl.) ¶¶ 72–76)). At the oral hearing, Petitioner stated, “[a]ll of the purposes of constraining the CLBs into the areas of the FPGA are relevant to dividing a silicon-based IC into PRUs.” Tr. 114:14–16; *see generally id.* at 69:21–70:4, 112:18–114:13.

We agree with Petitioner that the ’967 patent, Fields, and Su are all directed at efficient circuit design involving large and complex circuits, and determine that, as set forth in the VLSI textbook, FPGA is indeed a type of layout for physical design. We also credit the testimony of Dr. Ghiasi, who opines that:

While Fields presents this logical approach to IC floorplanning in the context of FPGA design, one of ordinary skill as of September 2000 would have understood that the general teachings of Fields could be applied to the design of an ASIC chip as well as an FPGA chip and would have been motivated to apply the teaching of Fields to solve the problem of very large IC chip design. . . . One of ordinary skill in the field of EDA design would be familiar with IC design for both ASIC and FPGA formats and would rely on teachings in the context of FPGA chip design, especially in the front end of an EDA design flow, through floorplanning and partitioning of the physical design in addressing problems in ASIC chip design, and vice versa.

Ex. 1009 ¶¶ 72–73. Even assuming *arguendo* the Board were to accept Patent Owner’s assertion that design of an FPGA is “completely different” from design of an integrated circuit, the Supreme Court’s decision in *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) stated, “[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.”

Thus, under KSR, such purportedly “different” teachings of Fields about FPGA design could be applicable to the physical design of an integrated circuit as described in the ’967 patent and in Su. We are persuaded by Petitioner’s evidence, including the VLSI textbook and the Ghiasi declaration, and find that one of ordinary skill in the art would have understood the applicability of Fields’ FPGA teachings to physical design of an integrated circuit as recited in claim 1 of the ’967 patent.

Second, Patent Owner argues the combination of Fields and Su does not “disclose”¹ claim 1’s recited selection of atomic blocks. PO Resp. 29–33. We have construed atomic block as “a netlist block that is indivisible for the purpose of physically partitioning the circuit design into place and route units (PRUs).” Patent Owner argues Fields “never states whether the program modules being regrouped are divisible or indivisible” (PO Resp. 29–31) and argues Su’s soft macros “are not indivisible for the purpose of placement; instead they are divided into smaller modules for placement” (PO Resp. 31–33).

In reply, Petitioner asserts “both Fields and Su disclose ‘selecting atomic blocks,’ because both disclose that certain blocks in the hierarchy are partitioned without being divided.” Pet. Reply 8–11. In particular, Petitioner asserts Figures 1 and 2 of Fields disclose that blocks N1–N13 and M1–M11 were selected as atomic blocks because they were partitioned into PRUs without being divided. Pet. Reply 10; Ex. 1005, Figs. 1, 2. Furthermore, Dr. Ghiasi states that by re-grouping sub-hierarchical modules

¹ Both parties use the term “disclose” throughout their arguments on the Fields and Su combination. For obviousness combinations, however, a reference need only “teach or suggest.”

N1–N13 and M1–M11 of the hierarchy’s branches into new modules, Fields discloses that the sub-hierarchical modules N1–N13 and M1–M11 are selected. Ex. 1009 ¶ 79. In Su, soft macros SM1, SM2, SM3, and SM4,5 were “formed,” i.e., selected as atomic blocks, because they were selected as indivisible units. Pet. Reply 10–11; Ex. 1006, 13, Fig. 2. We are persuaded by Petitioner’s reasoning and find that one of ordinary skill in the art would have understood Fields and Su to teach or suggest the selection of atomic blocks that are indivisible for purposes of a partitioning process.

Third, Patent Owner argues the combination of Fields and Su does not disclose the flattening of hierarchically arranged branches by eliminating superfluous layers of hierarchy above the atomic blocks, as recited in claim 1. PO Resp. 33–37. In particular, Patent Owner argues Fields does not eliminate levels of hierarchy, but rather, merely regroups modules by dividing them into smaller modules. *Id.* Patent Owner also argues Su’s soft macros SM1 and SM2 are not atomic blocks, but are “leaf-macros” at the bottom level of Su’s hierarchy. PO Resp. 36–37.

In reply, Petitioner asserts that in Fields, modules R0 and X0 were removed, and in Su, node SM1,2 is eliminated. Pet. Reply 11–14; Ex. 1005, Figs. 1, 4; Ex. 1006, Fig. 2(b). In addition, Petitioner asserts Su’s leaf macros contain standard cells and therefore are different from the ’967 patent’s leaf, or bottom, level. Pet. Reply 13–14. At the oral hearing, Petitioner added that Su “is taking the two hard blocks that are at different levels of the hierarchy to start with and it is moving them both up under the single layout plane level.” Tr. at 82:9–20.

As testified to by Dr. Ghiasi, in Fields, the level of hierarchy containing modules R0 and X0 (and UP0 and DD0) as depicted in Figure 1

is eliminated from Figure 4 in that the R0 and X0 modules have been divided and renamed as R1–R4 and X1–X2, respectively. Ex. 1009 ¶ 83. Fields describes the process as a re-grouping, or new grouping. Ex. 1005, 596, Figs. 1, 4. In Figure 2(b) of Su, the two hard macros HM1 and HM2 are first shown at two different levels of the “structural tree of the design,” and then are depicted after soft macro formation in the same layout plane, where “each hard macro is assigned into its corresponding region.” Ex. 1006, 13–14, Figs. 2(b) and 3; *see also* Ex. 1009 ¶ 84. While neither Fields nor Su explicitly describes the elimination of a level of hierarchy, we are persuaded based on the figures and accompanying text in both references, that one of ordinary skill in the art would have understood Fields and Su to teach or suggest the elimination of a level of hierarchy above the atomic blocks.

Lastly, Patent Owner argues Fields does not teach or suggest claim 1’s recited partitioning of atomic blocks into PRUs, because Fields does not describe physical partitioning of an IC design. PO Resp. 37–38. The Petition cites Figure 5 of Fields, which illustrates a floorplan with regions, “each of which corresponds to one of a plurality of PRUs.” Pet. 39, 43. In its Reply, Petitioner reiterates Figures 5 (and 6) of Fields depict floorplanning of circuit modules into areas of the device, quoting Fields’ description of “partitioning a large design into modules in the 3,000 to 5,000 gate range” and “constraining” configurable logic blocks into regions of the device. Pet. Reply 14–15; Ex. 1005, 594, 597, Figs 2, 3, 7; Ex. 1009 (Ghiasi Decl.) ¶ 85; *see also* Tr. 112:18–114:21.

We agree with Petitioner. We have construed PRU as “a section of the IC design created to represent the physical partitioning of the IC design.”

Section II.A. Fields expressly and repeatedly describes “partitioning” a large design of an FPGA device. Ex. 1005, Abstract, 594, 595, 599. We find that one of ordinary skill in the art would have understood that Fields’ modules (i.e., the recited “atomic blocks”) are partitioned into regions, which correspond to the recited “PRUs.” We also find that one of ordinary skill in the art would have read Fields, including its reference to ASICs (*id.* at 594) and understood that Fields’ teachings could be applied not only to FPGAs, but also to physical design of ICs in general.

We are persuaded the other elements of claim 1 are taught or suggested by Fields and Su. Pet. 34–43.

Analysis -- Claims 5, 23, 24, and 26

Petitioner cites to the declaration of Dr. Ghiasi and to Ling in explaining how Fields, Su, and Ling teach or suggest the limitations of dependent claims 5, 23, 24, and 26. Pet. 43–54. For claim 5, Petitioner relies on the Ghiasi declaration and Ling for the recited limitations of: (i) routing interconnections between said plurality of PRUs (*id.* at 43–44, citing Ex. 1009 ¶¶ 149, 160); (ii) assigning a port at an edge of a PRU where an interconnection crosses the edge, the port comprising an electrical contact (*id.* at 44–45, citing Ex. 1009 ¶ 161); (iii) pushing the interconnections inside the PRUs (*id.* at 45–46, citing Ex. 1009 ¶ 161); and (iv) creating a physical circuit layout for each PRU (*id.* at 46, citing Ex. 1009 ¶ 163). Ex. 1001, 18:11–20.

Petitioner also relies on the Ghiasi declaration to explain why one of ordinary skill in the art would have combined Ling with Fields and Su. Pet. 33–34, citing Ex. 1009 ¶ 158. Patent Owner does not argue, apart from its arguments with respect to claim 1, the additional limitations recited in

claim 5. We determine that Petitioner has shown by a preponderance of evidence that the combination of Fields, Su, and Ling teaches or suggests the limitations of claim 5.

Claim 23 depends from claim 1 and recites creating dummy ports enabling a net to traverse from a first PRU to a second PRU. Ex. 1001, 19:17–21. Petitioner again relies on the Ghiasi declaration and Ling. Pet. 48–49, citing Ex. 1009, ¶¶ 150–52, 167; Ex. 1007, 5:30–41, 9:4–9, 9:15–23, 6:23–36, Fig. 3. Patent Owner’s argument is identical to its argument against independent claim 31’s limitation of creating dummy ports, namely, that Ling’s description of “relatively optimal” placement of components in blocks compels a finding that any ports in Ling are permanent and not temporary or “dummy.” PO Resp. 40–41. We rejected this argument as to claim 31 (*see above*) and do so for claim 23 as well. We are persuaded that Ling’s Figure 3, and related disclosure in the specification, teaches or suggests the creation of temporary, or dummy, ports in sub-blocks 202A–D that are the starting or ending points of the CLK net routed between PRUs. *See* Pet. 48–49. We determine that Petitioner has shown by a preponderance of evidence that the combination of Fields, Su, and Ling teaches or suggests the limitations of claim 23.

Claim 24 depends from claim 23 and recites a first dummy port created on an atomic soft block in the first PRU and a second dummy port created on an atomic hard block in the second PRU. Ex. 1001, 19:23–26. Petitioner again relies on the Ghiasi declaration and Ling. Pet. 49–50. In particular, Ling discloses that the circuit design can include soft blocks and hard blocks, and that the sub-blocks containing the start and points of the CLK net may be soft blocks. Ex. 1007, 5:3–8, 11:11–15. Patent Owner

does not argue, apart from its arguments with respect to claim 23, from which claim 24 depends, the additional limitations recited in claim 24. We are persuaded by Petitioner's argument and determine that Petitioner has shown by a preponderance of evidence that the combination of Fields, Su, and Ling teaches or suggests the limitations of claim 24.

Claim 26 also depends from claim 23 and recites connecting the dummy ports by routing nets between them, determining where the routing nets cross edges of the PRUs, and then deleting the dummy ports and generating real ports where the routing nets cross the edges of the PRUs. Ex. 1001, 19:32–40. Patent Owner's argument is identical to its argument for a similar limitation in independent claim 31, namely, that Ling does not disclose deletion of dummy ports.

We found Ling did not disclose deletion of dummy ports as recited in claim 31, *see above*, and as to claim 26, we are again persuaded by Patent Owner's argument that Ling's sub-blocks allegedly containing dummy ports are not deleted but instead are added to the design hierarchy. PO Resp. 41–47. Moreover, as stated by Petitioner at the oral hearing, there simply is no actual deletion of alleged dummy ports in Ling, rather, merely “a construct.” Tr. 119:14–20. We decline to find a teaching or suggestion of deletion of dummy ports based only on an abstraction in Petitioner's proposed combination. We are not persuaded Petitioner sufficiently demonstrates that Fields, Su, and Ling teach or suggest the limitations of dependent claim 26.

Accordingly, based on our review of the Petition and the entirety of the evidence in the trial, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 5, 23, and 24 would have been obvious over Fields, Su, and Ling. We determine Petitioner has not

demonstrated by a preponderance of the evidence that claim 26 would have been obvious over Fields, Su, and Ling.

F. Claim 27: Asserted Obviousness Over Fields, Su, and Venkatesh

Petitioner contends dependent claim 27 is unpatentable under 35 U.S.C. § 103(a) as obvious over Fields, Su, and Venkatesh. Pet. 54–60. Claim 27 depends directly from claim 1 and recites “allocating slack time to PRUs in said plurality of PRUs.” Ex. 1001, 19:40–41.

Venkatesh (Exhibit 1008)

Venkatesh is titled, “Method for Hierarchical Time Drive Circuit Layout by Rebudgeting Timing Constraints of Plurality of Logical Blocks After Placement,” and describes a hierarchical timing-driven layout method for an integrated circuit. Ex. 1008, Abstract. A timing budgeter includes a Zero Slack Algorithm module that distributes slack (the amount of time between the arrival time of a signal at an output of a cell, block, or circuit, and the required arrival time of the signal) to each net (interconnection wire) of the circuit. *Id.* at Fig. 2, 4:7–11, 4:28–30, 5:19–27.

Analysis

Petitioner provides explanations of how Venkatesh teaches or suggests the limitations of dependent claim 27 regarding “allocating slack time to PRUs in said plurality of PRUs.” Pet. 57–60. The Petition contends Venkatesh describes partitioning a circuit design into a plurality of blocks, and discloses a Zero Slack Algorithm (“ZSA”) module that determines net timing constraints and “distributes slack to each net of the circuit.” Pet. 55, 57–58; Ex. 1008, 5:6–11, 6:5–9, 52–60, 7:42–45, and Figs. 6, 7. Petitioner further contends there existed motivation to combine Venkatesh with Fields and Su:

One of ordinary skill in the art at the time of filing would have been motivated to combine the teachings of Fields with Su and Venkatesh. Ex. 1009, ¶ 181. Each of Fields, Su, and Venkatesh are in the same technical area of endeavor: electronic design automation (“EDA”). *Id.* Each of Fields, Su, and Venkatesh are concerned with solving design problems in EDA that arise as a result of the increased size and complexity of ICs and seek to improve the physical design of ICs. *Id.* Where Fields and Venkatesh present partitioning modules into multiple PRUs, Su addresses the placement of modules or macros within a single PRU. *Id.* Su focuses on how to place the PRU contents (hard blocks, soft blocks, standard cells) within each PRU to fit within the floorplan. Fields, Venkatesh, and Su take different approaches to solving the same broader problem: how to translate the hierarchical design of the netlist into a workable floorplan for place and route. *Id.*

Pet. 56–57. We are persuaded that there is a preponderance of evidence showing the ZSA module of Venkatesh teaches or suggests the allocation of slack time to block structures (PRUs), and that Petitioner has provided articulated reasoning supported by rational underpinnings for combining Venkatesh with Fields and Su. Based on the entire record before us, we conclude that Petitioner has proved by a preponderance of the evidence that dependent claim 27 would have been obvious over Fields, Su, and Venkatesh.

III. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence the unpatentability of claims 5, 23, and 24 of the ’967 patent as obvious over Fields, Su, and Ling, and of claim 27 of the ’967 patent as obvious over Fields, Su, and Venkatesh. Petitioner has not demonstrated by a

preponderance of the evidence that claim 31 is anticipated by Fields, or that claim 26 would have been obvious over Fields, Su, and Ling.

IV. ORDER

Accordingly, it is

ORDERED that, based on Petitioner's showing by a preponderance of the evidence, claims 5, 23, 24, and 27 of the '967 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of this decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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