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Paper 35
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION, SONY ELECTRONICS INC.,
SONY MOBILE COMMUNICATIONS AB, and
SONY MOBILE COMMUNICATIONS (USA) INC.,
Petitioner,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

Case IPR2015-00158
Patent 7,296,121 B2

Before JENNIFER S. BISK, NEIL T. POWELL, and KERRY BEGLEY, *Administrative Patent Judges.*

POWELL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Sony Corporation, Sony Electronics Inc., Sony Mobile Communications AB, and Sony Mobile Communications (USA) Inc. (collectively, "Petitioner") filed a Petition requesting an *inter partes* review of claims 1–3, 8, 11, 12, and 14–25 (the "challenged claims") of U.S. Patent No. 7,296,121 B2 (Ex. 1001, "the '121 patent"). Paper 1 ("Pet."). On May 21, 2015, we instituted a review (Paper 7, "Institution Decision" or "Inst. Dec.") based upon Petitioner's assertion that claims 19–24 are unpatentable under 35 U.S.C. § 103. Inst. Dec. 35.

This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, Petitioner has shown by a preponderance of the evidence that claims 19–24 are unpatentable.

B. Related Matters

The parties indicate that the '121 patent is the subject of several proceedings in the United States District Court for the District of Delaware. Pet. 1; Paper 4, 1–2. In addition, other petitions seeking *inter partes* review of the '121 patent have been filed, including IPR2015-00159, IPR2015-00161, IPR2015-00163, IPR2015-00172, IPR2015-01353, and IPR2015-1376. Of these other proceedings at the Office, only IPR2015-00159 and IPR2015-00163 are ongoing.[1]

[1] IPR2015-01353 was terminated and the petitioner in that case was joined to IPR2015-00163. Similarly, IPR2015-01376 was terminated and the petitioner in that case was joined to IPR2015-00159.

C. The Pending Grounds of Unpatentability

We instituted *inter partes* review involving the following grounds of unpatentability:

Ground	Reference(s)	Challenged Claims
§ 103	Koster[2]	24
§ 103	Koster and Kuskin[3]	19–23

Petitioner supports its challenge with declarations executed by Dr. Daniel J. Sorin on November 3, 2014 (Ex. 1013) and on November 28, 2015 (Ex. 1015). Patent Owner relies on a declaration executed by Dr. Vojin Oklobdzija on August 11, 2015 (Ex. 2016).

D. The '121 Patent

The '121 patent relates to accessing data in computer systems that include more than one processor. Ex. 1001, 1:23–24. Specifically, the '121 patent discusses multiple processor systems with a point-to-point architecture—a cluster of individual processors (also referred to as processing nodes) that are directly connected to each other through point-to-point links, each with an associated cache memory. *Id.* at 4:38–40. To increase the number of available processors, multiple clusters may be connected. *Id.* at 4:50–53. Figure 1A is reproduced below.

[2] U.S. Patent No. 7,698,509 B1 (Ex. 1005) ("Koster").
[3] Jeffrey Kuskin et al., *The Stanford FLASH Multiprocessor*, *in* PROCEEDINGS OF THE 21ST ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE 302 (1994) (Ex. 1006, "Kuskin").

Figure 1A

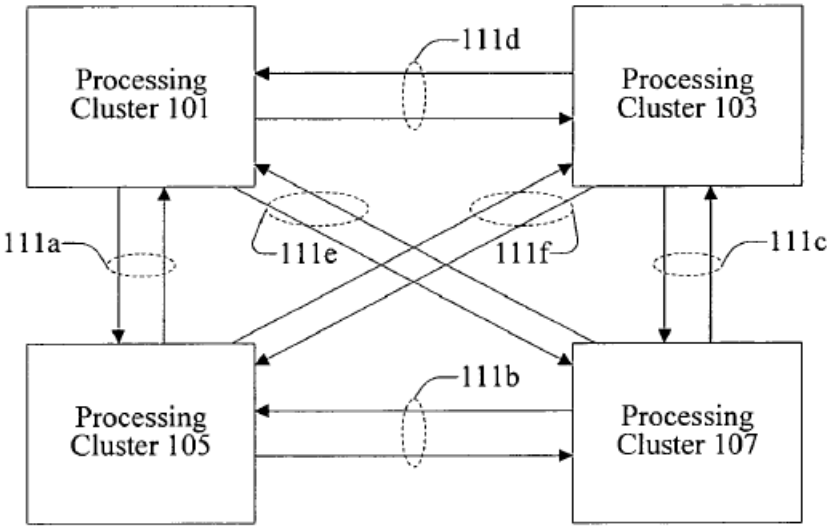

Figure 1A shows an example of a multiple cluster, multiple processor system described by the '121 patent. *Id.* at 6:10–12. Figure 1A includes four processing clusters: 101, 103, 105, and 107, each of which can, in turn, include multiple processors. *Id.* at 6:12–14. The clusters are connected through point-to-point links 111a–f. *Id.* at 6:14–16.

The '121 patent explains that cache coherency problems can arise in such a system, because it may contain multiple copies of the same data. *Id.* at 1:26–38. For example, if the caches of two different processors have a copy of the same data block and both processors "attempt to write new values into the data block at the same time," then the two caches may have different data values and the system may be "unable to determine what value to write through to system memory." *Id.* at 1:37–45. Solutions to cache coherency problems often involve an increase in communication traffic and a resulting decrease in efficiency. *Id.* at 1:23–26, 2:46–48. The '121 patent

discloses "techniques . . . for increasing data access efficiency in a multiple processor system," while also addressing cache coherency. *Id.* at 4:36–38.

The system disclosed by the '121 patent includes a probe filtering unit. *Id.* at 2:52–65. A probe is defined as "[a] mechanism for eliciting a response from a node to maintain cache coherency in a system." *Id.* at 5:45–47. As opposed to a traditional approach of broadcasting probes to all nodes, the probe filtering unit reduces traffic by intercepting the probes and transmitting them only to those nodes that require the information based on probe filtering information, i.e., "[a]ny criterion that can be used to reduce the number of clusters or nodes probed." *Id.* at 2:52–3:5, 14:50–52; *see id.* at 28:29–58, 29:43–46. The probe filtering unit may also accumulate responses from those nodes selected to receive the probes and respond to the node from which the probe originated. *Id.* at 3:5–8, 28:59–67, 29:46–51. Figure 18 of the '121 patent is reproduced below.

Figure 18

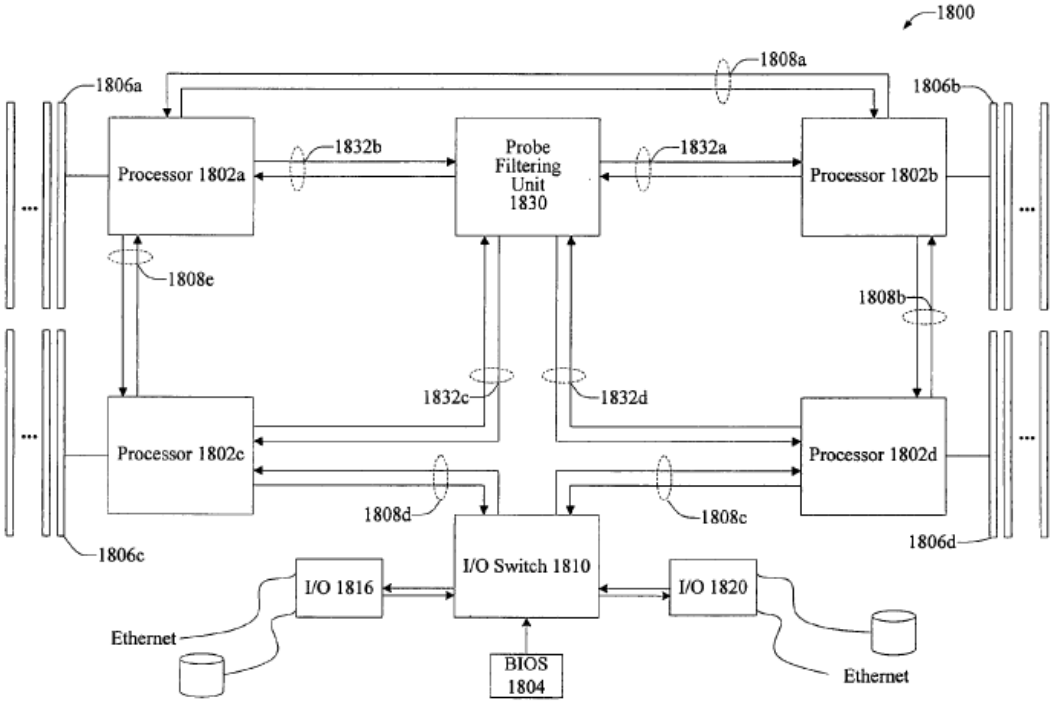

Figure 18 shows a multiple processor system with a probe filtering unit. *Id.* at 3:61–63, 26:58–27:20, Fig. 18. Specifically, Figure 18 depicts multiple processor system 1800 with processing nodes 1802a–d interconnected by point-to-point communication links 1808a–e. *Id.* at 26:58–27:1. System 1800 also includes probe filtering unit 1830 as well as I/O switch 1810, one or more Basic I/O systems ("BIOS") 1804, I/O adapters 1816, 1820, and a memory subsystem with memory banks 1806a–d. *Id.* at 3:61–63, 26:58–27:20, Fig. 18.

E. Challenged Claims

The challenged claims are all dependent and depend either directly or indirectly from independent claim 16. Claim 16 recites as follows:

> 16. A probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a

> first point-to-point architecture, each processing node having a cache memory associated therewith,
>
> the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories.

Ex. 1001, 32:7–15 (line break added).

II. ANALYSIS

A. Claim Construction

We interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). We presume a claim term carries its "ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question" at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (citation and quotations omitted). This presumption, however, is rebutted when the patentee acts as his own lexicographer by giving the term a particular meaning in the specification with "reasonable clarity, deliberateness, and precision." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner and Patent Owner proffer proposed constructions of various claim terms. In the Institution Decision, we construed several terms, including "states associated with selected ones of the cache memories." Inst. Dec. 8–13. After institution, the parties' briefing addressed only the construction of "states." We address below the parties' arguments regarding the construction of "states" and otherwise maintain our constructions from the Institution Decision.

1. "states"

Claim 16 recites "probe filtering information representative of *states* associated with selected ones of the cache memories." Before our Institution Decision, Patent Owner proposed a construction of the term "states." Prelim. Resp. 14–22. Patent Owner proposed that the term means "cache coherence protocol states associated with data blocks stored in selected ones of the cache memories" where a "cache coherence protocol state" means "the current state of a data block in a protocol used to maintain the coherency of caches, in which a data block can only be in one current state at a time, and in which the current state can transition to a different state upon one or more triggering events or conditions." Prelim. Resp. 14–15. In the Institution Decision, we did not adopt Patent Owner's proposed construction, but found that "the term is not limited to cache coherence protocol states and is broad enough to include the condition of presence—i.e., what is stored in cache memory." Inst. Dec. 10.

In its Response, Patent Owner continues to argue that "the appropriate construction of states is limited to cache coherence states, and does not include mere presence." Paper 17 ("PO Resp."), 2. Petitioner does not agree that the term should be so limited. Paper 25 ("Pet. Reply"), 2–5. In particular, Petitioner asserts that the broadest reasonable construction of the term "states" is not limited to cache coherency states (*id.* at 2–4) and is broad enough to encompass the condition of presence (*id.* at 4–5).

a. Cache Coherence States

The language of the challenged claims "states associated with selected ones of the cache memories" plainly links the "states" to "cache memories." In addition, in the challenged claims, the term "representative of states

associated with selected ones of the cache memories" modifies "*probe filtering information*" (Ex. 1001, 31:5–7, 32:14–15, 32:52–55 (emphasis added)), which the patent defines as "[a]ny criterion that can be used to reduce the number of clusters or nodes probed" (*id.* at 14:50–52). Thus, the recited "states" relate, not just to any aspect of the cache memory, but to the contents of that memory.

For the reasons discussed below, however, despite the arguments and evidence in Patent Owner's Response, we remain unpersuaded that the '121 patent supports limiting the broadest reasonable construction of "states" solely to cache coherence protocol states. A claim term will be interpreted more narrowly than its ordinary and customary meaning only under two circumstances: (1) the "patentee sets out a definition and acts as [its] own lexicographer," or (2) the "patentee disavows the full scope of a claim term either in the specification or during prosecution." *Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1330 (Fed. Cir. 2012). To disavow claim scope, the specification or prosecution history must "make[] clear that the invention does not include a particular feature" and the feature is then "deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification" or prosecution history, "might be considered broad enough to encompass the feature in question." *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001); *see Aventis*, 675 F.3d at 1330. To disavow claim scope, the patentee may "include[] in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." *Aventis*, 675 F.3d at 1330 (internal

quotations omitted). In this context, it is not sufficient "that the only embodiments, or all of the embodiments, contain a particular limitation." *Id.*

Here, beginning with the claims, the relevant language in the independent claims, "states associated with selected ones of the cache memories," expressly recites "states" alone—not cache coherency states, to which Patent Owner seeks to limit the term. Patent Owner's proposed construction seeks to add additional narrowing descriptive language to the term "states."

Moreover, the claims do not recite "cache coherence states" or "cache coherence protocol states." Dependent claim 3, which depends indirectly from claim 1, however, recites "a cache coherence controller" and "a cache coherence directory." Ex. 1001, 31:12–14. Similarly, claim 5, another claim that depends indirectly from claim 1, requires a "cache coherence controller." *Id.* at 31:24. Thus, had the patentees intended to limit "states," as recited in the independent claims of the '121 patent, to cache coherence states, they demonstratively could have done so by explicitly modifying the disputed term with "cache coherence"—but did not.[4]

[4] Patent Owner notes that our Institution Decision "preliminary determined that 'states' in the claims of the '121 Patent are not limited to 'cache coherence protocol states," "despite the fact that the Board determined that the term 'probe' in the claims should be construed as a 'mechanism for eliciting a response from a node to maintain cache coherency in a system.'" PO Resp. 2. We do not agree with Patent Owner's implication that our construction of "probe" conflicts in any way with our construction of "states." The two words recite different parts of the claimed invention. Moreover, the '121 patent expressly defines the term "probe" consistent with our construction (*see* Ex. 1001, 5:45–47; Inst. Dec. 8), but provides no definition for "state" or "states." If "states" were intended to be limited to cache coherency protocol states, the '121 patent could have provided an

Turning to the written description, we do not find persuasive Patent Owner's arguments that the remainder of the specification supports limiting "states" to cache coherency states. Rather, we agree with Petitioner that the '121 patent uses broad language in describing "states," explaining that "particular implementations may use a different set of states" and "[t]he techniques of the present invention can be used with a variety of different possible memory line states." Ex. 1001, 14:30–36; *see* Inst. Dec. 9–10; Reply 2–3.

Patent Owner asserts that the teachings of the '121 patent make it clear that its inventions are directed to the specific field of cache coherency and the term "state" has "a specific meaning in the field of cache coherency—a cache coherency state." PO Resp. 3–4; *see* Tr. 63:13–64:2. As to the field of the '121 patent, we find that it is directed, generally, to "data access and cache coherency in systems having multiple processors." *E.g.*, Ex. 1001, 2:39–47. The '121 patent explains that data access, and the disclosed invention, involve techniques for reducing probe traffic as well as cache coherency techniques. *See, e.g.*, *id.* at 1:21–27 ("The present invention relates to accessing data in a multiple processor system. More specifically, the present invention provides techniques for reducing memory transaction traffic in a multiple processor system. Data access in multiple processor systems can raise issues relating to cache coherency."); *see also, e.g.*, *id.* at [54] (title) ("Reducing Probe Traffic in Multiprocessor Systems");

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express definition for "state" or "states," as it does for "probes." Patent Owner does not provide evidence or reasoning persuading us that a person of ordinary skill in the art would find the express definition of "probes" as somehow limiting the term "states."

id. at 2:45–48 ("According to the present invention, various techniques are provided for reducing traffic relating to memory transactions in multiprocessor systems"). Although we agree with Patent Owner that the field of the '121 patent *includes* cache coherency, we are not persuaded that this fact, alone, limits the term "state" to "cache coherence states."

Patent Owner, in fact, concedes that the term "state" "may have many broad and different meanings . . . in the general field of computers." PO Resp. 4 (citing Ex. 2016 ¶ 15). Indeed, in our Institution Decision, we relied on a dictionary definition of "state" from the MICROSOFT COMPUTER DICTIONARY: "[t]he condition at a particular time of any of numerous elements of computing—a device, a communications channel, a network station, a program, a bit, or other element—used to report on or to control computer operations." Ex. 3001 (MICROSOFT COMPUTER DICTIONARY (5th ed. 2002)), 497–98. Patent Owner agrees that this dictionary is directed "to the entire field of computing." PO Resp. 4; Pet. Reply 4. And Patent Owner relies on this same dictionary when proposing a construction for another term in the '121 patent—"programmed." *See* IPR2015-00163, Paper 31, 15. Patent Owner has not persuaded us that a person of ordinary skill in the art would not base its definition of the term "states" on the field of computers generally, but instead would rely on a meaning specific to the "field of cache coherency."

To begin with, Patent Owner agrees that a person of ordinary skill in the art would have a degree in electrical engineering, computer engineering, or computer science and at least two years of experience in the design of multiprocessor systems. Ex. 2016 ¶ 8. Nothing in this definition points to a specific field, known as cache coherency, with its own terminology

displacing the more general terminology used by those in the field of computing.

Moreover, Patent Owner's position with respect to Koster belies Patent Owner's argument that, in the context of a patent describing data access and cache coherence in multiprocessor systems, the term "state," used on its own, necessarily refers to a cache coherency state. Koster, titled "snooping based cache-coherence filter for a point-to-point connected multiprocessing node," refers to his shadow tag memory as a "local state memory." Ex. 1005, [54], 6:11–12. Yet, Patent Owner takes the position that Koster's local state memory/shadow tag memory does not constitute "information representative of states associated with selected ones of the cache memories," as required by the disputed claim language. PO Resp. 13–16.[5] Essentially, Patent Owner attempts to argue in the claim construction section of its Response that a person of ordinary skill in the art would understand that, in the context of the '121 patent, the term "state" on its own, means "cache coherency state," where the actual cache coherency states encompass an open set of states used by any cache coherency protocol. *See*

[5] Indeed, in IPR2015-00163, Patent Owner argues that "the mere fact that Koster refers to his shadow tag memory as 'local state memory' does not mean that it contains 'information representative of states associated with selected ones of the cache memories' as that phrase is used in the '121 patent." IPR2015-00163, Paper 31, 23. Instead, according to Patent Owner, to determine the meaning of "local state memory," "it is necessary to consider what information Koster stores in the shadow tag memory and whether such information satisfies the properly construed limitation." *Id.* Patent Owner concludes that because tags only indicate the address of data, "despite Koster's reference to such tags as 'state' information," the tags "are not representative of cache coherency states as required by the properly construed limitations of the '121 patent." *Id.*

Prelim. Resp. 14–15; PO Resp. 1–7. However, when analyzing the prior art, which involves the same field as the '121 patent, Patent Owner takes the position that the same person of ordinary skill would understand the term "state" on its own does *not* mean cache coherency state. Patent Owner does not explain sufficiently why the term state would mean one thing in the '121 patent and another in Koster when both involve the same field of art.

Patent Owner relies, for its assertions, on a few excerpts of the '121 patent, which allegedly "demonstrate that the use of the term 'state' in the patent is directed to cache coherence protocol states." PO Resp. 5–7. For example, Patent Owner points to the following passage of the specification as "mak[ing] it clear that the relevant state is a cache coherence protocol state" (PO Resp. 5–6):

> It should be noted that *a coherence protocol* can contain several types of messages. In one example, a coherence protocol includes four types of messages; data or cache access requests, probes, responses, or probe responses, and data packets. Data or cache access requests usually target the home node memory controller. Probes are used to query each cache in the system. The probe packet can carry information that allows the caches to properly *transition the cache state for a specified line*.

Ex. 1001, 9:21–29 (emphases added). Similarly, Patent Owner points to the specification's statement that "[b]y using a *coherence directory*, global *memory line state information* (with respect to each cluster) can be maintained and accessed by a memory controller or a cache coherence controller in a particular cluster," asserting that this statement only makes sense if the coherence directory concerns solely cache coherence states. PO Resp. 6 (quoting Ex. 1001, 13:4–7).

We are not persuaded that these passages of the '121 patent limit the term "states" as asserted by Patent Owner. Neither of the passages relied upon by Patent Owner actually uses the term "state" as recited in the challenged claims. Instead, the first passage Patent Owner relies on for a narrower construction uses the term "*cache state*" and the second uses the term "*global memory line state information*." Thus, even if the passages describe a concept narrower than "states associated with selected ones of the cache memories," as recited in the challenged claims, this difference can be attributed to the fact that different terms are used. More importantly, these passages do not expressly disclaim or disavow the broader scope of the claim language, particularly given the expansive language used elsewhere in the specification allowing states to include "a variety of different possible memory line states." Ex. 1001, 14:30–36.

Patent Owner also points to Figures 7 and 8 of the '121 Patent as allegedly "strongly illustrative that the '121 patent uses 'state' to mean cache coherence protocol states." PO Resp. 7. According to Patent Owner, the specification equates the word state with cache coherence states by stating "*the coherence directory 701* [of Figure 7] *includes state information 713*" and by stating "[i]n some embodiments, the memory line states are modified, owned, shared, and invalid." *Id.* (quoting Ex. 1001, 13:55–59) (emphases added by Patent Owner). In other words, Patent Owner argues that because Figure 7 shows a column labeled "state," and describes this column as including in some embodiments the states used in common cache coherence protocols such as MOESI and MOSI, the term "state" must be equivalent to cache coherence protocol. *See* Tr. 77:20–78:18.

Figures 7 and 8, however, also are not persuasive as defining the term state because they are clearly described as exemplary embodiments. *See, e.g.*, Ex. 1001, 3:15–18; 4:11–35 ("[I]t is not intended to limit the invention to the described embodiments. On the contrary, it is intended to cover alternatives, modification, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims."); 13:44–59 (describing Figure 7 using the term "example" or "embodiment" no less than five times); 14:48–50; 30:57–64 ("[T]he scope of the invention should not be limited by reference to such advantages, aspects, and objects. Rather, the scope of the invention should be determined with reference to the appended claims."). We are not persuaded that Figure 7 shows anything more than what it purports to show—one example with a column labeled "state," that may refer to "memory line states" of "modified, owned, shared, and invalid." Again, nothing in this example expressly disclaims or disavows the broad claim language, particularly in light of other statements in the specification allowing states to include "a variety of different possible memory line states." Ex. 1001, 14:30–36.

Patent Owner further argues that the '121 patent distinguishes between state information and tags in certain examples disclosed therein. PO Resp. 14–15. We also find this information unpersuasive, as Patent Owner's citation of portions of the '121 patent that discuss both tags and state information does not persuade us that tags and state information are mutually exclusive, as these portions of the '121 patent are examples. *See id.* 14–15 (citing Ex. 1001, 7:67–8:4; 13:44–14:47; Fig. 7). Patent Owner does not identify any portion of the '121 patent that clearly disavows tags as mutually exclusive from state information.

Patent Owner also proffers extrinsic evidence to support its proposed construction of the term "state." Extrinsic evidence is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (citations omitted) (internal quotations omitted). For example, Patent Owner points to "one of the treatises on cache coherency," Daniel J. Sorin et al., A PRIMER ON MEMORY CONSISTENCY AND CACHE COHERENCE (2011) (Ex. 2010, "Sorin"), as equating the term "state" with cache coherence protocol states. PO Resp. 4 (citing Ex. 2010, 88–89; Ex. 2016 ¶ 15). We do not find this evidence persuasive. Evidence of the use of shorthand within one section in one publication does not indicate that that same shorthand will be recognized, by a person of ordinary skill, as necessarily having the same meaning in other contexts. Dr. Oklobdzija's testimony referring to this treatise does not persuade us to the contrary. *See* Ex. 2016 ¶ 15. Indeed, Dr. Sorin, as one of the authors of Sorin, testifies that Sorin does not use the term "state" as meaning only a cache coherence protocol state. Ex. 1015 ¶ 19; Pet. Reply 4. To the contrary, Dr. Sorin testifies that a person of ordinary skill in the art would not understand the term "states" in the disputed claim language as limited to cache coherency states. Ex. 1015 ¶¶ 17–18; Pet. Reply 4.

Patent Owner also points to another article, where the authors—three of whom are the authors of Sorin, discussed above—state that "[a] processor's access to a cache block is determined by the state of that block in its cache, and this state is *generally* one of the five MOESI (Modified, Owned, Exclusive, Shared, Invalid) states." PO Resp. 5 (citing Ex. 2003, 1) (emphasis added); *see* Reply 4. Again, this isolated use of a shorthand of

"states" in a publication, with several of the same authors as the other cited publication, does not persuade us that this shorthand is universally accepted to have a particular meaning whenever a particular type of software is being discussed. Moreover, the use of the term "generally" in this statement shows that it is not limiting the term "states" to cache coherency states, or more specifically, MOESI states. Therefore, we are not persuaded that Patent Owner's extrinsic evidence regarding ordinary meaning overcomes the intrinsic record of this case. *See Phillips*, 415 F.3d at 1318 ("[A] court should discount any expert testimony that is clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent.") (citations and internal quotations omitted).

In summary, we conclude that the recited "states" relate to the contents of cache memory, but are not limited solely to cache coherence protocol states.

b. Presence

Even if we did agree with Patent Owner's assertion that the term "states" is limited to cache coherence states, we find unpersuasive Patent Owner's arguments relating to presence.

The '121 patent directly touches on the subject of presence when discussing cache coherency states. For example, when describing certain embodiments associated with Figure 7, including cache coherency memory line states of "modified, owned, shared, and invalid," the '121 patent declares "[i]n the invalid state, a memory line is not currently available in cache associated with any remote cluster." Ex. 1001, 13:58–61. Patent Owner argues that, contrary to the ordinary meaning of these words, the

disclosed "invalid" state does not refer only to a lack of presence, but instead means that the memory line "can be present but invalid," because it cannot be rel[ied] on," or is "not available to use because it is invalid." Paper 34 ("Tr."), 80:20–81:13. Patent Owner, however, does not explain sufficiently why a person of ordinary skill in the art would understand the statement in this way, as opposed to the plain meaning of the "currently available" language in the specification. *See* Tr. 80:13–84:8.

Instead, Patent Owner points to other portions of the specification, asserting that the '121 patent teaches "'state' provides additional information about 'a particular cached line' that is known to already be 'somewhere' (i.e. it is already known to be present).'" PO Resp. 8. In particular, Patent Owner bases this assertion on a passage of the '121 patent stating "because the cache coherence directory provides information about ***where [i.e., in which cluster the line is present] memory lines are cached as well as their states,*** probes only need be directed toward the clusters in ***which the requested memory line is cached"*** and "***[t]he state of a particular cached line*** will determine what type of probe is generated." *Id.* at 7–8 (quoting Ex. 1001, 19:36–43 (emphases added by Patent Owner)). According to Patent Owner, this passage "plainly indicates" that the state of a memory line is different from where it is located and that "state" only exists for a cached line. *Id.* at 8.

Patent Owner also points to the '121 patent's discussion of an "occupancy vector" as demonstrating that the patent does not consider presence to be a state. PO Resp. 8–9. According to Patent Owner, the '121 patent's statement that "[a]ny mechanism for tracking what clusters hold a copy of the relevant memory line in cache [i.e., in which clusters the

memory line is present] is referred to herein as an occupancy vector," and its treatment of the "occupancy vector" different than the "state" filed in Figure 7, indicate that the '121 patent understands presence and "state" to be different. *Id.* (citing Ex. 1001, 13:55–57, 13:67–14:2, Fig. 7); Ex. 2016 ¶ 24.

We are not persuaded that the '121 patent limits cache coherency states as argued by Patent Owner. Intrinsic and extrinsic evidence contradicts Patent Owner's and Dr. Oklobdzija's suggestion that a cache coherency state necessarily needs to indicate more than whether a memory line is present in cache memory. As noted above, the '121 patent itself discloses that "[i]n the invalid state, a memory line is *not currently available* in cache associated with any remote cluster." Ex. 1001, 13:60–61 (emphasis added). As also noted above, the plain meaning of this statement is that the "invalid" cache coherence state indicates that a memory line is not present in cache memory, and Patent Owner has not explained persuasively its assertion to the contrary. *See* Tr. 80:13–84:8.

Moreover, none of the passages of the '121 patent cited by Patent Owner clearly limits the scope of "states." *See, e.g.*, Ex. 1001, 13:44–55 (stating multiple times that the embodiment depicted in Figure 7, with an occupancy vector, is an "example"). Regarding Patent Owner's citation of discussions in the '121 patent of states that provide information beyond whether specific data is present in a cache, we again note that the '121 patent expressly discloses that its invention encompasses use of states other than the examples discussed therein. *Id.* at 14:30–36.

Indeed, extrinsic evidence cited by Patent Owner and Dr. Oklobdzija explains that not present is a cache coherency state and that one meaning of the invalid cache coherency state is that the block is not present or available

in the cache. For example, Patent Owner and Dr. Oklobdzija cite Sorin and a book titled "Parallel Computer Architecture" and authored by David E. Culler et al. (Ex. 2011, "Culler"). Culler explains that in a Dragon protocol it discusses, "there is no explicit invalid (I) state" but that "if a block is not present in a cache at all, it can be imagined in a special invalid or not-present state." Ex. 2011, 302. Later, Culler discusses using the state "NP (not present)" in connection with the "MESI protocol." *Id.* at 307–310. Similarly, Sorin explains the cache coherence state of "I(nvalid)" as follows:

> The block is invalid. The cache either does not contain the block or it contains a potentially stale copy that it may not read or write. In this primer, we do not distinguish between these two situations, although sometimes the former situation may be denoted as the "Not Present" state.

Ex. 2010, 89. At his deposition, Dr. Oklobdzija testified that Sorin is a "competent" and Culler is a "very highly regarded" source regarding cache coherency. Ex. 1016, 38:3–39:11.

Thus, the '121 patent and the extrinsic evidence of record demonstrate that not present is a cache coherency state and that one meaning of the invalid cache coherency state is that the block is not present or available in the cache. Accordingly, we conclude that even if "state" requires a cache coherency state, it encompasses the cache coherency states of invalid, meaning the block is not present or available in the cache, and not present.

B. Obviousness of Claim 24 over Koster

1. Overview of Koster

Koster discloses a "snooping-based cache-coherence filter for a point-to-point connected multiprocessing node." Ex. 1005, [54]. In Koster, when a microprocessor requests data that is not available in its local cache, it sends

a request for that data to a snoop filter. *Id.* at abs. The snoop filter stores a copy of the tags of data stored in the local cache memories of each of the microprocessors. *Id.* When the snoop filter receives a request for data, it can determine which microprocessors have copies of the requested data and relay the data request only to those microprocessors. *Id.*

Figure 9 of Koster is reproduced below.

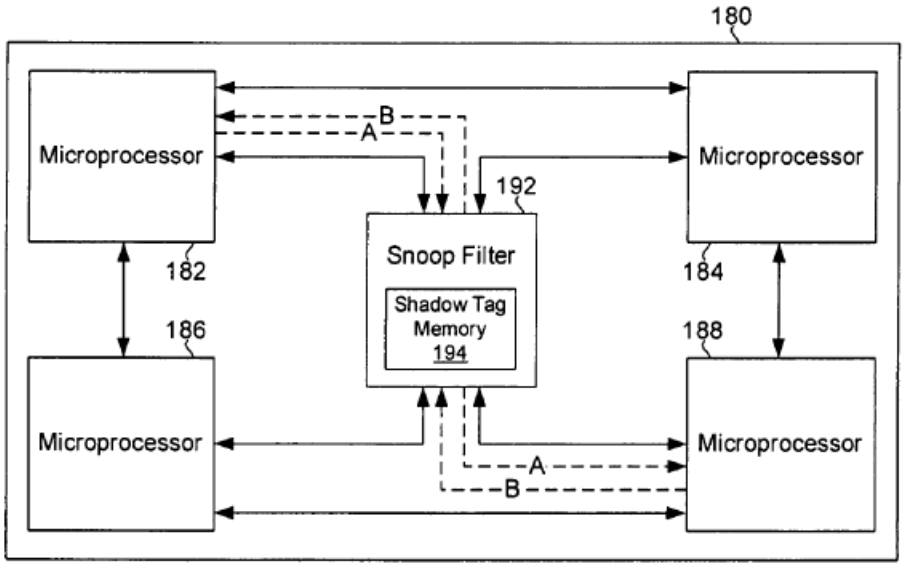

FIG. 9

Figure 9 shows an exemplary flow of messages in multiprocessing node 180 with four microprocessors 182, 184, 186, and 188 and snoop filter 192. *Id.* at 6:61–67. Microprocessor 182 requests data by issuing "broadcast A," which is routed to snoop filter 192. *Id.* at 6:67–7:3. Snoop filter 192 has shadow tag memory 194 that stores copies of the tags of data stored in the local cache memories of microprocessors 182, 184, 186, and 188. *Id.* at 7:3–6; 6:9–17. Upon receipt of broadcast A, snoop filter 192 determines whether any of the other three microprocessors have a copy of the requested data. *Id.* In Figure 9, snoop filter 192 determines that microprocessor 188 has a copy

of the requested data and forwards broadcast A to microprocessor 188. *Id.* at 7:6–10. Next, microprocessor 188 sends "response B (having a copy of the requested data)" to snoop filter 192, which, in turn, forwards response B back to requesting microprocessor 182. *Id.* at 7:10–14.

Koster notes that "[b]y forwarding response B through the snoop filter 192, the snoop filter 192 is able to update its shadow tag memory 194." *Id.* at 7:15–16. Koster, however, also discloses embodiments in which "a response from a microprocessor may be routed directly back to a requesting microprocessor." *Id.* at 7:17–19.

2. Discussion

Claim 24 recites "[a] set of semiconductor processing masks representative of at least a portion of the probe filtering unit of claim 16." Petitioner argues that Koster discloses all of the limitations recited in claim 16. Pet. 19–20. Petitioner argues that Koster's microprocessors correspond to the claimed "processing nodes" and that Koster's snoop filter corresponds to the claimed "probe filtering unit." *Id.* Petitioner argues that the snoop filter's shadow tag memory corresponds to the claimed "probe filtering information." *Id.* at 20. Petitioner also argues that the shadow tag memory "stores the tags of data stored in the local cache memories (*i.e.*, 'representative of states associated with selected ones of the cache memories')." *Id.* Regarding the limitation added by claim 24, Petitioner asserts that "[a]t the time Koster was filed (July 13, 2004), integrated circuits were necessarily created with a set of semiconductor masks." *Id.* at 25. Based on this, Petitioner concludes that it would have been obvious "to use a set of semiconductor processing masks representative of at least a portion of

the 'snoop filter' disclosed in Koster to create an integrated circuit implementing the 'snoop filter' of Koster." *Id.* at 25.

Patent Owner argues that Koster's shadow tag memory 164 and its tags do not teach the claim language "probe filtering information representative of states associated with selected ones of the cache memories," recited in claim 16. PO Resp. 13–16. Patent Owner rests this contention on its assertion that the claim language requires cache coherency states, in combination with an argument that "Koster's tags . . . are not representative of cache coherency states." *Id.* at 13. Patent Owner asserts that "a tag identifies a memory address but does not provide any information regarding the state of that memory address." *Id.* at 14. As noted above, Patent Owner contends that the '121 patent distinguishes between tags and state information in certain examples disclosed therein. *Id.* at 14–15. Patent Owner states that "[i]n its Decision on Institution, the Board found that Koster's tags indicate 'where specific data is cached (i.e., the presence of data in specific locations)' and that the 'states' limitation is broad enough to include the 'condition of presence.'" *Id.* at 15. Patent Owner argues that "[h]owever, for the reasons explained in the claim construction section above, the condition of presence is not a cache coherency state and therefore cannot satisfy this limitation." *Id.*

Petitioner responds that Patent Owner's arguments rest on an incorrect claim construction. Pet. Reply 5–6. Petitioner asserts that the proper construction of the disputed claim language includes the condition of presence, and that Koster's "tags indicate where specific data is cached (i.e., the presence of data in specific locations)." *Id.* Petitioner also asserts that Dr. Oklobdzija concedes that under the claim construction we set forth in the

Institution Decision, Koster teaches "states," as recited in claim 1. *Id.* at 6 (citing Ex. 1016, 186:17–24). Petitioner argues that "[t]herefore, Koster discloses the claim limitation of 'probe filtering information representative of states associated with selected ones of the cache memories.'" *Id.*

We have reviewed the evidence and arguments presented in the Petition, Patent Owner's Response, and Petitioner's Reply. Based on that review, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that all of the limitations of claim 24 are taught by, or rendered obvious in view of the teachings of Koster, and that claim 24, considered as a whole, would have been obvious over Koster. Pet. 19–20, 25; PO Resp. 1–16; Pet. Reply 1–8. We find Petitioner's citations and arguments persuasive, and we adopt them as the basis for our decision. Pet. 19–20, 25; Pet. Reply 1–8.

We are persuaded that Koster's tags and shadow tag memory teach the claim language "probe filtering information representative of states associated with selected ones of the cache memories." For the reasons explained in Section II.A.1.a *supra*, we do not agree with Patent Owner's argument that the broadest reasonable interpretation of this claim language requires cache coherency states. Additionally, as discussed in Section II.A.1.a *supra*, Patent Owner does not persuade us that the examples of tags and state information discussed in the '121 patent constitute a clear disavowal of tags as necessarily excluded from state information. *See* PO Resp. 14–15 (citing Ex. 1001, 7:67–8:4; 13:44–14:47; Fig. 7). Furthermore, Patent Owner's argument that tags are not state information fails to recognize that the claimed probe filtering information does not have to be states, it need only be "*representative* of states associated with selected ones

of the cache memories." Ex. 1001, 31:5–6 (emphasis added); *see* Tr. 74:11–15, 77:2–9.

Patent Owner does not dispute that Koster's shadow tag memory and its tags indicate where specific data is cached. *See* PO Resp. 15; Ex. 1001, at [57], 6:9–38, 6:61–7:16, 7:25–33, Figs. 9, 10; Pet. 20; Pet. Reply 5–6; Ex. 1013 ¶ 19; Ex. 1015 ¶ 20; Ex. 1016, 186:17–24. Additionally, Koster uses the information provided by the shadow tag memory and its tags in controlling where to send data requests. *See, e.g.*, Ex. 1001, 6:18–32; Pet. 20; Ex. 1013 ¶ 19. Accordingly, we are persuaded that Koster's shadow tag memory and its tags are representative of whether selected ones of the cache memories contain specific data, which is representative of the states of those cache memories. *See, e.g.*, Ex. 3001, 497–498 (setting forth definition of "state" as "[t]he condition at a particular time of any of numerous elements of computing—a device, a communication channel, a network station, a program, a bit, or other element—used to report on or to control computer operations."); Pet. 20; Pet. Reply 1–8; Ex. 1013 ¶ 19; Ex. 1015 ¶ 20; Ex. 1016, 186:17–24.

Additionally, even if the claim language "states associated with selected ones of the cache memories" did refer to cache coherency states, we are persuaded that Koster teaches the "probe filtering unit" recited in claim 16. As explained in Section II.A.1.b *supra*, even if we agreed with Patent Owner that the term "state" required a cache coherency state, the evidence of record demonstrates that it encompasses the cache coherency states of invalid, meaning the block is not present or available in the cache, and not present.

Given this, we find that Koster's shadow tag memory constitutes probe filtering information representative of cache coherency states associated with selected ones of its cache memories. As noted above, Patent Owner does not dispute that the tags in Koster's shadow tag memory indicate where specific data is cached. *See* PO Resp. 15; Ex. 1001, [57], 6:9–38, 6:61–7:16, 7:25–33, Figs. 9, 10; Pet. 20; Pet. Reply 5–6; Ex. 1013 ¶ 19; Ex. 1015 ¶ 20; Ex. 1016, 186:17–24; Ex. 2016 ¶ 47–48. By indicating where specific data is cached, Koster's tags and shadow tag memory are representative of which cache memories do not contain a copy of data. This is illustrated, for example, in Koster's disclosure that:

> By having the shadow tag memory 164, the snoop filter 162 forwards a received broadcast for requested data (by one of the microprocessors 152, 154, 156, 158 or from another multiprocessing node (not shown)) to a particular one of the microprocessors 152, 154, 156, 158 only if its shadow tag memory 164 indicates that the particular microprocessor has a copy of the requested data. Otherwise, if the snoop filter 162 determines that none of the microprocessors 152, 154, 156, 158 has a copy of the requested data, the snoop filter 162 is configured to cancel any subsequent relays of the broadcast to the microprocessors 152, 154, 156, 158, and instead, sends a message back to the requesting microprocessor (or multiprocessing node (not shown)) indicating that none of the other microprocessors (or none of the microprocessors) in the multiprocessing node 150 has a copy of the requested data.

Ex. 1005, 6:18–32. Thus, because Koster's tags and shadow tag memory are representative of which cache memories do not contain a copy of data, they are representative of the invalid cache coherency state, meaning that the block is not present or available in the cache, and they are representative of

the not present cache coherency state for those cache memories lacking a copy of a data line.

In sum, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claim 24 would have been obvious over Koster.

C. Obviousness of Claims 19–23 over Koster and Kuskin

1. Overview of Kuskin

Kuskin discusses the "FLASH multiprocessor." Ex. 1006, 302. Kuskin states that the FLASH multiprocessor supports "cache-coherent shared memory and high-performance message passing." *Id.* Figure 2.1 of Kuskin is reproduced below.

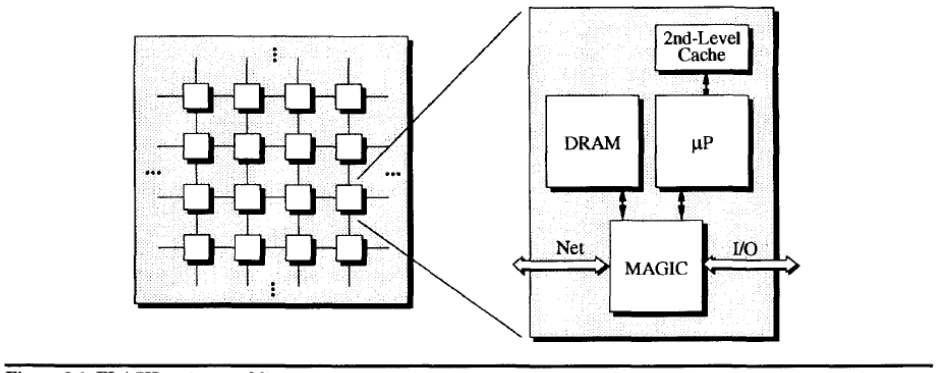

Figure 2.1. FLASH system architecture.

Figure 2.1 shows the FLASH system architecture. *Id.* at 303. FLASH "is a single-address-space machine" composed of a large number of identical processing nodes connected by an interconnection network. *Id.* Each node includes a microprocessor with its caches, a portion of the distributed main memory of the machine, and a "MAGIC node controller chip." *Id.*

Kuskin discloses that "[t]he MAGIC chip forms the heart of the node, integrating the memory controller, I/O controller, network interface, and a programmable protocol processor," which "allows for low hardware

overhead while supporting both cache-coherence and message-passing protocols in a scalable and cohesive fashion." *Id.* Kuskin states that "MAGIC includes a programmable protocol processor for flexibility." *Id.*

In addition to providing an overview of the FLASH architecture, Kuskin discusses FLASH protocols. *Id.* at 304–307. The FLASH protocols discussed include a cache-coherence protocol and a message-passing protocol. *Id.*

Kuskin also discusses a system-level simulator. *Id.* at 310–311. Kuskin discloses having "up and running" a detailed system-level simulator "written in C++ as a multithreaded memory simulator." *Id.* at 311. Kuskin states "[w]e have coded a C version of the block-transfer protocol in our system-level simulator and, for performance studies, have hand-coded some of the critical handlers in PP assembly language." *Id.* at 310. Kuskin also discloses "[l]atency and occupancy numbers . . . derived from our system-level simulator and our Verilog code" (*id.* at 302), further stating that "[o]n the hardware design front we are busily coding the Verilog description of the MAGIC chip" (*id.* at 311).

2. Discussion

Claim 19 recites "[a]t least one computer-readable medium having data structures stored therein representative of the probe filtering unit of claim 16." Each of claims 20–23 depends from claim 19 and recites additional limitations related to the computer-readable medium.

Petitioner asserts that Koster discloses all limitations of claim 16. Pet. 19–20. Petitioner asserts that the additional limitations recited in claims 19–23 are disclosed by Kuskin, and that Koster and Kuskin render claims 19–23 obvious. *Id.* at 26–29. Petitioner argues that it would have

been obvious to combine the teachings of Kuskin with those of Koster. *Id.* at 25–26. Petitioner notes that both references disclose solutions for cache coherency problems. *Id.* at 25. Petitioner asserts that Koster's system uses a plurality of microprocessors that are integrated circuits, whereas Kuskin discloses a "programmable protocol for flexibility" in its cache coherency architecture. *Id.* at 25–26. Citing Dr. Sorin's testimony, Petitioner further asserts that "it was known to those of ordinary skill in the art that implementing cache coherence using a programmable microprocessor afforded more flexibility than, for example, an ASIC." *Id.* at 26 (citing Ex. 1013 ¶ 22).

With respect to claim 19's recitation of "[a]t least one computer-readable medium having data structures stored therein representative of the probe filtering unit," Petitioner asserts that Kuskin discloses a computer-readable medium with data structures representative of a cache coherence controller. *Id.* Petitioner cites Kuskin's discussion of its cache coherence protocol and Kuskin's disclosure that: "The MAGIC chip forms the heart of the node, integrating the memory controller . . . and a programmable protocol processor. This integration allows for low hardware overhead while supporting [] cache-coherence . . . protocols in a scalable and cohesive fashion." *Id.* (citing Ex. 1006, 303–04).

Regarding claim 20's recitation that "the data structures comprise a simulatable representation of the probe filtering unit," Petitioner asserts that Kuskin discloses a simulatable representation of a cache coherence controller. *Id.* at 27. In support of this assertion, Petitioner argues that the authors of Kuskin actually simulated the system discussed in Kuskin. *Id.* (citing Ex. 1006, 310–11).

Claim 21 recites "[t]he at least one computer-readable medium of claim 20 wherein the simulatable representation comprises a netlist." Regarding this limitation, Petitioner argues that "Kuskin teaches building and simulating a cache coherency controller using hardware description language for a tangible chip," citing portions of Kuskin that discuss using Verilog. Pet. 27 (citing Ex. 1006, 302, 311). Citing page 58 of Exhibit 1012 and Dr. Sorin's testimony, Petitioner asserts that "[u]se of a Verilog description to create a tangible chip necessarily requires the creation of a simulatable representation comprising a netlist." *Id.* (citing Ex. 1012, 58; Ex. 1013 ¶ 25).

Regarding claim 22's recitation that "the data structures comprise a code description of the probe filtering unit" and claim 23's recitation that "the code description corresponds to a hardware description language," Petitioner asserts that Kuskin teaches implementing its cache coherency controller in Verilog. *Id.* at 28. Citing Dr. Sorin's testimony, Petitioner asserts that Verilog is a hardware description language. *Id.* at 28–29 (citing Ex. 1013 ¶ 24). Petitioner argues that "it would have been obvious to a person of ordinary skill in the art to implement the 'snoop filter' of Koster using a hardware description language (as shown in Kuskin) because that was the only commonly used method in the industry for programming hardware." *Id.* (citing Ex. 1013 ¶ 26). Petitioner concludes that claims 22 and 23 would have been obvious in view of Koster and Kuskin. *Id.*

We have reviewed the evidence and arguments presented in the Petition, Patent Owner's Response, and Petitioner's Reply. Based on that review, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that all of the limitations of each of claims 19–23 are taught

by, or rendered obvious in view of the teachings of Koster and Kuskin, and that each of these claims, considered as a whole, would have been obvious over the combination of Koster and Kuskin. Pet. 19–20, 25–29; PO Resp. 1–16; Pet. Reply 1–8. With respect to claims 19–23, we find Petitioner's citations and arguments persuasive, and we adopt them as the basis for our decision. Pet. 19–20, 25–28; Pet. Reply 1–8.

Patent Owner argues that "[a]s discussed in Section III.A.1 above, Koster fails to disclose the 'probe filtering information representative of states' limitation of claim 16. Since claims 19-23 depend from claim 16, Koster cannot disclose this limitation of dependent claims 19-23." PO Resp. 16. For the reasons discussed in Section II.B.2 *supra*, we find this argument unpersuasive.

In sum, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 19–23 would have been obvious over Koster and Kuskin.

D. Patent Owner's Motion to Amend Claims

Because we determine that claims 19–24 are unpatentable, we turn to Patent Owner's contingent request to enter proposed substitute claims 29–34.[6] Paper 18 ("Mot."), 1. Patent Owner states that each of the proposed substitute claims, 29–34, were drafted "by first converting the respective

[6] Patent Owner's Motion to Amend refers to "[p]roposed substitute claims 19-34," but then explains that "Patent Owner's claim appendix begins numbering the substitute claims at claim 29, and concludes at claim 34, and leaves claims 26-28 blank." Mot. 1, n.1. Accordingly, we interpret the reference to claims "[p]roposed substitute claims 19-34" as a typographical error.

original claim 19–24 to independent form, and then adding the same proposed new limitations." *Id.* at 2. The new limitations are as follows:

> wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface

Id.

Claim 29 is illustrative of the proposed substitute claims and is reproduced below. Language added to convert claim 19 into independent form is underlined and the proposed new limitations are underlined and italicized.

> 29. (Proposed Conditional Substitute for Challenged Claim 19) At least one computer-readable medium having data structures stored therein representative of a probe filtering unit ~~of claim 16~~ for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, *wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface*.

Ex. 2018, 1.

As the moving party, Patent Owner bears the burden of proof to establish that it is entitled to the relief requested. *See* 37 C.F.R. § 42.20(c). Entry of proposed amendments is not automatic, but occurs only upon the patent owner having met the requirements of 37 C.F.R. § 42.121 and demonstrating, by a preponderance of the evidence, the patentability of the proposed substitute claims. *Nike, Inc. v. Adidas AG*, No. 2015-1719, 2016 WL 537609, at *3–*5 (Fed. Cir. Feb. 11, 2016) ("[T]he Board did not err by placing the burden on [Patent Owner] to establish patentability over the prior art of [Patent Owner]'s proposed substitute claims."); *see Idle Free Systems, Inc. v. Bergstrom, Inc.*, IPR2012-00027, slip op. at 7–8 (PTAB June 11, 2013) (Paper 26, "*Idle Free*") (informative). For the reasons explained below, we conclude that Patent Owner has not met its burden with respect to proposed substitute claims 29–34.

A motion to amend claims must clearly identify the support for the proposed substitute claims. In particular, 37 C.F.R. § 42.121(b)(1) requires the patent owner to set forth the support in the original disclosure of the patent for each proposed substitute claim. Similarly, under 37 C.F.R. § 42.121(b)(2), the patent owner must set forth the support in an earlier-filed disclosure for each claim for which benefit of the filing date of the earlier filed disclosure is sought. 35 U.S.C. § 112 ¶ 1,[7] sets forth an enablement requirement, providing that the specification shall describe "the manner and process of making and using [the invention], in such full, clear, concise, and

[7] Section 4(c) of the AIA re-designated 35 U.S.C. § 112 ¶ 1, as 35 U.S.C. § 112(a). Because the '121 patent has an effective filing date before September 16, 2012 (effective date), we will refer to the pre-AIA version of 35 U.S.C. § 112.

exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the [invention]."[8] *Automotive Techs. Int'l v. BMW of North Am., Inc.*, 501 F.3d 1274, 1282 (Fed. Cir. 2007). This requirement is satisfied when "one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *Id.* (internal quotation marks omitted).

Patent Owner asserts that support for the proposed substitute claims, including each of the newly proposed limitations, is found in the originally filed application leading to the '121 patent, U.S. Patent Application No. 10/966,161 (Ex. 2020, "the '161 Application"), as well as priority document U.S. Patent Application No. 10/288,347 (Ex. 2006,[9] "the '347 Application"). Mot. 3–10.

Specifically, Patent Owner asserts that the new limitation "wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface" ("the protocol interface limitation") is

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[8] 35 U.S.C. § 316(d)(3) provides that an amendment under 35 U.S.C. § 316(d) may not enlarge the scope of the claims of the patent or introduce new matter. Similar to 35 U.S.C. § 132's prohibition on adding new matter to claim amendments, the prohibition of new matter in proposed substitute claims places a burden on the moving party to show those claims adhere to the requirements of 35 U.S.C. § 112, ¶ 1. *See Ariad Pharms., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1348 (Fed. Cir. 2010) (en banc) ("[P]rohibiting adding new matter to the claims has properly been held enforceable under § 112, first paragraph.").

[9] Exhibit 2006 contains two sets of page numbers. The first set of page numbers appears in the upper right corner of each page and starts with "1" on the first page of the exhibit. The second set of page numbers appears in the lower middle portion of each page and starts with "1" on the second page of the exhibit. We cite to the first set of page numbers.

supported by both the ’161 Application and the ’347 Application. *Id.* at 9–10. Patent Owner points to Figure 3, reproduced below, which is substantively identical in both the ’161 and ’347 Applications and in the ’121 patent. *Id.* at 9.

Figure 3

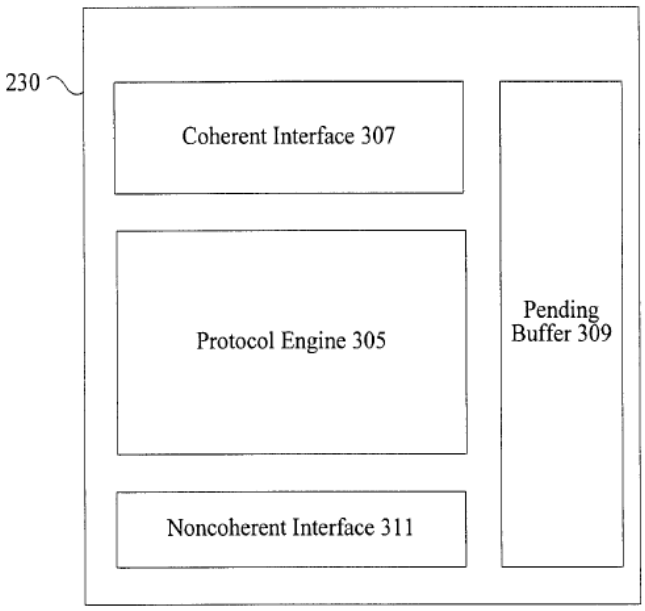

Figure 3 shows an example interconnection controller 230, including protocol engine 305 “configured to handle packets such as probes and requests received from processors in various clusters of a multiprocessor system.” Ex. 2020, 12:28–31; Ex. 2006, 12:20–23; Ex. 1001, 7:53–58. Interconnection controller 230 also includes “Coherent Interface 307” and “Noncoherent Interface 311.” Ex. 2020, 13:11–15; Ex. 2006, 13:4–10; Ex. 1001, 8:5–11. In addition, Patent Owner relies on several lines of text associated with Figure 3 in the ’161 and ’347 Applications. Mot. 9–10; Ex. 2020, 12:20–23, 13:11–17; Ex. 2006, 12:12–15, 13:4–10; Ex. 1001, 7:44–48, 8:5–14.

Petitioner argues that the disclosure relied upon by Patent Owner does not properly enable the protocol interface limitation, but instead "simply illustrates the broad proposition that the cache coherence controller 'can also include other interfaces such as a non-coherent protocol interface 311 for communicating with I/O devices.'" Paper 26 ("Opp. Mot."), 5 (quoting Ex. 1001, 8:8–11). According to Petitioner, the disclosure "identifies where the non-coherent protocol interface is located, but provides no details for how it is implemented." *Id.*

We agree with Petitioner that Patent Owner has not met its burden to show that its proposed substitute claims meet the enablement requirement of § 112 ¶ 1. More specifically, we agree that Patent Owner has not shown that the specifications of the '161 or '347 Applications enable the protocol interface limitation recited by each of the proposed substitute claims.

Considering first the specification of the '161 and '347 Applications, although Patent Owner points to several lines and one figure as describing the limitation, these disclosures simply identify the existence of a cache coherency controller with both a coherent and non-coherent protocol interface without providing any detail of how such a cache coherency controller would be implemented. *See* Ex. 2020, 12:20–23, 13:11–17; Ex. 2006, 12:12–15, 13:4–10; Ex. 1001, 7:44–48, 8:5–14. Figure 3 represents a concept of a cache coherence interface with two interfaces—but lacks any details that would show one skilled in the art how to make or use a cache coherence interface with two interfaces. *See* Ex. 2020, Fig. 3; Ex. 2006, Fig. 3. The specification describes Figure 3 as a "diagrammatic representation" of a cache coherence controller, and does not purport to show details of how the two interfaces would be implemented together in

such a controller. *See* Ex. 2020, 5:17, 12:28–13:21, Ex. 2006, 6:16, 12:20–13:14; Ex. 1001, 3:32–33, 7:53–8:19. This is supported by the testimony of Dr. Oklobdzija, who testified that Figure 3 (along with Figures 2 and 17 of the '121 patent) "point[] . . . to a non-coherent interface and the interconnections," but do not provide details regarding how to implement a coherent and non-coherent interface and instead "le[ave] someone . . . with ordinary skill in the art to . . . figure it out." Ex. 1016, 90:5–93:1, 95:14–96:10. Dr. Oklobdzija also agreed that "one of ordinary skill would not have already had in their knowledge how to build a system with [both] interface[s]." *Id.* at 90:5–17.

Moreover, the textual discussion of Figure 3, which is the only description of the protocol interfaces relied upon by Patent Owner, provides scant detail concerning how a cache coherence controller with both interfaces is built or operated. The specification states the following:

> The cache coherence controller 230 can also be configured to handle a non-coherent protocol to allow communication with I/O devices. In one embodiment, the cache coherence controller 230 is a specially configured programmable chip as a programmable logic device or a field programmable gate array.
>
> Figure 3 is a diagrammatic representation of one example of a cache coherence controller 230. According to various embodiments, the cache coherence controller includes a protocol engine 305 configured to handle packets such as probes and requests received from processors in various clusters of a multiprocessor system. . . .
>
> The cache coherence controller has an interface such as a coherent protocol interface 307 that allows the cache coherence controller to communicate with other processors in the cluster as well as external processor clusters. According to various

> embodiments, each interface 307 and 311 is implemented either as a full crossbar or as separate receive and transmit units using components such as multiplexers and buffers. The cache coherence controller can also include other interfaces such as a non-coherent protocol interface 311 for communicating with I/O devices. It should be noted, however, that the cache coherence controller 230 does not necessarily need to provide both coherent and non-coherent interfaces. It should also be noted that a cache coherence controller in one cluster can communicate with a cache coherence controller in another cluster.

Ex. 2020, 12:22–14:21; Ex. 2006, 11:14–12:14; Ex. 1001, 7:44–8:19. This general description fails to provide a structure or description of how a person having ordinary skill in the art would make or use a cache coherence controller with both types of interfaces. The most detailed language— "[i]n one embodiment, the cache coherence controller 230 is a specially configured programmable chip such as a programmable logic device or a field programmable gate array" and "[a]ccording to various embodiments, each interface 307 and 311 is implemented either as a full crossbar or as separate receive and transmit units using components such as multiplexers and buffers"—does not specifically describe how to implement the system. Instead, as confirmed by Dr. Oklobzjia, the sentence related to the cache coherence controller 230 "gives kind of [a] suggestion to – that this can be implemented as a programmable chip" and the sentence describing implementation of the interfaces is simply an "implementation hint." Ex. 1016, 100:18–102:20. According to Dr. Oklobzjia, the implementation details are "up to the engineers to – to figure out further." *Id.* at 101:10–20.

Indeed, Dr. Oklobdzija testified that prior to the filing date of the '121 patent, a person of ordinary skill in the art would not have known to

use *both* a coherent interface *and* a non-coherent interface at once. Ex. 2019 ¶¶ 11–12. Specifically, Dr. Oklobdzija testifies that, a reference that "reflects the state of the art of coherent and non-coherent interfaces" as of the alleged effective filing date of the '121 patent indicated that a system could use only one or the other of a coherent or non-coherent interface, but not both. *Id.* ¶ 12. Noticeably absent in Patent Owner's Motion is reference to any detailed discussion in the '121 patent of the how the cache coherence controller would operate with both interfaces at once, let alone such full, clear, concise, and exact terms as to enable any person skilled in the art, to make and use the system. Given the testimony of Dr. Oklobdzija, we cannot determine that Figure 3 and the few corresponding lines of description apprise one of ordinary skill how to make and use a cache coherence controller with both a coherent and non-coherent protocol interface. *See Automotive Techs. Int'l v. BMW of N. Am., Inc.*, 501 F.3d 1274, 1281–85 (Fed. Cir. 2007) (holding that electronic sensors were not enabled because the specification's general description failed to provide a structure or description of how a person having ordinary skill in the art would make or use the sensor).

This is true despite Dr. Oklobdzija's conclusory statement to the contrary. Ex. 2042 (Reply Declaration) ¶ 7 ("As I noted in my deposition, based simply on my review during the deposition itself, I believed, and I continue to believe, that the specification of the '121 Patent contains a number of 'implementation hint[s]' which would enable one of skill in the art to practice the coherent protocol interface' and 'non-coherent protocol interface' limitations without undue experimentation."). "It is the specification, not the knowledge of one skilled in the art, that must supply

the novel aspects of an invention in order to constitute adequate enablement." *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1366 (Fed. Cir. 1997). Although the knowledge of one skilled in the art is relevant, the novel aspect of an invention must be enabled in the patent. As noted above, according to Dr. Oklobdzija, prior to filing of the '121 patent, it was suggested that a system could use only one or the other of a coherent or non-coherent interface, but not both. Ex. 2019 ¶¶ 11–12. Given that the allegedly novel aspect of the invention is a cache coherence controller that uses both interfaces, which was unknown to a person of ordinary skill at the time, it is insufficient to merely provide "implementation hints" using known technologies to create that novel cache coherence controller. As was the case in *Genentech*, the portions of the specification relied upon by Patent Owner here provide "only a starting point, a direction for further research" on using a probe filtering unit with both protocol interfaces; it does not provide guidance to a person of ordinary skill in the art on how to make or use such system. 108 F.3d at 1366. Patent Owner, thus, fails to show that the specification provides "reasonable detail" sufficient to enable use of a probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface. We conclude that Patent Owner has not met its burden of showing that the protocol interface limitation is properly enabled under 35 U.S.C. § 112 ¶ 1.

Furthermore, because of the manner in which Patent Owner's Motion addresses Koster, Patent Owner's failure to demonstrate enablement of the proposed substitute claims results in a failure to demonstrate novelty and non-obviousness of the proposed substitute claims. When arguing how the limitations of the proposed substitute claims distinguish them from the

disclosures of the references of record, Patent Owner's Motion addresses Koster only by asserting that "[a]s to the Koster reference, because, as discussed above, all of the substitute claims find support in the '347 Application, the Koster reference is not prior art to any of the proposed substitute claims." Mot. 22. Because Patent Owner does not persuade us that the proposed substitute claims are enabled, we find unpersuasive Patent Owner's suggestion that the proposed substitute claims are entitled to the filing date of the '347 Application. *See Dynamic Drinkware, LLC v. National Graphics, Inc.*, 800 F.3d 1375, 1381 (Fed. Cir. 2015) ("For a patent to claim priority from the filing date of its provisional application, it must satisfy 35 U.S.C. § 119(e)(1) (2006) . . . . 'In other words, the specification of the *provisional* must 'contain a written description of the invention and the manner and process of making and using it, in such full, clear, concise, and exact terms,' 35 U.S.C. § 112 ¶ 1, to enable an ordinarily skilled artisan to practice the invention *claimed* in the *non-provisional* application.") (quoting *New Railhead Mfg., L.L.C. v. Vermeer Mfg. Co.*, 298 F.3d 1290, 1294 (Fed. Cir. 2002)); *Hyatt v. Boone*, 146 F.3d 1348 1352 (Fed. Cir. 1998) ("The earlier application must contain a written description of the subject matter of the interference count, and must meet the enablement requirement."); *see also Novo Nordisk Pharm., Inc. v. Bio-Tech. Gen. Corp.*, 424 F.3d 1347, 1359 (Fed. Cir. 2005) ("The issue of whether the 1983 PCT application was enabled was critical to the prosecution because, if the application was not enabled, Novo would not be able to rely upon the application's priority date to overcome the Brewer patent."). Accordingly, we also find unpersuasive Patent Owner's assertion that Koster is not prior art to the proposed substitute claims. With no other basis for asserting that

the proposed substitute claims are patentably distinct over Koster (by itself or in combination with other references of record), we conclude that Patent Owner has not met its burden of demonstrating patentability of the proposed substitute claims over the references of record. Thus, Patent Owner has not met its burden for proposed substitute claims 29–34.

III. CONCLUSION

For the reasons explained above, we determine the following:

(1) Petitioner has demonstrated by a preponderance of the evidence that claim 24 would have been obvious over Koster;

(2) Petitioner has demonstrated by a preponderance of the evidence that claims 19–23 would have been obvious over Koster and Kuskin;

(3) Patent Owner has not shown that its proposed substitute claims 29–34 are enabled or patentable over the prior art.

IV. ORDER

Accordingly, it is

ORDERED that claims 19–24 of the ’121 patent have been shown to be *unpatentable*;

FURTHER ORDERED that Patent Owner’s Motion to Amend Claims is *denied*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Case IPR2015-00158
Patent 7,296,121 B2

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