

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., HTC CORPORATION, HTC AMERICA, INC.,
SAMSUNG ELECTRONICS CO. LTD,
SAMSUNG ELECTRONICS AMERICA, INC., AMAZON.COM, INC.,
SONY CORP., SONY ELECTRONICS INC.,
SONY MOBILE COMMUNICATIONS AB,
SONY MOBILE COMMUNICATIONS (USA) INC.,
LG ELECTRONICS, INC., LG ELECTRONICS USA, INC., and
LG ELECTRONICS MOBILECOMM USA, INC.,¹
Petitioner,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

Case IPR2015-00163
Patent 7,296,121 B2

Before JENNIFER S. BISK, NEIL T. POWELL, and
KERRY BEGLEY, *Administrative Patent Judges*.

BISK, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Petitioners from IPR2015-01353 were joined with this proceeding. Paper 34.

INTRODUCTION

A. Background

Apple Inc., HTC Corporation, HTC America, Inc. Samsung Electronics Col, Ltd., Samsung Electronics America, Inc.,² and Amazon.com, Inc. (“Initial Petitioner”), filed a Petition requesting *inter partes* review of claims 1–6, 8–12, and 15–25 of U.S. Patent No. 7,296,121 B2 (Ex. 1001, “the ’121 patent”). Paper 1 (“Pet.”). On May 8, 2015, we instituted a review (Paper 18, “Institution Decision” or “Inst. Dec.”) based upon Petitioner’s assertion that claims 4–6, 11, and 19–24 are unpatentable under 35 U.S.C. §§ 102 and 103. Inst. Dec. 28. On July 1, 2015, in response to Petitioner’s request for rehearing, we added claim 12 to the review. Paper 22, 6.

On June 8, 2015, Sony Corp., Sony Electronics Inc., Sony Mobile Communications AB, Sony Mobile Communications (USA) Inc., LG Electronics, Inc., LG Electronics USA, Inc., and LG Electronics Mobilecomm USA, Inc. (collectively, “Subsequent Petitioner”), filed a Petition requesting *inter partes* review of the same claims of the ’121 patent and based on the same grounds as those instituted in IPR2015-00163. Case IPR2015-01353 (Paper 1, “Second Pet.”). The Subsequent Petitioner simultaneously filed a Motion for Joinder of its newly filed case with the Initial Petitioner’s previously instituted case. IPR2015-01353 (Paper 4,

² The Petition also lists Samsung Telecommunications America, LLC (“STA”) as a petitioner. Paper 6 (“Pet.”), 1. After the filing of the Petition, however, STA merged with and into Samsung Electronics America, Inc. Paper 12. Thus, STA no longer exists as a separate corporate entity. *Id.*

“Mot. for Joinder”). On October 5, 2015, we granted the Motion for Joinder and joined Subsequent Petitioners as petitioners in the instant proceeding.³ Paper 34; Case IPR2015-01353 (PTAB Oct. 5, 2015) (Paper 11).

This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, Petitioner has shown by a preponderance of the evidence that claims 4–6 and 19–24 are unpatentable. Petitioner has not shown by a preponderance of the evidence that claims 11 and 12 are unpatentable.

B. Related Matters

The parties indicate that the ’121 patent is the subject of several proceedings in the United States District Court for the District of Delaware. Pet. 1–2; Paper 11, 1–2. Initial Petitioners also filed three other petitions seeking *inter partes* review of the ’121 patent—IPR2015-00159, IPR2015-00161, and IPR2015-00172. In addition, another petition was filed seeking *inter partes* review of the ’121 patent—IPR2015-00158. See Paper 11, 4. Of these proceedings at the Office, only IPR2015-00159⁴ is ongoing and a final written decision in IPR2015-00159 is being issued concurrently with this Decision.

³ For purposes of this decision, we will cite only to Initial Petitioner’s Petition.

⁴ Subsequent Petitioners, who filed a petition and motion for joinder in IPR2015-01376, were also joined to IPR2015-00159. IPR2015-00159, Paper 29.

C. The Asserted Grounds of Unpatentability

Petitioner contends that claims 4–6, 11, 12, and 19–24 (“the challenged claims”) of the ’121 patent are unpatentable under 35 U.S.C. §102 or 103 based on the following grounds (Pet. 3):

Ground	References	Challenged Claims
§ 102	Koster ⁵	4–6, 11, and 12
§ 103	Koster and Smith ⁶	19–24

Petitioner supports its challenge with Declarations executed by Dr. Robert Horst on October 28, 2014 (Ex. 1014) and on December 1, 2015 (Ex. 1025). Patent Owner relies on a Declaration executed by Dr. Vojin Oklobdzija on August 11, 2015 (Ex. 2016).

D. The ’121 Patent

The ’121 patent relates to accessing data in computer systems that include more than one processor. Ex. 1001, 1:23–24. Specifically, the ’121 patent discusses multiple processor systems with a point-to-point architecture—a cluster of individual processors (also referred to as processing nodes) that are directly connected to each other through point-to-point links, each with an associated cache memory. *Id.* at 4:38–40. To increase the number of available processors, multiple clusters may be connected. *Id.* at 4:50–53. Figure 1A is reproduced below.

⁵ U.S. Patent No. 7,698,509 B1 (Ex. 1009) (“Koster”).

⁶ MICHAEL JOHN SEBASTIAN SMITH, *APPLICATION-SPECIFIC INTEGRATED CIRCUITS*, Addison-Wesley (1997) (Ex. 1008, “Smith”).

Figure 1A

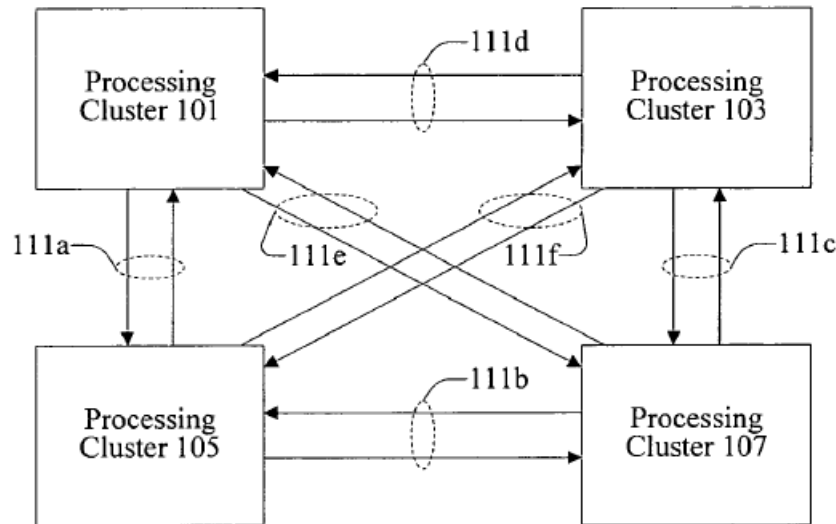


Figure 1A shows an example of a multiple cluster, multiple processor system described by the '121 patent. *Id.* at 6:10–12. Figure 1A includes four processing clusters: 101, 103, 105, and 107, each of which can, in turn, include multiple processors. *Id.* at 6:12–14. The clusters are connected through point-to-point links 111a–f. *Id.* at 6:14–16.

The '121 patent explains that cache coherency problems can arise in such a system, because it may contain multiple copies of the same data. *Id.* at 1:26–38. For example, if the caches of two different processors have a copy of the same data block and both processors “attempt to write new values into the data block at the same time,” then the two caches may have different data values and the system may be “unable to determine what value to write through to system memory.” *Id.* at 1:37–45. Solutions to cache coherency problems often involve an increase in communication traffic and a resulting decrease in efficiency. *Id.* at 1:23–26, 2:46–48. The '121 patent

discloses “techniques . . . for increasing data access efficiency in a multiple processor system,” while also addressing cache coherency. *Id.* at 4:36–38.

The system disclosed by the '121 patent includes a probe filtering unit. *Id.* at 2:52–65. A probe is defined as “[a] mechanism for eliciting a response from a node to maintain cache coherency in a system.” *Id.* at 5:45–47. As opposed to a traditional approach of broadcasting probes to all nodes, the probe filtering unit reduces traffic by intercepting the probes and transmitting them only to those nodes that require the information based on probe filtering information, i.e., “[a]ny criterion that can be used to reduce the number of clusters or nodes probed.” *Id.* at 2:52–3:5, 14:50–52; *see id.* at 28:29–58, 29:43–46. The probe filtering unit may also accumulate responses from those nodes selected to receive the probes and respond to the node from which the probe originated. *Id.* at 3:5–8, 28:59–67, 29:46–51. Figure 18 of the '121 patent is reproduced below.

Figure 18

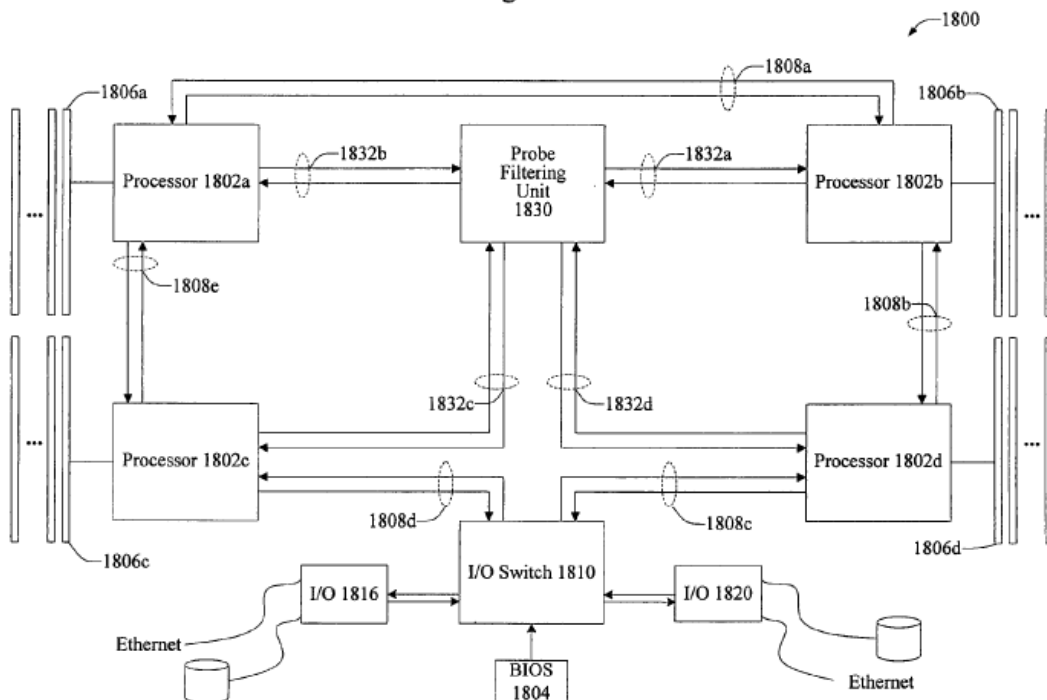


Figure 18 shows a multiple processor system with a probe filtering unit. *Id.* at 3:61–63, 26:58–27:20, Fig. 18. Specifically, Figure 18 depicts multiple processor system 1800 with processing nodes 1802a–d interconnected by point-to-point communication links 1808a–e. *Id.* at 26:58–27:1. System 1800 also includes probe filtering unit 1830 as well as I/O switch 1810, one or more Basic I/O systems (“BIOS”) 1804, I/O adapters 1816, 1820, and a memory subsystem with memory banks 1806a–d. *Id.* at 3:61–63, 26:58–27:20, Fig. 18.

E. Challenged Claims

The challenged claims are all dependent and depend either directly or indirectly from independent claims 1 and 16. Claims 1, 4, 16, and 19 are representative of the challenged subject matter and recite as follows:

1. A computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith,

the computer system further comprising a probe filtering unit which is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories.

4. The computer system of claim 1 wherein the plurality of processing nodes comprises a first cluster of processors, the computer system comprising a plurality of clusters of processors including the first cluster, the plurality of clusters being interconnected via a second point-to-point architecture.

16. A probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories

19. At least one computer-readable medium having data structures stored therein representative of the probe filtering unit of claim 16.

Ex. 1001, 30:65–31:7, 31:17–24, 32:7–15, 32:21–23 (line breaks added).

ANALYSIS

A. Level of Ordinary Skill in the Art

We begin our analysis by addressing the level of ordinary skill in the art. Dr. Horst and Dr. Oklobdzija agree that a person of ordinary skill in the art would have had at least a “bachelor’s degree in electrical engineering, computer engineering, or computer science” and “two years of experience in the design of multiprocessor systems.” Ex. 1014 ¶ 8; Ex. 2016 ¶ 8. We adopt this proposal as the level of ordinary skill in the art, based on the testimony of the parties’ experts as well as our review of the ’121 patent and the prior art involved in this proceeding.

B. Claim Construction

We interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b)); *see Cuozzo Speed Techs., LLC v. Lee*, No. 15–446, slip op. at 12–20 (S.C. June 20, 2016) (holding that 37 C.F.R. § 42.100(b) “represents a reasonable exercise of the rulemaking authority

that Congress delegated to the . . . Office”). We presume a claim term carries its “ordinary and customary meaning,” which is “the meaning that the term would have to a person of ordinary skill in the art in question” at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (citation and quotations omitted). This presumption, however, is rebutted when the patentee acts as his own lexicographer by giving the term a particular meaning in the specification with “reasonable clarity, deliberateness, and precision.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner and Patent Owner each proffer proposed constructions of several claim terms. Pet 4–14; PO Resp. 1–20; Reply 2–8. In the Institution Decision, we construed several terms, including “states associated with selected ones of the cache memories.” Inst. Dec. 7–15. We address below the parties’ post-institution arguments regarding the construction of “states” and otherwise maintain our constructions from the Institution Decision. We also address the parties’ post-institution arguments regarding the term “programmed.”

1. “states”

Claims 1 and 16 recite “probe filtering information representative of *states* associated with selected ones of the cache memories.” Ex. 1001, 31:5–7, 32:14–15 (emphasis added). Before our Institution Decision, each party proposed a construction of the term “states associated with selected ones of the cache memories.” Pet. 9–10; Paper 13 (“Prelim. Resp.”) 11–22. Petitioner argued that the term is “broad enough to encompass ‘any modes or conditions of selected ones of the cache memories.’” Pet. 10. Patent Owner proposed that the term means “cache coherence protocol states

associated with data blocks stored in selected ones of the cache memories” and that a “‘cache coherence protocol state’ means ‘the current state of a data block in a protocol used to maintain the coherency of caches, in which a data block can only be in one current state at a time, and in which the current state can transition to a different state upon one or more triggering events or conditions.’” Prelim. Resp. 11–12. In the Institution Decision, we did not adopt either party’s proposed construction, but found that “the term is not limited to cache coherence protocol states and is broad enough to include the condition of presence—i.e., what is stored in cache memory.” Inst. Dec. 12.

In its Response, Patent Owner continues to argue that “the appropriate construction of states is limited to cache coherence states, and does not include mere presence.” PO Resp. 2. Petitioner does not agree that the term should be so limited. Paper 42 (“Reply”), 2–5. In particular, Petitioner asserts that the broadest reasonable construction of the term “states” is not limited to the context of cache coherency (*id.* at 3–4) and is “broad enough to encompass the condition of presence” (*id.* at 5).

a. Cache Coherence States

The language of the challenged claims “states associated with selected ones of the cache memories” plainly link the “states” to “cache memories.” In addition, in the challenged claims, the term “representative of states associated with selected ones of the cache memories” modifies “*probe filtering information*” (Ex. 1001, 31:5–7, 32:14–15, 32:52–55 (emphasis added)), which the patent defines as “[a]ny criterion that can be used to reduce the number of clusters or nodes probed” (*id.* at 14:50–52). Thus, the recited “states” relate not just to any aspect of the cache memory, but to the contents of that memory. See Inst. Dec. 8–10.

For the reasons discussed below, however, despite the arguments and evidence in Patent Owner’s Response, we remain unpersuaded that the ’121 patent supports limiting the broadest reasonable construction of “states” solely to cache coherence protocol states. A claim term will be interpreted more narrowly than its ordinary and customary meaning only under two circumstances: (1) the “patentee sets out a definition and acts as [its] own lexicographer,” or (2) the “patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1330 (Fed. Cir. 2012). To disavow claim scope, the specification or prosecution history must “make[] clear that the invention does not include a particular feature” and the feature is then “deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification” or prosecution history, “might be considered broad enough to encompass the feature in question.” *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001); *see Aventis*, 675 F.3d at 1330. To disavow claim scope, the patentee may “include[e] in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.” *Aventis*, 675 F.3d at 1330 (internal quotations omitted). In this context, it is not sufficient “that the only embodiments, or all of the embodiments, contain a particular limitation.” *Id.*

Here, beginning with the claims, the relevant language in the independent claims, “states associated with selected ones of the cache memories,” expressly recites “states” alone—not cache coherency states, to which Patent Owner seeks to limit the term. As Petitioner points out, Patent

Owner's proposed construction seeks to add additional narrowing descriptive language to the term "states." See Reply 2.

Moreover, the claims do not recite "cache coherence states" or "cache coherence protocol states." Dependent claim 3, which depends indirectly from claim 1, however, recites "a cache coherence controller" and "a cache coherence directory." Ex. 1001, 31:12–14. Similarly, claim 5, another claim that depends indirectly from claim 1, requires a "cache coherence controller." *Id.* at 31:24. Thus, had the patentees intended to limit "states," as recited in the independent claims of the '121 patent, to cache coherence states, they demonstratively could have done so by explicitly modifying the disputed term with "cache coherence"—but did not.⁷ See Reply 3–4.

Turning to the written description, we do not find persuasive Patent Owner's arguments that the remainder of the specification supports limiting "states" to cache coherency states. Rather, we agree with Petitioner that the

⁷ Patent Owner notes that our Institution Decision "preliminarily determined that 'states' in the claims of the '121 Patent are not limited to 'cache coherence protocol states,' 'despite the fact that the Board determined that the term 'probe' in the claims should be construed as a 'mechanism for eliciting a response from a node to maintain cache coherency in a system.'" PO Resp. 2. We do not agree with Patent Owner's implication that our construction of "probe" conflicts in any way with our construction of "states." The two words recite different parts of the claimed invention. Moreover, the '121 patent expressly defines the term "probe" consistent with our construction (see Ex. 1001, 5:45–47; Inst. Dec. 8), but provides no definition for "state" or "states." If "states" were intended to be limited to cache coherency protocol states, the '121 patent could have provided an express definition for "state" or "states," as it does for "probes." Patent Owner does not provide evidence or reasoning persuading us that a person of ordinary skill in the art would find the express definition of "probes" as somehow limiting the term "states."

'121 patent uses broad language in describing “states,” explaining that “particular implementations may use a different set of states” and “[t]he techniques of the present invention can be used with a variety of different possible memory line states.” Ex. 1001, 14:30–36; *see* Inst. Dec. 11; Pet. 9; Reply 2–3.

Patent Owner asserts that the teachings of the '121 patent make it clear that its inventions are directed to the specific field of cache coherency and the term “state” has “a specific meaning in the field of cache coherency—a cache coherency state.” PO Resp. 3–4; *see* Paper 51 (“Tr.”), 63:13–64:2. As to the field of the '121 patent, we find that it is directed, generally, to “data access and cache coherency in systems having multiple processors.” *E.g.*, Ex. 1001, 2:39–42. The '121 patent explains that data access, and the disclosed invention, involve techniques for reducing probe traffic as well as cache coherency techniques. *See, e.g., id.* at 1:21–27 (“The present invention relates to accessing data in a multiple processor system. More specifically, the present invention provides techniques for reducing memory transaction traffic in a multiple processor system. Data access in multiple processor systems can raise issues relating to cache coherency.”); *see also, e.g., id.* at [54] (title) (“Reducing Probe Traffic in Multiprocessor Systems”); *id.* at 2:45–48 (“According to the present invention, various techniques are provided for reducing traffic relating to memory transactions in multi-processor systems”). Although we agree with Patent Owner that the field of the '121 patent includes cache coherency, we are not persuaded that this fact, alone, limits the term “state” to “cache coherence states.”

Patent Owner, in fact, concedes that the term “state” “may have many broad and different meanings . . . in the general field of computers.” PO

Resp. 4 (citing Ex. 2016 ¶ 15). Indeed, in our Institution Decision, we relied on a dictionary definition of “state” from the MICROSOFT COMPUTER DICTIONARY: “[t]he condition at a particular time of any of numerous elements of computing—a device, a communications channel, a network station, a program, a bit, or other element—used to report on or to control computer operations.” Ex. 3001 (MICROSOFT COMPUTER DICTIONARY (5th ed. 2002)), 497–98. Patent Owner agrees that this dictionary is directed “to the entire field of computing.” PO Resp. 4; Reply 4. And as Petitioner points out, Patent Owner relies on this same dictionary when proposing a construction for another term in the ’121 patent—“programmed.” See PO Resp. 15. Patent Owner has not persuaded us that a person of ordinary skill in the art would not base its definition of the term “states” on the field of computers generally, but instead would rely on a meaning specific to the “field of cache coherency.”

To begin with, as discussed above, Patent Owner agrees that a person of ordinary skill in the art would have a degree in electrical engineering, computer engineering, or computer science and at least two years of experience in the design of multiprocessor systems. Ex. 1014 ¶ 8; Ex. 2016 ¶ 8. Nothing in this definition points to a specific field, known as cache coherency, with its own terminology displacing the more general terminology used by those in the field of computing.

Moreover, Patent Owner, itself, admits that in the context of a patent describing data access and cache coherence in multiprocessor systems, the term “state,” used on its own, does not necessarily refer to a cache coherency state. Specifically, when discussing Koster, titled “Snooping-based Cache-Coherence Filter for a Point-to-Point Connected Multiprocessing Node,”

Patent Owner argues that “the mere fact that Koster refers to his shadow tag memory as ‘local state memory’ does not mean that it contains ‘information representative of states associated with selected ones of the cache memories’ as that phrase is used in the ’121 patent.” PO Resp. 23. Instead, according to Patent Owner, to determine the meaning of “local state memory,” “it is necessary to consider what information Koster stores in the shadow tag memory and whether such information satisfies the properly construed limitation.” *Id.* Patent Owner concludes that because tags only indicate the address of data, “despite Koster’s reference to such tags as ‘state’ information,” the tags “are not representative of cache coherency states as required by the properly construed limitations of the ’121 patent.” *Id.*

Essentially, Patent Owner attempts to argue, in the claim construction section of its Response, that a person of ordinary skill in the art would understand that, in the context of the ’121 patent, the term “state” on its own, means “cache coherency state,” where the actual cache coherency states encompass an open set of states used by any cache coherency protocol. *See* Prelim. Resp. 11–12; PO Resp. 2–7. However, when analyzing the prior art, which involves the same field as the ’121 patent, Patent Owner asserts that the same person of ordinary skill would understand the term “state” on its own does *not* mean cache coherency state, but instead means something more broad, as, for example, the term is defined in the general field of computers. Patent Owner does not explain sufficiently why the term state would mean one thing in the ’121 patent and another in Koster when both involve the same field of art.

Patent Owner relies, for its assertions, on a few excerpts of the ’121 patent, which allegedly “demonstrate that the use of the term ‘state’ in

the patent is directed to cache coherence protocol states.” PO Resp. 5–6. For example, Patent Owner points to the following passage of the Specification as “mak[ing] it clear that the relevant state is a cache coherence protocol state”:

It should be noted that *a coherence protocol* can contain several types of messages. In one example, a coherence protocol includes four types of messages; data or cache access requests, probes, responses, or probe responses, and data packets. Data or cache access requests usually target the home node memory controller. Probes are used to query each cache in the system. The probe packet can carry information that allows the caches to properly *transition the cache state for a specified line*.

Id. at 6 (quoting Ex. 1001, 9:21–29) (emphases added by Patent Owner). Similarly, Patent Owner points to the Specification’s statement that “[b]y using a *coherence directory*, *global memory line state information* (with respect to each cluster) can be maintained and accessed by a memory controller or a cache coherence controller in a particular cluster,” asserting that this statement only makes sense if the coherence directory concerns solely cache coherence states. PO Resp. 6–7 (quoting Ex. 1001, 13:4–7) (emphases added by Patent Owner).

We are not persuaded that these passages of the ’121 patent limit the term “states” as asserted by Patent Owner. Neither of the passages relied upon by Patent Owner actually uses the term “state” as recited in the challenged claims. Instead, the first passage Patent Owner relies on for a narrower construction uses the term “*cache state*” and the second uses the term “*global memory line state information*.” Thus, even if the passages describe a concept narrower than “states associated with selected ones of the cache memories,” as recited in the challenged claims, this difference can be

attributed to the fact that different terms are used. More importantly, these passages do not expressly disclaim or disavow the broader scope of the claim language, particularly given the expansive language used elsewhere in the Specification allowing states to include “a variety of different possible memory line states.” Ex. 1001, 14:30–36.

Patent Owner also points to Figures 7 and 8 of the ’121 patent as allegedly “strongly illustrative that the ’121 Patent uses ‘state’ to mean cache coherence protocol states.” PO Resp. 7. According to Patent Owner, the Specification equates the word “state” with cache coherence states by describing Figure 7 as “*the coherence directory 701 includes state information 713*” and by stating “[i]n some embodiments, the memory line states are modified, owned, shared, and invalid.” *Id.* (quoting Ex. 1001, 13:55–59) (emphases added by Patent Owner). In other words, Patent Owner argues that because Figure 7 shows a column labeled “state,” and describes this column as including in some embodiments the states used in common cache coherence protocols such as MOESI and MOSI, the term “state” must be equivalent to cache coherence protocol. *See* Tr. 77:20–78:18.

Figures 7 and 8, however, also are not persuasive as defining the term state because they are clearly described as exemplary embodiments. *See, e.g.,* Ex. 1001, 3:15–18, 4:11–35 (“[I]t is not intended to limit the invention to the described embodiments. On the contrary, it is intended to cover alternatives, modification, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.”), 13:44–59 (describing Figure 7 using the term “example” or “embodiment” no less than five times), 14:48–50, 30:57–64 (“[T]he scope of the invention

should not be limited by reference to such advantages, aspects, and objects . . . the scope of the invention should be determined with reference to the appended claims.”). We are not persuaded that Figure 7 shows anything more than what it purports to show—one example with a column labeled “state,” that may refer to “memory line states” of “modified, owned, shared, and invalid.” Again, nothing in this example expressly disclaims or disavows the broad claim language, particularly in light of other statements in the Specification allowing states to include “a variety of different possible memory line states.” Ex. 1001, 14:30–36.

Patent Owner further argues that the ’121 patent distinguishes between state information and tags in certain examples disclosed therein. PO Resp. 22–23. We also find this information unpersuasive, as Patent Owner’s citation of portions of the ’121 patent that discuss both tags and state information does not persuade us that tags and state information are mutually exclusive, as these portions of the ’121 patent are examples. *See id.* at 22–23 (citing Ex. 1001, 7:67–8:4; 13:44–14:47; Fig. 7). Patent Owner does not identify any portion of the ’121 patent that clearly disavows tags as mutually exclusive from state information.

Patent Owner also proffers extrinsic evidence to support its proposed construction of the term “state.” Extrinsic evidence is “less significant than the intrinsic record in determining the legally operative meaning of claim language.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (citations omitted) (internal quotations omitted). For example, Patent Owner points to “one of the treatises on cache coherency,” DANIEL J. SORIN ET AL., A PRIMER ON MEMORY CONSISTENCY AND CACHE COHERENCE (2011) (Ex. 2010, “Sorin”), as equating the term “state” with cache coherence

protocol states. PO Resp. 4 (citing Ex. 2010, 88–89; Ex. 2016 ¶ 15). We do not find this evidence persuasive. Evidence of the use of shorthand within one section in one publication does not indicate that that same shorthand will be recognized, by a person of ordinary skill, as necessarily having the same meaning in other contexts. Dr. Oklobdzija’s testimony referring to this treatise does not persuade us to the contrary. *See* Ex. 2016 ¶ 15.

Patent Owner also points to another article, where the authors—three of whom are the authors of Sorin, discussed above—state that “[a] processor’s access to a cache block is determined by the state of that block in its cache, and this state is *generally* one of the five MOESI (Modified, Owned, Exclusive, Shared, Invalid) states.” PO Resp. 5 (citing Ex. 2003, 1) (emphasis added); *see* Reply 4. Again, this isolated use of a shorthand of “states” in a publication, with several of the same authors as the other cited publication, does not persuade us that this shorthand is universally accepted to have a particular meaning whenever a particular type of software is being discussed. Moreover, the use of the term “generally” in this statement shows that it is not limiting the term “states” to cache coherency states, or more specifically, MOESI states. Therefore, we are not persuaded that Patent Owner’s extrinsic evidence regarding ordinary meaning overcomes the intrinsic record of this case. *See Phillips*, 415 F.3d at 1318 (“[A] court should discount any expert testimony that is clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent.”) (citations and internal quotation marks omitted).

In summary, we conclude that the “states” in the claim language “states associated with selected ones of the cache memories,” as recited in

independent claims 1 and 16 of the '121 patent, relate to the contents of cache memory, but are not limited solely to cache coherence protocol states.

b. Presence

Even if we agreed with Patent Owner's assertion that the term "states" is limited to cache coherence states, we find unpersuasive Patent Owner's arguments relating to presence. PO Resp. 2–10.

The '121 patent directly touches on the subject of presence when discussing cache coherency states. For example, when describing certain embodiments associated with Figure 7, including cache coherency memory line states of "modified, owned, shared, and invalid," the '121 patent declares "[i]n the invalid state, a memory line is not currently available in cache associated with any remote cluster." Ex. 1001, 13:58–61. Patent Owner argues that, contrary to the ordinary meaning of these words, the disclosed "invalid" state does not refer only to a lack of presence, but instead means that the memory line "can be present but invalid," because it cannot be "rel[ied] on," or is "not available to use because it is invalid." Tr. 80:20–81:13. Patent Owner, however, does not explain sufficiently why a person of ordinary skill in the art would understand the statement in this way, as opposed to the plain meaning of the "currently available" language in the Specification. See Tr. 80:13–84:8.

Instead, Patent Owner points to other portions of the Specification, asserting that the '121 patent teaches "'state' provides additional information about 'a particular cached line' that is known to already be 'somewhere' (i.e. it is alre[a]dy known to be present)." PO Resp. 8. In particular, Patent Owner bases this assertion on a passage of the '121 patent stating "because the cache coherence directory provides information about **where [i.e., in**

which cluster the line is present] memory lines are cached as well as their states, probes only need be directed toward the clusters in *which the requested memory line is cached*” and “[t]he state of a particular cached line will determine what type of probe is generated.” *Id.* (quoting Ex. 1001, 19:36–43 (emphases added by Patent Owner)). According to Patent Owner, this passage “plainly indicates” that the state of a memory line is different from where it is located and that “state” only exists for a cached line. *Id.*

Patent Owner also points to the ’121 patent’s discussion of an “occupancy vector” as demonstrating that presence is not considered a state. PO Resp. 9. According to Patent Owner, the ’121 patent’s statement that “[a]ny mechanism for tracking what clusters hold a copy of the relevant memory line in cache [i.e., in which clusters the memory line is present] is referred to herein as an occupancy vector,” and its treatment of the “occupancy vector” different than the “state” field in Figure 7, indicate that the ’121 patent understands presence and “state” to be different. *Id.* at 9–10 (citing Ex. 1001, 13:55–57, 13:67–14:2, Fig. 7); Ex. 2016 ¶ 24.

Intrinsic and extrinsic evidence contradicts Patent Owner’s and Dr. Oklobdzija’s suggestion that a cache coherency state necessarily needs to indicate more than whether a memory line is present in cache memory. As noted above, the ’121 patent itself discloses that “[i]n the invalid state, a memory line is *not currently available* in cache associated with any remote cluster.” Ex. 1001, 13:60–61 (emphasis added). As also noted above, the plain meaning of this statement is that the “invalid” cache coherence state indicates that a memory line is not present in cache memory, and Patent Owner has not explained persuasively its assertion to the contrary. *See* Tr. 80:13–84:8.

Moreover, none of the passages of the '121 patent cited by Patent Owner clearly limits the scope of “states.” *See, e.g.*, Ex. 1001, 13:44–55 (stating multiple times that the embodiment depicted in Figure 7, with an occupancy vector, is an “example”). Regarding Patent Owner’s citation of discussions in the '121 patent of states that provide information beyond whether specific data is present in a cache, we again note that the '121 patent expressly discloses that its invention encompasses use of states other than the examples discussed therein. *Id.* at 14:30–36.

Indeed, extrinsic evidence cited by Patent Owner and Dr. Oklobdzija explains that not present is a cache coherency state and that one meaning of the invalid cache coherency state is that the block is not present or available in the cache. For example, Patent Owner and Dr. Oklobdzija cite Sorin and a book titled “Parallel Computer Architecture” and authored by David E. Culler et al. (Ex. 2011, “Culler”). Culler explains that in a Dragon protocol it discusses, “there is no explicit invalid (I) state” but that “if a block is not present in a cache at all, it can be imagined in a special invalid or not-present state.” Ex. 2011, 302. Later, Culler discusses using the state “NP (not present)” in connection with the “MESI protocol.” *Id.* at 307–310.

Similarly, Sorin explains the cache coherence state of “I(nvalid)” as follows:

The block is invalid. The cache either does not contain the block or it contains a potentially stale copy that it may not read or write. In this primer, we do not distinguish between these two situations, although sometimes the former situation may be denoted as the “Not Present” state.

Ex. 2010, 89. At his deposition, Dr. Oklobdzija testified that Sorin is a “competent” and Culler is a “very highly regarded” source regarding cache coherency. Ex. 1026, 38:3–39:11.

Thus, the '121 patent and the extrinsic evidence of record demonstrate that not present is a cache coherency state and that one meaning of the invalid cache coherency state is that the block is not present or available in the cache. Accordingly, we conclude that even if “state,” as recited in independent claims 1 and 16 of the '121 patent, requires a cache coherency state, it encompasses the cache coherency states of invalid, meaning the block is not present or available in the cache, and not present.

2. “*programmed*”

Claim 11 recites “wherein each of the processing nodes is *programmed* to complete a memory transaction after receiving a first number of responses to a first probe, the first number being fewer than the number of processing nodes.” We did not construe “programmed” explicitly in the Institution Decision. In the analysis of this limitation, however, we referred to a dictionary definition of “program” as “[i]nstructions given to a computer . . . to perform certain tasks.” Inst. Dec. 21–22 n.7. Patent Owner asserts that the term “programmed” should be construed to refer to a device that has been “configured by a sequence of instructions.” PO Resp. 13. According to Patent Owner, this construction is consistent with the '121 patent and with various dictionary definitions, including the definition cited by the Institution Decision. *Id.* at 14–15 (citing Ex. 1001, 28:8–24, 29:1–3, 27:67–28:2; Ex. 2012, 359; Ex. 2013, 590–91; Ex. 2014, 931). Patent Owner adds that, at a minimum, the broadest reasonable interpretation of “programmed” must exclude hardwired logic. *Id.* at 17–19 (citing Ex. 2012, 214; Ex. 2015, 15/3; Ex. 2016 ¶¶ 38–39).

Petitioner asserts that Patent Owner’s interpretation of the term “programmed” is too narrow and proposes a construction of “designed to

perform a sequence of operations, regardless of whether this design is in hardware or software.” Reply 5–8. Petitioner argues that Patent Owner does not cite to any language in the ’121 patent that limits the nature of programming and contends that “programmed” should be given its ordinary meaning. Tr. 43:17–24; *see* Reply 6–8. According to Petitioner, the ’121 patent does not use the words “instruction” or “execute” and makes no distinction between hardwired logic and the relevant portion of the claimed processors. *Id.* at 6. Petitioner also states that the dictionaries to which Patent Owner cites include “reasonable definitions for programming that defy [Patent Owner’s] proposal, such as ‘to work out a sequence of operations to be performed by (a mechanism).’” Reply 6 (quoting Ex. 2014, 931).

We agree with Petitioner’s assertions that the ’121 patent does not define or use the term “programmed” in a manner inconsistent with the plain and ordinary meaning. None of the passages of the ’121 patent specification to which the parties cite define or limit the scope of the term. *See* Ex. 1001, 7:49–52, 27:67–28:24; PO Resp. 13–14, 27 (citing Ex. 1001, 27:64–28:24, 29:1–3); Reply 6–7 (citing Ex. 1001, 7:49–52, 28:2–5).

The heart of the dispute regarding this limitation, however, lies in whether the disclosure of microprocessors as devices in a system necessarily discloses that those microprocessors are “programmed.” Because the ’121 patent does not illuminate this issue, but instead the parties rely on expert testimony and other extrinsic evidence to support their respective positions, we consider this issue to more properly fall within the category of unpatentability as opposed to claim construction. *See* Pet. 34–36; PO Resp. 12–19, 25–29; Reply 5–8. Thus, we do not further construe the

term “programmed” other than to note that the ’121 patent uses the term in the ordinary and customary manner. *See* Ex. 1001, 7:49–52, 27:64–28:24, 29:1–3; Ex. 2012, 359; Ex. 2013, 590–91; Ex. 2014, 931.

C. Anticipation of Claims 4–6, 11, and 12 by Koster

1. Overview of Koster

Koster discloses a “Snooping-based Cache-Coherence Filter for a Point-to-Point Connected Multiprocessing Node.” Ex. 1009, [54]. In Koster, when a microprocessor requests data that is not available in its local cache, it sends a request for that data to a snoop filter. *Id.* at [57]. The snoop filter stores a copy of the tags of data stored in the local cache memories of each of the microprocessors. *Id.* When the snoop filter receives a request for data, it can determine which microprocessors have copies of the requested data and relay the data request only to those microprocessors. *Id.*

Figure 9 of Koster is reproduced below.

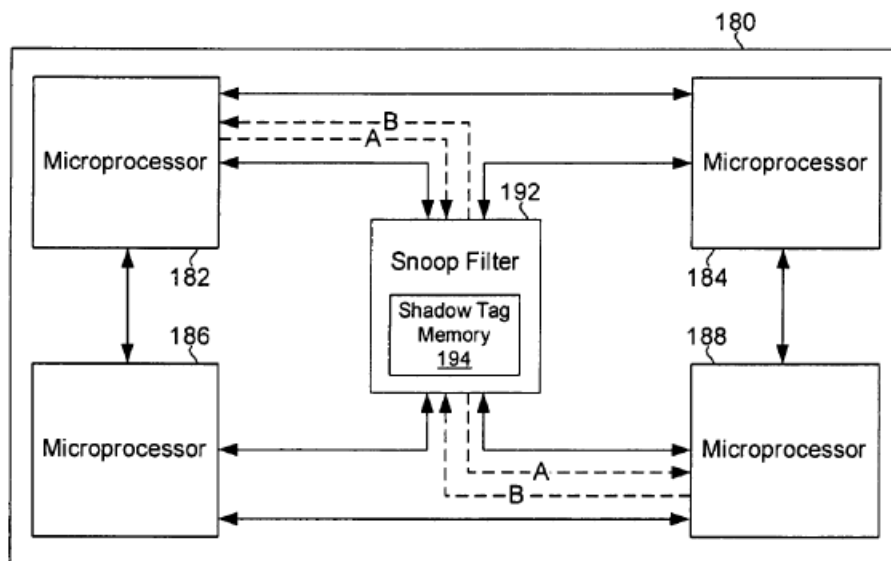


FIG. 9

Figure 9 shows an exemplary flow of messages in multiprocessing node 180 with four microprocessors 182, 184, 186, and 188 and snoop filter 192. *Id.* at 6:61–67. Microprocessor 182 requests data by issuing “broadcast A,” which is routed to snoop filter 192. *Id.* at 6:67–7:3. Snoop filter 192 has shadow tag memory 194 that stores copies of the tags of data stored in the local cache memories of microprocessors 182, 184, 186, and 188. *Id.* at 7:3–6; 6:9–17. Upon receipt of broadcast A, snoop filter 192 determines whether any of the other three microprocessors have a copy of the requested data. *Id.* In Figure 9, snoop filter 192 determines that microprocessor 188 has a copy of the requested data and forwards broadcast A to microprocessor 188. *Id.* at 7:6–10. Next, microprocessor 188 sends “response B (having a copy of the requested data)” to snoop filter 192, which, in turn, forwards response B back to requesting microprocessor 182. *Id.* at 7:10–14.

Koster notes that “[b]y forwarding response B through the snoop filter 192, the snoop filter 192 is able to update its shadow tag memory 194.” *Id.* at 7:15–16. Koster, however, also discloses embodiments in which “a response from a microprocessor may be routed directly back to a requesting microprocessor.” *Id.* at 7:17–19.

2. Discussion

Petitioner asserts that claims 4–6, 11, and 12 are anticipated by Koster. Pet. 31–37. Petitioner supports its assertion with testimony from Dr. Horst. Ex. 1014 ¶¶ D-2–D-4. Petitioner argues that Koster’s microprocessors correspond to the claimed “processing nodes” and that Koster’s snoop filter corresponds to the claimed “probe filtering unit.” Pet. 26–28. Petitioner also argues that Koster discloses probe filtering

information through the disclosure of the tags stored in shadow tag memory 164. Pet. 28.

In the Decision to Institute, we determined that Petitioner had shown a reasonable likelihood of prevailing on this proposed ground of unpatentability. Inst. Dec. 19–24. We have reviewed Petitioner’s anticipation arguments and supporting evidence, including Koster’s disclosure, the detailed arguments appearing on pages 31–38 of the Petition, and the testimony of Dr. Horst. Despite the counter-arguments in Patent Owner’s Response, and the evidence cited therein, which we also have considered, Petitioner has shown, by a preponderance of the evidence, that each of claims 4–6 is unpatentable under 35 U.S.C. § 102 as anticipated by Koster. Petitioner, however, has not shown, by a preponderance of the evidence that Koster anticipates claims 11 and 12.

a. “states associated with selected ones of the cache memories”

Patent Owner argues that Koster does not disclose “probe filtering information” “representative of states associated with selected ones of the cache memories,” as recited by claims 4–6, 11, and 12. PO. Resp. 21–24. Patent Owner rests this contention on its assertion that the claim language requires cache coherency states, in combination with an argument that “Koster’s tags . . . are not representative of cache coherency states.” *Id.* at 21. Patent Owner asserts that “a tag identifies a memory address but does not provide any information regarding the state of that memory address.” *Id.* at 21. As noted above, Patent Owner contends that the ’121 patent distinguishes between tags and state information in certain examples disclosed therein. *Id.* at 22–23. Patent Owner states that “[i]n its Decision

on Institution, the Board found that Koster's tags indicate 'where specific data is cached (i.e., the presence of data in specific locations)' and that the 'states' limitation is broad enough to include the 'condition of presence.'" *Id.* at 24. Patent Owner argues that "[h]owever, for the reasons explained in the claim construction section above, the condition of presence is not a cache coherency state and therefore cannot satisfy this limitation." *Id.*

Petitioner responds that Patent Owner's arguments rest on an incorrect claim construction. Reply 8–9. Petitioner asserts that the proper construction of the disputed claim language includes the condition of presence, and that Koster's tags "provide the snoop filter with addresses identifying locations of copies of requested data that are in a *valid* cache coherency state." *Id.* at 8–12. Petitioner argues that "Koster discloses that the snoop filter 162 filters probes 'with reference to probe filtering information representative of states associated with selected ones of the cache memories' as recited in claims 1 and 16." *Id.* at 13.

We are persuaded that Koster's tags and shadow tag memory teach the claim language "probe filtering information representative of states associated with selected ones of the cache memories." For the reasons explained above, we do not agree with Patent Owner's argument that the broadest reasonable interpretation of this claim language requires cache coherency states. Additionally, as discussed above, Patent Owner does not persuade us that the examples of tags and state information discussed in the '121 patent constitute a clear disavowal of tags as necessarily excluded from state information. See PO Resp. 22–23 (citing Ex. 1001, 7:67–8:4, 13:44–14:47, Fig. 7). Furthermore, Patent Owner's argument that tags are not state information fails to recognize that the claimed probe filtering information

does not have to be states, it need only be “*representative* of states associated with selected ones of the cache memories.” Ex. 1001, 31:5–6 (emphasis added); see Tr. 74:11–15, 77:2–9.

Patent Owner does not dispute that Koster’s shadow tag memory and its tags indicate where specific data is cached. See PO Resp. 21; Ex. 1001, at [57], 6:9–38, 6:61–7:16, 7:25–33, Figs. 9, 10; Pet. 31; Reply 8–9; Ex. 1014 ¶¶ D-12–D-14; Ex. 1027, 186:17–24. Additionally, Koster uses the information provided by the shadow tag memory and its tags in controlling where to send data requests. See, e.g., Ex. 1001, 6:18–32; Pet. 20; Ex. 1014 ¶ D-15. Accordingly, we are persuaded that Koster’s shadow tag memory and its tags are representative of whether selected ones of the cache memories contain specific data, which is representative of the states of those cache memories. See, e.g., Ex. 3001, 497–498 (setting forth definition of “state” as “[t]he condition at a particular time of any of numerous elements of computing—a device, a communication channel, a network station, a program, a bit, or other element—used to report on or to control computer operations.”); Pet. 31; Reply 8–13; Ex. 1014 ¶¶ D-12–D-15; Ex. 1016, 186:17–24.

Additionally, even if the claim language “states associated with selected ones of the cache memories” did refer to cache coherency states, we are persuaded that Koster discloses the “probe filtering unit” recited in claim 1. As explained above, even if we agreed with Patent Owner that the term “state” required a cache coherency state, the evidence of record demonstrates that it encompasses the cache coherency states of invalid, meaning the block is not present or available in the cache, and not present.

Given this, we find that Koster's shadow tag memory constitutes probe filtering information representative of cache coherency states associated with selected ones of its cache memories. As noted above, Patent Owner does not dispute that the tags in Koster's shadow tag memory indicate where specific data is cached. *See* PO Resp. 21; Pet. 31; Reply 8–9; Ex. 1014 ¶¶ D-12–D-14; Ex. 1027, 186:17–24; Ex. 2016 ¶¶ 47–48. By indicating where specific data is cached, Koster's tags and shadow tag memory are representative of which cache memories do not contain a copy of data. This is illustrated, for example, in Koster's disclosure that:

By having the shadow tag memory 164, the snoop filter 162 forwards a received broadcast for requested data (by one of the microprocessors 152, 154, 156, 158 or from another multiprocessing node (not shown)) to a particular one of the microprocessors 152, 154, 156, 158 only if its shadow tag memory 164 indicates that the particular microprocessor has a copy of the requested data. Otherwise, if the snoop filter 162 determines that none of the microprocessors 152, 154, 156, 158 has a copy of the requested data, the snoop filter 162 is configured to cancel any subsequent relays of the broadcast to the microprocessors 152, 154, 156, 158, and instead, sends a message back to the requesting microprocessor (or multiprocessing node (not shown)) indicating that none of the other microprocessors (or none of the microprocessors) in the multiprocessing node 150 has a copy of the requested data.

Ex. 1009, 6:18–32.

Thus, because Koster's tags and shadow tag memory are representative of which cache memories do not contain a copy of data, they are representative of the invalid cache coherency state, meaning that the block is not present or available in the cache, and they are representative of

the not present cache coherency state for those cache memories lacking a copy of a data line.

b. “programmed”

Patent Owner also argues that Koster does not disclose that “each of the processing nodes is programmed to complete a memory transaction after receiving a first number of responses,” as required by claims 11 and 12.

PO Resp. 25–29. We agree with Patent Owner that Petitioner has not demonstrated sufficiently that this limitation is inherent to the disclosure of Koster. Inherency can be established when the “prior art necessarily functions in accordance with, or includes, the claimed limitations.” *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349 (Fed. Cir. 2002).

“Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *In re Oelrich*, 666 F.2d 578, 581 (CCPA 1981).

Petitioner argues that Koster discloses the limitation, because Koster describes an example in which a microprocessor receives only a single response to its request. Pet. 35–36. Therefore, according to Petitioner, Koster’s requesting microprocessor “must be,” or is necessarily, programmed to complete a memory transaction after receiving a first number of responses (more specifically, one response) to a request. *Id.*

In our Institution Decision, we found that “Petitioner has shown sufficiently that Koster discloses ‘wherein each of the processing nodes is programmed to complete a memory transaction after receiving a first number of responses to a first probe,’” as recited by claim 11. Inst. Dec. 21; Paper 22, 4. Specifically, we were “persuaded, on th[e] record [before us],

that Koster, by discussing microprocessors, inherently discloses that this is done via some sort of programming.” Inst. Dec. 21 (citing the definition of microprocessor from NEWTON’S TELECOM DICTIONARY 523, 661 (20th ed. 2004)).

Patent Owner does not dispute that the processors described by Koster “complete a memory transaction after receiving a first number of responses to a first probe.” See PO Resp. 25–34. Patent Owner, however, argues that “there is no reason why Koster’s processors must necessarily be configured using programming as opposed to using any other mechanism for implementing the operation described by Koster.” *Id.* at 26. For example, according to Patent Owner, the functionality could be implemented via hardwired logic, which does “not meet the claim requirement that ‘each of the processing nodes is *programmed* to complete a memory transaction after receiving a first number of responses to a first probe.’” *Id.* at 26–27. Patent Owner supports these arguments with testimony from Dr. Oklobdzija, who opines that “[t]here are numerous ways in which the operations described by Koster could be implemented without any use of ‘programming’ . . . [f]or example, such functionality could be implemented via hardwired logic.” *Id.* ¶ 56.

More specifically, Patent Owner—with support from Exhibit 2015, ELECTRICAL ENGINEER’S REFERENCE BOOK (16th ed. 2003), cited in its Response—argues that there are “three main classes of digital systems,” including “traditional hard-wired systems,” “truly programmable systems” and a “middle class . . . programmable logic.” Tr. 93:4–25, 99:21–23; see Ex. 2015, 15/3; PO Resp. 16–17. Patent Owner concedes that both truly programmable systems *and* the middle class of programmable logic, which

includes field programmable gate arrays (“FPGAs”), qualify as “programmed.” Tr. 95:11–22, 100:3–4, 101:3–102:8, 107:20–22; Ex. 2015, 15/3; *see also* Ex. 1001, 7:49–52 (referring to a FPGA as a “programmable chip”). However, according to Patent Owner, traditional hard-wired circuitry is not programmed. Tr. 95:22–25, 99:21–23, 102:5–8, 107:23–25; *see* PO Resp. 17–18, 26; Ex. 2016 ¶¶ 38–39; Ex. 2015, 15/3.

Patent Owner provides additional evidence to support this position. According to Dr. Oklobdzija, the difference between traditional hardwired logic and programmable systems is that in a hardwired system, the “sequence of operations is governed by the physical interconnection of the digital processing elements,” which are “inflexible because the design is specific to a particular processing function: if the processing function is changed, then the processing elements and their interconnections have to be altered.” Ex. 2016 ¶ 39 (citing Ex. 2015, 15/3). Programmable systems, on the other hand, can be controlled using “a prescriptive program of instructions (i.e. software).” *Id.* In other words, the difference is that devices falling within the middle category, programmable logic, can be “configured” or “designed” using software, while traditional hardwired logic cannot. *See* Ex. 2016 ¶ 39 (citing Ex. 2015, 15/3); PO Resp. 17–18, 26 (citing Ex. 2015, 15/3); Ex. 2015, 15/3; Ex. 1008, 33, 187, 316⁸ (explaining that a “key element[]” of an FPGA is that a designer “uses custom software, tailored to each programming technology and FPGA architecture, to design and implement the programmable connections” and that one component of an FPGA is “design software” that allows it to be “program[ed]”).

⁸ Many pages of Ex. 1008 have two page numbers. For purposes of this decision, our references to Ex. 1008 use the bottom-most page number.

Patent Owner also cites to the MICROSOFT COMPUTER DICTIONARY, which distinguishes hardwired from programming. PO Resp. 17 (citing Ex. 2012, 214). Specifically, the dictionary defines “hardwired” as “[b]uilt into a system using hardware such as logic circuits, *rather than accomplished through programming.*” Ex. 2012, 214 (emphasis added); *see id.* at 359 (defining programming).

Petitioner fails to proffer evidence sufficient to rebut Patent Owner’s evidence that Koster’s disclosure of a microprocessor does not necessarily disclose that the microprocessor is programmed. Dr. Horst, in his original declaration, asserts that “a requesting microprocessor must be programmed to complete a memory transaction after receiving a first number of responses to a first data request.” Ex. 1014 ¶¶ D-17–D-18. This assertion, however, is conclusory, and does not sufficiently explain why the microprocessor must be programmed or exclude possibilities other than programming. *See id.*; PO Resp. 27. In particular, Dr. Horst’s original declaration testimony provides no discussion or explanation as to whether a microprocessor composed solely of hardwired logic would necessarily be programmed and whether the functionality described in Koster could not be implemented using hardwired logic. *See* Ex. 1014 ¶¶ D-17–D-18; PO Resp. 27.

In his reply declaration, Dr. Horst testifies that “the term ‘programmed’ is commonly used to describe the design and configuration of hardwired logic.” Ex. 1025 ¶ 2. Dr. Horst, however, supports this conclusory statement only by reference to FPGAs, which fall within Patent Owner’s described middle class of devices, programmable logic devices, which Patent Owner itself concedes are programmed. *Id.* ¶¶ 3–5; *see* Tr. 95:11–22, 100:3–4, 101:3–102:8, 107:20–22; Ex. 2015, 15/3 (explaining

that FPGAs are “programmable . . . logic devices . . . that can be programmed” to implement certain functions); Ex. 1001, 7:59–52 (referring to a FPGA as a “programmable chip”). Thus, Dr. Horst’s testimony does not address all possible means by which the microprocessor disclosed in Koster could be implemented or even all hardwired logic—only a subset of hardware devices that can be “inter-wired in different configurations according to a manufacturer’s programming.” Ex. 1025 ¶ 3.

Dr. Horst does not provide testimony sufficient to support Petitioner’s position that all microprocessors, even those that are purely hardwired, are programmed. *See, e.g.*, Tr. 99:21–100:2; Ex. 1014 ¶¶ D-17–D-18; Ex. 1025 ¶¶ 2–6. Nor does Dr. Horst’s testimony exclude the possibility that Koster’s microprocessors implement traditional hardwired logic to complete a memory transaction upon receiving responses. *See, e.g.*, Ex. 1014 ¶¶ D-17–D-18; Ex. 1025 ¶¶ 2–6. Petitioner does not point to any other evidence adequate to show that Koster’s disclosure of the use of a microprocessor within its system, by itself, necessarily discloses that the microprocessor is programmed. *See, e.g.*, Pet. 34–37; Reply 13–15.

We, therefore, agree with Patent Owner that Petitioner has not demonstrated, by a preponderance of the evidence, that Koster discloses “each of the processing nodes is programmed to complete a memory transaction after receiving a first number of responses to a first probe,” as recited in claim 11 and inherited by claim 12, and thus that Koster anticipates claims 11 and 12.

c. Conclusion

We have reviewed the evidence and arguments presented in the Petition, Patent Owner’s Response, and Petitioner’s Reply. Based on that

review, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that all of the limitations of claims 4–6, but not claims 11 and 12, are disclosed by Koster. Pet. 23–37; PO Resp. 20–34; Reply 8–19.

D. Obviousness of Claims 19–24 over Koster and Smith

1. Overview of Smith

Smith, titled “Application-Specific Integrated Circuits,” describes the design of application-specific integrated circuits (ASICs). Ex. 1008, 18, 20–21. For example, Smith describes ten design steps used to design an ASIC. *Id.* at 33–35. The ten design steps are described as follows:

1. *Design entry.* Enter the design into the ASIC design system, either **using a hardware description language (HDL)** or schematic entry.
2. *Logic synthesis.* Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a **netlist**—a description of the logic cells and their connections.
3. *System partitioning.* Divide a large system into ASIC-sized pieces.
4. *Prelayout simulation.* Check to see if the design functions correctly.
5. *Floorplanning.* Arrange the blocks of the netlist on the chip.
6. *Placement.* Decide the locations of cells in a block.
7. *Routing.* Make the connections between cells and blocks.
8. *Extraction.* Determine the resistance and capacitance of the interconnect.
9. *Postlayout simulation.* Check to see the design still works with the added loads of the interconnect.

Id. Smith also describes masks as the tools used to create ASICS. *Id.* at 45.

2. Discussion

Claim 19 depends from claim 16 and claims 20–23 depend, directly or indirectly, from claim 19. All these claims further recite “[a]t least one computer-readable medium having data structures stored therein representative of the probe filtering unit.” Claim 24 depends from claim 16 and further adds “[a] set of semiconductor processing masks representative of at least a portion of the probe filtering unit.” Petitioner asserts that Koster discloses all limitations of claim 16. Pet. 37–38. Petitioner asserts that the additional limitations recited in claims 19–24 are disclosed by Smith, and that Koster and Smith render claims 19–24 obvious. *Id.* 51–55.

Petitioner concedes that Koster does not describe expressly “the specific hardware used to implement the snoop filter,” but asserts that “it would have been obvious to one having ordinary skill in the art at the time of the ’121 patent to implement the snoop filter . . . as an application-specific integrated circuit (ASIC).” *Id.* at 52 (citing Ex. 1014 ¶ D-32). According to Petitioner, ASICs can “reduce cost and improve reliability” of a microelectronic system and “a chip designed to handle the interface between memory and a microprocessor,” such as the snoop filter, “is appropriately designed as an ASIC.” *Id.* (quoting Ex. 1008, 3–4); Ex. 1014 ¶¶ D-33–D-35. Petitioner further points out that Smith describes using design software to layout and simulate the design of an ASIC and a person of ordinary skill in the art would understand that this would produce data structures stored on one or more computer readable mediums, as recited in claim 19. *Id.* at 53–54 (quoting Ex. 1008, 16–18); Ex. 1014 ¶ D-37. In addition, Petitioner asserts that “Smith teaches that there must be a set of semiconductor masks

representative of at least a portion of the memory controller,” as recited in claim 24. *Id.* at 54–55 (citing Ex. 1008, 28); Ex. 1014 ¶ 39.

We have reviewed the evidence and arguments presented in the Petition, Patent Owner’s Response, and Petitioner’s Reply. Based on that review, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that all of the limitations of each of claims 19–24 are taught by, or rendered obvious in view of the teachings of Koster and Smith, and that each of these claims, considered as a whole, would have been obvious over the combination of Koster and Smith. Pet. 37–38, 51–55; PO Resp. 34–35; Pet. Reply 1–8. With respect to claims 19–24, we find Petitioner’s citations and arguments persuasive, and we adopt them as the basis for our decision. Pet. 19–20, 25–28; Reply 19.

Patent Owner argues that “[a]s discussed in Section III.A.1 above, Koster fails to disclose the ‘probe filtering information representative of states’ limitation of claim 1. Since claim 16 includes this same limitation, and since claims 19–24 depend from claim 16, Koster cannot disclose this limitation of dependent claims 19–24. Nor do the Petitioners allege that Smith discloses this missing limitation.” PO Resp. 34. For the reasons discussed above in our analysis of the “states” limitation, we find this argument unpersuasive.

In sum, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 19–24 would have been obvious over Koster and Smith.

E. Patent Owner’s Motion to Amend Claims

Because we determine that claims 19–24 are unpatentable, we turn to Patent Owner’s contingent request to enter proposed, amended claims 29–

34.⁹ Mot. 1. Patent Owner states that each of the proposed substitute claims 29–34 were drafted “by first converting the respective original claim 19–24 to independent form, and then adding the same proposed new limitations.”

Mot. 2. The new limitations are as follows:

wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface

Id.

Claim 29 is illustrative of the proposed substitute claims and is reproduced below. Language added to convert claim 19 into independent form is underlined and the proposed new limitations are underlined and italicized.

29. (Proposed Conditional Substitute for Challenged Claim 19) At least one computer-readable medium having data structures stored therein representative of a probe filtering unit of claim 16 for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, *wherein said states comprise cache*

⁹ Patent Owner’s Motion to Amend refers to “[p]roposed substitute claims 19-34,” but then explains that “Patent Owner’s claim appendix begins numbering the substitute claims at claim 29, and concludes at claim 34, and leaves claims 26-28 blank.” Mot. 1, n.1. Accordingly, we interpret the reference to claims “[p]roposed substitute claims 19-34” as a typographical error.

coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

Ex. 2018, 2.¹⁰

As the moving party, Patent Owner bears the burden of proof to establish that it is entitled to the relief requested. *See* 37 C.F.R. § 42.20(c). Entry of proposed amendments is not automatic, but occurs only upon the patent owner having met the requirements of 37 C.F.R. § 42.121 and demonstrating, by a preponderance of the evidence, the patentability of the proposed substitute claims. *Nike, Inc. v. Adidas AG*, No. 2015-1719, 2016 WL 537609, at *3–*5 (Fed. Cir. Feb. 11, 2016) (“[T]he Board did not err by placing the burden on [Patent Owner] to establish patentability over the prior art of [Patent Owner]’s proposed substitute claims.”); *see Idle Free Sys., Inc. v. Bergstrom, Inc.*, IPR2012-00027, slip op. at 7–8 (PTAB June 11, 2013) (Paper 26, “*Idle Free*”) (informative). For the reasons explained below, we conclude that Patent Owner has not met its burden with respect to proposed substitute claims 29–34.

A motion to amend claims must clearly identify the support for the proposed substitute claims. In particular, 37 C.F.R. § 42.121(b)(1) requires the patent owner to set forth the support in the original disclosure of the

¹⁰ Ex. 2018 appears to be a duplicate of the exhibit filed in IPR2015-00159 instead of the exhibit referred to in the motion and begins numbering substitute claims at claim 26. Mot. 1 n.1 (“Patent Owner’s claim appendix begins numbering the substitute claims at claim 29 . . . and leaves claims 26–28 blank.”). However, because proposed claims 29–34 are identical in the two cases, the filing mistake has no impact on our decision.

patent for each proposed substitute claim. Similarly, under 37 C.F.R. § 42.121(b)(2), the patent owner must set forth the support in an earlier-filed disclosure for each claim for which benefit of the filing date of the earlier filed disclosure is sought. 35 U.S.C. § 112 ¶ 1¹¹ sets forth an enablement requirement, providing that the specification shall describe “the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the [invention].”¹² *Automotive Techs. Int’l v. BMW of N. America, Inc.*, 501 F.3d 1274, 1282 (Fed. Cir. 2007). This requirement is satisfied when “one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation.” *Id.* (internal quotation marks omitted).

Patent Owner asserts that written description support for the proposed substitute claims, including each of the newly proposed limitations, is found in the originally filed application leading to the ’121 patent, U.S. Patent Application No. 10/966,161 (Ex. 1021, “the ’161 Application”), as well as

¹¹ Section 4(c) of the AIA re-designated 35 U.S.C. § 112 ¶ 1, as 35 U.S.C. § 112(a). Because the ’121 patent has a filing date before September 16, 2012 (effective date), we will refer to the pre-AIA version of 35 U.S.C. § 112.

¹² 35 U.S.C. § 316(d)(3) provides that an amendment under 35 U.S.C. § 316(d) may not enlarge the scope of the claims of the patent or introduce new matter. Similar to 35 U.S.C. § 132’s prohibition on adding new matter to claim amendments, the prohibition of new matter in proposed substitute claims places a burden on the moving party to show those claims adhere to the requirements of 35 U.S.C. § 112, ¶ 1. *See Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1348 (Fed. Cir. 2010) (en banc) (“[P]rohibiting adding new matter to the claims has properly been held enforceable under § 112, first paragraph.”).

priority document U.S. Patent Application No. 10/288,347 (Ex. 1022, “the ’347 Application”).¹³ Mot. 3–10.

Specifically, Patent Owner asserts that the new limitation “wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface” (“the protocol interface limitation”) is supported by both the ’161 Application and the ’347 Application. *Id.* at 9–10. Patent Owner points to Figure 3, reproduced below, which is substantively identical in both the ’161 and ’347 Applications and in the ’121 patent. *Id.* at 9.

Figure 3

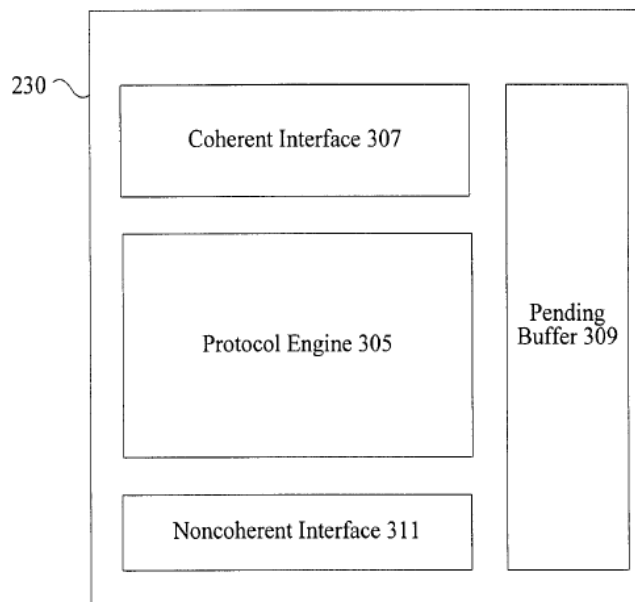


Figure 3 shows an example interconnection controller 230, including protocol engine 305 “configured to handle packets such as probes and

¹³ Each page of Ex. 1021 and 1022 has two page numbers on the bottom. For purposes of this decision, our references to these exhibits use the bottom-most page number.

requests received from processors in various clusters of a multiprocessor system.” Ex. 1021, 13:28–31; Ex. 1022, 12:20–23; Ex. 1001, 7:53–58. Interconnection controller 230 also includes “Coherent Interface 307” and “Noncoherent Interface 311.” Ex. 1021, 14:11–15; Ex. 1022, 13:4–10; Ex. 1001, 8:5–11. In addition, Patent Owner relies on several lines of text associated with Figure 3 in the ’161 and ’347 Applications. Mot. 9; Ex. 1021, 13:22–14:21; Ex. 1022, 11:14–12:14; Ex. 1001, 7:44–48, 8:5–14.

Petitioner argues that the disclosure relied upon by Patent Owner does not properly enable the protocol interface limitation, but instead “simply illustrates the broad proposition that the cache coherence controller ‘can also include other interfaces such as a non-coherent protocol interface 311 for communicating with I/O devices.’” Paper 41 (“Opp. Mot.”), 5 (quoting Ex. 1001, 8:8–11). According to Petitioner, the disclosure “identifies where the non-coherent protocol interface is located, but provides no details for how it is implemented.” *Id.*

We agree with Petitioner that Patent Owner has not met its burden to show that its proposed substitute claims meet the enablement requirement of § 112 ¶ 1. More specifically, we agree that Patent Owner has not shown that the Specifications of the ’161 or ’347 Applications enable the protocol interface limitation recited by each of the proposed substitute claims.

Considering first the Specifications of the ’161 and ’347 Applications, although Patent Owner points to several lines and one figure as describing the limitation, these disclosures simply identify the existence of a cache coherency controller with both a coherent and non-coherent protocol interface without providing any detail of how such a cache coherency controller would be implemented. *See* Ex. 1021, 12:20–23, 13:11–17;

Ex. 1022, 12:12–15, 13:4–10; Ex. 1001, 7:44–48, 8:5–14. Figure 3 represents a concept of a cache coherence controller with two interfaces—but lacks any details that would show one skilled in the art how to make or use a cache coherence controller with two interfaces. See Ex. 2021, Fig. 3; Ex. 2022, Fig. 3. The Specifications describe Figure 3 as a “diagrammatic representation” of a cache coherence controller, and does not purport to show details of how the two interfaces would be implemented together in such a controller. See Ex. 1021, 6:17, 13:28–14:21; Ex. 1022, 6:16, 12:20–13:14; Ex. 1001, 3:23–24, 7:53–8:19. This is supported by the testimony of Dr. Oklobdzija, who testified that Figure 3 (along with Figures 2 and 17 of the ’121 patent) does not provide details regarding how to implement a coherent and non-coherent interface and instead “le[aves] someone . . . with . . . ordinary skill in the art to . . . figure it out.” Ex. 1026, 90:5–93:1, 95:14–96:10. Dr. Oklobdzija also agreed that “one of ordinary skill would not have already had in their knowledge how to build a system with [both] interface[s].” *Id.* at 90:5–17.

Moreover, the textual discussion of Figure 3, which is the only description of the protocol interfaces relied upon by Patent Owner, provides scant detail concerning how a cache coherence controller with both interfaces is built or operated. The Specifications state the following:

The cache coherence controller 230 can also be configured to handle a non-coherent protocol to allow communication with I/O devices. In one embodiment, the cache coherence controller 230 is a specially configured programmable chip such as a programmable logic device or a field programmable gate array.

Figure 3 is a diagrammatic representation of one example of a cache coherence controller 230. According to various embodiments, the cache coherence controller includes a protocol engine 305 configured to handle packets such as probes and

requests received from processors in various clusters of a multiprocessor system. . . .

. . .

The cache coherence controller has an interface such as a coherent protocol interface 307 that allows the cache coherence controller to communicate with other processors in the cluster as well as external processor clusters. According to various embodiments, each interface 307 and 311 is implemented either as a full crossbar or as separate receive and transmit units using components such as multiplexers and buffers. The cache coherence controller can also include other interfaces such as a non-coherent protocol interface 311 for communicating with I/O devices. It should be noted, however, that the cache coherence controller 230 does not necessarily need to provide both coherent and non-coherent interfaces. It should also be noted that a cache coherence controller in one cluster can communicate with a cache coherence controller in another cluster.

Ex. 1022, 11:14–12:14; *see* Ex. 1021, 13:22–14:21; Ex. 1001, 7:44–8:19.

This general description fails to provide a structure or description of how a person having ordinary skill in the art would make or use a cache coherence controller with both types of interfaces. The most detailed language— “[i]n one embodiment, the cache coherence controller 230 is a specially configured programmable chip such as a programmable logic device or a field programmable gate array” and “[a]ccording to various embodiments, each interface 307 and 311 is implemented either as a full crossbar or as separate receive and transmit units using components such as multiplexers and buffers”—does not specifically describe how to implement the system. Instead, as confirmed by Dr. Oklobdzia, the sentence related to the cache coherence controller 230 “gives kind of [a] suggestion to – that this can be implemented as a programmable chip” and the sentence describing implementation of the interfaces is simply an “implementation hint.”

Ex. 1026, 100:18–102:20. According to Dr. Oklobdzija, the implementation details are “up to the engineers to – to figure out further.” *Id.* at 101:10–20.

Indeed, Dr. Oklobdzija testified that prior to the filing date of the ’121 patent, a person of ordinary skill in the art would not have known to use *both* a coherent interface *and* a non-coherent interface at once. Ex. 2019 ¶ 11–12. Specifically, Dr. Oklobdzija testifies that, a reference that “reflects the state of the art of coherent and non-coherent interfaces” as of the alleged effective filing date of the ’121 patent indicated that a system could use only one or the other of a coherent or non-coherent interface, but not both. *Id.* ¶ 12. Noticeably absent in Patent Owner’s Motion is reference to any detailed discussion in the ’121 patent of the how the cache coherence controller would operate with both interfaces at once, let alone such full, clear, concise, and exact terms as to enable any person skilled in the art, to make and use the system. Given the testimony of Dr. Oklobdzija, we cannot determine that Figure 3 and the few corresponding lines of description apprise one of ordinary skill how to make and use a cache coherence controller with both a coherent and non-coherent protocol interface. *See Automotive Techs.*, 501 F.3d at 1281–85 (holding that electronic sensors were not enabled because the specification’s general description failed to provide a structure or description of how a person having ordinary skill in the art would make or use the sensor).

This is true despite Dr. Oklobdzija’s conclusory statement to the contrary. Ex. 2042 (Reply Declaration) ¶ 7 (“[B]ased simply on my review during the deposition itself, I believed, and I continue to believe, that the specification of the ’121 Patent contains a number of ‘implementation hint[s]’ which would enable one of skill in the art to practice the ‘coherent

protocol interface’ and ‘non-coherent protocol interface’ limitations without undue experimentation.”). “It is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of an invention in order to constitute adequate enablement.” *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1366 (Fed.Cir.1997). Although the knowledge of one skilled in the art is relevant, the novel aspect of an invention must be enabled in the patent. As noted above, according to Dr. Oklobdzija, prior to filing of the ’121 patent, it was suggested that a system could use only one or the other of a coherent or non-coherent interface, but not both. Ex. 2019 ¶¶ 11–12.

Given that the allegedly novel aspect of the invention is a cache coherence controller that uses both interfaces, which was unknown to a person of ordinary skill at the time, it is insufficient to merely provide “implementation hints” using known technologies to create that novel cache coherence controller. As was the case in *Genentech*, the portions of the Specifications of the ’347 and ’161 Applications relied upon by Patent Owner here provide “only a starting point, a direction for further research” on using a probe filtering unit with both protocol interfaces; they do not provide guidance to a person of ordinary skill in the art on how to make or use such system. 108 F.3d at 1366. Patent Owner, thus, fails to show that the Specifications of the ’347 and ’161 Applications provide “reasonable detail” sufficient to enable use of a probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface. *Id.*

We conclude that Patent Owner has not met its burden of showing that the protocol interface limitation is properly enabled under 35 U.S.C. § 112 ¶ 1.

Furthermore, because of the manner in which Patent Owner's Motion addresses Koster, Patent Owner's failure to demonstrate enablement of the proposed substitute claims results in a failure to demonstrate novelty and non-obviousness of the proposed substitute claims. When arguing how the limitations of the proposed substitute claims distinguish them from the disclosures of the references of record, Patent Owner's Motion addresses Koster only by asserting that "[a]s to . . . Koster . . . , because, as discussed above, all of the substitute claims find support in the '347 Application, . . . Koster . . . is not prior art to any of the proposed substitute claims." Mot. 22. Because Patent Owner does not persuade us that the proposed substitute claims are enabled by the disclosure in the '347 Application, we find unpersuasive Patent Owner's suggestion that the proposed substitute claims are entitled to the filing date of the '347 Application. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) ("For a patent to claim priority from the filing date of its provisional application, it must satisfy 35 U.S.C. § 119(e)(1) (2006) 'In other words, the Specification of the *provisional* must 'contain a written description of the invention and the manner and process of making and using it, in such full, clear, concise, and exact terms,' 35 U.S.C. § 112 ¶ 1, to enable an ordinarily skilled artisan to practice the invention *claimed* in the *non-provisional* application.") (quoting *New Railhead Mfg., L.L.C. v. Vermeer Mfg. Co.*, 298 F.3d 1290, 1294 (Fed. Cir. 2002)); *Hyatt v. Boone*, 146 F.3d 1348, 1352 (Fed. Cir. 1998) ("The earlier application must contain a written description of the subject matter of the interference count, and must meet the enablement requirement."); *see also Novo Nordisk Pharm., Inc. v. Bio-Tech. Gen. Corp.*, 424 F.3d 1347, 1359 (Fed. Cir. 2005) ("The issue of

whether the 1983 PCT application was enabled was critical to the prosecution because, if the application was not enabled, Novo would not be able to rely upon the application's priority date to overcome the Brewer patent."). Accordingly, we also find unpersuasive Patent Owner's assertion that Koster is not prior art to the proposed substitute claims. With no other basis for asserting that the proposed substitute claims patentably distinguish over Koster (by itself or in combination with other references of record), we conclude that Patent Owner has not met its burden of demonstrating patentability of the proposed substitute claims over the references of record.

Thus, Patent Owner has not met its burden for proposed substitute claims 29–34.

CONCLUSION

For the reasons explained above, we determine the following:

- (1) Petitioner has demonstrated by a preponderance of the evidence that claims 4–6 would have been anticipated by Koster;
- (2) Petitioner has demonstrated by a preponderance of the evidence that claims 19–24 would have been obvious over Koster and Smith;
- (3) Petitioner has not demonstrated that claims 11 and 12 would have been anticipated by Koster; and
- (4) Patent Owner has not shown that its proposed substitute claims 29–34 are enabled or patentable over the prior art.

ORDER

Accordingly, it is

ORDERED that claims 4–6 and 19–24 of the '121 patent have been shown to be *unpatentable*; and

FURTHER ORDERED that Patent Owner's motion to amend is *denied*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Case IPR2015-00163

Patent 7,296,121 B2

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