

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.,
Petitioner,

v.

ATI TECHNOLOGIES ULC,
Patent Owner.

Case IPR2015-00327
Patent 6,897,871 B1

Before JONI Y. CHANG, BRIAN J. McNAMARA, and
JAMES B. ARPIN, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

DECISION

Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

BACKGROUND

LG Electronics, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) to institute an *inter partes* review of claims 1–3, 5, 6, 8–11, 13, 15, 17, 18, and 20 (the “challenged claims”) of U.S. Patent No. 6,897,871 B1 (Ex. 1101, “the ’871 Patent”). 35 U.S.C. § 311. The Petition identifies LG Electronics U.S.A., Inc. and LG Electronics MobileComm U.S.A., Inc. as real parties-in-interest with Petitioner. ATI Technologies ULC (“Patent Owner”) filed a Preliminary Response (Paper 12, “Prelim. Resp.”), contending that the Petition should be denied as to all challenged claims. We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons described below, we do not institute an *inter partes* review on the grounds advanced in the Petition.

PENDING LITIGATION

The ’871 Patent is the subject of a patent infringement lawsuit brought by Patent Owner, against Petitioner in *Advanced Micro Devices, Inc. v. LG Electronics, Inc.*, Case No. 3:14-cv-01012-SI, in the Northern District of California. Petitioner has filed a second petition for *inter partes* review of the ’871 Patent (“the Companion Case”). See IPR2015-00326, Paper 2.

THE ’871 PATENT (EXHIBIT 1001)

In computer graphics systems, a three-dimensional shape is represented by collection of simple polygons called “primitives.” Ex. 1101, col. 1, ll. 11–12. Primitives are formed by the interconnection of individual

pixels. *Id.* at col. 1, ll. 15–17. Color and texture are applied to the individual pixels that comprise the shape based on their location within the primitive and the primitive's orientation relative to the generated shape. *Id.* at col. 1, ll. 17–19.

A three dimensional shape represented by a wireframe collection of primitives is transformed into colored images by two graphics-processing operations: (i) vertex operations and (ii) pixel operations. Prelim. Resp. 3 (citing Ex. 1101, col. 1, ll. 11–60). To orient the wireframe model as desired, matrix transformations applied to vertices V_x , V_y , V_z of the primitives generate new vertices $V_{x'}$, $V_{y'}$, $V_{z'}$, which then are translated into pixels to generate a rendered object that can be displayed as a two dimensional image. Prelim. Resp. 4 (citing Ex. 1101, col. 1, ll. 36–49). Pixel operations performed on each pixel of the rendered object determine the pixel's color and appearance. *Id.* (citing Ex. 1101, col. 1, ll. 50–54).

Conventional graphics processors include “shaders” that specify how and with what corresponding attributes a final image is generated on a screen or other device. Ex. 1101, col. 1, ll. 24–27. Conventional graphics processors require both a vertex shader and a pixel shader to render an object. *Id.* at col. 1, ll. 61–62. A vertex shader accepts as inputs the data representing the vertices V_x , V_y , V_z , applies the matrix transformation, and provides angularly oriented vertices $V_{x'}$, $V_{y'}$, $V_{z'}$. A pixel shader operating at the pixel level provides the color value associated with each pixel of the rendered object. *Id.* at col. 1, ll. 50–54.

The '871 Patent employs a unified shader capable of performing both vertex operations and pixel operations. *Id.* at col. 2, ll. 37–39. A multiplexer receives vertex data at a first input, and pixel parameter data and

attribute data from a rasterization engine at a second input. *Id.* at col. 3, ll. 60–65. In response to a control signal, an arbiter circuit selects one of a plurality of inputs for processing, and a shader coupled to the arbiter performs vertex operations or pixel operations based on the selected one of the inputs. *Id.* at col. 2, ll. 41–49. A control signal generated by the arbiter determines which of the two multiplexer inputs is provided to the unified shader. *Id.* at col 3, l. 65–col. 4, l. 1. According to an arbitration scheme implemented in the arbiter, vertex data at the first input is transmitted to the unified shader if there are sufficient resources available in the unified shader to operate on the vertex data; otherwise interpolated pixel data on the second multiplexer input is passed to the unified shader. *Id.* at col. 4, ll. 2–8.

The unified shader includes a general purpose register for storing the plurality of selected inputs, a sequencer for storing logical and arithmetic instructions used to perform vertex and pixel manipulation operations, and a processor capable of executing both floating point arithmetic and logical operations on the selected inputs according to the instructions stored in the sequencer. *Id.* at col. 2, ll. 50–57. According to the arbitration scheme, if the general purpose register in the unified shader does not have sufficient space to store incoming vertex data, the arbiter does not transmit the vertex data. *Id.* at col. 5, ll. 23–26. Instead instructions for pixel calculation operations are carried out in the unified shader until enough registers become available to perform vertex operations. *Id.* at col. 5, ll. 29–33. When vertex data is transmitted to the unified shader, the resulting vertex data is transferred to a render back end block that converts the resulting vertex data to a format suitable for display. *Id.* at col. 5, ll. 54–59.

ILLUSTRATIVE CLAIM

Claim 1, which is drawn to a graphics processor, and claim 15, which is drawn to a unified shader, are reproduced below and are illustrative:

1. A graphics processor, comprising:
an arbiter circuit for selecting one of a plurality of inputs in response to a control signal; and
a shader, coupled to the arbiter circuit, operative to process the selected one of the plurality of inputs, the shader including means for performing vertex operations and pixel operations, and performing one of the vertex operations or pixel operations based on the selected one of the plurality of inputs, wherein the shader provides a [sic] appearance attribute.

15. A unified shader, comprising:
a general purpose register block for maintaining data;
a processor unit; and
a sequencer, coupled to the general purpose register block and the processor unit, the sequencer maintaining instructions operative to cause the processor unit to execute vertex calculation and pixel calculation operations on selected data maintained in the general purpose register block.

ART CITED IN PETITION

Name	Reference Identification	Date	Exhibit No.
Stuttard	US 7,363,472 B2	Apr. 22, 2008	Ex. 1104
Owens	Polygon Rendering on a Stream Architecture	2000	Ex. 1105
Kizhepat	US 7,376,811 B2	May 20, 2008	Ex. 1106
Kurihara	US 5,500,939	Mar. 19, 1996	Ex. 1107
Open GL	The Open GL	July 24, 2002	Ex. 1108

	Graphics System: A Specification (Version 1.4)		
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GROUND S ASSERTED IN PETITION

Claims	Basis	References
1, 2, 5, 13 and 15	35 U.S.C. § 102 (e)	Stuttard
3, 6, 8, 10, and 11	35 U.S.C. § 103 (a)	Stuttard in view of Open GL
9, 17, and 18	35 U.S.C. § 103 (a)	Stuttard in view of Kizhepat
20	35 U.S.C. § 103 (a)	Stuttard in view of Kurihara
1, 2, 5, 6, 8, 13, 15, and 17	35 U.S.C. § 102 (b)	Owens
10 and 11	35 U.S.C. § 103 (a)	Owens
3	35 U.S.C. § 103 (a)	Owens in view of Open GL
9 and 18	35 U.S.C. § 103 (a)	Owens in view of Kizhepat
20	35 U.S.C. § 103 (a)	Owens in view of Kurihara

CLAIM CONSTRUCTION

This proceeding concerns the same patent and claims as those challenged in related case IPR2014-00326. *LG Electronics, Inc. v. ATI Technologies ULC*, Case IPR2015-00326. We adopt the same claim constructions in this proceeding:

Including/includes

Petitioner contends that we should construe the term “including/includes,” e.g., as reflected in the claims, to mean “contains or

connected to” because the Specification discloses that the recited element in claim 18, i.e., a multiplexer, is connected to a shader, rather than being a part of a shader. Pet. 8–9. Patent Owner contends that the ordinary meaning should apply and that “including/includes” should be construed to mean “contains.” Prelim. Resp. 17–19. Claim 15 recites a shader, claim 17 recites the shader of claim 15 “further including a selection circuit,” and claim 18 recites the shader of claim 17 “wherein the selection circuit is a multiplexer and the control signal is provided by an arbiter.” These claims are facially clear and we are not persuaded that we should construe “including” to have any meaning other than its ordinary meaning, i.e., that the shader in claim 17 is limited to one having a selection circuit, and in claim 18 the shader is limited to one in which the selection circuit is a multiplexer and an arbiter supplies the control signal.

Means for performing vertex operations and pixel operations (and performing one of the vertex operations or pixel operations based on the selected one of the plurality of inputs)

We construe the “means for performing vertex operations and pixel operations and performing one of the vertex operations or pixel operations based on the selected one of the plurality of inputs” to include *a register, an instruction sequencer capable of providing instructions for performing vertex operations and pixel operations, and a processor capable of floating point, arithmetic, and logical operations on a selected input.*

Arbiter circuit

Claim 1 functionally recites the arbiter as a structure that can be used for selecting one of a plurality of inputs in response to a control signal. Thus, claim 1 itself defines the arbiter circuit and no further construction of the term is required. Although claim 1 does not require that the arbiter itself

generate the control signal, claim 18 recites that “the control signal is provided by the arbiter.” However, neither claim 1 nor claim 18 recites an arbitration scheme, as urged by Patent Owner. Thus, we construe the term “arbiter” as used in claim 18 to mean *a circuit for selecting one of the plurality of inputs*.

ISSUES UNDER 35 U.S.C. § 325(d)

Introduction

Patent Owner contends that we should exercise our discretion and decline to institute a trial of Petitioner’s challenges based on Stuttard and Owens because Petitioner presents arguments that are substantially the same as the argument Petitioner advanced in the Companion Case. Prelim. Resp. 20–24. Patent Owner notes that Petitioner relies primarily on four references, Lindholm¹ and Rich² in the Companion Case (IPR2015-00326) and Stuttard and Owens in this proceeding (IPR2015-00327). *Id.* at 20–22.

Stuttard

Petitioner states that Stuttard discloses a graphics system that first receives vertex data from a host system, in which a processing element (“PE”) performs geometric processing and the transformed vertex data is output from the PEs to local memory to be sorted by region by binning units. Pet. 13 (citing Ex. 1104, col. 9, ll. 61–62; col. 10, ll. 4–5; col. 7, ll. 24–27). Petitioner notes that, in Stuttard’s graphics processing pipeline, the transformed vertex data is sent back from the local memory and rasterization is performed on the sorted data via a mathematical evaluation (“MME”)

¹ U.S. Patent No. 7,015,913 B1, issued Mar. 21, 2006 to Lindholm et al. (“Lindholm”).

² U.S. Patent No. 5,808,690 to Rich, issued Sept. 15, 1998.

circuit. *Id.* at 13–14. Petitioner contends that the transformed data and the original data correspond to the plurality of inputs and that after the MME processes the data into pixel data, additional processing can be carried out by the PEs on the pixels within a primitive. *Id.* at 14. Petitioner further contends that “because the thread manager 102 controls both the type of data (*via* channel controller 108) and the instructions (*via* array controller 104) associated with the type of data provided to processing elements 1061, the thread manager 102 corresponds to the claimed ‘*arbiter circuit*’ of claim 1.” *Id.* at 15.

Patent Owner contends that Stuttard’s system operates in discrete, sequential phases, such that pixel operations occur only after completion of geometric processing. Prelim. Resp. 28. In our analysis of Rich in the Decision to Institute for the Companion Case, we considered the implications of a system in which vertex and pixel operations are performed sequentially. *LG Electronics, Inc. v. ATI Technologies ULC*, Case IPR2015-00326, slip op. at 22–23 (PTAB July 10, 2015)(Paper 13). As a sequential system, the input selected and the corresponding instructions executed depend on what step of the processing sequence is underway. Thus, the performance of vertex operations and pixel operations is not based on the selected one a plurality of inputs; instead the selection of the input is based on whether vertex or pixel operations are being executed.

There is extensive overlap in the challenges based on Stuttard in this Petition, and those in the Companion Case based on Rich. *See LG Electronics, Inc. v. ATI Technologies ULC*, Case IPR2015-00326, slip op. at 21–23 (PTAB July 10, 2015)(Paper 13) (discussing Rich). The sequential performance of vertex and pixel operations in the system disclosed by

Stuttard is similar to the system disclosed by Rich, which also performs vertex and pixel operations in sequence. *Id.* Petitioner does not address why Stuttard would be applied differently from Lindholm or Rich, or explain why its challenges based on Stuttard are not based on substantially the same arguments as those advanced in the Companion Case concerning Rich or Lindholm.

Owens

Petitioner contends that Owens uses a stream programming model in which “separate kernels can run on multiple nodes of a system while data flows in streams from one node to another.” Pet. 40 (citing Ex. 1105, 25). Noting that parallel ALU clusters perform both vertex and pixel operations, Petitioner contends that, in Owens, each ALU cluster performs both vertex and pixel operations and that instructions from the stream controller via the host processor will sequence and issue stream operations that will select the streams that will be sent to the ALU clusters. *Id.* at 42 (citing Ex. 1105, 25). Petitioner also argues that the stream controller discloses the claimed arbiter circuit because the stream controller controls microcontrollers to provide the program kernels that operate on the streams. *Id.* Patent Owner responds that Owens does not state that the stream controller selects streams. Prelim. Resp. 35. Patent Owner argues that Owens states only that the stream controller communicates with the host and sequences and issues stream operations, meaning only that the stream controller places those operations in some sequence or order. *Id.*

In our analysis of Lindholm in the Decision to Institute in the Companion Case, we addressed the implications of *parallel* execution pipelines that perform either vertex or pixel processing. *LG Electronics, Inc.*

v. ATI Technologies ULC, Case IPR2015-00326, slip op. at 11–15 (PTAB July 10, 2015) (Paper 13). As discussed above, Petitioner notes that Owens discloses parallel ALUs that perform vertex and pixel processing. Pet. 40. In the Companion Case, we discussed in detail how, in Lindholm, an execution pipeline determines whether resources and inputs are available to conduct vertex or pixel processing and, based on that determination, selects inputs and executes vertex or pixel operations accordingly. *LG Electronics, Inc. v. ATI Technologies ULC*, Case IPR2015-00326, slip op. at 12–14 (PTAB July 10, 2015) (Paper 13). In this Petition, Petitioner provides only general statements, which Patent Owner disputes, as to how Owens selects a data stream. Prelim. Resp. 35 (citing Pet. 42). Petitioner does not address how Owens is applied differently from either Lindholm or Rich or explain why its challenges based on Owens are not based on substantially the same arguments as those advanced in IPR2015-00326 concerning Rich or Lindholm.

We have discretion to decline to institute *inter partes* review. See 35 U.S.C. § 314(a) (institution is discretionary, not mandatory); 37 C.F.R. § 42.108(a) (“[T]he Board *may* authorize the review to proceed on all or some of the challenged claims and on all or some of the grounds of unpatentability asserted for each claim.”; emphasis added). All of the challenges in this proceeding are based on Stuttard and Owens, alone or in combination with other references. We have reviewed the similarities between the disclosures in Stuttard and Owens and the disclosures in Rich and Lindholm in the Companion case, as well as the arguments advanced by Petitioner in each case. “In determining whether to institute or order a proceeding under . . . chapter 31, the Director may take into account

whether, and reject the petition or request because, the same or substantially the same *prior art or arguments* previously were presented to the Office.”

35 U.S.C. § 325(d) (emphasis added). We approach our discretion to decline review on a case-by-case basis. *Conopco, Inc. v. Procter & Gamble Co.*, Case IPR2014-00628, slip op. at 10 (PTAB Oct. 20, 2014) (Paper 21). In consideration of the above, we find that at least the arguments advanced by Petitioner concerning Stuttard and Owens are the same or substantially the same as those advanced by Petitioner concerning Lindholm and Rich in IPR2015-00326. Therefore, we exercise our discretion and decline to institute a trial on Petitioner’s challenges in this proceeding.

ORDER

In consideration of the foregoing, we do not institute *inter partes* review in this proceeding.

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