

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.,
Petitioner,

v.

ADVANCED MICRO DEVICES, INC.,
Patent Owner.

Case IPR2015-00329
Patent 6,266,715 B1

Before BRIAN J. MCNAMARA, RAMA G. ELLURU, and
JAMES B. ARPIN, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

DECISION
Denying Request for Rehearing
37 C.F.R. § 42.71(d)

I. INTRODUCTION

LG Electronics, Inc. (“Petitioner”) filed a Petition (Paper 2 (“Pet.”)) to institute an *inter partes* review of claims 1, 10, 13, 22, 24, and 25 (the “challenged claims”) of Patent No. US 6,266,715 B1 (Ex. 1001, “the ’715 patent”), pursuant to 35 U.S.C. §§ 311–319. Pet. 1. Petitioner challenged these claims of the ’715 patent on the following three grounds (Pet. 14–58):

Claims	Grounds	References
1, 10, and 25	35 U.S.C. § 103(a)	USBN9602 (Ex. 1004) and Intel 8237 (Ex. 1006)
1, 10, and 25	35 U.S.C. § 103(a)	EIFUFAL501 (Ex. 1009) and Intel 8237 (Ex. 1006)
1, 10, 13, 22, 24, and 25	35 U.S.C. § 103(a)	USB97C100 (Ex. 1011) and Dunninghoo (Ex. 1013)

Advanced Micro Devices, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 12; “Prelim. Resp.”).

For the reasons discussed in our Decision on Institution (Paper 13, “Dec. on Inst.”), we denied institution of an *inter partes* review of any of the challenged claims. Pursuant to 37 C.F.R. § 42.71(d), Petitioner filed a Request for Rehearing (Paper 14, “Reh’g Req.”), seeking reconsideration of our Decision on Institution. For the reasons set forth below, Petitioner’s Request for Rehearing is *denied*.

II. DISCUSSION

37 C.F.R. § 42.71(d) provides that:

A party dissatisfied with a decision may file a request for rehearing, without prior authorization from the Board. The burden of showing a decision should be modified lies with the party challenging the decision. *The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place*

where each matter was previously addressed in a motion, opposition, or a reply.

(Emphasis added.) When rehearing a Decision on Institution, the Board reviews the decision for an abuse of discretion. 37 C.F.R. § 42.71(c).

Petitioner asserts three bases for its Request for Rehearing. Reh’g Req. 1–2. First, Petitioner argues that we overlooked or misapprehended evidence regarding the proper construction of the claim limitation: “a plurality of USB endpoints, each selectively programmed for one of the/a plurality of DMA channels during the DMA mode of the USB controller,” and, consequently, we failed to give that limitation its “broadest reasonable interpretation.” *Id.* at 2–4. Second, Petitioner argues that we overlooked or misapprehended evidence with respect to whether the combination of the teachings of USBN9602 and Intel 8237 would have rendered the subject matter of certain challenged claims obvious. *Id.* at 4–6. Third, Petitioner argues that we misapprehended or overlooked evidence with respect to whether the combination of the teachings of USB97C100 and Dunnihoo would have rendered the subject matter of certain challenged claims obvious. *Id.* at 6–11.

1. Claim Construction

With regard to its first basis, Petitioner argues that we improperly narrowed our construction of the limitation: “a plurality of USB endpoints, each selectively programmed for one of the/a plurality of DMA channels during the DMA mode of the USB controller” by requiring that each USB endpoint be programmed for a different DMA channel. Reh’g Req. 3. In particular, Petitioner argues that, because we adopted a construction that was “consistent with the Specification of the ’715 Patent” (*id.* (quoting Dec. on Inst. 18)), we adopted a construction that was narrower than the “broadest reasonable construction” and that improperly imported limitations from the Specification into the claim limitation (*id.*).

In our Decision on Institution, we noted that “[t]here is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the specification. *See In re Translogic Tech. Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).” Dec. on Inst. 7. Consequently, we began our construction with the plain and ordinary meaning of the limitations of the claim. As we explained in the Decision on Institution,

Claims 1 and 25 recite “a plurality of USB endpoints, *each selectively programmed for one of [the/a] plurality of DMA channels during the DMA mode of the USB controller.*” Ex. 1001, col. 11, ll. 65–67, col. 13, ll. 40–42 (emphasis added). Petitioner acknowledges that, although this limitation may be construed to provide for each USB endpoint to be programmed for a *different* DMA channel, the claim language does not require that construction. Pet. 18. Instead, Petitioner suggests that limitation may be construed to provide for each USB endpoint to be programmed for the *same* DMA channel. *Id.* (citing Ex. 1003 ¶¶ 66, 67). We disagree.

Dec. on Inst. 17. We determined that, contrary to Petitioner’s assertion, the plain and ordinary meaning of the claim limitation requires each USB endpoint to be programmed for a different DMA channel. We then noted that that Dr. Bagherzadeh’s unsupported opinion testimony was unpersuasive, and that our assessment of the plain and ordinary meaning of this limitation was consistent with the disclosure in the Specification.¹ *Id.* at 17–18 (citing Ex. 1003 ¶¶ 66, 67 (“I believe that it is appropriate to disclose *how I read* the plain language of the claim.”) (emphasis added)). Thus, we did not overlook or misapprehend

¹ In its arguments with respect to each of the bases for its Request for Rehearing, Petitioner asserts that “the Patent Owner provided no expert testimony regarding its interpretation of this claim language but relied purely on attorney argument.” Reh’g Req. 3; *see id.* at 5–6, 9. However, Patent Owner may not present new testimonial evidence at this stage of the proceeding. 37 C.F.R. § 42.107(c).

Petitioner's evidence, but we were not persuaded that Petitioner's proposed construction is the broadest reasonable interpretation of this limitation. *Id.* at 18 (citing *Translogic Tech. Inc.*, 504 F.3d at 1257).

2. *Combination of the Teachings of USBN9602 and Intel 8237*

With regard to Petitioner's second basis, Petitioner argues that we improperly imported two additional limitations into our construction of the claims and then found that the proposed combination of the teachings of USBN9602 and Intel 8237 failed to teach or suggest those limitations. Reh'g Req. 4. In particular, Petitioner notes that we stated in our Decision on Institution that "such a combination [of USBN9602 and Intel 8237] only permits one of the plurality of endpoints of USBN9602 to be connected to one DMA channel of Intel 8237 *at a time.*" *Id.* (quoting Dec. on Inst. 19 (emphasis added by Petitioner)). Petitioner argues that this analysis improperly imports a "temporal limitation" into the claim. *Id.* Further, Petitioner notes that we stated in our Decision on Institution that "Petitioner's proposed combination of two USBN9602 controllers would not necessarily teach *the same Function Address for each of the plurality of endpoints.*" *Id.* (quoting Dec. on Inst. 19) (emphasis added). Petitioner argues that this analysis improperly imports a requirement that the "USB controller . . . have the same Function Address for all of the endpoints" into the claim. *Id.* at 5.

We determined that the proposed combination does not teach or suggest the existing limitation that each USB endpoint is programmed for a different DMA channel. Dec. on Inst. 19. Because "USBN9602 teaches that, '[a]ccording to the USB specification, up to 31 such endpoint pipes are supported at any given time, *each with the same Function Address*'" (Dec. on Inst. 20 (quoting Ex. 1004, 4)), we were persuaded that Petitioner failed to demonstrate that a person of ordinary skill in the art would have had reason to combine the two USBN9602 controllers

with one Intel 8237 controller in the manner proposed in the Petition to achieve the USB device, USB host, or USB controller, as recited in the challenged claims (*id.* at 19–20).

With respect to the combination of the teachings of two USBN9602 controllers and Intel 8237 controller, Petitioner argues that we were “mistaken as to how the USBN9602 controllers operate.” Reh’g Req. 5. In particular, Petitioner argues that two USBN9602 controllers “would only support a maximum of 14 total endpoints, “well below the maximum number of 31 endpoint pipes required by the USB specification.” *Id.* (citing Dec. on Inst. 19, 20). Nevertheless, Petitioner fails to show where this argument was raised in its Petition. *See* 37 C.F.R. § 42.71(d). In addition, Petitioner argues that “Patent Owner summarily asserts that a person of ordinary skill in the art would not add a second USBN9602 controller to the device because of the ‘significant modifications that would be required and that were contrary to prevailing market forces.’” *Id.* (citing Prelim. Resp. 28). Petitioner contends that Patent Owner’s arguments are unsupported and conclusory. *Id.* at 6. We did not rely, however, on Patent Owner’s argument, quoted by Petitioner, in reaching our decision; and Petitioner fails to show otherwise. We could not overlook or misapprehend arguments that Petitioner did not make or evidence that Petitioner did not present. Patent Owner’s arguments, upon which we did not rely, are not relevant to the reconsideration of our Decision on Institution.

3. Combination of the Teachings of USB97C100 and Dunnihoo

With regard to Petitioner’s third basis, Petitioner presents three arguments relating to the combination of the teachings of USB97C100 and Dunnihoo in support of its Request for Rehearing. Reh’g Req. 6–11. First, Petitioner argues that we misapprehended the relevance of Dunnihoo’s arbiter’s effect on the data path. *Id.* at 6–8. Second, Petitioner argues that we improperly concluded that

Petitioner's reason for combining the teachings of these references to increase the number of data paths between the USB device and the USB host was based on improper hindsight. *Id.* at 8–10. Third, Petitioner argues that we overlooked or misapprehended Petitioner's explanation of how each of the endpoints is programmed selectively for one of the plurality of DMA channels. *Id.* at 10–11.

a. Arbiter's Effect on the Data Path

For purposes of our Decision on Institution, we adopted Petitioner's construction of the limitation "DMA channel" to mean "a path for moving data *directly* to or from memory locations *without processor intervention*." Dec. on Inst. 8 (citing Pet. 11) (emphases added). Referring to Dunnihoo's Figure 3, Petitioner argues that Dunnihoo teaches a data path that extends from a first DMA controller, i.e., SIE DMA 86, to RAM 82 *via arbiter 84*. Reh'g Req. 7 (reproducing Ex. 1013, Fig. 3). Initially, we determined that, because data is moved between SIE DMA 86 and RAM 82 via arbiter 84, Dunnihoo does not describe a "path for moving data *directly* to or from memory locations." *Id.* (citing Dec. on Inst. 24–25).

In addition, Petitioner's declarant, Dr. Bagherzadeh, states that "[a]n arbiter acts as traffic control between the 8051 microcontroller [72], the Intel DMA Controller[, i.e., 8237 DMA Controller 74,] and the SIEDMA[, i.e., SIE DMA 86]." Ex. 1003 ¶ 98 (citing Ex. 1013, 12); *see also* Ex. 1013, claim 4 ("said arbiter arbitrates access of said first DMA controller, said second DMA controller and said microcontroller to said RAM"). We are persuaded that 8051 microcontroller 72, 8237 DMA Controller 74, or SIE DMA 86 are processors (Ex. 1013, col. 6, ll. 30–31; *see* Prelim. Resp. 41) or interfaces to processors (*see* Ex. 1006, 1), and that Dunnihoo's Figure 3 depicts each of these devices as providing input to arbiter 84. Contrary to Petitioner's assertion in the Request for Rehearing, we are not

persuaded that any of these devices, e.g., processors (Prelim. Resp. 41 (citing Ex. 1013, col. 6, ll. 30–31)), need be placed between SIE DMA 86 and RAM 84 in order to *intervene* in the moving of the data. Because arbiter 84 controls the data flow to RAM 84 in accordance with signals from 8051 microcontroller 72, 8237 DMA Controller 74, or SIE DMA 86 and “only allows access to the RAM by one controller at a time” (Prelim. Resp. 41 (citing Ex. 1013, col. 6, ll. 45–48)), we also are persuaded that 8051 microcontroller 72, 8237 DMA Controller 74, or SIE DMA 86 intervenes in the flow of data to RAM 84 via arbiter 84. Dec. on Inst. 25.

b. Increasing Dunnihoo’s Data Path to Two Data Paths

In the Decision on Institution, we agreed with Patent Owner that Petitioner’s reason for increasing Dunnihoo’s data path to two data paths” is not supported by evidence and “Petitioner’s proposed reason for combining the teaching of these references is based on hindsight improperly gleaned from the challenged claims.” Reh’g Req. 8 (quoting Dec. on Inst. 26). Petitioner argues that it provided a reason for modifying the teachings of Dunnihoo to increase Dunnihoo’s disclosed data path to two data paths. *Id.* In particular, Petitioner argues that

one of ordinary skill in the art would be motivated to do so because packets from the USB host destined for the Dunnihoo controller’s RAM in the USB device and packets from the USB device destined for the USB host would no longer share the same data path, thus increasing the efficiency of the SIE and the Dunnihoo controller as a whole.

Id. at 8–9 (quoting Pet. 46).

Nevertheless, Petitioner supports this argument only by citation to the insufficiently supported testimony of Petitioner’s declarant, Dr. Bagherzadeh. Pet. 46 (citing Ex. 1003 ¶ 109). Dr. Bagherzadeh asserts that a person of ordinary skill in the art would increase the disclosed data path to two data paths, citing to teachings in the Patent No. US 4,637,015 to Bobey (Ex. 1016) that “[i]t is known

to incorporate DMA channel handling capabilities in the microprocessor integrated circuit chip itself, one example of such a chip being the Intel 80186 microprocessor. This microprocessor provides for two DMA channels, which are typically used respectively for transmitting and receiving data packets.” Ex. 1003 ¶ 109 (quoting Ex. 1016, col. 1, ll. 5–36). Petitioner, however, does not indicate where it included arguments based on the teachings of Bobey regarding *packet* transmission and reception via a *shared* DMA channel in the Petition, and the only citation that we find to Bobey in the Petition is in Petitioner’s Exhibit List (Pet. iii.). Although we considered Petitioner’s argument and the relevant testimony of Dr. Bagherzadeh (Dec. on Inst. 25 (quoting Pet. 46)), after reviewing the arguments and evidence, we were not persuaded that Petitioner has shown sufficiently that a person of ordinary skill in the art would have modified the teachings of Dunnihoo in the manner proposed for the reason proffered (*id.* at 26).²

Thus, in the absence of sufficient supporting evidence, we are not persuaded by Petitioner that we improperly concluded that Petitioner’s reason for combining the teachings of these references to increase the number of data paths between the USB device and the USB host was based on improper hindsight.

c. Selecting Tx and Rx Queues Depending on USB Endpoint Polled

Similarly, Petitioner argues that we overlooked Petitioner’s evidence regarding the modification of Dunnihoo’s path into two paths. Reh’g Req. 9 (citing Pet. 49). In particular, Petitioner argues that, in view of Dunnihoo’s disclosure of the Tx and Rx queues (Pet. 49 (citing Ex. 1013, col. 6, ll. 53–55)),

² As noted above, Dr. Bagherzadeh cited to Bobey (Ex. 1016) in his declaration. Petitioner’s citation to Dr. Bagherzadeh’s testimony (Pet. 46) does not incorporate Dr. Bagherzadeh’s remarks on Bobey into the Petition. Petitioner fails to explain the significance of Bobey’s teachings to the applied references or to its arguments and does not propose to combine expressly Bobey’s teachings with those of the other applied references in its asserted grounds for unpatentability.

“Dunnihoo’s disclosure of selecting the appropriate channel depending on the USB endpoint polled is sufficient and anticipates ‘a plurality of USB endpoints, each selectively programmed for one of the plurality of DMA channels’” (Reh’g Req. 9–10 (citing Pet. 49)). We noted, however, that Dunnihoo already teaches separate transmit and receive packet paths 92, 94 (*E.g.*, Ex. 1013, col. 6, ll. 49–59; *see* Dec. on Inst. 24 (reproducing Ex. 1013, Fig. 3 (as annotated))) and considered Petitioner’s arguments regarding these separate paths (*see* Dec. on Inst. 25–26 (quoting Prelim. Resp. 47 (discussing arguments presented at Pet. 49))). Further, we note that Dunnihoo teaches that “[the Tx and Rx] queues do not store packets (the *packets* are stored in *the single ported RAM*). Rather, *the queue stores packet numbers or other identifiers* for the packets stored in the RAM.” Ex. 1013, col. 4, ll. 48–51 (emphases added); *see id.* at col. 6, ll. 15–19. As we indicated in the Decision on Institution, we did not overlook these arguments; instead, we found them insufficiently supported and unpersuasive. Dec. on Inst. 26.

III. ORDER

For the reasons given, it is

ORDERED that Petitioner’s Request for Rehearing is *denied*.

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