

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMERICAN MEGATRENDS, INC.,
MICRO-STAR INTERNATIONAL CO., LTD,
MSI COMPUTER CORP.,
GIGA-BYTE TECHNOLOGY CO., LTD., and
G.B.T., INC.,
Petitioners,

v.

KINGLITE HOLDINGS, LLC,
Patent Owner.

Case IPR2015-01081
Patent 5,987,604

Before GLENN J. PERRY, TREVOR M. JEFFERSON, and
BRIAN J. McNAMARA, Administrative Patent Judges.

McNAMARA, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and
37C.F.R. § 42.73

BACKGROUND

On October, 29, 2015, we instituted an *inter partes* review of claims 1–30 of U. S. Patent No. 5,987,604 ("the '604 Patent"). Paper 18 ("Dec. to Inst."). Patent Owner filed a Patent Owner Response (Paper 30, "PO Resp."), Petitioner filed a Petitioner Reply (Paper 39, "Pet. Reply"). Patent Owner filed a Motion to Exclude (Paper 23, "Mot. To Exclude"), Petitioner filed an Opposition (Paper 43, "Opp. To Mot. To Exclude"), and Patent Owner filed a Reply (Paper 44 "Reply to Opp. to Mot. To Exclude"). A transcript of an oral hearing held on June 29, 2016 (Paper 46, "Hr'g Tr.") has been entered into the record.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. §318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

Having reviewed the arguments of the parties and the supporting evidence, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims are unpatentable.

THE '604 PATENT

The '604 Patent discloses an x86 based system in which a system management interrupt (SMI) invokes an operating mode known as system management mode (SMM). Ex. 1001, col. 3, ll. 10–20. In SMM, system firmware is used to perform power management or control other system functions, e.g., controlling hardware specific features, in a manner that is transparent to the operating system and applications software. *Id.*

The '604 Patent discloses creating a virtual monitor that runs under SMM with memory paging to execute SMI code in virtual mode, thereby allowing SMM code written to run below the 1 MB boundary to execute

above the 1 MB boundary by mapping the entire SMI handler above the 1 MB boundary and executing the code as a page enabled, protected mode, virtual task with SMM. *Id.* at col. 2, ll. 27–35. When an SMI is generated, the central processing unit (CPU) asserts an SMI activate (SMIACT) control signal to access system management random access memory (SMRAM) 20, which is a dedicated memory space not accessible to the operating system or application software. *Id.* at col. 3, ll. 21–27, col. 6, ll. 6–10. After storing the current operating location for return purposes in SMRAM 20, CPU 14 jumps to a location in SMRAM 20 to execute the SMI handler code that performs the system management activity. *Id.* at col. 3, ll. 27–31. Upon completion of the system management activity, control is returned to the previously interrupted operating system. *Id.* at col 3, ll. 31–37.

The '604 Patent notes that conventional SMIs execute slowly because they operate below the 1 MB boundary in an uncached memory area, in order to avoid cache conflict with overlapping memory. *Id.* at col. 1, ll. 26–31. Such conventional SMMs operate in real mode with 4GB memory segments and 1 MB addressable program memory and are relatively slow. According to the '604 Patent, a conventional alternative approach transfers SMI code and data from a region above the 1 MB boundary to a cacheable region below the 1 MB boundary, allowing standard execution of SMI code in real mode, but requiring transfer of the SMI code back to a cacheable area above the 1 MB area after completing the SMI. *Id.* at col. 1, ll. 37–45.

In accordance with the invention in the '604 Patent, the data and code in SMRAM 20 located in the physical memory is mapped to location 22, which is above the 1 MB region in system space 50. *Id.* at col. 6, ll. 10–14, col. 7, ll. 27–30. CPU 14 then jumps to a location in SMRAM 20 that is

above the 1 MB region in the system address space 50 to execute the SMI handler code. *Id.* at col. 6, l. 15–19, col. 7, ll. 32–37. The SMI handler then jumps to location 24, which must be within 64 K of location 22, where the CPU mode change takes place, configuring CPU 14 to operate in protected mode. *Id.* at col 6, ll. 20–28.

The SMI handler then creates page tables and is configured to create a task state segment (TSS) and input/output (I/O) bit map, unless they were created during power on self-test (POST). *Id.* at col. 6, ll. 31– 39. The SMI handler then invokes the paging feature of CPU 14 and switches to virtual mode. *Id.* at col. 6, ll. 53–54.

In virtual mode, CPU 14 determines logical operations the same way as in real mode and the physical address is determined using the page tables. *Id.* at col. 6, l. 66–col. 7, l. 1. The SMI handler begins the task required to perform system management activities. *Id.* at col. 7, ll. 1–3. During execution of system management activities, the software occasionally configures the processor to operate in protected mode to facilitate execution of specific tasks, such as cache flushes and accessing the floating point unit of the CPU. *Id.* at col. 7, ll. 3–6. Upon completion of the special task, the SMI handler configures the CPU to operate in virtual mode to resume system management activity. *Id.* at col. 7, ll. 12–14.

Upon completion of system management activity, the SMI handler configures the CPU to exit the virtual mode, causing the CPU to operate in the protected mode. *Id.* at col. 7, ll. 14–19. Paging is then disabled and the SMI handler executes a resume instruction to return control to the previously interrupted operating system or application execution. *Id.* at col 7, ll. 18–22.

ILLUSTRATIVE CLAIM

Claims 1, 11 and 21 are independent. Claim 1 is drawn to an apparatus, claim 11 is drawn to a method, and claim 21 is drawn to a computer-executable process. Claim 1 is representative:

1. An apparatus for executing instructions in a system management mode in a processor-based system, comprising:
a memory for storing instruction sequences by which the processor-based system is processed;
a processor having a system address space, the processor for executing the stored instruction sequences; and
wherein the stored instruction sequences cause the processor to:
(a) configure the processor to operate in a protected mode while in system management mode, the processor operating at an address greater than one megabyte; (b) invoke a paging feature of the processor; (c) configure the processor to operate in a virtual mode; and (d) process the instruction sequences stored, wherein the process steps occur upon the receipt of an instruction to process a system management request.

Independent claims 11 and 21 recite as limitations parts (a)–(d) of the wherein clause of claim 1.

ART CITED IN PETITIONER’S CHALLENGES

Petitioner cited the following references in its challenges to patentability:

Reference	Designation	Exhibit No.
U.S. Patent No. 5,644,755, iss. July 1, 1997.	Wooten	Ex. 1002
U.S. Patent No. 6,093,213, iss. July 25, 2000.	Favor	Ex. 1003

Advanced Micro Devices, <i>Preliminary Enhanced AM686[®] Microprocessor Family Publication #19225 Rev. B Amendment/0</i> (1995).	Am686 Manual	Ex. 1004
3 Intel, <i>Pentium[®] Processor Family Developer's Manual</i> (1995).	Pentium Manual	Ex. 1005
Robert W. Collins, <i>The Caveats of Pentium System management Mode</i> (May 1, 1997), http://www.drdobbs.com/the- caveats-of-pentium-system- management/184410199 (last visited 8/11/2014).	Collins	Ex. 1006
IBM, <i>IBM 6x86 Microprocessor Sixth Generation Superscalar Superpipelined x86- Compatible CPU</i> (1996).	IBM 6x86	Ex. 1012
3 Intel, <i>Intel Architecture Software Developer's Manual</i> (1997).	ASDM	Ex. 1013

GROUND OF INSTITUTION

In our Decisions to Institute, we instituted trial on the following grounds:

Claims 1–4, 11–14, and 21–24 as obvious under 35 U.S.C. § 103 over the combination of Collins and the Pentium Manual;

Claims 1–4, 11–14, and 21–24 as obvious under 35 U.S.C. § 103 over the combination of Collins, the Pentium manual and IBM 6x86; and

Claims 5–10, 15–20, and 25–30 as obvious under 35 U.S.C. § 103 over the combination of Collins, the Pentium Manual and ASDM.

CLAIM CONSTRUCTION

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their “broadest reasonable construction in light of the specification of the patent” in which they appear. 37 C.F.R. § 42.100(b); *see also Cuozzo Speed Techs., LLC, v. Lee*, 136 S. Ct. 2131, 2141–46 (2016). The terms also are generally given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Our Decision to Institute applies the following claim constructions, which the parties do not dispute, and we apply these same constructions in this Decision.

Protected Mode: ordinary meaning as discussed in the Dictionary of Computer Terms¹ cited by Patent Owner; i.e., “[A] mode of processor operation in which an 80286 or later generation x86 microprocessor can access the largest possible amount of memory.” Dec. to Inst. 9–10.

System Management Mode (SMM): an operating mode that is entered in response to a dedicated SMI and that uses a dedicated memory space to implement power management and enhanced system functions in firmware in a manner that is transparent to the operating system and applications software. *Id.* at 10–11.

¹ Douglas Downing & Michael Covington, BARRON’S BUSINESS GUIDES, DICTIONARY OF COMPUTER TERMS (3d. ed. 1992) (“Dictionary”).

Virtual Mode: a task running in protected mode in which the processor emulates an 8086 processor, such that the execution environment is the same as that of a real-address mode.² *Id.* at 11–12.

Paging: [A] memory management process for mapping logical addresses to physical addresses. *Id.* at 12–13.

PATENT OWNER’S MOTION TO EXCLUDE

Collins (Ex. 1006)

Collins is cited in each of the grounds on which we instituted trial. Therefore, we first address Patent Owner’s Motion to Exclude Collins.

Petitioner identifies Collins as an article published in Dr. Dobbs’s Journal on May 1, 1997. Pet. 22, 26. The version of Collins filed with the Petition as Ex. 1006 is a reproduction of Collins downloaded on August 14, 2014 from a website identified as <http://www.dr Dobbs.com/the-caveats-of-pentium-system-management/184410199> (“dr.dobbs URL”). Ex. 1006, 1. The reproduction states “The Caveats of Pentium System Management Mode By Robert R. Collins, May 1, 1997.” *Id.* at 1. The article also includes the following copyright notice: “Copyright © 1997, Dr. Dobbs Journal.” *Id.* at 6.

Patent Owner challenges the admissibility of Ex. 1006, arguing that the version of Collins proffered by Petitioner is not an accurate or genuine

² According to ASDM in the real-address mode execution environment, the processor supports a 1 M-byte physical address space divided into segments, each of which can be up to 64 Kbytes in length, and the base of the segment is specified with a 16 bit segment selector, which is zero extended to form a 20 bit offset from address 0 in the address space, and in which a physical address is formed by adding the offset to the 20 bit segment base. Ex. 1013 § 15.1, pp. 435–436.

duplicate of that reference as originally published. Mot. To Exclude 2. According to Patent Owner, accessing the Wayback Machine archives of Internet webpages showed that the dr.dobbs URL was under construction as of November 17, 2000 and that the version proffered by Petitioner could not have existed in 1997. *Id.* (citing, Ex. 2004, Declaration of Christopher Frerking, (“Frerking Decl.”) ¶3).

Patent Owner conflates the existence of the dr.dobbs URL with the authenticity of the Collins article. The existence of the URL in 1997 is not the issue before us. Petitioner does not claim to have downloaded Collins from a 1997 URL. Exhibit 1006 clearly shows that the copy of Collins was downloaded on August 11, 2014 from the dr.dobbs URL. The issue before us is whether the copy of the article proffered in Ex. 1006 is a duplicate, i.e., a counterpart produced by a mechanical, photographic, chemical, *electronic*, or other equivalent process or technique that *accurately reproduces the original*. Fed. R. Evid. 1001(c) (emphasis added). As Patent Owner notes “[a] duplicate is admissible to the same extent as the original unless a genuine question is raised about the original’s authenticity or the circumstances make it unfair to admit the duplicate.” Mot. To Exclude. 2–3 (citing Fed. Rule of Evid. 1003).

Following our Decision to Institute, Petitioner responded to Patent Owner’s evidentiary objection to Collins by serving on Patent Owner supplemental evidence, i.e., the Declaration of Robert Collins (“Collins Decl.”), a copy of Collins as it appeared in the May 1997 Dr. Dobbs Journal, and a copy of the cover page of the May 1997 Dr. Dobbs Journal publication obtained from the Georgia Tech Library. Mot. To Exclude 3. Patent Owner

declined to withdraw its objection and, as part of this Motion to Exclude, filed Petitioner's supplemental evidence as Ex. 2007.

Noting that the cover page indicates the Georgia Tech Library received the May 1997 Dr. Dobbs Journal on April 7, 1997, Patent Owner suggests that Petitioner seeks to move the date of the reference back to April 1997. Mot to Exclude 4. Indeed, in its opposition to the Patent Owner Response, Petitioner argues that Collins was circulated to libraries as early as April 7, 1997 and cites the testimony of Robert Collins that his article was in circulation about a month before the May 1, 1997 publication date. Pet. Reply 20 (citing Collins Decl., Ex. 2007 ¶ 1; Ex. A). Patent Owner contends that Petitioner provided the hard copy of Collins and the Collins Declaration as supplemental evidence to overcome an objection, but because Petitioner did not file the supplemental evidence in this proceeding, Petitioner may not rely upon it for the substantive purpose of arguing an earlier date of publication. Mot. To Exclude 4.

We need not reach the issue of whether Petitioner can rely on the Exhibit 2007 filed by Patent Owner because Petitioner has not provided any evidence that Collins was accessible to the public prior to its publication date of May 1, 1997. For example, Petitioner has not demonstrated how Collins would have been catalogued in any library or made accessible to the public. Thus, the only date we ascribe to Collins is May 1, 1997.

Patent Owner also notes that the cover page in 1997 refers to a URL (www.ddj.com) that is different URL associated with Exhibit 1006. Mot. To Exclude 3–4. However, as discussed above, the existence of any particular web page is not the issue before us.

Patent Owner acknowledges that the publication in which Collins originally appeared, Dr. Dobb's Journal, was, in May 1997, published in hard copy form. Mot. To Exclude 2. However, Patent Owner argues that the version of Collins provided by Petitioner as Ex. 1006 is not a duplicate of the article appearing originally in hard copy form. Mot. To Exclude. 2.

Although the web site on which Collins appears in Ex. 1006 is not a copy of the article in its original form, we direct our inquiry to the contents of the article. "When the only concern is with getting the words or other contents before the court with accuracy and precision, a counterpart serves equally well as the original, if the counterpart is the product of a method which insures accuracy and genuineness." Fed. R. Evid. 1003, Advisory Committee Notes. Patent Owner acknowledges that there is no difference between the contents of Collins in Ex. 1006 and the contents of the hard copy of Collins, as published in the May 1997 Dr. Dobbs Journal. Hr'gTr. 53. Therefore, we conclude that Ex. 1006 is an admissible duplicate of the original Collins article and we deny Patent Owner's Motion to Exclude Ex. 1006.

Polyudov Declaration (Ex. 1014)

Patent Owner has also objected to and moved to exclude the declaration testimony of Petitioner's expert Feliks Polyudov, (Ex. 1014 ("Polyudov Decl.)) on the ground that he has been employed by Petitioner AMI for 15 years and is therefore biased. Mot. To Exclude 6–7. Mr. Polyudov acknowledges his past and current employment by AMI and states that he is not being compensated specially for his work in this proceeding and that his compensation is not dependent upon the results of this proceeding. Polyudov Decl. ¶ 5. Patent Owner does not challenge Mr.

Ployudov's qualifications or offer any evidence that Mr. Polyudov is biased, other than his employment at AMI. Nor does Patent Owner present any evidentiary basis for excluding Mr. Polyudov's testimony.

Although Mr. Polyudov's employment background may affect the weight we assign his testimony, his status as an employee of AMI alone does not disqualify him. In consideration of the above, Patent Owner's Motion to Exclude Exhibit 1014 is denied.

ANTEDATING OF COLLINS

We begin with Patent Owner's contention that Collins, published in May 1997, is not prior art because the inventor of the '604 Patent, David Edrich, asserts prior invention, declaring that "the invention had been disclosed to Intel engineers around April 1, 1997, meaning that the invention had been conceived of by no later than that date." PO Resp. 14–15; Ex. 2002, Declaration of David Edrich ("Edrich Decl.") ¶ 9. As evidence of this earlier conception, Patent Owner relies on a Phoenix Technologies Invention Disclosure Form that states:

The invention idea has been disclosed to Intel Engineers, informally, as a possible solution since around April 1, 1997. On July 1, 1997 Phoenix Engineers will be doing pre-alpha testing of the 440BX chipset. Part of this testing is to include SMI execution above 1 Megabyte so this invention is scheduled to be tested then but that is not the primary concern of the July effort.

Ex. 2003 ¶ 8. The invention disclosure, which identifies Mr. Edrich as the sole inventor, states that it was prepared on June 18, 1997, but does not indicate who prepared it, and is not signed.

Petitioner contends that Mr. Edrich's testimony is entitled to no weight because his assertions about discussions with Intel engineers are hearsay, he is a paid consultant to Patent Owner, the disclosure is unsigned

and uncorroborated, and because among several alleged inventive concepts asserted in the disclosure, it is not possible to determine if the invention referenced in Mr. Edrich's declaration is the same invention as that claimed in the '604 Patent. Pet. Reply 15–17.

“Conception must be proved by corroborating evidence which shows that the inventor disclosed to others his ‘completed thought expressed in such clear terms as to enable those skilled in the art’ to make the invention.” *Coleman v. Dines*, 754 F.2d 353, 359 (Fed. Cir. 1985). The requirement of “independent” corroboration requires evidence other than the inventor's testimony. *In re NTP, Inc.* 654 F.3d 1279, 1291 (Fed. Cir. 2011). Patent Owner offers no corroborating evidence to support Mr. Edrich's testimony. There is no contemporaneous evidence supporting the statements in Mr. Edrich's declaration and there is no testimony corroborating Mr. Edrich's declaration. For example, the Intel engineers are not identified and there is no written record of what Mr. Edrich disclosed to these Intel engineers. Indeed, prior to the invention form dated June 18, 1997, there is no written record of what Mr. Edrich alleges he invented. Although the invention disclosure states that testing was to be conducted, Patent Owner provides no evidence that such testing was conducted or that any testing proved the concept, as purportedly conceived in April 1997.

In view of the absence of any corroboration of prior invention by Mr. Edrich, we conclude Collins is prior art.

ANALYSIS OF PRIOR ART CHALLENGES

Introduction

We resolve the question of obviousness on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). The test for obviousness is whether the combination of references, taken as a whole, would have suggested the patentees’ invention to a person having ordinary skill in the art. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

The Supreme Court has made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415 (2007). Whether a patent claiming the combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *Id.* at 417. To reach this conclusion, however, requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention. *Id.* As the Supreme Court recognized, in many cases a person of ordinary skill “will be able to fit the teachings of multiple patents together like pieces of a puzzle,” recognizing that a person of

ordinary skill “is also a person of ordinary creativity, not an automaton.”
KSR at 420–21. Against this general background, we consider the references, other evidence, and arguments of the parties.

Claims 1–4, 11–14, and 21–24 As Obvious Over Collins and Pentium Manual

Petitioner contends that Collins discloses a protected mode and a virtual mode while in a separate x86 state known as SMM, if the device is programmed to perform SMM (which Collins states, it most likely is not). Pet. 26 (citing Ex. 1006, 4). The paragraph from Collins cited by Petitioner is entitled “Using Protected Mode Within SMM” and discloses the capability of operating in protected mode, if the SMM was programmed to do it. Ex. 1006, 4. Petitioner notes that the processor can execute directly in real address mode 8086 software in a multitasking environment, i.e., a virtual-8086 (“v86”) mode. Pet. 26. Petitioner also cites the disclosure in Collins concerning using SMM to create a CPL-0 v86 task, which Petitioner argues shows enabling virtual mode while employing SMM in protected mode. *Id.*

Petitioner cites the Pentium Manual as disclosing a processor architecture including paging with a real mode, a protected mode, and an SMM mode, *id.* at 26–27 (citing Ex. 1005, 40), and memory management features, such as paging, *id.* at 27 (citing Polyudov Decl. ¶ 141). Petitioner further argues that a person of ordinary skill would have recognized that protected mode permits instructions located between 1 MB and 4 GB of memory to be accessed by the processor and that protected mode features the ability to execute directly real-address mode 8086 software in a protected, multi-taking environment. *Id.*

In its claim charts Petitioner cites the Pentium Manual as disclosing the elements of claim 1, including, SMM (Pet. 28), SMRAM (*id.*), relocating RAM to an address above 1 MB (*id.* at 29), invoking a paging feature (*id.*), configuring the processor to operate in a virtual mode (*id.* at 29–30), processing the instructions stored (*id.*) wherein the processing steps occur upon receipt of a system management request (*id.*). Petitioner cites Collins as disclosing operating in a protected mode while in SMM (*id.* at 29), invoking a paging feature of the processor (*id.*) and configuring the processor to operate in a virtual mode (*id.* at 30). Petitioner has also provided claim charts that support its challenges to claims 2–4, 11–14, and 21–24 on this ground.

According to Petitioner, a person of ordinary skill in the art would have been motivated to combine Collins and the Pentium Manual because they describe features of the Pentium processor having SMM, protected and virtual modes. *Id.* at 27.

Patent Owner contends that the '604 Patent overcomes problems in the prior art by teaching that “SMRAM should be mapped to occupy an area of memory having unique addressable locations above 1 Mbyte.” PO Resp. 4 (citing Ex 2010, Expert Report of Dr. John Levy from C.D. Cal. Case No. CV14-03009-JVS(PJWx) (“Levy Report.”) ¶ 7).³ Patent Owner states that

³ Paragraph 7 of the Levy Declaration does not address this issue; it identifies a course Dr. Levy taught at San Francisco State University. The Levy Report submitted as Exhibit 2010 in this proceeding appears to be taken from co-pending district court litigation. The Levy Report appears to address the '604 Patent at Paragraphs 31–49. It is not clear what paragraph of the Levy Report (or any other Exhibit) supports this statement in the Patent Owner Response. We also note that in paragraph 40, apparently referring to issues in the district court, the Levy Report states that the only

“[t]he ’604 Patent discloses creating a virtual monitor that runs under SMM with memory paging to execute SMI code in virtual mode, thereby allowing SMM code written to run below the 1 Megabyte boundary to execute above the 1 Megabyte boundary.” Hr’g Tr. 23:15–19; Levy Report ¶ 38 (citing Ex. 1001, col. 2, ll. 27–32). According to Patent Owner, the programmatic addressing solution described in the ’604 Patent is different from override addressing solutions supported by all of the cited prior art, because the ’604 Patent offers the only addressing solution for operating SMM with instructions above 1 Megabyte. PO Resp. 5.

Patent Owner argues that the Pentium Manual teaches an involved, instruction intensive procedure for using SMM mode addressing with special overrides per instruction, i.e., override prefixes, to operate with SMRAM code above 1 Mbyte so that SMM addressing can reach up to 4 Gbytes of address space. PO Resp. 8–9. According to Patent Owner, “the ’604 Patent claims do not describe using SMM mode addressing to operate at an address above 1 Mbyte, as disclosed in the Pentium Manual. Ex. 2010 ¶15.”⁴

claim at issue is claim 11. This proceeding concerns claims 1–30. Thus, it is unclear if Patent Owner meant to reference a different document. However, we will not scour the record to determine Patent Owner’s intentions.

⁴ The Levy Report in Ex. 2010 does not address this issue at paragraph 15. Paragraph 15 states that Dr. Levy applies the plain and ordinary meaning to terms not construed by the court. It is unclear if Patent Owner’s reference to the Pentium Manual as Ex. 2010 is intended to refer to Ex. 1005, as designated at page 6 in our Decision to Institute or Ex. 1013, which is another Pentium manual. In Exhibit 1005, Chapter 15, which is 9 pages long and has a number of subsections, concerns Input-Output and § 15.3 is titled “Protected Mode I/O.” In Exhibit 1013, Chapter 15, which is 28 pages long and includes numerous subsections, is titled “8086 Emulation” and includes a discussion of real address mode and virtual address mode.

Instead, such claims teach a programmatic approach that minimizes instructions, instead of relying on what is disclosed in Collins and the Pentium Manual.” PO Resp. 9.

Petitioner argues that recognizing SMM involved executing 16 bit code in a 32 bit code execution environment, the '604 Patent merely utilizes virtual 8086 mode for its intended purpose (i.e., to execute 16 bit code in a protected mode environment that supports multitasking), instead of utilizing real mode to run SMM-related code. Pet. Reply 1. According to Petitioner, it is undisputed that a programmatic solution to multitasking (protected mode, paging, and virtual mode) is taught in the Intel Pentium Manual. Pet. Reply 2–3. Petitioner cites the Pentium Manual as disclosing paging in protected mode, transitioning to virtual 8086 mode in protected mode and the usefulness of paging for virtual 8086 multitasking in protected mode. *Id.* Petitioner also notes that the salient characteristics of SMM, as embodied in the challenged claims 1, 4, 11, 14, 21, and 24 are taught explicitly by the Pentium Manual. *Id.* (citing Ex. 1005 at 41, 493–502). Petitioner further argues that functionality inherent in protected mode coexisting with operation in SMM was known in the prior art relating to the x86 processor. *Id.* at 3 (citing Ex. 1006, 4; Ex. 1012, § 2.9.5).

Patent Owner identifies prior art cache coherency problems resulting from overlaid SRAM implementations in which the processor cannot differentiate between system memory and its internal cache, so that cache may contain cached instructions at normal addresses that are at the same address of the SMM instructions. PO Resp. 2. Patent Owner reviews

However, as noted above, we will not scour the record to determine Patent Owner's intentions

problems with prior art solutions (turning off the cache and treating SMRAM as non-cacheable negates the value of having processor cache; flushing the cache to make it useable may not be possible with all legacy chipsets; relocating SMRAM space in a non-overlaid environment introduces jump restrictions). *Id.* at 3–4. According to Patent Owner, the '604 Patent overcomes these problems by mapping SMRAM to occupy an area of memory having unique addressable locations above 1 Mbyte. *Id.* at 4.

Claim 1 recites “the processor operating at an address above 1 Mbyte.” The specification of the '604 Patent discloses that SMM is invoked via assertion of the SMI signal to the CPU, which asserts the SMI_{ACT} control signal, which accesses SMRAM 20. Ex. 1006, col. 6, ll. 6–10. The specification further states: “In accordance with the principles of the present invention, the data and code of SMRAM 20 located in physical memory is first mapped into a location that is above 1 Megabyte in the system address space, as shown in Fig. 5.” *Id.* at col. 6, ll. 10–14. However, as Petitioner notes, independent claims 1, 11, and 21 of the '604 Patent do not mention SMRAM and do not recite relocating SMRAM or mapping SMRAM above 1 Mbyte. Pet. Reply. 7–8. In general, “even if *all of the embodiments* discussed in the patent included a specific limitation, it would not be proper to import from the patent’s written description limitations that are not found in the claims themselves.” *Cadence Pharm. Inc. v. Exela PharmSci Inc.*, 780 F.3d 1364, 1369 (Fed. Cir. 2015) (emphasis added) (citations omitted) (internal quotation marks omitted). Further, “it is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication

in the intrinsic record that the patentee intended the claims to be so limited.” *Epos Techs. Ltd. v. Pegasus Techs. Ltd.*, 766 F.3d 1338, 1341 (Fed. Cir. 2014). No such indication is apparent from the record in this proceeding.

In addition, Petitioner notes that Patent Owner’s expert Dr. Levy concedes that entry into protected mode necessarily means that one is executing instructions above 1 Mbyte of memory, as recited in the claims of the ’604 Patent. *Id.* at 5 (citing Ex. 1020, Transcript of IPR Deposition of Dr. John Levy (“Levy IPR Tr.”) 41:10–42:9; Ex. 1018, Transcript of C.D. Cal. District Court Case Deposition of Dr. John Levy (“Levy D. Ct. Tr.”) 101, 121). In his IPR deposition, Dr. Levy initially stated that “protected mode enables the accessing and execution of instructions above the first megabyte of system memory, but it does not necessarily require it.” Levy IPR Tr. 41:4–7. However, in his district court deposition Dr. Levy testified differently, as follows:

Q; In fact, any point in time you’re talking about protected mode you’re talking about the processor operating at an address greater than 1 megabyte, right?

A: Yes.

Levy D. Ct. Tr. 101:5–9. When confronted with the apparent difference between the IPR deposition and his testimony in the district court deposition, Dr. Levy stood by his testimony from the district court deposition. IPR Tr. 41:16–21. Thus, we understand Patent Owner’s expert to concede that entry into the protected mode means that one is executing instructions above 1 Mbyte of memory, as recited in the claims. Thus this feature of independent claim 1, 11, and 21 is taught by the combination of the Collins and the Pentium Manual.

Patent Owner contends that the combination of Collins and Pentium Manual teaches away from the limitation recited in independent claims 1, 11, and 21 of “the processor operating at an address greater than one megabyte.” PO Resp. 6. Exemplary claim 1 recites “the stored instruction sequences cause the processor to: (a) configure the processor to operate in a protected mode while in a system management mode, the processor operating at an address greater than one megabyte.” Patent Owner does not argue that Collins fails to disclose this limitation. Instead, Patent Owner cites Collins’ disclosure of problems that can occur when the SMBASE is set above 1 Mbyte. PO Resp. 7 (citing Ex. 1006, 3). Patent Owner emphasizes that Collins explicitly states “I would strongly discourage anybody from attempting to do such a thing.” *Id.* Patent Owner further argues that Collins’ testimony that he did not relocate SMBASE above 1 Mbyte himself and that in performing step (a) of the ’604 Patent, inventor Erdich was doing what Collins recommended against. *Id.* at 6, 8.

Petitioner responds that Patent Owner’s expert, Dr. Levy testified that, in his description of using protected mode within SMM, Collins is not attempting to dissuade a reader from configuring the processor into SMM, protected mode and virtual 8086 mode. Pet. Reply, 12 (citing Levy IPR Tr., 61:14–25 “reading this [“Using Protected Mode Within SMM, Collins 4] you would know that you could simultaneously be in system management mode and protected mode and v86 mode [.]”). Dr. Levy also testified that in the context of Collins’ disclosure of “Using Protected Mode Within SMM”, a person of ordinary skill would know that one could simultaneously be in system management mode and protected or v86 mode. Levy IPR Tr. 63:20–64:25. Dr. Levy also testifies that the Pentium manuals describe the

capability of entering protected mode or v86 mode while in SMM. *Id.* at 65:19–66:1. Inventor David Edrich also testified that prior art x86 documentation taught him that the x86 architecture allowed functioning in both protected mode and SMM simultaneously. Pet. Reply 4 (citing Ex. 1021, IPR Deposition Testimony of David Edrich (“Edrich IPR Tr.”) 49:14–20. Thus, we conclude using protected mode while in SMM is taught by the prior art.

Petitioner also notes that Dr. Levy acknowledged that prior art taught entering protected mode while in SMM and then employing paging at least three years before the purported invention in the ’604 Patent. Pet. Reply 4. (citing Levy IPR Tr. 43:8–44:16, Ex. 1019 § 3.3.2).

Nevertheless, Patent Owner argues that statements in the Collins article teach away from using SMM in protected mode. PO Resp. 9. To constitute a proper “teaching away,” the teaching of the applicable prior art reference must be evaluated from a technological perspective, not merely a comparative perspective. For instance, it is not a “teaching away” unless one with ordinary skill in the art would have understood that teaching as conveying that the method or structural configuration at issue reasonably cannot be expected to achieve what it is required to achieve according to the claimed invention. *See, e.g., Syntex (U.S.A) LLC v. Apotex, Inc.*, 407 F.3d 1371, 1380 (Fed. Cir. 2005) (“Under the proper legal standard, a reference will teach away when it suggests that the developments flowing from its disclosures are unlikely to produce the objective of the applicant’s invention.” (citing *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994))). Further, “just because better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes.” *In re*

Mouttet, 686 F.3d 1322, 1334 (Fed. Cir. 2012). In that regard, one is not significantly “taught away” from a “particularly preferred embodiment” by the suggestion that something else may be even better. *In re Susi*, 440 F.2d 442, 446 n.3 (CCPA 1971). Applying these standard as discussed below, Collins does not teach away from the claimed invention.

Collins is critical of Intel documentation stating that “I will discuss the caveats of SMM and minutiae that you would never have gleaned by reading Intel’s documentation.” Ex. 1006, 1. Collins explicitly states that the caveats he discusses may not apply to future Pentium processors and “are discussed in this column to give you a better understanding of how the Pentium processor works, and to be used as warning signs for your own SMM development.” *Id.* Thus, Collins anticipates that users will implement the approach he discusses.

Patent Owner also argues that relocating the SMM handler above 1 Mbyte, as recited in step (a) of claims 1, 11, and 21 is what the inventor is doing and that step (a) is what Collins teaches, but tells people not to do because of the problems associates with it. PO Resp. 8 (citing Collins Tr. 84). In discussing the modification of segment registers, Collins states:

you must take care when modifying some of these locations, especially the segment registers. But any competent programmer who understands the SMM architecture knows all of the fields of the State Save Map . . . , knows the ramifications of changing these locations, and may modify these locations without fear of unpredictable results.

Ex. 1006, 3. Collins provides code listings for the user to change the initial address of the SMM handler by modifying the SMBASE and to adjust the

code segment (CS)⁵ register so that service interrupts return properly. *Id.* at 3, 7. Collins cautions the user when the SMBASE has been set above 1 Mbyte, “it will be impossible to have any segment register (other than an unmodified code segment register) point to any data within the SMM handler.” *Id.* at 3. Therefore Collins cautions that if interrupts are needed, one cannot return to the interrupted code. *Id.* at 3. For this reason, Collins recommends against this approach. *Id.* at 2–4. This statement by Collins, however, does not teach away from the technique, but instead cautions the user and recommends avoiding setting SMBASE above 1 Mbyte in circumstances where interrupts are needed.

Petitioner also cites the testimony of its expert, Mr. Polyudov, that entering protected mode overcomes these problems identified by Collins. Pet. Reply 14 (citing Ex. 1022, Transcript of Deposition of Feliks Polyudov (“Polyudov Tr.”) 102–103, stating “interrupt management, which in the context of BIOS SMI handler is not needed when SMI handler is executed interrupt handler typically disabled. So that word of caution doesn’t apply to interrupt handlers” and “inability to initialize segment registers to point to SMRAM . . . the same section [of Collins] provides guidance on how to work on it . . . see what the section [of the Pentium manual that talks about protected mode] says. That we are in the 16-bit execution mode, but we have to deal with 32-bit address. So the natural inclination here would be to . . . switch to a mode that can naturally handle 32-bit addresses, such as protected mode, which is described in the same [Pentium] manual.”).

Collins notes that upon entering SMM:

⁵ Segment registers are discussed at Ex. 1013, 68.

all registers have some initial values, and you're operating in a version of real mode in which all segments have 4 GB limits (also known as big real mode or flat real mode). The processor is capable of entering protected mode, v89 mode, or even loading and executing an operating system, if the SMM handler is programmed to do such a thing (which it probably wasn't). Yet, when the RSM instruction (RESUME to the user program) is executed, the entire state of the original interrupted program is restored, and execution continues exactly where it left off.

Id. at 4.

As discussed above, Patent Owner acknowledges that Collins discloses moving the SMM handler above 1 Mbyte and that this is a feature of the claimed subject matter. PO Resp. 8 (citing Collis Tr. 84). We find that Collins' detailed explanation with code listings and cautions to the user about potential consequences, offered in the context of providing sophisticated users an understanding SMM, is not teaching away.. The caveats Collins puts in his article do not support a finding that Collins teaches away from the invention.

We are also not persuaded by Patent Owner's argument that Collins criticism of Intel documentation is a reason that a person of ordinary skill would not be motivated to combine Collins teachings with those of the Pentium Manual. PO Resp. 11–14. Patent Owner contends that Collins' disparaging remarks are antithetical to the requisite suggestion to combine prior art references. *Id.* 12. However, Collins explicitly purports to supplement the Pentium Manuals with information that a user would not otherwise have gleaned from them. Ex. 1006, 1. Collins also makes explicit reference to various parts of the Pentium Manual. *See, e.g.*, Ex. 1006, 2 (referencing Chapter 20 of the Pentium Processor Developers Manual, Volume 3). Thus, we conclude that a person of ordinary skill would have

been motivated to combine the teachings of Collins and the Pentium Manual and that independent claims 1, 11, and 21 are disclosed by this combination of references.

Claims 1, 11, and 21 recite as step (b) invok[ing] a paging feature of the processor. Petitioner cites Collins disclosure of creating a CPL-0 v86 task as indicative of paging and the Pentium Manual disclosure concerning software implementation in protected mode as disclosing this feature. Pet. 29 (citing Ex. 1006, 4–5, Polyudov Decl. ¶¶ 105–51, 170; Ex. 1005 402–403). Patent Owner does not argue that this limitation is not found in the asserted prior art.

Patent Owner instead argues Petitioner has not demonstrated that when invoking paging in SMM, a page table is created, as recited in dependent claims 2, 3, 12, 13, 22 and 23. PO Resp. 10. Petitioner responds that Mr. Polyudov testified that a PG bit indicating paging is enabled can be set when at least two page tables are created, i.e., the page directory and at least one second-level page. Pet. Reply 23 (citing Ployudov Decl. ¶ 150, referencing Ex. 1005, 403). Thus, according to Petitioner, Mr. Polyudov concluded that a page table is created in SMM by virtue of setting the PG bit while in SMM. *Id.*

Patent Owner further argues that a person of ordinary skill would have been aware of *Erratum* No. 8 in the Pentium Pro Processor Specification Update that indicated Mode C paging in SMM causes incorrect page tables and that there were no plans to correct the problem. PO Resp. 10–11 (citing Ex. 2020, 9)⁶. Exhibit 2020 is dated January 1999, more than one year after

⁶ Patent Owner appears to be referencing Ex. 2020 ¶ 8.

the application that led to issuance of the '604 Patent. Thus, it provides no insight into what a person of ordinary skill would have understood on the filing date of the application for the '604 Patent. In addition, as Petitioner points out, only Mode C paging (a 36 bit address extension which uses 2 Mbyte pages) is implicated by this discussion and other paging modes, such as Mode B paging, are not affected. Pet. Reply 22 (citing Ex. 2020, 27 [see ¶ 34]).

We also note that the subject matter apparently cited by Patent Owner in Ex. 2020 states “paging, in general, is not support by SMM,” and “large size pages are not supported in SMM.” Ex. 2008 ¶ 8. The implications of these statements are not clear, given that the cited subject matter also concerns a condition in which mode C paging is in use during SMM, “an SMI is serviced and the SMM handler switches to mode C paging with a different set of page tables.” *Id.* As Petitioner points out, the purported “bug” would not have been detected if it were not known publicly to use paging in SMM. Pet. Reply. 22. Taken together these circumstances indicate that a person of ordinary skill would understand paging to have been available in SMM mode. For the reasons discussed above, the current record supports our finding that paging, as recited in step (b) of independent claims 1, 11, and 21 and dependent claims 2, 3, 12, 13, 22, and 23 is disclosed in SMM with the processor operating at an address greater than 1 Mbyte, as recited in step (a).

Our discussion above addresses specific disputed limitations recited in claims 1–3, 11–13, and 21–23 specifically. Claims 4, 14, and 24 recite performing a near jump to a second location and configuring the processor to operate in protected mode. Petitioner’s claim charts cite the Pentium

Manual for its disclosure that in SMM the CPU can access or jump anywhere within the 4 Gbyte logical address space and perform a near jump anywhere within the 4 Gbyte address space. *See, e.g.*, Pet. 31 (citing Ex. 1005, 502). Petitioner cites Collins and the Pentium Manual as disclosing operating in protected mode in SMM. *Id.* at 29, 31 Based on the full record before us, including the citations in Petitioner’s claim charts and Petitioner’s arguments noted above, we find that Petitioner has demonstrated the references disclose the remaining limitations recited in claims 1–4, 11–14, and 21–24. Pet. 28–33.

In consideration of the above, we conclude that Petitioner has demonstrated by a preponderance of the evidence that claims 1–4, 11–14, and 21–24 are obvious under 35 U.S.C. § 103(a) over the combination Collins and the Pentium Manual.

Claims 1–4, 11–14, and 21–24 As Obvious Over the Combination of Collins, the Pentium Manual and IBM6x86

Anticipating Patent Owner’s argument that Collins’ disclosure of operating in protected mode while in SMM is equivocal, Petitioner contends that IBM 6x86 unequivocally teaches configuring a processor to protected mode, while in SMM. Pet. 34 (citing Ex. 1012 § 2.9.5, page 95 “[w]ithin the SMI service routine, protected mode may be entered and exited as required, and real or protected mode device drivers may be called.” (emphasis omitted)). Petitioner contends that, like the Pentium Manual, IBM 6x86 teaches the same underlying technical concepts. *Id.* at 34. Petitioner notes that IBM 6x86 teaches SMM memory space up to 4GB, real mode applications running in virtual mode, and enabling paging so that from protected mode a transition can be made to virtual mode to run real mode above the 1 MB limit. *Id.* at 34–35. Petitioner contends that a person of

ordinary skill in the art would have been motivated by a desire to maximize the utility of the Pentium processor to combine IBM 6x86 with Collins and the Pentium Manual. *Id.* at 35–36.

According to Patent Owner, Petitioner equates the teaching in the 6x86 Manual to those in the Pentium Manual, but in contrast to Petitioner's view that the Pentium's teaching of relocating SMRAM to an address above 1 Mbyte equates to the claim limitation requiring that the processor operate at 1 an address above 1 Mbyte, the 6x86 Manual does not disclose setting SMRAM above 1 Mbyte. PO Resp. 18. Patent Owner contends that running real mode above the 1 Mbyte limit is unrelated to the processing operation in protected mode while in SMM at an address greater than 1 Mbyte. *Id.* Patent Owner further contends that the SMM memory space accesses in the 6x86 manual are always uncacheable, regardless of where SMRAM is located. *Id.* Citing basic cache methodology differences between the 6x86 Manual and the Pentium Manual, Patent Owner argues that a person of ordinary skill would not have found it obvious to combine the 6x86 Manual with the Pentium Manual because the 6x86 Manual would not assist a reader of the Pentium Manual in solving cache performance issues, regardless of where it executed SMM code or, because the 6x86 Manual would make SMM memory spaces uncacheable, it would teach away from the combination with the Pentium Manual. PO Resp. 18–19.

Petitioner notes that the caching methodologies are not the subject of any of the claims of the '604 Patent, and instead Petitioner relies on the 6x86 Manual to bolster Collin's teaching of an SMI handler that enters protected mode. Pet. Reply 21.

IBM 6x86 § 2.9.5 concerns SMI Service routine execution and states that upon entry into SMM, after the SMM header has been saved and the registers are set to their reset value, the Code Segment (CS) register is loaded with the base, as defined by the ARR3 register, and a limit of 4 GB. Then the SMI service routine begins execution at the SMM base address in real mode. Ex. 1012 § 2.9.5. This section also states: “Within the SMI service routine, protected mode may be entered and exited as required and real or protected mode device drivers may be called.” *Id.* In view of this explicit disclosure, we agree with Petitioner that a person of ordinary skill would have been motivated to combine this teaching in the 6x86 Manual with that of Collins and the Pentium Manual and arrive at the claimed subject matter. We also reference our discussion above concerning the disclosures in Collins and the Pentium Manual as supporting the obviousness of claims 1–4, 11–14, and 21–24.

Claims 5–10, 15–20 and 25–30 As Obvious Over the Combination of Collins, the Pentium Manual and ASDM

Petitioner contends that, because ASDM discloses the architecture and programming development of all Intel architecture processors, it would have been obvious to combine its teachings related to SMM, protected mode, mode, and related memory conventions with Collins and the Pentium Manual. Pet. 50. As to independent claims 1, 11, and 21, Petitioner notes that ASDM discloses saving the state of the floating point unit (FPU) while in SMM by placing the processor in 32 bit protected mode before saving the FPU state. *Id.* (citing Ex. 1013, 347). Petitioner argues that ASDM describes relocating the SMRAM to an address above 1 MB and running ASDM code above 1 MB. *Id.* at 50–51 (citing Ex. 1013, 350).

Patent Owner contends that Petitioner has not established a motivation to combine these references because, aside from citing superficial similarities, e.g. ASDM's discussion of 32 bit architecture processors that include the Pentium, describing similar architectures and capabilities is insufficient to establish obviousness. PO Resp. 21. Thus, according to Patent Owner, Petitioner has not explained sufficiently why one would have been motivated to make the combination. *Id.* As Petitioner points out, however, Patent Owner understates the significance to one of ordinary skill of ASDM, which is an Intel software manual describing the architecture and programming environment of all Intel architecture processors that cross references the processors described in the Pentium Manual. Pet. Reply 23.

Patent Owner also contends that the asserted combination teaches away from the limitation reciting the processor operating at an address greater than 1 Megabyte. Patent Owner cites ASDM as disclosing problems that can occur with setting SMBASE above 1 Mbyte, arguing that the collective teaching of Collins, Pentium and ASDM counsels against implementing SMRAM above 1 Mbyte. PO Resp. 22. Petitioner characterizes Patent Owner's argument that ASDM teaches away as stemming from Collins recommendation of locating the SMI Handler below the 1MB limit while ASDM teaches locating the SMI handler above the 1MB limit. Pet. Reply 23–24. In either case, Collins describes how to implement this approach, and although he cautions the user, and recommends avoiding setting SMBASE above 1 Mbyte in circumstances where interrupts are needed, as discussed above, Collins does not teach away from the technique.

We addressed Petitioner’s arguments concerning specific claims in our Decision to Institute. Dec. to Inst. 22–25. Claims 5, 15 and 25 recite determining if control should be transferred to instruction sequences for executing a task that requires the processor to be configured to operate in in protected mode, if so configuring the processor to operate in protected mode, and otherwise continuing to process the instruction sequences stored. Patent Owner contends that ASDM fails to disclose that the processor could operate in protected mode while in SMM, as recited in claims 1, 11, and 21 from which claims 5, 15, and 25 depend, and instead shows a transition of state that requires the processor to switch to protected mode and then to return to SMM (i.e., return to the SM handler). PO Resp. 23–24 (citing Ex. 1013 at 348). Petitioner notes that ASDM discloses in some instances it will not be necessary to enter protected mode, in which case the SMM handler will operate uninterrupted. Pet. 52 (citing Polyudov Dec. ¶ 196). However, Petitioner also notes that in some instances, an SMM task is performed in protected mode. Pet. Reply (citing Polyudov Decl. ¶¶ 191, 195; Ex. 1013, 347). ASDM explicitly states: “[I]n some instances (for example, prior to powering down system memory when entering a 0-volt suspend state), it is necessary to save the state of the FPU while in SMM . . . the safest way to perform this task is to place the processor in protected mode before saving the FPU state,” Ex. 1013, 347. The subject matter cited by Patent Owner at page 348 of Exhibit 1013 is prefaced by the statement “[T]he following guidelines should be used when going into protected mode from an SMI handler to save and restore the FPU state.” Ex. 1013, 348. ASDM also states “[T]he SMI handler may continue to execute in protected mode after the FPU state has been saved and return safely to the interrupted program

from the protected mode.” *Id.* In consideration of the above, we agree with Petitioner that the combination of Collins, Pentium Manual and ASDM discloses the features recited in claims 5, 15, and 25.

Patent Owner’s argument concerning claims 6, 16, and 26, and claims 7–10, 17–20, and 27–30 is that the transition of state diagram of the Pentium Manual contradicts the limitation of operating “in protected mode while in system management mode” in the independent claims from which these claims depend. We have addressed this limitation previously in this decision and find that Petitioner has demonstrated it is disclosed in the combination of the references.

Finally, in this Decision, we adopt our analysis and apply our findings from the Decision to Institute concerning these claims. Dec. to Inst. 22–25.

CONCLUSION

In consideration of the above, we conclude that Petitioner has demonstrated by a preponderance of the evidence that:

Claims 1–4, 11–14, and 21–24 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Collins and the Pentium Manual;

Claims 1–4, 11–14, and 21–24 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Collins, the Pentium manual and IBM 6x86; and

Claims 5–10, 15–20, and 25–30 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Collins, the Pentium Manual and ASDM.

We also deny Patent Owner’s Motion to Exclude for the reasons discussed herein.

ORDER

In consideration of the above it is:

ORDERED that claim 1–30 of the '604 Patent are unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude is
DENIED; and

FURTHER ORDERED, that because this is a final written decision,
parties to the proceeding seeking judicial review of the decision must
comply with the notice and service requirements of 37 C.F.R. § 90.2.

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PATENT OWNER

IPR2015-01081
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