Trials@uspto.gov
Tel: 571.272.7822

Paper 37
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMERICAN MEGATRENDS, INC., MICRO-STAR INTERNATIONAL CO., LTD., MSI COMPUTER CORP., GIGA-BYTE TECHNOLGY, CO., LTD., AND G.B.T., INC.,
Petitioner,

v.

KINGLITE HOLDINGS INC.,
Patent Owner.

Case IPR2015-01141
Patent 6,633,976 B1

Before GLENN J. PERRY, BRIAN J. MCNAMARA, and BARBARA A. PARVIS, *Administrative Patent Judges.*

PARVIS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and
37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

American Megatrends, Inc., Micro-Star International Co., Ltd., MSI Computer Corp., Giga-Byte Technology Co., Ltd., and G.B.T., Inc.

("Petitioner") filed a Petition and a Corrected Petition (Paper 9, "Pet.")[1] to institute an *inter partes* review of claims 1–17 (the "challenged claims") of U.S. Patent No. 6,633,976 B1 (Ex. 1001, "the '976 Patent"). On November 10, 2015, we entered a Decision to Institute a trial (Paper 15, "Dec. to Inst.") on the following challenges to patentability of the claims.

References	Basis	Claims challenged
U.S. Patent No. 5,671,413 ("Shipman") (Ex. 1004) and U.S. Patent No. 5,835,760 ("Harmer") (Ex. 1003)	§ 103(a)	1–5 and 8–17
Shipman, Harmer, and U.S. Patent No. 5,999,989 ("Patel") (Ex. 1006)	§ 103(a)	6
Shipman, Harmer, and PARTIES[2]	§ 103(a)	7[3]

Kinglite Holdings Inc. ("Patent Owner") filed a Patent Owner Response (Paper 23, "PO Resp."). Patent Owner also filed the Declaration of Dr. Shahin Nazarian ("Dr. Nazarian's Declaration" or "Nazarian Declaration"). Ex. 2008. Petitioner filed a Reply (Paper 29, "Pet. Reply"). In support of its positions, Petitioner cites to the Declaration of Mr. Michael

[1] Unless otherwise noted, citations herein will be to the Corrected Petition (Paper 9).

[2] American National Standards Institute (ANSI), *Protected Area Run Time Interface Extensions Services* (Working Paper No. T13 D1367, Aug. 23, 1999) ("PARTIES") (Ex. 1011).

[3] Although the Petition indicates that claim 7 is challenged on the basis of Shipman and Harmer (Pet. 13–14), we note that Petitioner also relies on PARTIES in its contentions (Pet. 37). We, therefore, treated Petitioner's contentions regarding claim 7 as a separate ground.

Perla (Ex. 1012). Petitioner filed a Motion to Exclude the deposition transcript of Mr. Perla (Paper 31, "Motion to Exclude"), which Patent Owner opposed (Paper 34, "Oppn. Motion to Exclude").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). Having reviewed the arguments of the parties and the supporting evidence, for the reasons set forth below, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims of the '976 Patent are unpatentable.

B. Related Proceedings

Petitioner and Patent Owner identify, as related proceedings, lawsuits in the United States District Court for the Central District of California captioned *Kinglite Holdings Inc. v Giga-Byte Tech. Co.*, Case Number 1:14-cv-04989 and *Kinglite Holdings Inc. v. Micro-Star Int'l Co.*, Case Number 1:14-cv-03009. Pet. 6-7; Paper 13.

C. The '976 Patent

The '976 Patent relates to storing basic input output system (BIOS) modules of a computer in a protected area, transferring the BIOS modules to memory, and executing the BIOS modules to configure the computer. Ex. 1001, 1:9–12. The '976 Patent describes a dispatch manager that determines which BIOS modules are required for operation of the computer and, if a required BIOS module is not stored in system memory, the dispatch manager copies required BIOS modules into system memory from a secondary nonvolatile storage device. *Id.* at 3:16–26.

D. Illustrative Claim

Of the challenged claims, claims 1 and 14 are independent. Each of claims 2–13 and 15–17, depends, directly or indirectly, from claim 1 or 14. Independent claim 1 is illustrative and is reproduced below (*id.* at 10:5–67).

> 1. A method for processing basic input output system (BIOS) modules of a computer having a central processing unit (CPU), a computer bus, and a critical nonvolatile storage device, comprising the steps of:
>
> storing a predetermined small amount of BIOS initialization code in a first portion of the critical nonvolatile storage device that is operative to initialize the CPU and the system memory;
>
> storing a dispatch manager in a second portion of the critical nonvolatile storage device that is operative to selectively load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer;
>
> turning on the computer;
>
> executing the predetermined small amount of BIOS initialization code to initialize the CPU and the system memory;
>
> copying the dispatch manager from the critical nonvolatile storage device to the system memory; and
>
> executing the dispatch manager to execute the predetermined number of tasks to initialize the computer.

E. Claim Construction

1. Legal Standard

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *cf. Cuozzo Speed Techs., LLC v. Lee*, 136 S.Ct. 2131, 2144–46 (upholding the use of the broadest reasonable interpretation standard as the claim

construction standard to be applied in an *inter partes* review proceeding). Consistent with the rule of broadest reasonable interpretation, claim terms also are generally given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc*., 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999).

2. Decision to Institute

In the Decision to Institute, we determined the broadest reasonable interpretation of the following terms: "small amount of BIOS initialization code," "BIOS modules," "a dispatch manager . . . that is operative to selectively load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer," "critical nonvolatile storage device," and "system memory." Dec. to Inst. 5–10. In its Patent Owner Response, Patent Owner's contentions implicitly relate to the construction of the term "selectively load," within the phrase "a dispatch manager . . . that is operative to selectively load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer." PO Resp. 8–11. We discuss Patent Owner's contentions regarding this term below.

Neither party's argument persuades us to revise our interpretations of "small amount of BIOS initialization code," "BIOS modules," "critical nonvolatile storage device," and "system memory." Accordingly, we adopt

as final our determinations as set forth in the Decision to Institute regarding the broadest reasonable interpretations of those terms. Dec. to Inst. 5–7, 9, 10.

3. "a dispatch manager . . . that is operative to selectively load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer"

Each of independent claims 1 and 14 recites "a *dispatch manager* . . . that is operative to *selectively* load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer" (emphasis added). In the Decision to Institute, we determined that the broadest reasonable interpretation of "a dispatch manager . . . that is operative to selectively load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer" is "program code that issues fetched instructions and . . . is operative to identify a predetermined number of tasks relating to completing initialization of the computer, load these tasks, and iteratively execute these tasks." Dec. to Inst. 8.

Additionally, we determined that although claim 1 recites "selectively load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer," because "claim 1 also recites 'comprising the steps of,' other tasks not relating to initialization also may be loaded and executed." *Id.* In particular, we explained that "[c]omprising" is a term of art used in claim language, which means that the named elements are essential, but other elements also may be included to constitute additional components within the scope of the claim. *Id.* (citing *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997)).

Patent Owner does not dispute expressly our construction or provide a proposed construction. PO Resp. 10, 11. Patent Owner, however, implicitly contends that the broadest reasonable interpretation of "selectively load" is "loading more than one, but less than all, components." *Id.* at 11. Patent Owner's contentions are vague as to what constitutes "all, components," and therefore, Patent Owner's position is vague as to what constitutes less than all components. Additionally, Patent Owner does not point to intrinsic evidence to clarify or support its position, such as a definition or examples in the '976 Patent Specification. *Id.* at 10, 11. Also, Patent Owner's declarant does not testify regarding claim construction.

As support for its contention, Patent Owner points only to Mr. Perla's deposition testimony "[a]s Dr. Perla acknowledged, loading all modules would not be 'selective' loading." PO Resp. 10 (citing Ex. 2006, 22:22–24). We look to Mr. Perla's deposition testimony to obtain clarification of Patent Owner's contention and determine whether Mr. Perla's testimony supports Patent Owner's position. Mr. Perla's deposition testimony relied upon by Patent Owner, along with immediately preceding testimony, is reproduced below.

> Q. Claim 1 of the '976 Patent, what does "selectively load" mean?
>
> A. It would refer to the use of a packing list or some predetermined array of modules that would need to be loaded, presumably smaller than the available modules that were either *shipped on the ROM or shipped on the entire platform*.
>
> Q. If all modules were loaded, that would not be selective loading?
>
> A. That would be correct.

Ex. 2007, 22:15–24 (emphasis added).

Mr. Perla does not provide guidance regarding what modules would be "shipped on the ROM or shipped on the entire platform." *Id.* For instance, his testimony leaves open the possibility that modules other than BIOS modules meet the criteria of being shipped on the ROM or shipped on the entire platform. Accordingly, all BIOS modules could be less than all the modules that are the subject of the testimony above. Because Mr. Perla's testimony is unclear, we find that Mr. Perla's testimony standing alone does not support that "selectively load" requires loading less than all BIOS modules. Instead, we find that Mr. Perla's testimony is consistent with the broadest reasonable interpretation in the Decision to Institute that Patent Owner does not challenge expressly.

For completeness, we turn to the claims and the '976 Patent Specification to determine if the broadest reasonable interpretation of "selectively load" requires loading less than all the BIOS modules. We do not find a requirement of loading less than all the BIOS modules. Each of claims 1 and 14 recites that the dispatch manager "is operative to selectively load and iteratively execute a predetermined number of tasks relating to *complete initialization of the computer*." The '976 Patent Specification describes "[s]elected BIOS modules" as those that are "required for operation of the computer." Ex. 1001, 2:24, 25. Other description in the '976 Patent Specification reiterates the actual recitation of the claim. *See, e.g., id.* at 2:65–67; 5:32–35; 6:34–38. The only other description in the '976 Patent Specification describes "selected BIOS modules as those that are "identified in its list of tasks to execute." *Id.* at 3:10–12; *see also id.* at 5:40–43 ("The dispatch manager 17 executes the *list of tasks* contained

therein to cause all required BIOS modules to be loaded into the system memory 13" (emphasis added).)

Accordingly, we are not persuaded to revise our determinations in the Decision to Institute regarding the broadest reasonable interpretation of "a dispatch manager . . . that is operative to selectively load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer," recited in claims 1 and 14. Additionally, we are not persuaded to revise our determination in the Decision to Institute regarding the meaning of the term "comprising" in the claims. We, however, determine that the broadest reasonable interpretation of "selectively load" encompasses the only examples set forth in the specification, i.e., loading BIOS modules that are "identified in its list of tasks to execute." *Id.* at 3:10–12; *see also id.* at 5:40–43 ("The dispatch manager 17 executes the *list of tasks* contained therein to cause all required BIOS modules to be loaded into the system memory 13" (emphasis added).)

II. PATENT OWNER'S DECLARATION

Patent Owner filed the Declaration of Dr. Shahin Nazarian (Ex. 2008), which is two pages long (Paragraphs 1 through 6). Although Patent Owner identifies Dr. Nazarian's Declaration in its Exhibit List (PO Resp. iii), Patent Owner does not cite to or otherwise expressly rely on Dr. Nazarian's Declaration in the Patent Owner Response. *See generally* PO Resp.

"The Board may exclude or give no weight to the evidence where a party has failed to state its relevance or to identify specific portions of the evidence that support the challenge." 37 C.F.R. § 42.104 (b)(5); *see also* 37 C.F.R. §§ 42.23, 42.120 ("Oppositions and replies must comply with the content requirements of motions" and "[a] patent owner response is filed as

an opposition."). The Office Patent Trial Practice Guide provides "[t]he [Patent Owner] response . . . should include any affidavits or additional factual evidence sought to be relied upon *and explain the relevance of such evidence*." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012) (emphasis added).

Because Patent Owner did not cite to or otherwise expressly rely on Dr. Nazarian's Declaration in the Patent Owner Response (*see generally* PO Resp.), we give no weight to Dr. Nazarian's Declaration (Ex. 2008). So that this Decision addresses to the fullest extent possible the parties' contentions and evidence, and in view of the brevity of Dr. Nazarian's Declaration, below we discuss his testimony. We, however, provide this analysis without determining whether Petitioner reasonably could have understood Dr. Nazarian's testimony as pertaining to a particular Patent Owner contention such that Petitioner had notice to provide responsive contentions in its Petitioner Reply.

III. ANALYSIS

A. Overview

A patent claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103(a). The question of obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the

prior art; (3) the level of skill in the art;[4] and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Additionally, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

B. Obviousness of Claims 1–5 and 7–17

Petitioner contends that each of claims 1–5 and 7–17 of the '976 Patent is rendered obvious by the combined teachings of Shipman and Harmer. Pet. 14–50.

1. Shipman

Shipman relates to an object-oriented BIOS system using data compression. Ex. 1004, 1:7–9. The services provided by Shipman's BIOS are implemented via independently executable service components. *Id.* at Abstract. The BIOS is provided with a decompression dispatcher for decompressing and dispatching the service components into random access memory (RAM) of the computer system for execution. *Id.* at 1:37–41. When dispatching components, the decompression dispatcher works from a Packing List. *Id.* at 5:27–28. The Packing List provides information regarding the types of components that have been packed into the ROM. *Id.*

[4] Petitioner's declarant proposes a definition for a person of ordinary skill in the art. Ex. 1012 ¶ 14. Patent Owner does not challenge Petitioner's declarant's proposed definition and does not propose an alternative. To the extent necessary and for purposes of this Decision, because we find Mr. Perla's testimony to be persuasive, we adopt Petitioner's definition.

at 5:32–34. Shipman teaches a flow for dispatching components. *Id.* at 2:39–40.

Each BIOS component is self-contained and performs a certain task or function. *Id.* at 3:7–8. Figure 1 of Shipman is reproduced below.

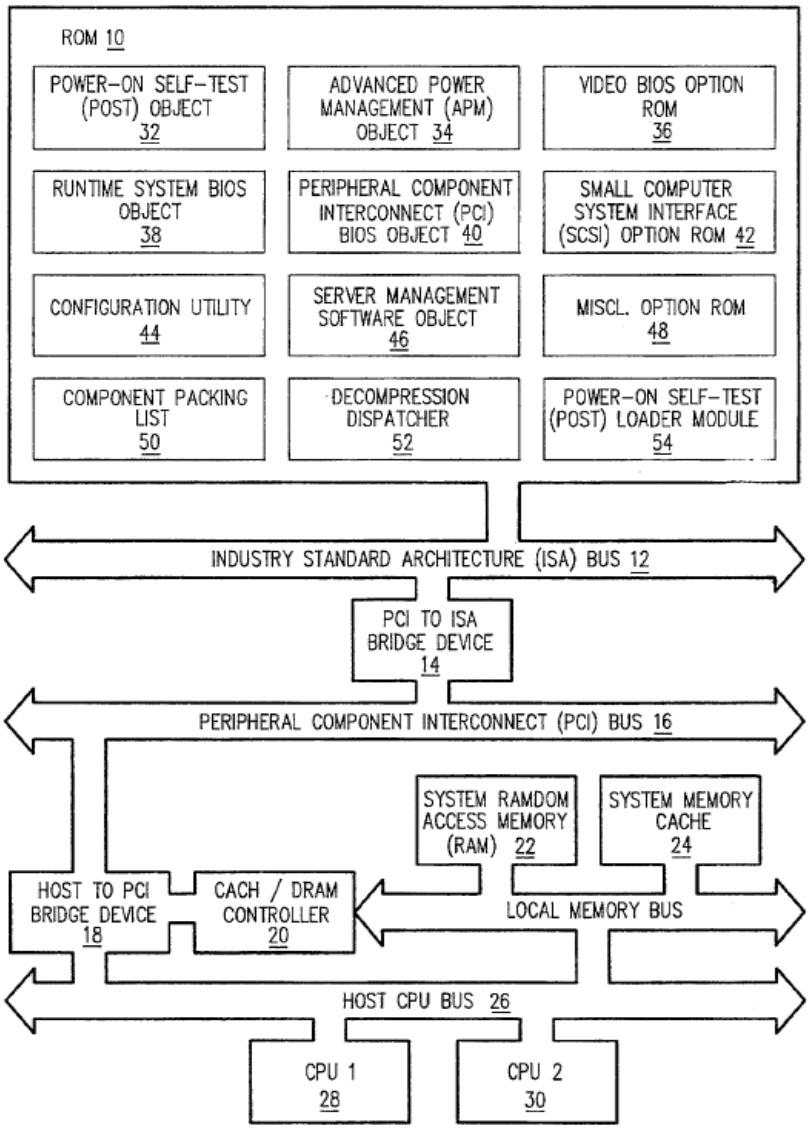


FIG. 1

Figure 1 is a block diagram of a computer system including a set of BIOS programs.

As illustrated in Figure 1, Shipman's BIOS is organized into a set of BIOS components 32 through 54, each of which is capable of being dispatched as an independent executable object. *Id.* 3:5–8. The BIOS components fall into three major types: initialization components, runtime components, and functional components. *Id.* at 3:10–12. An example of an initialization component is the POST Object. *Id.* 4:53–54. As shown in Figure 1, the BIOS is encoded in ROM 10. *Id.* at 3:1–2. The BIOS transfers data instructions between a CPU to peripheral devices. *Id.* at 1:14–16.

2. Harmer

Harmer relates to a method for operating a computer system using BIOS. Ex. 1003, 1:5–9. At least a portion of BIOS is stored in memory of a peripheral device. *Id.* at Abstract. Harmer teaches an example in which a first portion of BIOS is stored in ROM in a host computer. *Id.* at 6:49–51. A second portion of BIOS is stored in memory of a peripheral device. *Id.* at 6:51–53. The second portion of the BIOS is retrieved and stored in RAM. *Id.* at 6:54–55. Harmer teaches a first portion of BIOS that includes small amount of initialization code 124. *Id.* at 9:38–40.

3. Claims 1 and 14

Claims 1 and 14 are the only independent challenged claims. Claim 1 recites a method for processing BIOS modules, comprising the steps discussed below. Claim 14 is similar to claim 1, except claim 14 recites two additional limitations, which are noted below.

a. The Petition

The preamble of each of claim 1 and claim 14 includes the following recitation "[a] method for processing basic input output system (BIOS) modules of a computer having a central processing unit (CPU), a computer

bus, and a critical nonvolatile storage device." The preamble of claim 14 further recites "secondary nonvolatile storage device." Although Petitioner does not dispute that the preamble is limiting to the extent that it provides antecedent basis for elements recited in the body of the claim, Petitioner contends that "BIOS modules" recited in the preamble is not a limitation recited in the body of claim 1. Pet. 19. Petitioner, however, contends this is of no consequence as Shipman teaches BIOS modules. *Id.* Petitioner points to Shipman's teaching that "[t]he BIOS stored in read only memory (ROM) is organized into a set of components," such as "a set of BIOS components (32 through 54), each of which is capable of being dispatched as an independent executable object." *Id.* at 19, 20 (citing Ex. 1004, 1:60–63, 3:5–8, Fig. 1).

For the remaining structural elements recited in the preamble, i.e., a central processing unit (CPU), a bus, and a critical nonvolatile storage device, Petitioner points to Figure 1 of Shipman. *Id.* at 20. Figure 1 of Shipman illustrates a block diagram of a computer system comprising the following inter-connected components "CPU 1" 28, "CPU 2" 30, "PERIPHERAL COMPONENT INTERCONNECT (PCI) BUS" 16, "INDUSTRY STANDARD ARCHITECTURE (ISA) BUS" 12, "SYSTEM RANDOM ACCESS MEMORY (RAM)" 22, "SYSTEM MEMORY CACHE" 24, and "ROM" 10. Ex. 1004, Fig. 1. Petitioner also points to the flow diagram shown in Figure 12, as well as other teachings regarding storing instructions in memory. Pet. 19–21, 40 (citing Ex. 1004, 1:60–63, 14:35–38, Figs. 1, 12; Ex. 1012 ¶¶ 58, 65–67).

For the secondary nonvolatile storage device recited in claim 14, Petitioner points to Shipman's teaching of "disk drives" (*id.* at 29, 47 (citing

Ex. 1004, 1:16)) and Harmer's teaching of a "mass memory storage peripheral computer device" (*id.* at 29 (citing Ex. 1003, 6:59–64)). Petitioner additionally relies on the declaration testimony of Mr. Perla that a person of ordinary skill in the art would have understood "that a disk drive is mass media storage that is nonvolatile and separate from the BIOS ROM." Ex. 1012 ¶ 127 (citing Ex. 1004, 1:14).

Each of claim 1 and claim 14 also recites "storing a predetermined small amount of BIOS initialization code in a first portion of the critical nonvolatile storage device that is operative to initialize the CPU and the system memory." Petitioner points to the BIOS flow diagram illustrated in Figure 2 of Shipman and related teachings, including step 202, i.e., "code that 'tests and initializes the memory controller related components,'" as well as steps 204 and 206, i.e., "initializ[ing] a decompression dispatcher" and "dispatching BIOS modules," including "initialization modules such as POST." *Id.* at 22 (citing Ex. 1004, 2:32–33, 4:53–54, 12:10–16, Fig. 2). With respect to the recitation of "small amount," Petitioner also points to Harmer's teaching of "a small amount of initialization code 124." Pet. 22, 23 (citing Ex. 1003, 9:38–40). Petitioner additionally relies on Mr. Perla's testimony (*id.* at 21–23 (citing Ex. 1012 ¶¶ 41, 70–73)), including his testimony that "initializing the CPU immediately after power up has been a part of commercial personal computers (PCs) since the 1980s." *Id.* (citing Ex. 1012 ¶ 72).

Each of claim 1 and 14 additionally recites "storing a dispatch manager in a second portion of the critical nonvolatile storage device that is operative to selectively load and iteratively execute a predetermined number of tasks relating to complete initialization of the computer." Petitioner

points to Shipman's teaching that "[t]he decompression dispatcher, which 'is responsible for all dispatching activities,'" is stored in ROM 10. *Id.* at 24, 25 (citing Ex. 1004, 1:37–40, Fig. 1). Regarding the operation of Shipman's dispatcher, Petitioner points to Shipman's teaching that "[e]ach of Shipman's modules 32–54 is 'capable of being dispatched as an independent executable object," and "[t]he flowchart of Fig. 5," which Petitioner contends "illustrates that the decompression dispatcher selectively loads and iteratively executes the modules." *Id.* at 25 (citing Ex. 1004, 2:39–40, 3:5–10, Fig. 5). Petitioner provides more specificity regarding its contentions relating to the operation of Figure 5, as well as dispatching tasks relating to initialization of the computer. *Id.* at 25, 26, 41 (citing Ex. 1004, 1:66–2:3, 5:27–29, 5:32–34, 12:63–13:2, Fig. 5). Petitioner also relies on the testimony of Mr. Perla (*id.* at 24–26, 40–41 (citing Ex. 1012 ¶¶ 81–85)), including his testimony that a "module is selected based on packing information" (Ex. 1012 ¶ 82).

Claim 14 further recites "storing a predetermined number of BIOS modules on the secondary nonvolatile storage device that are operative to control operation of the computer." As noted above, Petitioner points to Shipman's teaching of "disk drives" (Pet. 29, 47 (citing Ex. 1004, 1:16)) and Harmer's teaching of a "mass memory storage peripheral computer device" (*id.* at 29 (citing Ex. 1003, 6:59–64)) for the secondary nonvolatile storage device.

For storing a predetermined number of BIOS modules on such secondary storage, Petitioner points to Harmer's teaching of storing "[a] second portion of the system BIOS [ ] within the mass memory storage of the mass memory storage peripheral computer device." Pet. 29, 48 (citing

Ex. 1003, 6:59–64); *see also* Ex. 1003, Abstract ("The arrangement and method of the invention allows at least a portion of the BIOS to be stored within the mass memory storage of a mass memory storage peripheral computer device rather than being stored within ROM."). Petitioner relies on other teachings of Shipman and Harmer, as well as the testimony of Mr. Perla. Pet. 29, 30, (citing Ex. 1003, 4:63–67, 6:64–67; Ex. 1012 ¶¶ 127, 149, 162, 163, 169).

Each of claims 1 and 14 further recites after "turning on the computer," "executing the predetermined small amount of BIOS initialization code to initialize the CPU and the system memory," "copying the dispatch manager from the critical nonvolatile storage device to the system memory," and "executing the dispatch manager." Claim 14 further recites that the dispatch manager "execute[s] the predetermined number of tasks to completely initialize the computer, which predetermined number of tasks include sequentially copying selected BIOS modules from the protected area of the secondary nonvolatile storage device to the system memory and sequentially executing the copies BIOS modules to initialize the computer." These recitations involve executing stored code, discussed above.

Petitioner additionally provides reasons to combine Harmer and Shipman. *Id.* at 16–18. For instance, Petitioner points to a similarity, "Shipman suggests that its BIOS initialization code in step 202 is 'small'" (Pet. 22 (citing Ex. 1012 ¶ 75)) and "Harmer teaches that the initialization code can be a 'small amount'" (*id.* (citing Ex. 1003, 9:38–40)). Against this background, Petitioner contends that a person of ordinary skill in the art "would be motivated to combine Harmer with Shipman in order to minimize

initialization code, which has the benefit of reducing 'the cost of the ROM as much as possible.'" *Id.* at 22–23 (citing Ex. 1003, 11:42–45).

As an additional reason to combine, Petitioner points to another similarity: "[l]ike Shipman, Harmer divides the BIOS." *Id.* at 16. In view of this similarity, Petitioner, in reliance on the testimony of Mr. Perla, contends that a person of ordinary skill in the art would have been motivated to combine Shipman and Harmer because Harmer encourages a person of ordinary skill in the art to store some BIOS in secondary memory to reduce the cost of ROM. *Id.* at 16–17 (citing Ex. 1012 ¶¶ 29, 103, 107, 151, 162, 163, 169). Mr. Perla testifies that Harmer encourages a person of ordinary skill in the art to store BIOS in a secondary nonvolatile memory device (e.g., disk drive) to reduce or eliminate the cost of expansion BIOS ROM associated with the secondary memory when the secondary memory is a peripheral computer device. Ex. 1012 ¶ 162 (citing Ex. 1003, 4:63–67). Mr. Perla further testifies that a secondary nonvolatile memory device is an obvious choice to store relocated expansion BIOS because it is "one among a few possibilities," and Harmer "explains that value, and use, of an 'expansion BIOS' in relationship to BIOS." *Id.* ¶ 163 (citing Ex. 1003, 1:20–50).

b. The Patent Owner Response and Petitioner Reply

With respect to independent claim 1, Patent Owner contends "**Dr. Perla's Opinions Should be Disregarded**" (PO Resp. 2–5), Petitioner has not shown a "**Motivation to Combine**" (*id.* at 6–8), and the asserted references do not teach "**Storing**" (*id.* at 8–10), "**Selectively Load**" (*id.* at 10, 11), and "**Small Amount of BIOS Initialization Code**" (*id.* at 13–15). With respect to claim 14, Patent Owner also contends that the asserted

references do not teach "**Secondary Nonvolatile Storage Device**" and "**Protected Area**." *Id.* at 12–13. We evaluate each of these contentions in turn.

First, we consider Patent Owner's contention that Mr. Perla's testimony should be disregarded. *Id.* at 2–4. Patent Owner, more specifically, contends "Dr. Perla fabricates an aspect of modularity purportedly included in Harmer's teachings." *Id.* at 2. We, however, note that Patent Owner acknowledges that Shipman "contemplates modularity." *Id.* During the oral hearing, Patent Owner again similarly acknowledged, "I agree, Shipman does teach BIOS modularity." Tr. 29:3–4. Additionally, Patent Owner did not dispute that the asserted references taken together teach "BIOS module." *See generally* PO Resp.

Regarding Patent Owner's contentions that Dr. Perla's testimony should be disregarded because he fabricated an aspect of modularity in Harmer (*id.* at 2), Patent Owner first draws attention a single sentence in Mr. Perla's declaration that states that Harmer "permits portions of BIOS stored in RAM or a hard drive to be expansion BIOS" and, "**therefore contemplates BIOS modularity.**" *Id.* at 3 (citing Ex. 1012 ¶ 56). Patent Owner then contends that during his deposition Mr. Perla made a concession regarding his declaration testimony and, therefore, "scrambled," and led counsel "on a wild goose chase" to supplement his declaration. *Id.* at 3, 4. We do not agree with Patent Owner's characterization of Mr. Perla's testimony.

Regarding the asserted concession, Patent Owner, more specifically, contends that Mr. Perla "conceded that a Harmer BIOS portion would not satisfy the Board's construction of BIOS module." *Id.* at 3 (citing Ex. 2007,

28:7–8, 28:10–16, 29:7–23). However, consistent with Mr. Perla's declaration testimony, during his deposition, Mr. Perla testified as follows regarding expansion BIOS in Harmer:

> Q. . . By the way, do you understand *BIOS extension to be synonomous with a BIOS module*?
>
> A. *Yes*.
>
> Q. And what about a BIOS extension would make it a module?
>
> A. *The nature of including additional components that would be loaded after an initial BIOS has been executed* from the burned-in ROM on the platform.

Ex. 2007, 30:3–11 (emphasis added).

As was clarified later, the word "extension" above means "expansion." *Id.* at 31:11–16. Considering Mr. Perla's testimony in its entirety, we do not find that Mr. Perla conceded during his deposition, but instead we find that Mr. Perla's deposition testimony, including the testimony emphasized above, is consistent with his declaration testimony that Harmer's teachings of expansion BIOS are similar to those teachings in Shipman relied upon by Petitioner. *Compare* Ex. 1012 ¶ 56 *with* Ex. 2007, 30:3–11.

Additionally, we find that Patent Owner's deposition questions are phrased too narrowly to support Patent Owner's contention. In particular, in its questioning of Mr. Perla during his deposition, Patent Owner's counsel asked whether Harmer's BIOS portions are "synonymous" with the recitation of "BIOS module" (Ex. 2007, 28:10, 11) and whether certain of passages of Harmer would "necessarily" "satisfy the board's definition of BIOS module" (*id.* at 36:19–37:1). Even if Petitioner were relying on Harmer for teaching modules, which is not the case here, an obviousness inquiry involves what the asserted reference teaches or suggests.

We turn to Patent Owner's contentions that Mr. Perla "scrambled to find anything in Harmer that suggested BIOS modularity" and led "counsel on a wild goose chase." PO Resp. 3–4. Patent Owner's contention does not take into consideration that Patent Owner's counsel specifically asked for more examples, i.e., "In Harmer, do you see any teachings that you believe teach BIOS modularity *other than references to expansion BIOS or BIOS portions*?" Ex. 2007, 31:17–19 (emphasis added).

Additionally, Patent Owner cherry-picks certain bits of Mr. Perla's testimony taking them out of the context of the deposition questions and the teachings of the references. For example, Patent Owner contends that Mr. Perla testified that "element 18, which is a peripheral device" is a BIOS module. PO Resp. 4. However, considering Mr. Perla's testimony in context, after confusion regarding the cover of Harmer (Ex. 2007, 32:6–17 (questioning includes "I'm sorry" by Patent Owner's counsel)), Mr. Perla points to Harmer's peripherals (*id.* at 33, 34), which Harmer teaches are related, i.e., "the expansion BIOS *of a peripheral device*" (Ex. 1003, 3:14 (emphasis added)). That Patent Owner chose not to request clarification does not undermine the accuracy of Mr. Perla's testimony as a whole. Accordingly, we do not agree with Patent Owner's characterization of Mr. Perla's testimony.

Second, we consider Patent Owner's contention that Petitioner has not shown a "**Motivation to Combine**." PO Resp. 6. Patent Owner, more specifically, contends:

> As noted above in Section III, Dr. Perla opined that one would have been motivated to combine the Harmer and Shipman references given that both deal with BIOS modularity. As further described in that section, Dr. Perla's deposition testimony showed that there was ***no*** support for that opinion, as Harmer's purported BIOS modularity was fiction.

PO Resp. 6.

For the reasons discussed above, we do not agree with Patent Owner that there was no support for Mr. Perla's testimony. Regarding Patent Owner's contention that Mr. Perla's testimony regarding Harmer "was fiction," we do not agree, particularly in light of Petitioner's use of this testimony to show similarities in the teachings of Shipman and Harmer as a reason to combine the teachings of the references. More specifically, Patent Owner contentions pertain to one of these similarities, i.e., Petitioner's contention that "[l]ike Shipman, Harmer divides the BIOS" (Pet. 16). Contrary to Patent Owner's contention that Mr. Perla's declaration testimony is based on "fiction" (PO Resp. 6), as Petitioner correctly notes (Pet. 16), Harmer teaches, for example, "includ[ing] ROM storage memory (peripheral ROM) for containing a first portion but not all of the expansion BIOS associated with the particular peripheral computer device" (Ex. 1003, 5:39–43) (*see also id.* at Abstract ("The arrangement and method of the invention allows at least a portion of the BIOS to be stored within the mass memory storage of a mass memory storage peripheral device rather than being stored within ROM.").

Patent Owner also contends "Petitioners cannot have it both ways—either expansion BIOS is an example of a BIOS module . . . or it is a cost one would seek to eliminate in combining the references." PO Resp. 6, 7. Petitioner's proposed modification, however, is that Shipman's BIOS

modules are relocated from ROM to a secondary nonvolatile storage device and Petitioner's reason to modify is to reduce the costs of an expensive ROM. (Pet. 15-16). Petitioner, in reliance on the testimony of Mr. Perla, contends that a person of ordinary skill in the art would have been motivated to combine Shipman and Harmer because Harmer encourages a person of ordinary skill in the art to store some BIOS in secondary memory to reduce the cost of ROM. Pet. 16–17 (citing Ex. 1012 ¶¶ 29, 103, 107, 151, 162, 163, 169).

Consistent with Petitioner's contention, Mr. Perla testifies, for example, that Harmer encourages a person of ordinary skill in the art to store BIOS in a secondary nonvolatile memory device (e.g., disk drive) to reduce or eliminate the cost of expansion BIOS ROM associated with the secondary memory when the secondary memory is a peripheral computer device. Ex. 1012 ¶ 162 (citing Ex. 1003, 4:63–67); *see also* Pet. 17 (citing Ex. 1003, 4:57–61, 4:63–67). We give Mr. Perla's testimony substantial weight (*see* 37 C.F.R. § 42.65), as it is consistent with Harmer's teachings, referenced therein, including those set forth below:

> The arrangement and method allow at least a portion of the BIOS to be stored within the mass memory storage of a mass memory storage peripheral device which is connected to the host computer. The BIOS stored within the mass memory storage may be expansion BIOS associated with any particular peripheral computer device and/or expansion BIOS associated with the mass memory storage peripheral computer device itself. The BIOS stored within the mass memory storage may also be system BIOS associated with the host computer. This approach significantly reduces or even eliminates the need for and cost of the expansion BIOS ROM for the particular peripheral computer device and/or the expansion BIOS ROM for the mass memory storage peripheral computer device.

Ex. 1003, 4:53–67.

Mr. Perla further testifies that a secondary nonvolatile memory device is an obvious choice to store relocated expansion BIOS because it is "one among a few possibilities," and Harmer "explains that value, and use, of an 'expansion BIOS' in relationship to BIOS." *Id.* ¶ 163. We again give Mr. Perla's testimony substantial weight because it is consistent with the teachings of Harmer discussed above, including Harmer's teaching of allowing a portion of BIOS associated with either a peripheral or the host to be stored in peripheral storage and the cost benefits of doing so. Ex. 1003, Abstract, 4:53–67. Mr. Perla's testimony is further consistent with Harmer's teaching of a flexible arrangement that allows peripherals to interconnect. Specifically, as Mr. Perla testifies (Ex. 1012 ¶ 163), Harmer teaches "[t]he PCI peripheral bus" is designed "to be both processor and computer system architecture independent" thereby "allow[ing] the same peripheral computer device to be connected to a variety of different host systems" (*id.* at 1:20–50).

Patent Owner, additionally, contends that because Mr. Perla did not personally encounter Shipman and Harmer at the time of invention, a person of ordinary skill in the art would not have combined the teachings of the two references. PO Resp. 7. Patent Owner's contention is contrary to legal precedent that a person of ordinary skill in the art is presumed to be aware of all pertinent prior art. *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 454 (Fed. Cir. 1985). Patent Owner does not provide persuasive legal support for its reliance on personal familiarity by Mr. Perla with the asserted prior art references.

Patent Owner further contends "[t]here is also a disincentive to combining Shipman and Harmer." PO Resp. 8. Patent Owner overstates the teachings of the references in an attempt to draw a distinction: "[g]iven Shipman's purposeful exclusion of secondary storage, and Harmer's express use of such storage, one of skill in the art would not have thought to combine these two references." *Id.; see also* Ex. 2008 ¶¶ 4–6. To the contrary, as discussed above, Shipman implicitly supports the use of BIOS modules in secondary storage. Moreover, even if Patent Owner's contention regarding Shipman's exclusion were true, such an omission would not amount to a criticism or discrediting. *See DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) ("A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not 'criticize, discredit, or otherwise discourage' investigation into the invention claimed.") (*quoting In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)).

As discussed above, the Petition provides an additional reason to combine the teachings of Harmer and Shipman. Specifically, Petitioner points to another similarity: "Shipman suggests that its BIOS initialization code in step 202 is 'small'" (Pet. 22 (citing Ex. 1012 ¶ 75)) and "Harmer teaches that the initialization code can be a 'small amount'" (*id.* (citing Ex. 1003, 9:38–40)). Against this background, Petitioner contends that a person of ordinary skill in the art "would be motivated to combine Harmer with Shipman in order to minimize initialization code, which has the benefit of reducing 'the cost of the ROM as much as possible.'" *Id.* at Pet. 22–23 (citing Ex. 1003, 11:42–45). Patent Owner does not challenged this reason to combine Shipman and Harmer. PO Resp. 6–8. We find that Petitioner's

contentions and Mr. Perla's testimony are consistent with the teachings of the references cited therein and, accordingly, we give Mr. Perla's testimony substantial weight.

A proper obviousness analysis requires an articulated reasoning with rational underpinnings to support a motivation to combine teachings. *In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006). Based on the complete record now before us, for the reasons given, we find reasonable Petitioner's asserted rationale and we are persuaded that Petitioner has satisfied its burden in providing articulated reasoning with rational underpinnings to support the legal conclusion of obviousness.

Third, we turn to Patent Owner's contention that the asserted references do not teach "**Storing**" a predetermined small amount of BIOS code recited in claims 1 and 14. PO Resp. 8–10. We start by noting that we agree with Petitioner (Pet. Reply 1) that Patent Owner's contention pertains only to teachings identified by Petitioner for the first storing step, but not other "storing" steps.

Regarding Patent Owner's contention with respect to the first step, Patent Owner, more specifically, contends that these teachings occur "after powering on," rather than "occur[ring] before the computer is powered on," as recited in claims 1 and 14. PO Resp. 8, 9. Petitioner's contentions, however, pertain to the recitation considered in its entirety, including recitation of code that "is *operative to* initialize the CPU and the system memory" (emphasis added). Petitioner's contentions, for example, pertaining to Figure 2 of Shipman (Pet. 21–23), explain that the code is operative to initialize the CPU and system memory, i.e., "TEST AND INITIALIZE MEMORY CONTROLLER RELATED COMPONENTS"

(Ex. 1004, Fig. 2). In the context of the claim, the function following "operative to" is performed as part of the execution step after the computer is turned on. The "executing" step performed after turning on the computer is discussed further below.

With respect to "storing a predetermined small amount of BIOS initialization code" that occurs prior to turning on the computer, although Patent Owner does not contend that an express construction is needed (PO Resp. 8, 9), we note an example in the '976 Patent Specification. In particular, the '976 Patent Specification describes as background that BIOS "is typically stored in nonvolatile memory" and that it "brings up (initializes) a computer system when it is *powered on*." Ex. 1001, 1:4–17 (emphasis added).

With respect to Patent Owner's identification of Petitioner's contention pertaining to "Box 202 of Figure 2" (PO Resp. 8, 9 (citing Ex. 1012 ¶ 69)), as Petitioner correctly notes (Pet. 21, 22), Shipman teaches Figure 2 is part of the BIOS. Ex. 1004, 2:32–33, 12:8–10). According to Shipman, background art includes "[i]n IBM compatible personal computers a set of programs called basic input/output system (BIOS) are encoded in read-only memory (ROM)." Ex. 1001, 1:12–14. As Petitioner also correctly contends, Shipman provides further teachings regarding storing BIOS in non-volatile memory. *See, e.g.*, Pet. 16, 19, 20, 25, 26, 40, 41 (citing Ex. 1004, Abstract, 1:37–45, 1:60–63, Fig. 1); *see also* Ex. 2007, 47 (citing Ex. 1004, 65–67 (describing that BIOS is "pre-stored in the non-volatile storage"). Shipman's teachings are consistent with the plain and ordinary meaning of "storing" and the example set forth in the '976 Patent Specification.

Petitioner additionally points to Harmer's teachings, as well as the '976 Patent Specification's description of Harmer. Pet. 16 (citing Ex. 1001, 1:55–60; Ex. 1003, 5:39–43).[5] As Petitioner correctly notes (*id.*), Harmer teaches "includ[ing] ROM storage memory (peripheral ROM) for containing a first portion but not all of the expansion BIOS." Ex. 1003, 5:39–43. Harmer additionally describes background art including that "the ROM may be manufactured with the expansion BIOS programmed into the ROM at the time of manufacture of the ROM." Ex. 1003, 4:24–27. Furthermore, in its description of Harmer, the '976 Patent Specification describes that Harmer teaches "[a] first portion of the BIOS (initialization code) is stored in a read only memory (ROM)." Ex. 1001, 1:44–46.

We further note that in response to a similar contention by Patent Owner in its Preliminary Response, in the Decision to Institute, we noted that it would have been obvious to one of ordinary skill in the art to store code that is to be executed later. Dec. to Inst. 16, 17. Patent Owner has not contested this finding. PO Resp. 8, 9; *see also* Pet. Reply 1.

Based on the complete record now before us, for the reasons given, we are persuaded that Petitioner has shown sufficiently that the asserted art teaches or suggests the first storing step recited in claims 1 and 14.

Fourth, we consider Patent Owner's contention that the asserted references do not teach "**Selectively Load**," recited in claims 1 and 14. PO Resp. 10, 11. Patent Owner more specifically contends that "Dr. Perla found himself modifying his opinions wholesale on the fly during his deposition" and "[b]ecause the Board instituted this proceeding based upon Dr. Perla's

[5] The '976 Patent Specification describes Harmer. *Compare id.* at 1:36–39 *with* Ex. 1003, [11], [45], [54].

original opinion regarding selective loaded—an opinion that turns out to be unfounded, the Board should confirm the patentability of the subject claims." *Id.* at 11.

Patent Owner's contention that Dr. Perla's "original opinion . . . turns out to be unfounded" (PO Resp. 11) is based on Patent Owner's characterization of Mr. Perla's testimony that "selectively load" would refer to "presumably smaller than the available modules that were either *shipped on the ROM or shipped on the entire platform*" (Ex. 2007, 22:15–21 (emphasis added)), which we discussed above with respect to claim construction. In particular, Patent Owner contends that "[a]s Dr. Perla acknowledged, loading all modules would not be 'selective' loading" and, therefore, "[a]pparently, Dr. Perla believes that, in Figure 5, Shipman teaches loading options between one class component and all class components." PO Resp. 11 (citations omitted).

Although, for the reasons discussed above with respect to claim construction, we are not persuaded that the claims require an option between one class component and all class components, for completeness, we make two sets of findings. In particular, we make (1) findings based on the interpretation in the Decision to Institute, and (2) separate and independent findings based on an interpretation of "selectively load" that is limited to loading more than one, but less than all the BIOS modules.

We now turn to the first set of findings, i.e., findings based on the interpretation in the Decision to Institute. Applying the broadest reasonable interpretation discussed above with respect to claim construction (Dec. to Inst. 8) we consider whether the combination of Shipman and Harmer teaches "program code that issues fetched instructions and . . . is operative to

identify a predetermined number of tasks relating to completing initialization of the computer, load these tasks, and iteratively execute these tasks." Starting with "selectively load," i.e., the first portion, as discussed above with respect to claim construction, we determine that the broadest reasonable interpretation of "selectively load" encompasses the only examples set forth in the specification, i.e., loading BIOS modules that are "identified in its list of tasks to execute." *Id.* at 3:10–12; *see also id.* at 5:40–43 ("The dispatch manager 17 executes the *list of tasks* contained therein to cause all required BIOS modules to be loaded into the system memory 13" (emphasis added).)

As Petitioner correctly notes (Pet. 24), like dispatch manager 17 of the '976 Patent Specification, Shipman teaches a decompression dispatcher including BIOS modules 32 through 54 (Ex. 1004, Fig. 1, 3:6). As Petitioner also correctly notes (Pet. 25), each of BIOS modules 32 through 54 "is capable of being dispatched as an independent executable object" (Ex. 1004, 3:6–8). Additionally, like "the list of tasks" (Ex. 1001, 5:40–43) of the '976 Patent Specification, as Petitioner correctly notes (Pet. 26), Shipman teaches "[w]hen dispatching components the decompression dispatcher works from a Packing List provided in the ROM image by the BIOS build process" (Ex. 1004, 5:27–29). Petitioner additionally relies on the testimony of Mr. Perla (Pet. 25) that a person of ordinary skill in the art would have known that Shipman teaches an algorithm for selectively loading. Ex. 1012 ¶ 82 (citing Ex. 1004, Fig. 5). We give Mr. Perla's testimony substantial weight because it is consistent with the teachings of the asserted art.

Furthermore, like the '976 Patent Specification's example of executing the list of tasks to load required BIOS modules into system

memory 13, as Petitioner correctly notes (Pet. 25), Shipman teaches a flow diagram of how components are dispatched (Ex. 1004, 12:49–50). Like the '976 Patent Specification description of loading BIOS modules into exemplary system memory 13, which is "random access memory (RAM) 13" (Ex. 1001, 4: 37–38), Shipman teaches that the dispatcher "decompresses the component at the index count and places the decompressed Code in RAM (514)" (*id.* at 12:63–65). Similarly, Shipman further describes component decompression with respect to Figure 12 (*see* Ex. 1004, Fig. 5, step 514) and with respect to Figure 12, Shipman teaches "[a] RAM memory block large enough to hold the specified component is found" (*id.* at 14:18–19; *see also id.* at 3:50 ("System random access memory, RAM, (22)").

Turning to the second portion, i.e., "relating to completing initialization of the computer, load these tasks, and iteratively execute these tasks," as Petitioner correctly notes (Pet. 25), Shipman teaches that BIOS components "fall into three major types" one of which is "initialization components." Ex. 1004, 3:10–12. Additionally, as Petitioner correctly notes (Pet. 22–26), initialization is performed first (*see, e.g.*, Ex. 1004, 1:66–2:3 ("Initialization components are dispatched during a Power On Self Test (POST) cycle such that the initialization components are active during initialization. The initialization components are terminated prior to loading an operating system."); *see also id.* at Fig. 2). Petitioner additionally relies on (Pet. 26 Mr. Perla's testimony that "Shipman shows that the predetermined number of tasks relates to complete initialization of the computer" (Ex. 1012 ¶ 85 (citing Ex. 1004, 4:46–49). We give Mr. Perla's

testimony substantial weight because it is consistent with the teachings of the asserted art.

Additionally, as Petitioner correctly contends (Pet. 25 (citing Ex. 1004, 2:39–40, 12:63–13:2, Fig. 5)), the flowchart of Figure 5 illustrates that the decompression dispatcher selectively loads and iteratively executes the tasks (*see, e.g.*, Ex. 1004, 12:63–13:2). Petitioner also relies on the testimony of Mr. Perla (Pet. 25) that Shipman teaches a dispatcher that "iteratively execute[s] a predetermined number of tasks because those tasks are predetermined according to packing information" Ex. 1012 ¶ 84 (citing Ex. 1004, 5:27–29) and that Shipman's process is iterative (*id.* ¶ 83). We give Mr. Perla's testimony substantial weight because it is consistent with the teachings of the asserted art.

Additionally, to the extent that Patent Owner contentions pertain to code that is operative to execute after the computer is initialized, because claim 1 also recites "comprising the steps of," other tasks not relating to initialization also may be loaded and executed. Dec. to Inst. 8. As we also discussed above with respect to claim construction, we determine that we need not modify our determination regarding the term "comprising."

Next, for completeness, we turn to the second, independent set of findings, i.e., findings based on an interpretation of "selectively load" that is limited to loading more than one, but less than all the BIOS modules. As discussed above, as Petitioner correctly notes (Pet. 25), each of BIOS modules 32 through 54 "is capable of being dispatched as an independent executable object" (Ex. 1004, 3:6–8). Patent Owner acknowledges that Shipman "contemplates modularity." PO Resp. 2; *see also* Tr. 29:3–4 ("I agree, Shipman does teach BIOS modularity.").

Against this background, Petitioner points to Shipman's Figure 5 for teaching "selectively load." Pet. 25, 26 (citing Ex. 1004, 12:63–13:2, Fig. 5); *see also* Ex. 1012 ¶¶ 82, 83 ("Figure 5 is a flowchart depicting an algorithm where each module is selected based on packing information that indexes each module.") As Petitioner further explains, "Shipman's flowchart in FIG. 5 selects and loads modules one-by-one based on a list of modules identified in a packing list." Pet. Reply 3.

Consistent with Petitioner's contentions, Figure 5, which is a flow diagram of how components are dispatched, indicates in step 502 that the dispatch process begins by assuming that only one component of a class is to be loaded setting a default count to "1." *Id.* at 12:49–52. Step 504 tests whether all components in the class are to be loaded. *Id.* at 12:55–56. As can be seen in Figure 5, reproduced below with annotations, processing performed in step 504 results in two possibilities, i.e., "NO" and "YES." Ex. 1004, Fig. 5 (step 504). Accordingly, the number of components in a class that are loaded may be less than all components in that class.

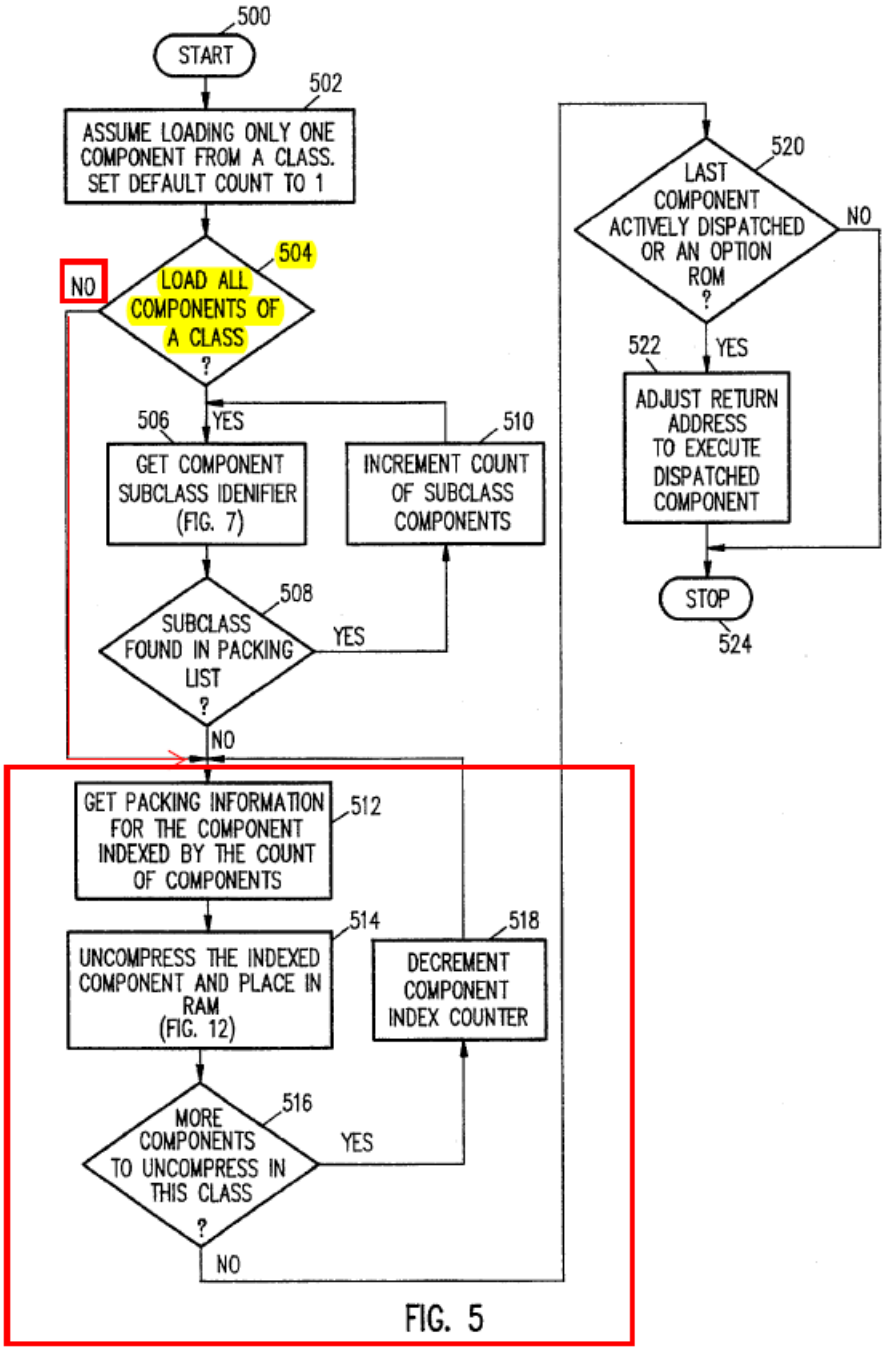


FIG. 5

Figure 5 illustrates a flow diagram of how components are dispatched.

If the result is "NO" to the question of whether to load all components of a class, the process moves to step 512 to get packing information for the component indexed by the count of components. *Id.* at Fig. 5. Because step

512 indicates multiple components, i.e., "BY THE COUNT OF COMPONENTS," the teaching of step 512 is consistent with Petitioner's contentions that Figure 5 depicts processing less than all components, but more than one component of a class. Additionally, in step 516 a check is performed to determine whether "MORE COMPONENTS TO UNCOMPRESS IN THIS CLASS." *Id.* Step 516 provides further support for Petitioner's contention.

Accordingly, as an independent reason that we are persuaded by Petitioner's contentions, even if "selectively load" were limited to meaning loading more than one, but less than all, the BIOS modules, we are still persuaded that Shipman teaches this limitation. The possibility that all components of a class could be loaded does not change the fact that the Shipman teaches another option.

Based on the complete record now before us, for the reasons given, we are persuaded that Petitioner has shown sufficiently that the asserted art teaches the "selectively load" recited in claims 1 and 14, under both the broadest reasonable interpretation, and even under a more limited interpretation, as set forth above.

Fifth, we consider Patent Owner's contention that the asserted references do not teach "**Small Amount of BIOS Initialization Code,**" recited in claims 1 and 14. PO Resp. 13–15. As discussed above with respect to the first "storing" step, Petitioner's contentions, for example, pertaining to Figure 2 of Shipman (Pet. 21–23), explain that the code is operative to initialize the CPU and system memory, i.e., "TEST AND INITIALIZE MEMORY CONTROLLER RELATED COMPONENTS" (Ex. 1004, Fig. 2). This is the same as the claim recitation, i.e., "a

predetermined small amount of BIOS initialization code . . . that is operative to initialize the CPU and the system memory."

With respect to the step of "executing" that same predetermined small amount of BIOS initialization code, Patent Owner contends the execution of the code identified by Petitioner "would include more than initializing the CPU and the system memory—it would also include initializing the dispatch manger." PO Resp. 14. Patent Owner more specifically contends that "[e]ven step 202, labeled 'test and initialize memory controller related components' is beyond the Board's definition of 'small amount of BIOS code.'" *Id.* (citing Ex. 1004, 6:51–59). Patent Owner further contends "[t]his, in turn, would improperly conflate 'executing the predetermined small amount of BIOS initialization code' and 'executing the dispatch manager' limitation of the subject claims." *Id.*

As supporting evidence, Patent Owner points to only Figure 2 of Shipman and the text reproduced below. PO Resp. 13–15.

> The POST Loader component handles all hardware generated resets (i.e., power on, front panel, etc.) and software generated resets after being processed by the Shutdown Handler. This component resides uncompressed in the ROM image and may not be dispatched into DRAM. The primary responsibility of this module is to configure enough of the system to gain 2 Mb of DRAM, activate the decompression dispatcher, and cause *the main Power On Self Test* to be decompressed and dispatched.

Ex. 1004, 6:51–59 (emphasis added).

"[T]he main" POST (*id.*) referenced above is not the same step 202 of Figure 2 (*id.* at Fig. 2). More specifically, as Petitioner correctly contends (Pet. 19–23, Pet. Reply 4), step 202 is performed *before* steps 204 and 206,

and *only* steps 204 and 206 pertain to "POST" (Ex. 1001, Fig. 2). Figure 2 of Shipman, with annotations, is reproduced below.

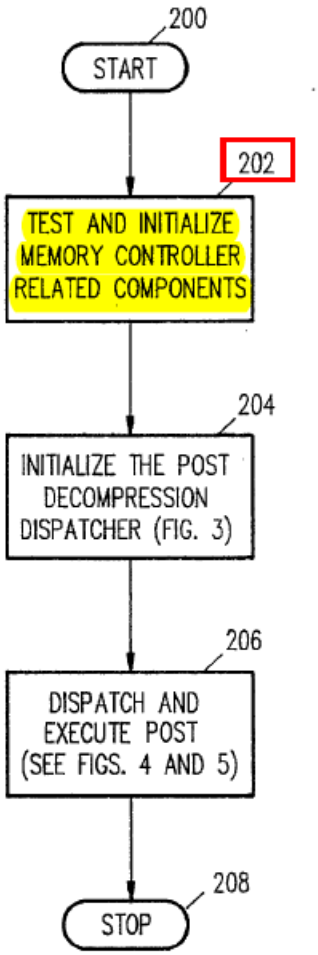


FIG. 2

The teachings of Figure 2 are contrary to Patent Owner's contention that the execution of the code identified by Petitioner "would include more than initializing the CPU and the system memory—it would also include initializing the dispatch manger." PO Resp. 14. Contrary to Patent Owner's contention, step 202 of Figure 2 teaches "TEST AND INITIALIZE MEMORY CONTROLLER RELATED COMPONENTS" (Ex. 1004, Fig.

2), which is the same as the disputed recitation, i.e., "executing a predetermined small amount of BIOS initialization code *to initialize the CPU and the system memory*" (emphasis added). Step 202 is performed before steps 204 and 206, which teach initializing the POST dispatcher and dispatching and executing POST, respectively. Ex. 1004, Fig. 2. Additionally, Patent Owner's contention that reliance on Shipman, "improperly conflate[s] 'executing the predetermined small amount of BIOS initialization code' and 'executing the dispatch manager' limitation of the subject claims" (PO Resp. 14) is not consistent with the teachings of Shipman showing step 202 as a separate, initial step, performed prior to initializing the dispatcher (Ex. 1004, Fig. 2).

Based on the complete record now before us, for the reasons given, we are persuaded that Petitioner has shown sufficiently that the asserted art teaches the two executing steps recited in claims 1 and 14 disputed by Patent Owner.

Finally, we consider Patent Owner's contention that the asserted references do not teach "**Secondary Nonvolatile Storage Device**" and "**Protected Area**," recited in claim 14. PO Resp. 12–13. Starting with "secondary nonvolatile storage device" recited in claim 14, Patent Owner again argues that Mr. Perla's "opinion regarding secondary storage is so baseless as to be frivolous." *Id.* at 13. Patent Owner, first, contends that Mr. Perla testifies that Shipman's executable service components teach a secondary nonvolatile storage device. *Id.* at 12. Patent Owner, next, contends that Mr. Perla testifies "a secondary storage device 'could be anything.'" *Id.*

We do not agree with Patent Owner's characterization of Mr. Perla's testimony. With respect to Patent Owner's first contention, Mr. Perla testifies in response to Patent Owner's counsel's question as follows: "Can you tell me where in Shipman there is a teaching of the ability to access a storage device?" Ex. 2007, 47:7–9. Patent Owner's contention does not focus on the question asked, which is directed to the ability to access storage. The question does not pertains to "copying" as in "sequentially *copying* selected BIOS modules from the protected area of the secondary nonvolatile storage device to the system memory," recited in claim 14.

Regarding accessibility, Mr. Perla's testimony regarding the "independently executable service components being pre-stored in the nonvolatile memory" (Ex. 2007, 47:10–15), referred to by Patent Owner above, pertains to Shipman's BIOS modularity (Ex. 1004, 16:65–67). Mr. Perla refers to the decompression dispatcher "pre-stored in the non-volatile storage" (*id.*), which decompresses the component stored in ROM 10 (Ex. 1004, Fig. 1) "and places the decompressed Code in RAM (514)" (*id.* at 12:64, 65).

Patent Owner's second contention that Mr. Perla testifies "a secondary storage device 'could be anything'" (PO Resp. 12) is also not a correct characterization of Mr. Perla's testimony identified by Patent Owner. The testimony Patent Owner identifies (PO Resp. 12) is reproduced below, along with subsequent testimony.

> Q. What's the secondary storage device there?
>
> A. It could be anything. It could be a disc. It could be flash memory. It could be a secondary EEPROM stored on the platform.
>
> Q. Let's take each of those in turn. Is it possible to store compressed and uncompressed data on the same disc?

> A. Yes.
> Q. All right. Is it possible to store compressed and uncompressed data on a hard drive?
> A. Yes. You could compress a component of the hard drive.

Ex. 2007, 47:16–48:1.

Taken in context, Mr. Perla's testimony is understood reasonably to refer to "a disc," "flash memory," and "a secondary EEPROM" (*id.*) as examples of secondary storage taught by Shipman and Harmer. Patent Owner's follow-up questions indicate that during the deposition, Patent Owner understood Mr. Perla's testimony as identifying examples of secondary memory. Patent Owner had the opportunity, but chose not to seek, clarification regarding "anything" or has not pointed us to clarifying testimony that supports Patent Owner's contention.

Mr. Perla's deposition testimony is consistent with his declaration testimony. As noted above, Petitioner points to Shipman's teaching of "disk drives" (Pet. 29, 47 (citing Ex. 1004, 1:16)) and Harmer's teaching of a "mass memory storage peripheral computer device" (*id.* at 29 (citing Ex. 1003, 6:59–64)) for the secondary nonvolatile storage device. Petitioner also relies on Mr. Perla's testimony. Pet. 29 (citing Ex. 1012 ¶¶ 127, 149). For example, Mr. Perla testifies "Shipman describes 'disk drives'" and a person of ordinary skill in the art would have understood "that a disk drive is mass media storage that is nonvolatile and separate from the BIOS ROM." Ex. 1012 ¶¶ 127. As an additional example, Mr. Perla testifies "Harmer demonstrates that it was known to store some BIOS modules in a secondary memory (e.g., mass memory) that is separate from the nonvolatile memory

that stores the small amount of initialization code." *Id.* ¶ 149 (citing Ex. 1003, 6:59–64).

We now turn to Patent Owner's contention regarding "**Protected Area**," recited in claim 14. PO Resp. 13. Although Patent Owner begins by pointing to Mr. Perla's testimony regarding the meaning of "protected area," Patent Owner does not dispute the Petitioner's contentions regarding how the asserted art teaches "protected area." PO Resp. 13 (citing Ex. 2007, 51:15–18). Instead, Patent Owner contends, "[a]s noted above, Shipman is incompatible with a secondary storage device." *Id.* (citing Ex. 2007, 54:3–8).

One cannot show non-obviousness by attacking references individually where the rejections are based on combinations of references. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986); *In re Keller*, 642 F.2d 413, 426 (CCPA 1981). Patent Owner's contention that "Shipman is incompatible" with a hard drive is a repeat of its contentions regarding motivation to combine, which we discuss above.

Even after consideration of Patent Owner's contentions and evidence, we are persuaded by Petitioner's contentions and evidence. For example, we are persuaded by Mr. Perla's testimony that "Harmer teaches that the selected BIOS modules may be stored in a protected area" of secondary storage. Ex. 1012 ¶ 169 (citing Ex. 1003, 15:25, 26). Harmer teaches "[a] variety of methods may be used to protect this portion of the hard drive" and "a utility program may be proved to allow this protected portion of the hard drive to be accessed when and if an update or correct of the portion of the expansion BIOS stored on the hard drive is desired." Ex. 1003, 15:21–27. When asked by Patent Owner's counsel at deposition, Mr. Perla also

identified teachings in Shipman regarding protected area. Ex. 2007, 51:19–52:7 (citing col. 10, 29–32)). We also are persuaded by Mr. Perla's testimony that Harmer "encourages" a person of ordinary skill "to use a protected memory area in order to prevent a user from accessing the BIOS modules during normal use." Ex. 1012 ¶ 170.

Based on the complete record now before us, for the reasons given, we are persuaded that Petitioner has shown sufficiently that the asserted art teaches "secondary nonvolatile storage device" and "protected area," recited in claim 14.

c. Conclusion for Claims 1 and 14

Petitioner's contentions and claim charts persuasively read all elements of each of claims 1 and 14 onto the combined teachings of Shipman and Harmer. Additionally, for the reasons given above, including that we find that his testimony is consistent with the evidence cited therein, we give Mr. Perla's testimony substantial weight (37 C.F.R. § 42.65). We determine that the record supports Petitioner's contentions and adopt Petitioner's contentions discussed above as our own. Despite the counter-arguments in the Patent Owner Response, and the evidence cited therein, which we also have considered, for the foregoing reasons, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 14 are unpatentable as obvious over Shipman and Harmer.

4. Dependent Claims 2–5, 8–13, and 15–17

Claim 2 depends, directly, from claim 1 and recites additional steps similar to those recited in claim 14. For the reasons discussed above with respect to claim 14, we are persuaded that, on this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing the

unpatentability of claim 2. Patent Owner's contention regarding "protected area" (PO Resp. 13) is discussed above with respect to claim 14. Patent Owner does not provide further separate contentions regarding claim 2.

Claim 3 depends, directly, from claim 1, claim 4 depends, directly, from claim 2, and claim 15 depends, directly, from claim 14. Each of claims 3, 4, and 15 recites determining which BIOS modules are required for operation of the computer, determining if a required BIOS module is stored in system memory, copying the required BIOS module from secondary nonvolatile storage device to system memory, if it is not in system memory, and executing the BIOS module.

Regarding determining which BIOS modules are required for operation of the computer, Petitioner points to Shipman's teaching of a packing list used by the decompression dispatcher to dispatch components and a flow chart of execution of the dispatch component. Pet. 32–33, 43–44 (citing Ex. 1004, 1:38–41, 2:14–23, 4:33–36, 5:14–16, 5:40–45, 12:55–56, 13:3–14, Figs. 5, 6; Ex. 1012 ¶ 110). Each of claims 3, 4, and 15 recites, "determining which BIOS modules are required for operation of the computer." Ex. 1001, 10:19–20, 10:33–34, 12:6–7. We are persuaded by Petitioner's argument and evidence that Shipman's BIOS components are required for operation of the computer. For example, Shipman's set of BIOS components (32 through 54) include components that power on and manage the power of the computer (32 and 34), provide video (36), perform runtime BIOS (38), provide interconnection, interfaces, and configuration (40, 42, 44), and manage software (46). Ex. 1004, Fig. 1.

Claims 5, 8, 9, 10, 11, and 12 depend, directly, from claim 2 and recite that the secondary nonvolatile storage device comprises a specific

memory, such as a hard disk drive, compact disk ROM, flash memory, floppy disk drive, Zip drive, and SuperDisk drive, respectively. Claim 16 depends, directly, from claim 14 and recites that the secondary nonvolatile storage device is selected from a group comprising the specific memories listed above. We have reviewed Petitioner's contentions and evidence (Pet. 45–47), and are persuaded that Petitioner has shown sufficiently that these additional features are taught or suggested by Shipman and Harmer.

Claim 13 depends, directly, from claim 1 and claim 17 depends, directly, from claim 14. Each of claims 13 and 17 recites "launching an operating system of the computer after all required BIOS modules are copied to the system memory and executed." Ex. 1001, 10:64–66, 12:24–27. Upon review, on this record, we are persuaded by Petitioner's contentions and evidence (Pet. 39, 47 (citing Ex. 1003, 1:66–2:3, Ex. 1012 ¶ 147)) with respect to claims 13 and 17.

With respect to claims 3–5, 8–13, and 15–17, Patent Owner does not argue separately these claims and, instead, relies on its contentions for the independent claims. Petitioner's contentions and claim charts persuasively read all elements of each of claims 2–5, 8–13, and 15–17 onto the combined teachings of Shipman and Harmer. Additionally, for the reasons given above, including that we find that his testimony is consistent with the evidence cited therein, we give Mr. Perla's testimony substantial weight (37 C.F.R. § 42.65). We determine that the record supports Petitioner's contentions and adopt Petitioner's contentions discussed above as our own. Despite the counter-arguments in the Patent Owner Response, and the evidence cited therein, which we also have considered, for the foregoing

reasons, we determine that Petitioner has demonstrated by a preponderance of the evidence that each of claims 2–5, 8–13, and 15–17 is unpatentable.

C. Obviousness of Claim 6

Petitioner contends that claim 6 of the '976 Patent is rendered obvious by the combined teachings of Shipman, Harmer, and Patel. Pet. 50–51. Claim 6 depends from claim 5, discussed above, and further recites, "wherein the hard disk drive comprises a vendor protected area, a user area, and said protected area."

1. Patel

Patel teaches enhancing robustness of Plug-and-Play BIOS. Ex. 1006, Abstract. According to Patel, the isolation routines of the Plug-and-Play methodology rely on the use of a 72-bit serial identifier that manufacturers ensure will be different for any two devices in the system. *Id.* at 9:8–11.

2. Claim 6

Regarding "wherein the hard disk drive comprises a vendor protected area, a user area, and said protected area" as recited in claim 6 (Ex. 1001, 10:45–47), Petitioner, for example, points to Patel's teaching of storing a 32-bit value unique to each unit as corresponding to the vendor protected area. Pet. 51 (citing Ex. 1006, 9:11–15). Regarding "user area" and "protected area," Petitioner relies on Shipman and Harmer, as well as its contentions for independent claim 14. *Id.* at 50, 51. Petitioner, in reliance on the testimony of Mr. Perla, contends a person of ordinary skill in the art would have understood that the vendor protects this value from being over-written. *Id.* (citing Ex. 1012 ¶ 179). Petitioner additionally contends that a person of ordinary skill in the art would have found it obvious to combine Shipman,

Harmer, and Patel so that a vendor can specify a unique identity for each manufactured unit. *Id.* (citing Ex. 1012 ¶¶ 180, 181).

Patent Owner contends "Dr. Perla admitted that, on the one hand, Patel teaches a hard disk drive (Ex. 200[7], 59:7–60:6), but, on the other hand, it did not occur to Patel to locate the 32-bit value in that disk drive (*id.* at 60:20–61:11)." PO Resp. 15. Patent Owner contends "claim 6, which requires that the vendor protected area be part of the hard drive, is non-obvious." *Id.*

Again, we do not agree with Patent Owner's characterization of Mr. Perla's testimony. Mr. Perla's testimony is reproduced below.

> Q. Where do they say that any of those are stored on a hard drive? And again, actually I'm asking for the unique 32-bit area that stores a vendor-specified mass storage device identifier that you reference in paragraph 179.
>
> A. Lines 11 through 15. "Each vendor is assigned a unique 32-bit value with which the serial bit identifier of each device the vendor provides must begin."
>
> Q. That's Column 9?
>
> A. Yes, it is.
>
> Q. Does that say anything about hard drive 114?
>
> A. Those particular lines do not say anything that would reference back to the 114 in Partel -- in Patel.

Ex. 2007, 60:25–61:11. Contrary to Patent Owner's contention, Mr. Perla's testimony relates to "particular lines" of Patel, not Patel in its entirety (*id.*).

Patent Owner's contention also is based on an improper attempt to show non-obviousness by attacking references individually where the rejections are based on combinations of references. *In re Merck & Co., Inc.*, 800 F.2d at 1097; *In re Keller*, 642 F.2d at 426. Like his deposition testimony above, in his declaration Mr. Perla points to Patel's teaching of use of "a vendor protected area," (Ex. 1012 ¶ 179 (Ex. 1006, 9:11–15)),

which is relied upon by Petitioner (Pet. 50, 51). Consistent with Mr. Perla's testimony, Patel teaches "ensur[ing] that each device in the system has a different non-zero 72-bit (9byte) serial identifier." Ex. 1006, 9:15–17. Mr. Perla also testifies "[i]t would have been obvious to include vendor protected areas in any commercially available hard disk in order to allow a vendor to specify a unique identity for each manufactured device." Ex. 1012 ¶ 180.

Petitioner's contentions and claim charts persuasively read all elements of claim 6, including the further recitation noted above, onto the combined teachings of Shipman, Harmer, and Patel. We also find that Petitioner has articulated sufficient reasoning with a rational underpinning as to why one of ordinary skill in the art would have combined Shipman, Harmer, and Patel. Additionally, for the reasons given above, including that we find that his testimony is consistent with the evidence cited therein, we give Mr. Perla's testimony substantial weight (37 C.F.R. § 42.65). We determine that the record supports Petitioner's contentions and adopt Petitioner's contentions discussed above as our own. Despite the counter-arguments in the Patent Owner Response, and the evidence cited therein, which we also have considered, for the foregoing reasons, we determine that Petitioner has demonstrated by a preponderance of the evidence that claim 6 is unpatentable.

D. Obviousness of Claim 7

Petitioner contends that claim 7 of the '976 Patent is rendered obvious by the combined teachings of Shipman, Harmer, and PARTIES. Pet. 37–39. Claim 7 depends from claim 2 and further recites, "wherein the protected BIOS module area comprises a formatted area created using Protected Area Run-Time Interface Extensions Services (PARTIES) technology."

1. PARTIES

PARTIES teaches a standard for specifying a BIOS interface for accessing an area of ATA drives that normally is hidden. Ex. 1011, 4.

2. Claim 7

Regarding the further recitation in claim 7, in particular, "wherein the protected BIOS module area comprises a formatted area," Petitioner points to Harmer's teaching of a protected BIOS module area, i.e., "the portion of the expansion BIOS may be stored in a portion of the mass memory storage which is not user accessible." Pet. 46 (citing Ex. 1003, 15:17–24). Regarding the recitation in claim 7 that the formatting be "created using Protected Area Run-Time Interface Extensions Services (PARTIES) technology," Petitioner, in reliance on the testimony of Mr. Perla, contends PARTIES technology would have been "within the general knowledge" of a person of ordinary skill in the art. Pet. 39 (citing Ex. 1012 ¶ 132). Petitioner also points to PARTIES' teaching of formatting a storage area for protection. Pet. 37–39 (citing Ex. 1011, 4, 10, 14, 15, 19). Additionally, Petitioner, in reliance on the testimony of Mr. Perla, contends that a person of ordinary skill in the art would have found it obvious to combine Shipman, Harmer, and PARTIES explaining that PARTIES technology for "protecting memory" would have been "a known technique applied to protect Harmer's memory that needs protection." Pet. 38–39, 46 (citing Ex. 1012 ¶¶ 132–134).

Patent Owner contends that Petitioner has not shown that PARTIES was made sufficiently accessible to the public interested in the art. PO Resp. 5. Patent Owner, however, acknowledges that the inventor of the '976 Patent did not invent technology referred to as PARTIES.

> JUDGE PARVIS: The ’976 patent refers to PARTIES; is that correct, in column 6?
>
> MR. SUMMERFIELD: Yes. And as a matter of fact, the related application was for the same inventor.
>
> JUDGE PARVIS: And for example, starting around 6 line 18 of column 6, it refers to NCITS D11367 for PARTIES. And it talks about the PARTIES specification. That reference number is the same as the specification the petitioner pointed to; is that correct?
>
> MR. SUMMERFIELD: Yes. And my guess is the document number didn’t change from when it was originally created as version zero until whatever iteration was published.
>
> JUDGE PARVIS: So in the '976 patent, would you agree that this PARTIES technology was not invented by Mr. Stevens; is that correct, the inventor of the '976 patent?
>
> MR. SUMMERFIELD: Whatever was disclosed in PARTIES?
>
> JUDGE PARVIS: When he’s referring to the PARTIES specification, he’s talking about something, a specification, a third-party specification?
>
> MR. SUMMERFIELD: Yes.
>
> * * *
>
> JUDGE PARVIS: In the specification there’s a sentence that says the PARTIES, Protected Area Run-Time Interface technology, allows the system to reserve space on a hard drive for system use. This is in column 6 starting at about line 40. Would the patent owner agree that that technology was known to one of ordinary skill in the art?
>
> MR. SUMMERFIELD: Yes. Yes, but we think they are relying on PARTIES for more than that. But yes, we would certainly agree that anything that's described in the background section describing the prior art would have been known to a hypothetical person of skill.

Tr. 39:1–40:17.

In the Decision to Institute, we noted our finding that the ’976 Patent refers to “NCITS D11367 (PARTIES)” (Ex. 1001, 6:20), “ANSI PARTIES” (*id.* at 7:1), and indicates that PARTIES is “Protected Area Run-Time

Interface Extensions Services" (*id.* at 6:41–42). As Petitioner notes (Pet. 37), PARTIES indicates that it is a document prepared by a Technical Committee of ANSI. Ex. 1011, 1. Exhibit 1011 bears a working document number, i.e., "T13 D1367," "Revision 0," and the date "August 23, 1999." *Id.* Additionally, PARTIES indicates that it was made available for review and comment, that permission is granted to reproduce the document for the purposes of standardization, and that it was printed on August 27, 1999. *Id.* 1, 4.

We determine that Petitioner has shown that PARTIES technology would have been within the general knowledge of a person of ordinary skill in the art for two independent reasons. The first of these reasons is based on waiver. First, we noted in our Decision to Institute acknowledgments by the inventor in the '976 Patent Specification of the existence of PARTIES technology, identified again above. Dec. to Inst. 25 n. 5. Patent Owner does not dispute those findings. *See generally* PO Resp. Patent Owner's indication that the Petitioner is relying on PARTIES for "more than that" (Tr. 40:13, 14) is not commensurate with the scope of the claim. In particular, the further recitation of claim 7 is simply "a formatted area created using Protected Area Run-Time Interface Extensions Services (PARTIES) technology."

Furthermore, not only did Patent Owner fail to dispute, but instead acknowledges, that the inventor of the '976 Patent did not invent the PARTIES technology referenced therein. Tr. 39:1–21. Additionally, Patent Owner acknowledges that the PARTIES technology described in the '976 Patent for allowing the system to reserve space on a hard drive for system use would have been known to a person of ordinary skill in the art. *Id.* at

40:7–17. Accordingly, we determine that Patent Owner at least has waived any dispute that the further recitation in claim 7 regarding PARTIES was within the general knowledge of one of ordinary skill in the art. *See* 37 C.F.R. §§ 42.23, 42.120 ("Oppositions and replies must comply with the content requirements of motions" and "[a] patent owner response is filed as an opposition.").

For completeness, as a second independent reason, we find that the PARTIES document itself, i.e., Exhibit 1011 is circumstantial evidence that the '976 Patent Specification PARTIES references are to background art. In particular, the '976 Patent refers to "NCITS D11367 (PARTIES)" (Ex. 1001, 6:20), which includes the same number ("D1367") found on the PARTIES document (Ex. 1011, 1). Additionally, the '976 Patent Specification refers to "ANSI PARTIES" (Ex. 1001, 7:1) and the PARTIES document indicates it was prepared by "ANSI®" (Ex. 1011, 4). Furthermore, the '976 Patent Specification indicates that PARTIES is "Protected Area Run-Time Interface Extensions Services" (*id.* at 6:41–42) and the PARTIES document has the same name (Ex. 1011, 4). For this independent reason, we determine that Petitioner has shown that the further recitation of claim 7 was taught by the combined teachings of Shipman, Harmer, and the PARTIES technology that would have been within the general knowledge of a person of ordinary skill in the art.

Petitioner's contentions and claim charts persuasively read all elements of claim 7, including the further recitation noted above, onto the combined teachings of Shipman, Harmer, and the PARTIES technology that would have been within the general knowledge of a person of ordinary skill in the art. We also find that Petitioner has articulated sufficient reasoning

with a rational underpinning as to why one of ordinary skill in the art would have combined Shipman, Harmer, and the PARTIES technology that would have been within the general knowledge of a person of ordinary skill in the art (Pet. 38, 39, 46 (citing Ex. 1012 ¶¶ 132–34). Additionally, for the reasons given above, including that we find that his testimony is consistent with the evidence cited therein, we give Mr. Perla's testimony substantial weight (37 C.F.R. § 42.65). We determine that the record supports Petitioner's contentions and adopt Petitioner's contentions discussed above as our own. Despite the counter-arguments in the Patent Owner Response, and the evidence cited therein, which we also have considered, for the foregoing reasons, we determine that Petitioner has demonstrated by a preponderance of the evidence that claim 7 is unpatentable.

IV. PETITIONER'S MOTION TO EXCLUDE

Petitioner filed a Motion to Exclude Exhibit 2010, which is the deposition transcript of Mr. Perla, who testifies in support of Petitioner's contentions. Paper 31. Patent Owner opposes the Motion to Exclude. Paper 34.

We need not reach the merits of Petitioner's Motion to Exclude Evidence because, even without excluding portions of Mr. Perla's testimony, we have decided in Petitioner's favor. Accordingly, Petitioner's Motion to Exclude is dismissed as moot.

V. CONCLUSION

For the foregoing reasons, we conclude that Petitioner has demonstrated by a preponderance of the evidence that claims 1–5 and 8–17 are unpatentable, under 35 U.S.C. § 103(a), as obvious over the combined teachings of Shipman and Harmer; claim 6 is unpatentable, under 35

U.S.C. § 103(a), as obvious over the combined teachings of Shipman, Harmer, and Patel; and claim 7 is unpatentable, under 35 U.S.C. § 103(a), as obvious over the combined teachings of Shipman, Harmer, and the PARTIES technology that would have been within the general knowledge of one of ordinary skill in the art. We also dismiss Petitioner's Motion to Exclude.

VI. ORDER

For the reasons given, it is:

ORDERED that claims 1–17 of the '976 Patent are unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Vivek Ganti
vg@hkw-law.com

Gregory Ourada
go@hkw-law.com

PATENT OWNER:

Christopher Frerking
chris@ntknet.com