

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD,
SAMSUNG ELECTRONICS AMERICA, INC., and
SAMSUNG SEMICONDUCTOR, INC.,
Petitioner,

v.

IMPERIUM (IP) HOLDINGS,
Patent Owner.

Case IPR2015-01231
Patent 6,271,884 B1

Before JAMES B. ARPIN, BART A. GERSTENBLITH, and
CHARLES J. BOUDREAU *Administrative Patent Judges*.

GERSTENBLITH, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. *Background*

Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively, “Petitioner”) filed a Petition (Paper 4, “Pet.”) requesting institution of *inter partes* review of claims 1–6, 14, and 17–19 of U.S. Patent No. 6,271,884 B1 (Ex. 1001, “the ’884 patent”). Imperium (IP) Holdings (“Patent Owner”) filed a Preliminary Response (Paper 14, “Prelim. Resp.”). We have jurisdiction under 35 U.S.C. § 314.

Under 35 U.S.C. § 314(a), an *inter partes* review may be instituted only if “the information presented in the [P]etition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the [P]etition.” See 37 C.F.R. § 42.108(c).

For the reasons given below, on this record, we are persuaded that Petitioner has not established a reasonable likelihood of prevailing with respect to at least one challenged claim of the ’884 patent. Accordingly, we *deny* the Petition and decline to institute an *inter partes* review of the ’884 patent.

B. *Related Proceedings*

The parties represent that the ’884 patent is asserted in *Imperium IP Holdings (Cayman) Ltd. v. Samsung Electronics Co., et al.*, No. 4:14-cv-00371 (ALM) (E.D. Tex.). Pet. 6; Paper 13, 1. Patent Owner also identifies several other litigations in which the ’884 patent is asserted. Paper 13, 1.

C. *Real Parties-in-Interest*

The Petition identifies Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. as real parties-

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in-interest. Pet. 5. Patent Owner identifies itself as the sole real party-in-interest. Paper 13, 1.

D. The References

Petitioner relies on the following references:

U.S. Patent No. 6,567,123 B1, issued May 20, 2003 (Ex. 1004, “Hashimoto”);

U.S. Patent No. 5,966,173, issued October 12, 1999 (Ex. 1005, “Inuiya”);

Japanese Patent Application Disclosure No. H1-204578, published August 17, 1989 (Ex. 1007, “Kinugawa”); and

U.S. Patent No. 5,293,225, issued March 8, 1994 (Ex. 1035, “Nishiyama”).

E. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–6, 14, and 17–19 of the '884 patent on the following grounds:

Reference(s)	Basis	Claims challenged
Hashimoto	§ 102(e)	1–5 and 14
Hashimoto and Kinugawa	§ 103(a)	1–6 and 14
Hashimoto and the knowledge of a person of ordinary skill in the art	§ 103(a)	14 and 17–19
Hashimoto, Nishiyama, and the knowledge of a person of ordinary skill in the art	§ 103(a)	17–19
Hashimoto, Nishiyama, Kinugawa, and the knowledge of a person of ordinary skill in the art	§ 103(a)	17–19
Hashimoto and the knowledge of a person of ordinary skill in the art	§ 103(a)	17–19
Inuiya	§ 102(e)	1–5 and 14
Inuiya and Kinugawa	§ 103(a)	1–6 and 14

Petitioner supports its challenge with a declaration executed by Dr. Dean P. Neikirk (Ex. 1003, “the Neikirk Declaration”).

F. The '884 Patent

The '884 patent is directed to “digital imaging systems, and more particularly to a digital imaging system with reduced flicker caused by fluorescent lighting.” Ex. 1001, 1:6–8. The '884 patent explains:

Digital imagers typically have a parameter known as integration time, which is simply the amount of time the electronic component of the pixel is allowed to capture light energy for each frame. By adjusting the integration time, the intensity of the image can be adjusted, enhancing images and preventing

saturation at high intensities. . . . By setting the integration time to be some integral multiple of an intensity period of a lighting source . . . flicker is reduced because the amount of light captured during an integration period is independent of where the integration period starts and ends relative to the variations in lighting intensity.

Id. at 1:47–59.

Figures 3A and 3B¹ of the '884 patent are reproduced below.

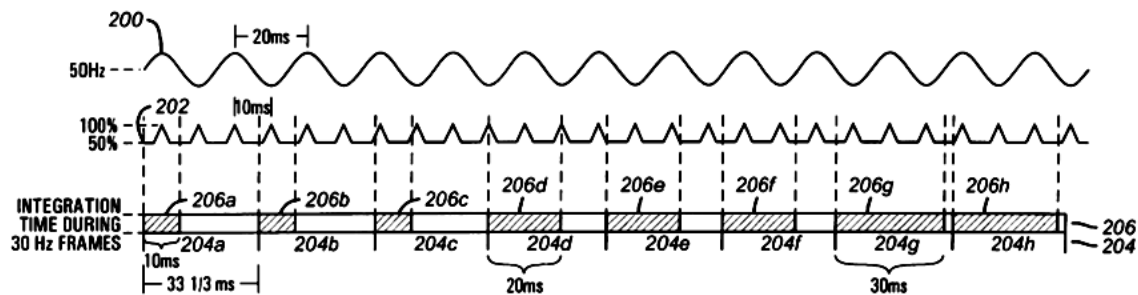


FIG. 3A

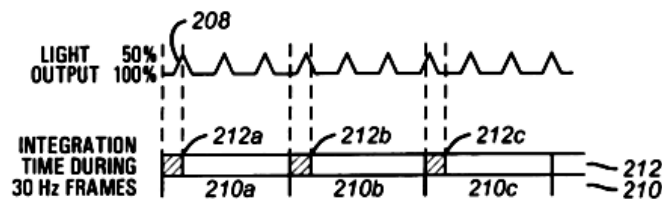


FIG. 3B

Figures 3A and 3B “are timing diagrams illustrating how the implementation of integration time according to the invention ‘decouples’ the light captured during integration from where within a particular lighting cycle the integration time begins.” *Id.* at 2:22–26.

Figure 3A shows “a 50 Hz signal 200 used to drive a typical European fluorescent light, as well as an associated light output signal 202 of such a

¹ The '884 patent refers to Figures 3A and 3B alternatively as 3a and 3b. Compare Ex. 1001, 2:22 with *id.* at 3:66, 4:46.

fluorescent light.” *Id.* at 4:3–5. “The light output peaks during peak voltage, so the period of the peak intensity of light output is 10 milliseconds, or one-half of the 20 millisecond period of the 50 Hz signal 200. The intensity thus peaks at a rate of 100 Hz,” or twice the frequency of the driving current. *Id.* at 4:5–9. Additionally, the ’884 patent explains:

In conjunction with the 50 Hz signal 200 and the light output signal 202, shown are a sequence of frames 204 illustrating corresponding integration periods 206. Specifically, in a first three $33\frac{1}{3}$ millisecond frames 204a, 204b and 204c, shown are 10 millisecond integration times 206a, 206b, and 206c. Assuming, for example, the integration time is the period of time in FIG. 2 from when the row 102b is reset until row 102b is read, at the end of the integration time, the row 102b will be read and reset for the following frame. Comparing the integration time 206a to the integration time 206c, it is seen that the peak intensity of the light output signal 202 occurs in the middle of the integration time 206a, but that during the integration time 206c portions of two separate peaks are captured. According to the invention, however, by setting the integration time to some multiple of the ten millisecond period of the light output 202, the amount of light captured during the integration time 206a is the same as the amount of light captured during the integration time 206c (assuming the image has not appreciably changed) because the system integrates a multiple of the period of the light output.

Id. at 4:10–30. Further, Figure 3A shows three subsequent frames—204d, 204e, and 204f—using 20 millisecond integration times, 206d, 206e, and 206f, as well as two additional frames 204g and 204h, showing 30 millisecond integration periods 206g and 206h. *See id.* at 4:31–44.

The ’884 patent contrasts the integration periods illustrated in Figure 3A with the integration periods shown in Figure 3B. *Id.* at 4:45–46. In Figure 3B, integration periods 212 are not an integral multiple of the

period of the peak intensity of light output 208; instead, integration periods 212 are approximately 5 millisecond periods 212a, 212b, and 212c. *Id.* at 4:46–52. In Figure 3B, “the amount of light captured is dependent on where the integration time begins and ends. Certain integration times can lead to a slow moving band of light on a resulting image.” *Id.* at 4:55–58. Accordingly, the ’884 patent proposes reducing “this flicker . . . by providing an integration time, such as the integration time[s] 206, that are a multiple of the period of the peak of light output 202.” *Id.* at 4:59–62.

Figure 4 of the ’884 patent is reproduced below.

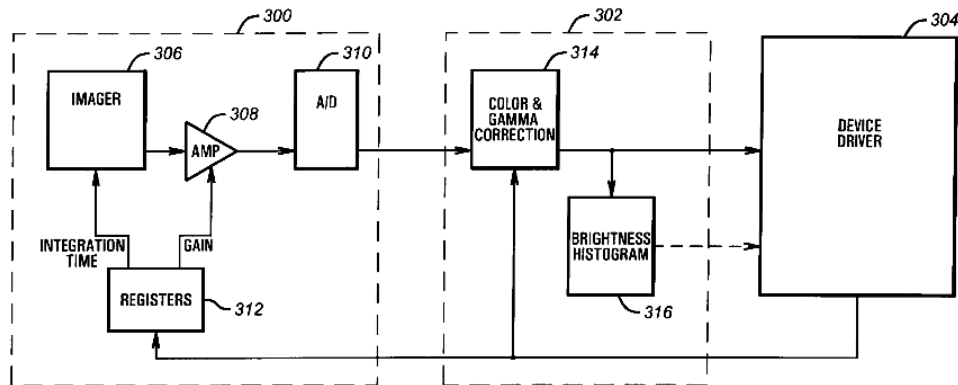


FIG. 4

Figure 4 of the ’884 patent “is a block diagram of an imaging system implemented according to the invention to reduce lighting induced flicker.” *Id.* at 2:27–29.

The ’884 patent teaches that brightness control can be achieved, in part, by adjusting the integration time via registers 312. *Id.* at 5:52–54. In particular, the registers may set the integration time to approximately 10 milliseconds, 20 milliseconds, and 30 milliseconds, as shown in Figure 3A, which “provides three levels of intensity control.” *Id.* at 5:57–58. In the example shown in Figure 4, amplifier 308 “provides for eight

levels of amplification. This provides a finer resolution enhancement of the original three levels set by the integration time.” *Id.* at 5:60–64. Changing the gamma tables of the color and gamma correction block 314 can provide further refinement. *Id.* at 5:65–67. Thus, the ’884 patent explains that “by using the three gain levels of integration time, the eight level[s] of analog gain, and the multiple levels of digital gamma correction, a fine degree of brightness control can be achieved, all while maintaining the integration time at integral multiples of the period of the peak intensity of light output.” *Id.* at 5:67–6:6. Additionally, device driver 304 “preferably monitors the data from the brightness histogram 316, and over time alters the overall system gain, providing automatic gain control for the entire system.” *Id.* at 6:6–9.

G. Illustrative Claims

Claims 1 and 14 are the only independent claims challenged in this proceeding. Claims 2–6 depend directly or indirectly from claim 1, and claims 17–19 depend directly or indirectly from claim 14. Independent claims 1 and 14 are illustrative of the claimed subject matter and are reproduced below:

1. A method of reducing flicker caused by lighting having a periodic intensity using an imager having a pixel integration time, the method comprising the steps of:
 - setting the integration time to an integral multiple of the period of the periodic intensity of the lighting;
 - determining an amount to vary an overall system gain;
 - and
 - adjusting the overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity.

Ex. 1001, 6:63–7:6.

14. An imager for a digital camera with reduced flicker caused by lighting having a periodic intensity, the imager providing data for a plurality of pixels, the imager comprising:
- programmable integration time circuitry that controls an integration time of the plurality of pixels;
 - an integration time adjustment block coupled to the programmable integration time circuitry, the integration time adjustment block setting the integration time to an integral multiple of the period of the periodic intensity of the lighting; and
 - an overall gain control block that adjusts an overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity.

Id. at 7:47–8:4.

II. CLAIM CONSTRUCTION

Although Petitioner presents constructions for several claim terms,² no terms require express construction for purposes of this Decision.

III. ANALYSIS

A. *Anticipation of Claims 1–5 and 14 by Hashimoto*

Petitioner asserts that Hashimoto discloses each and every element of claims 1–5 and 14 of the '884 patent. Pet. 28–50. The Petition includes detailed claim charts³ identifying where Hashimoto allegedly discloses the elements of each challenged claim. *Id.*

² Petitioner points to the parties' proposed constructions for several claim terms in their civil action before the United States District Court for the Eastern District of Texas. Pet. 18–19 & 19 n.8.

³ Petitioner's claim charts are not a model of clarity. For example, Petitioner provides a single chart addressing its first six grounds. In relation to claim 1, Petitioner's chart is intended to address its first and second asserted grounds. Petitioner includes citations to Hashimoto and Kinugawa, a

Patent Owner asserts that Petitioner’s analysis fails to show how Hashimoto discloses the “adjusting the integration time while maintaining the integration time at an integral multiple” step as recited in claim 1, and “adjust[ing] an overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity,” as recited in claim 14. Prelim. Resp. 14, 24. Instead, Patent Owner contends that Petitioner relies upon the same disclosure of Hashimoto for the above “adjusting” step of claim 1 and “overall gain control block” element of claim 14, as Petitioner asserts discloses the “setting” step⁴ of claim 1 and integration time adjustment block setting the integration time” element of claim 14. *Id.* at 14–15.

1. *Hashimoto*

Hashimoto relates to “electronic cameras which can provide smooth moving images to a liquid crystal display for recorded image confirmation with contracted evaluation value computing circuit for AE (automatic exposure), AF (auto focus) and AWB (auto white balance).” Ex. 1004, 1:5–11. Hashimoto explains that “[a] second object of the invention is to provide an electronic camera, which can suppress image brightness variations even

reference relied upon for Petitioner’s second ground, in the same chart (*see* Pet. 29), and in a footnote asserts that “[t]o the extent it is argued that this element is not disclosed by Hashimoto,” one of ordinary skill in the art would have motivated to combine a teaching from Kinugawa. *See id.* at 30 n.12. Petitioner’s approach results in extremely long footnotes, containing extensive substantive argument, and breaks up Petitioner’s claim chart such that in at least one instance only two lines appear on a given page of the Petition. *See id.* at 30. In light of the issues and analysis presented, we are able to discern sufficiently Petitioner’s positions.

⁴ The “setting” step of claim 1 refers to “setting the integration time to an integral multiple of the period of the periodic intensity of the lighting.”

in the case when photoelectric charge is accumulated in a cycle capable of flicker cancellation.” *Id.* at 3:66–4:2. Hashimoto discloses an electronic camera including

means for setting the photoelectric charge accumulation time of the image pick-up device can set the photoelectric charge accumulation time discretely so that the photoelectric charge accumulation time can be changed to values free from flicker, and sets the photoelectric charge accumulation time variably in combination with gain control by gain control means.

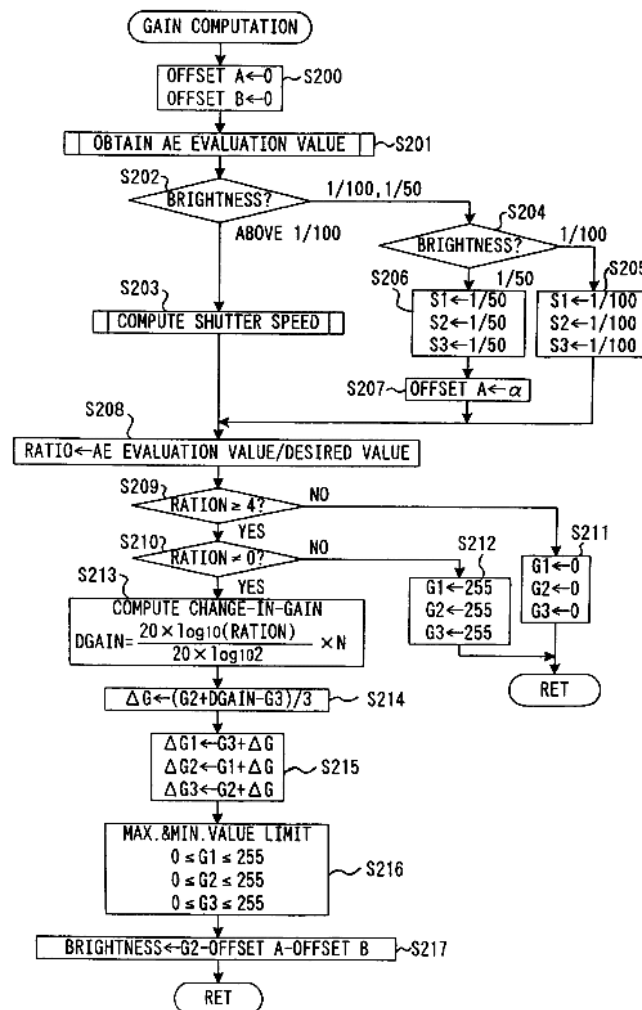
Id. at 4:55–63.

Hashimoto provides an example of “suppressing image flicker in photography under fluorescent lamp illumination.” *Id.* at 8:26–44. When an illumination device is driven at 60 Hz, “no image flicker is produced when the frame rate is 60 or 30 or 15 Hz.” *Id.* at 8:39–41. “When the illumination device is driven at 50 Hz, however, image flicker is produced. In this case, the image flicker can be removed by setting the shutter speed to 1/100 [or] 1/50.”⁵ *Id.* at 8:41–44.

⁵ Petitioner recognizes implicitly that Hashimoto contains a typographical error because Petitioner and Dr. Neikirk change the language quoted above from “setting the shutter speed to 1/100 to 1/50” to “setting the shutter speed to 1/100 or 1/50.” Pet. 21 (citing Ex. 1004, 8:40–44; Ex. 1003 ¶ 21); Ex. 1003 ¶ 21. Patent Owner alters similarly Hashimoto’s disclosure. See Prelim. Resp. 9 (“‘by **setting** the shutter speed’ at 1/100 or 1/50”).

Hashimoto's Figure 10 is reproduced below.

FIG. 10



Hashimoto's Figure 10 is "a flowchart for describing a gain computation process in the AE process step of the flow chart of [Figure] 9." *Id.* at 6:50–51.

Hashimoto explains the following with respect to the gain computation process depicted in Figure 10:

At the outset of this routine, the CPU 17 initializes offsets A and B (step S200). In this embodiment of the control status, the brightness (i.e., brightness of the scene) is controlled with the

gain at shutter speed of 1/100. So long as the camera is always operated at the shutter speed of 1/100, the brightness can be judged with the sole gain. Actually, however, various shutter speeds are used. Accordingly, when the shutter speed is changed from 1/100, gain is corrected or controlled with the offset, thus obtaining proper brightness control. The offset A is used when the shutter speed is changed from 1/100 to 1/50, and the offset B is used when the shutter speed is changed from 1/100 to a higher speed.

Id. at 11:9–20.

2. Discussion

Independent claim 1 is directed to a method of reducing flicker comprising, *inter alia*, “setting the integration time to an integral multiple of the period of the periodic intensity of the lighting” and “adjusting the overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity.” Ex. 1001, 6:66–67, 7:3–6. With respect to the “setting” step of claim 1, Petitioner relies on Hashimoto’s disclosure of setting the shutter speed to 1/100 or 1/50, each of which is an integral multiple of the period of the periodic intensity of the lighting, “when the illumination device is driven at 50 Hz.” Pet. 28–29 (citing Ex. 1004, 4:64–5:8, 7:8–30, 8:26–40, 8:41–44) (other citations omitted)). With respect to the “adjusting” step of claim 1, Petitioner quotes two portions of Hashimoto. First, Petitioner notes that “[a] second object of the invention is to provide an electronic camera, which can suppress image brightness variations even in the case when photoelectric charge is accumulated in a cycle capable of flicker cancellation.” *Id.* at 31 (quoting Ex. 1004, 3:64–4:2). Second, Petitioner notes that “[b]y combining the photoelectric charge accumulation time changes with the gain control as in the above construction, it is possible to reduce image brightness variations

and obtain smooth images not giving any sense of uncomfortability.” *Id.* (quoting Ex. 1004, 4:64–5:8).⁶

Patent Owner contends that Petitioner cites to the same portions of Hashimoto as teaching both the setting and adjusting steps of claim 1. Prelim. Resp. 14. Patent Owner acknowledges that Hashimoto discloses the *setting* step of claim 1. *Id.* at 15 (“Indeed, Hashimoto’s process includes the step of checking brightness, and setting a shutter speed at 1/100 **or** 1/50 (a computed speed)” (citing Ex. 1004, 11:35–52)). Patent Owner, however, asserts that Petitioner fails to explain how the cited portions of Hashimoto disclose the *adjusting* step of claim 1. *Id.* Specifically, Patent Owner contends that the cited portion of Hashimoto and Figure 10 fail to disclose the adjusting step. *Id.*

We agree with Petitioner and Patent Owner that Hashimoto discloses the setting step of claim 1. Petitioner, however, has not persuaded us, on this record, that Hashimoto likely discloses the claimed adjusting step. First, the citations and parentheticals in Petitioner’s claim charts do not, on their face, teach or suggest this step. Second, even though Petitioner points to Hashimoto’s disclosure of combining photoelectric charge accumulation time changes with gain control, Petitioner does not explain how Hashimoto actually combines these two features. Hashimoto’s discussion of gain control, in the context of Figure 10, suggests that gain is controlled via offsets, specifically offset A or offset B. *See, e.g.*, Ex. 1004, 11:15–20

⁶ In addition, Petitioner cites to paragraph 74 of the Neikirk Declaration (Pet. 31), which cites to the same portion of Hashimoto but does not provide additional explanation as to how this disclosure teaches the “adjusting” step of claim 1. Ex. 1003 ¶ 74 (citing Ex. 1004, 4:64–5:8; Ex. 1003, footnotes 1–5, 7).

(“Accordingly, when the shutter speed is changed from 1/100, the gain is corrected or controlled with the offset, thus obtaining proper brightness control. The offset A is used when the shutter speed is changed from 1/100 to 1/50, and the offset B is used when the shutter speed is changed from 1/100 to a higher speed.”). In Hashimoto’s discussion of gain control, however, Petitioner does not identify, and we are unable to discern, a teaching of “adjusting the overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity.”⁷

Independent claim 14 is directed to an imager for a digital camera, comprising, *inter alia*, “an integration time adjustment block . . . setting the integration time to an integral multiple of the period of the periodic intensity of the lighting” and “an overall gain control block that adjusts an overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity.” For the “overall gain control block that adjusts an overall system gain” limitation of claim 14, Petitioner relies on a disclosure from Hashimoto that is similar to the disclosure Petitioner relied upon for the “adjusting” step of claim 1. Pet. 38 (quoting Ex. 1004, 4:55–63) (“the

⁷ Petitioner’s claim chart for the “adjusting” step of claim 1 includes citations to twelve different textual portions of Hashimoto, one of which includes a span of seven columns, and ten different figures. Pet. 31. Of those citations, only two include parentheticals quoting the language of Hashimoto. Although Petitioner’s first sentence in its claim chart succinctly identifies the elements of Hashimoto that Petitioner contends correspond to the individual limitations of the “adjusting” step, Petitioner’s additional citations beyond those for which it provides parentheticals do not assist us in understanding Petitioner’s position.

electronic camera according to [the] first aspect [of Hashimoto's invention], wherein the means for setting the photoelectric charge accumulation time of the image pick-up device can set the photoelectric charge accumulation time discretely so that the photoelectric charge accumulation time can be changed to values free from flicker and sets the photoelectric charge accumulation time variably in combination with gain control by gain control means").

Petitioner's attempt to show that Hashimoto teaches the "overall gain control block" of claim 14 suffers from the same deficiencies discussed above with respect to the "adjusting" step of claim 1. Specifically, Petitioner does not show that the quoted portion of Hashimoto, or the text encompassed within Petitioner's numerous string citations,⁸ teach "adjust[ing] an overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity."

Accordingly, on the record before us, Petitioner has not established a reasonable likelihood of prevailing on the assertion that Hashimoto discloses each and every element of claims 1–5 and 14 of the '884 patent.

⁸ Petitioner's claim chart for the "gain control block" element of claim 14 includes citations to eleven different textual portions of Hashimoto, one of which includes a span of seven columns, and nine different figures. Pet. 38. Of those citations, only two include parentheticals quoting the actual language of Hashimoto. Although Petitioner's first sentence in its claim chart succinctly identifies which elements of Hashimoto Petitioner contends correspond to the individual limitations of the "gain control block" element, Petitioner's additional citations beyond those for which it provides parentheticals do not assist us in understanding Petitioner's position. *Id.*

B. Obviousness of Claims 1–6, 14, and 17–19

As noted above, claims 2–6 depend from claim 1, and claims 17–19 depend from claim 14. Petitioner relies upon the same teachings of Hashimoto, discussed above with respect to claims 1 and 14, in Petitioner’s challenges to (1) claims 1–6 and 14 as obvious over Hashimoto and Kinugawa; (2) claims 14 and 17–19 as obvious over Hashimoto and the knowledge of a person of ordinary skill in the art; (3) claims 17–19 as obvious over Hashimoto, Nishiyama, and the knowledge of a person of ordinary skill in the art; (4) claims 17–19 as obvious over Hashimoto, Nishiyama, Kinugawa, and the knowledge of a person of ordinary skill in the art; and (5) claims 17–19 as obvious over Hashimoto and the knowledge of a person of ordinary skill in the art. *See, e.g.*, Pet. 31 (referring to Petitioner’s discussion of claim 1), 38 (referring to Petitioner’s discussion of claim 14). Petitioner does not assert that Kinugawa, Nishiyama, or the knowledge of one of ordinary skill in the art⁹ remedies the deficiencies discussed above with respect to claims 1 and 14, or that the “adjusting” step of claim 1 and the “gain control block” of claim 14 would have been obvious in light of any of these additional references or teachings.

Accordingly, for the reasons discussed above with respect to Hashimoto and claims 1 and 14, Petitioner has not established, on the record before us, a reasonable likelihood of prevailing on the assertions that as of

⁹ For the purposes of this Decision, we need not decide whether Petitioner’s reliance upon the knowledge of a person of ordinary skill in the art violates 35 U.S.C. § 311(b), which limits the grounds under which a petitioner may request cancellation of claims in an *inter partes* review to “a ground that could be raised under section 102 or 103 and *only on the basis of prior art consisting of patents or printed publications*” (emphasis added).

the effective filing date of the claimed invention: (1) claims 1–6 and 14 would have been obvious over Hashimoto and Kinugawa; (2) claims 14 and 17–19 would have been obvious over Hashimoto and the knowledge of a person of ordinary skill in the art; (3) claims 17–19 would have been obvious over Hashimoto, Nishiyama, and the knowledge of a person of ordinary skill in the art; (4) claims 17–19 would have been obvious over Hashimoto, Nishiyama, Kinugawa, and the knowledge of a person of ordinary skill in the art; and (5) claims 17–19 would have been obvious over Hashimoto and the knowledge of a person of ordinary skill in the art.

C. Anticipation of Claims 1–5 and 14 by Inuiya

Petitioner asserts that Inuiya discloses each and every element of claims 1–5 and 14 of the '884 patent. Pet. 50–59. The Petition includes detailed claim charts identifying where Inuiya allegedly discloses the elements of each challenged claim. *Id.*

Patent Owner asserts that Petitioner's analysis fails to show how Inuiya discloses the “adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity” step, as recited in claim 1, and “adjust[ing] an overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity,” as recited in claim 14. Prelim. Resp. 17–19, 24. Instead, Patent Owner contends that Petitioner relies upon the same disclosure of Inuiya for the above “adjusting” step of claim 1 and “overall gain control block” element of claim 14, as Petitioner asserts discloses the “setting” step of claim 1 and integration time adjustment block setting the integration time” element of claim 14. *Id.* at 17–18.

1. *Inuiya*

Inuiya relates to a video camera, a printer apparatus, and “a method of controlling the video camera and . . . printer apparatus.” Ex. 1005, 1:13–20. *Inuiya* discusses the problem of flicker: “when a subject illuminated by a fluorescent lamp is photographed and the resulting image is played back in the form of a movie, there will be cases in which the image flickers and appears unattractive.” *Id.* at 2:8–11. Accordingly, one of *Inuiya*’s objects “is to prevent the impression of flickering of a reproduced image resulting from the effects of flicker.” *Id.* at 2:34–36. *Inuiya* explains that:

A video camera according to a ninth aspect of the present invention compris[ing] shutter implementing means for periodically repeating exposure performed at a first high shutter speed one time in a prescribed plurality of successive frames and exposure performed at an ordinary shutter speed at other times . . . [and] control means . . . for controlling the shutter implementing means in such a manner that the first high shutter speed and the ordinary shutter speed in the shutter implementing means will become an identical shutter speed that corresponds to a positive whole-number multiple of the period of an AC power supply of a light source generating the illuminating light, and controlling the amplifier circuit in such a manner that the amplification factors of the amplifier circuit become identical with regard to the first and second video signals.

. . .

The frequency of flicker of an illuminating device such as a fluorescent lamp corresponds to the AC frequency of the commercial power supply. If it is assumed that a shutter speed (e.g., $1/100$ of a second) equivalent to a whole-number multiple of the period (e.g., $1/50$ of a second) of the commercial power supply, then the average level of the video signal representing the image of each frame will be constant and flickering of the reproduced image can be prevented.

According to the invention, and by virtue of the above-described technique, it is determined whether the subject is

being influenced by flickering ascribable to light from a fluorescent lamp or the like. When it is judged that the subject is being affected by flicker, exposure is carried out at an identical shutter speed corresponding to a whole-number multiple of the period of the AC power supply. This means that the reproduced image will not flicker.

In an embodiment of the ninth aspect of the invention, the shutter speed corresponding to the positive whole-number multiple of the frequency of the AC power supply is a value lower than that of the high shutter speed but higher than that of the ordinary shutter speed.

This makes it possible to obtain a video signal capable of reproducing a blur-free, sharp still picture that is not affected by flicker.

In another embodiment of the ninth aspect of the invention, the video camera further comprises brightness measuring means for measuring brightness of the subject, and shutter control means, which is responsive to the fact that brightness of the subject measured by the brightness measuring means is below a prescribed level, for controlling the shutter implementing means in such a manner that the high shutter speed will become the ordinary shutter speed.

Id. at 12:37–13:2.

Further, Inuiya explains that:

the output of the automatic gain control circuit 6 can be held at a constant level also by varying the amplification factors of the automatic gain control circuit with respect to the first and second video signals in conformity with the illumination of the subject without controlling the diaphragm.

Furthermore, in foregoing embodiment, the high shutter speed and ordinary shutter speed are both changed to the shutter speed of $\frac{1}{100}$ of a second when flickering of light from a fluorescent lamp is detected. However, an arrangement may be adopted in which these shutter speeds are changed to the ordinary shutter speed of $\frac{1}{60}$ of a second when illumination of the subject is low. Further, when flickering is detected, the high shutter speed and ordinary shutter speed may both be

changed to the ordinary shutter speed of $\frac{1}{60}$ of a second irrespective of the magnitude of the subject illumination.

Id. at 34:62–35:11.

2. Discussion

Petitioner’s analysis with respect to Inuiya suffers from the same deficiencies as those noted above with respect to Hashimoto. Specifically, although Petitioner shows that Inuiya teaches the first step of claim 1, setting the integration period to an integral multiple of the period of the periodic intensity of the lighting (*see* Pet. 51), Petitioner, fails to show persuasively that Inuiya likely discloses the “adjusting” step of claim 1. Petitioner’s claim chart¹⁰ includes two parenthetical quotations for the “adjusting” step of claim 1 (*id.* at 53–54), but each speaks to Inuiya’s disclosure of “setting” the integration period, not “adjusting” the period as claimed. *See* Pet. 53–54 (quoting Ex. 1005, 11:61–12:61, 12:62–13:6).¹¹

Petitioner’s discussion of how Inuiya teaches the “overall gain control block” of claim 14 suffers the same deficiency. In particular, none of Petitioner’s parentheticals shows that Inuiya “adjusts an overall system gain by adjusting the integration time while maintaining integration time at an integral multiple of the period of the periodic intensity,” as recited in

¹⁰ Petitioner’s claim chart for the “adjusting” step of claim 1 includes citations to twenty-four different textual portions of Inuiya, several of which span one or more columns, and ten different figures. Pet. 53–54. Petitioner may not rely on numerous citations to a reference without expressly tying the cited disclosure to the language of the challenged claims.

¹¹ In addition, Petitioner cites to paragraph 100 of the Neikirk Declaration (Pet. 54), which cites to the same portion of Inuiya but does not provide additional explanation as to how this disclosure teaches the “adjusting” step of claim 1 (Ex. 1003 ¶ 100).

claim 14. Pet. 58–59. Further, Petitioner notes that Inuiya explains that, “[w]hen the illumination of the subject is low, the shutter speed is adjusted by the shutter control circuit 12 in such a manner that the output signal of the automatic gain control circuit 6 is maintained at a constant level in order to obtain a reproduced image having a suitable brightness.” Pet. 59 (quoting Ex. 1005, 28:1–5). As Patent Owner argues, this teaching supports the position that “shutter speed is adjusted while ***maintaining***, rather than adjusting, the output of automatic gain control circuit 6 ‘at a constant level.’” Prelim. Resp. 19 (quoting Ex. 1005, 28:4).

Accordingly, on this record, we are not persuaded that Petitioner has established a reasonable likelihood of prevailing on the assertion that Inuiya discloses each and every element of claims 1–5 and 14 of the ’884 patent.

D. Obviousness of Claims 1–6 and 14 over Inuiya and Kinugawa

As noted above, claims 2–6 depend from claim 1. Petitioner relies upon the same teachings of Inuiya, discussed above with respect to claims 1 and 14, in Petitioner’s challenges to claims 1–6 and 14 as obvious over Inuiya and Kinugawa. *See, e.g.*, Pet. 54 (referring to Petitioner’s discussion of claim 1). Petitioner does not assert that Kinugawa remedies the deficiencies discussed above with respect to claims 1 and 14, or that, in particular, the “adjusting” step of claim 1 and the “gain control block” of claim 14 would have been taught or suggested by Kinugawa.

Accordingly, for the reasons discussed above, Petitioner has not established, on this record, a reasonable likelihood of prevailing on the assertion that Inuiya and Kinugawa would have rendered the subject matter of claims 1–6 and 14 obvious as of the effective filing date of the claimed invention.

IV. CONCLUSION

For the foregoing reasons, we are persuaded that the information presented in the Petition does not demonstrate that there is a reasonable likelihood that Petitioner would prevail in challenging any of claims 1–6, 14, and 17–19 of the '884 patent as unpatentable.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied* as to all challenged claims of the '884 patent; and

FURTHER ORDERED that no *inter partes* review is instituted.

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