

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMERICAN MEGATRENDS, INC., et al.,
Petitioner,

v.

KINGLITE HOLDINGS INC.,
Patent Owner.

Case IPR2015-01487
Patent 6,308,265 B1

Before GLENN J. PERRY, TREVOR M. JEFFERSON, and
BRIAN J. McNAMARA, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

DECISION

Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

BACKGROUND

American Megatrends, Inc., Micro-Star International Co., Ltd, MSI Computer Corp., Giga-Byte Technology Co., Ltd., and G.B.T., Inc. (collectively, “Petitioner”) filed a Petition, Paper 7, and Corrected Petition, Paper 9 (“Pet.”), to institute an *inter partes* review of claims 1–19 (the “challenged claims”) of U.S. Patent No. 6,308,265 B1 (“the ’265 Patent”). 35 U.S.C. § 311. Kinglite Holdings, Inc. (“Patent Owner”) timely filed a Preliminary Response, Paper 12 (“Prelim. Resp.”), contending that the petition should be denied as to all challenged claims. We have jurisdiction under 37 C.F.R. § 42.4(a) and 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Having considered the arguments and the associated evidence presented in the Petition and the Preliminary Response, for the reasons described below, we do not institute an *inter partes* review.

REAL PARTIES IN INTEREST

Petitioner identifies the individual petitioner entities as the only real parties-in-interest. Pet. 8–9.

PENDING LITIGATION

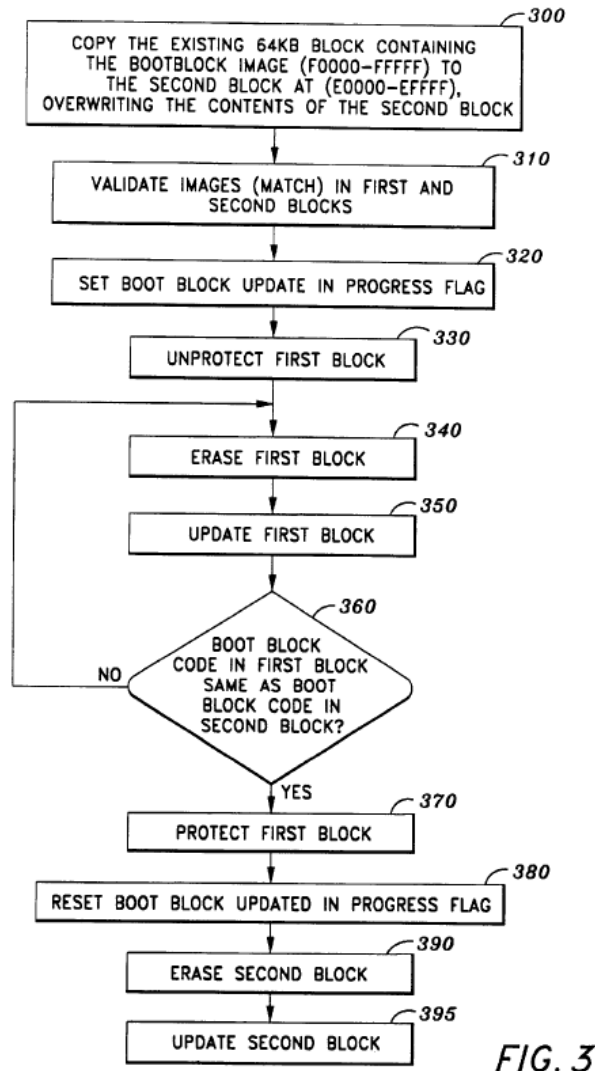
The Petition identifies that following related litigation: *Kinglite Holdings Inc. v. Giga-Byte Tech. Co. Ltd., et al.*, CV 14-04989 JVS (PJWx) (C.D. Ca); and *Kinglite Holdings Inc. v. Micro-Star Int’l Co. Ltd., et al.*, CV 14-03009 JVS (PJWx) (C.D. Ca). Petitioner also identifies the following *inter partes* reviews as related matters: IPR2015-001079; IPR2015-01081;

IPR2015-01094; IPR2015-01132; IPR2015-01133; IPR2015-01140;
PR2015-0114; IPR2015-01188; IPR2015-01189; IPR2015-01191; IPR2015-
01197; IPR2015-01487; IPR2015-01488; and IPR2015-01515.

THE '265 PATENT (EXHIBIT 1001)

The '265 Patent concerns the preservation of certain code or data, in particular the boot block code, within a 'protected' memory segment, while also allowing for updates of other code that is stored in the same segment. Ex. 1001, col. 1, ll. 9–12. The '265 Patent explains that a computer's Basic Input/Output system (BIOS), which contains system programs that provide access to disk drives, interfaces, and graphic adapters, is stored in a non-volatile random access memory (NVRAM), such as an electronically programmable read only memory (EPROM) or Flash RAM. *Id.* at col. 1, ll. 20–25. In conventional computers, a self-contained portion of the BIOS, known as the boot block, is write protected, so that upon reset after BIOS update (flash), its code can act as a mini-BIOS to read the updated BIOS image and write it to the flash part of the NVRAM. *Id.* at col. 1, ll. 48–65. As a result of the small size of the boot block relative to other code, using symmetrical memories with the same size segment wastes memory space, but using non-symmetrical flash memories with different size segments is more expensive. *Id.* at col. 2, l. 2–col. 3, l. 12.

The '265 Patent discloses a method of protecting the boot block code while allowing updating of BIOS code. Abstract. Figure 3 below is a flowchart depicting the claimed method of protecting the boot block code.



The '265 Patent discloses boot block code and other code are stored in a first writable segment of flash memory that is usually set to be protected. *Id.* at col. 3, ll. 31–34. All the data in the first writable segment is copied into a second writable segment, which then is validated. *Id.* at col. 3, ll. 34–38. Next, the first writable segment is set to an unprotected, writable state, erased, and updated with new code, including the boot block code. *Id.* at col. 3, ll. 38–44. The boot block code in the updated first writable segment is compared to the boot block code in the second writable segment, and if

they are identical, the first block is protected as non-writable. *Id.* at col. 3, ll. 44–51. As Figure 3 shows, the second block can then be erased and written over.

ILLUSTRATIVE CLAIM

Method claim 1 and apparatus claim 9 are illustrative:

1. A method of protecting first boot block code and allowing an update to other code or data residing in a same segment or region as the first boot block code, wherein the first boot block code and the other code or data is stored in a first writable segment of a memory that is initially set to a protected non-writable state, the method comprising the steps of:
 - a) copying all information stored in the first writable segment of the memory into a second writable segment of the memory;
 - b) validating the copied information in the second writable segment of the memory;
 - c) setting the first writable segment to a non-protected, writable state;
 - d) erasing all information stored in the first writable segment;
 - e) updating the first writable segment with updated code or data, the updated code or data including second boot block code;
 - f) comparing the second boot block code stored in the first writable segment with the first boot block code stored in the second writable segment;
 - g) if the comparison in step f) is such that the second and first boot block codes respectively stored in the first and second rewritable segments are identical, setting the first rewritable segment to the protected, non-writable state.

9. An apparatus for providing protection for boot block code, comprising
- a memory that consists of a plurality of segments including at least two equal sized segments, each of the segments being capable of being erased and rewritten to, wherein the boot block code is stored in a first of the equal sized segments along with other data stored in said first of the equal sized segments, and a copy of at least the boot block code in the first of the equal sized segments to be copied to a second of the equal sized segments,\
 - and a processor programmed to compare the boot block code stored in the first of the equal sized segments with the boot block code stored in the second of the equal sized segments to verify that the boot block code stored in the first of the equal sized segments and the boot block code stored in the second of the equal sized segments are identical; if so, said first of the equal sized segments being updated with updated code at least a portion of which includes the boot block code of the second of the equal sized segments.

ART CITED IN PETITIONER'S CHALLENGES

Petitioner cites the following references in its challenges to patentability:

Reference	Designation	Exhibit No.
U.S. Patent No. 5,432,297 issued July 11, 1995	Grote	Ex. 1004
U.S. Patent No. 6,148,441 issued Nov. 14, 2000	Woodward	Ex. 1003
U.S. Patent No. 6,031,757 issued Feb. 29, 2000	Chuang	Ex. 1005

CHALLENGES ASSERTED IN PETITION

Claims	Statutory Basis	Challenge
9	35 U.S.C. § 103	Obvious over Grote and Woodward
1–8, 10–19	35 U.S.C. § 103	Obvious over Grote, Woodward, and Chuang

CLAIM CONSTRUCTION

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their “broadest reasonable construction in light of the specification of the patent” in which they appear. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC.*, 793 F.3d 1268, 1278-79 (Fed. Cir. 2015). Applying that standard, we interpret the claim terms according to their ordinary and customary meaning in the context of the patent’s written description. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

The parties dispute the proper construction of the following terms:

Boot block code: It is unclear whether Petitioner proposes a specific construction for boot block code. Petitioner cites the discussion in the ’265 Patent of the boot block code as a “mini-BIOS” and the ’265 Patent’s statement that the boot block code may be considered a “non-updateable portion of the BIOS code.” Pet. 11–12 (citing Ex. 1001, col 3, ll. 12–13). Patent Owner notes that the claimed methods do not prevent the boot block code from being overwritten because, according to the claimed method, the boot block code is copied and protected, then overwritten and checked against the protected copy to make sure the newly stored boot block code is

unchanged from the original, protected version. Prelim. Resp. 8–9. In consideration of the above, we construe the boot block code to mean *a portion of the BIOS code whose content is intended to remain unchanged*.

Comparing the first boot block code stored in the first writable segment with the second boot block code stored in the second writable segment: Petitioner notes that this limitation, which appears in claim 13, states that the first boot block code is stored in the first writable memory and contrasts that with claim 1, which states that the second boot block code is stored in the first writable memory. Pet. 12. Petitioner contends that although this recitation is indefinite because it contradicts a previous limitation in claim 13, the limitation should be construed in the same manner as its counterpart in claim 1. Pet. 12. Patent Owner appears to agree, stating that, notwithstanding the claim language, it should be construed in the same manner as its counterpart in claim 1 to mean “comparing the second boot block code stored in the first writable segment with the first boot block code stored in the second writable segment.” Prelim. Resp. 10. According to Patent Owner, such an interpretation is supported by the specification of the ’265 Patent. *Id.* (citing Ex. 1001, col. 6, ll. 33–38). Although this interpretation appears to contradict the plain language of claim 13, in view of the positions of the parties, for purposes of this Decision only, we construe this limitation of claim 13 in the same manner as that of its counterpart in claim 1.

Wherein, if a reboot occurs when the flag is in the reset state, the reboot will occur using the first boot block code stored in the second writable segment and not the second boot block code stored in the first writable segment: Petitioner asserts that this limitation in claim 7 is also

indefinite because it is not supported by the specification and contradicts Fig. 3, which states that the computer will be booted up from the boot block code in the first region. Pet. 12–13. Petitioner proposes that the limitation be construed to mean that the reboot will occur using second boot block code stored in the first writable segment, rather than the first boot block code stored in the second writable segment. *Id.* at 13. Patent Owner appears to agree with Petitioner’s construction, arguing that the limitation means “wherein if a reboot occurs when the flag is in the reset state, the reboot will occur using the second boot block code stored in the first writable segment and not the first boot block code stored in the second writable segment.” Prelim. Resp. 10. As support for this construction, Patent Owner cites the disclosure in the ’265 Patent that in the ninth step of Figure 3, with the boot-block-in-progress flag reset, the PC will be allowed to boot up from the boot block code in the first region. *Id.* at 10–11 (citing Ex. 1001, col. 7, ll. 4–7). Although this interpretation appears to contradict the plain language of claim 7, in view of the positions of the parties, for purposes of this Decision only, we construe this limitation of claim 7 to mean that when the boot-in-progress flag is reset, the computer will be allowed to boot up from the second boot block code stored in the first writable segment.

ANALYSIS OF PETITIONER’S PRIOR ART CHALLENGES

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying

factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Claim 9 As Obvious Over Grote and Woodward

Analysis of Arguments Concerning Grote

Petitioner contends that Grote discloses the same general copy-compare-update procedure as that performed by the apparatus recited in claim 9. Pet. 15. Patent Owner argues that Petitioner oversimplifies claim 9 of the '992 Patent as reciting the copy-compare-update process disclosed by Grote. Prelim. Resp. 15. Noting that the '265 Patent discloses that “[A]fter updating the first region with an updated BIOS image, the '265 Patent checks ‘whether the contents of the boot block code of the flashed in image within the first region is exactly the same as the copied boot block code with in the second region,’” Patent Owner emphasizes that claim 9 recites “said first of the equal sized segments being updated with updated code at least a portion of which includes the boot block code of the second equal sized segments.” *Id.* at 15–16 (citing Ex. 1001, col. 6, ll. 35–38). According to Patent Owner, Grote does not disclose the claimed verification of new code downloaded onto the EEPROM against the “old code” (*id.* at 15–16), nor the claimed equal sized memory segments (*id.* at 17–22).

Grote discloses a boot strap loading system that employs dual, separable EEPROM units to facilitate safe reprogramming of bootstrap loader software. Ex. 1004, Abstract. Grote describes providing a computer system with first and second EEPROM regions, both of which are adapted to

store bootstrap loader code, with one of the regions designated as that which will be utilized to oversee the next machine reboot. *Id.* at col. 2, ll. 52–57. .

Grote discloses a preferred embodiment in which both the base and auxiliary EEPROMs are always available, so that in a normally running non-remap mode, the base flash EEPROM appears at the boot address of the CPU, and in a remap mode used during reprogramming of the base flash set, the auxiliary flash EEPROM address appears at the boot address of the CPU. Ex. 1004, col. 3, l. 66–col. 4, l. . Patent Owner argues that in Grote a fall-back (fail-safe) copy of the original code (“old code”) is stored in the auxiliary EEPROM in case the “new code” does not work, and that Grote does not verify the “new code” against the old code stored in the auxiliary EEPROM. *Id.* at 16. According to Patent Owner, Grote only teaches switching back to the fail-safe “old code” in the auxiliary EEPROM if the image base EEPROM does not boot. *Id.* at 17 (citing Ex. 1004, col. 5, ll. 35–41, col. 6, ll. 12–17).

Petitioner states that Grote discloses comparing the contents of a “Base EEPROM” with the contents of an “Auxiliary EEPROM” to verify integrity and mirrors the claimed feature of updating the first equal sized segment of a memory by stating that the Base EEPROM is programmed with new code after the comparison. Pet. 15–16 (citing Ex. 1004, Fig. 3, col. 7, ll. 5–10). The subject matter Petitioner cites at column 7 is in claim 4 of Grote, which is a further limitation on the method of switching between the base and auxiliary memories recited in Grote claim 1. Claim 4 of Grote discloses “comparing the most recently loaded initialization instructions copied from said base memory into the auxiliary memory region to the initialization instructions currently residing in said base memory region.”

Ex. 1004, col. 7, ll. 5–10. Grote describes entering a reload mode in two ways: (1) manually, to allow a new system program to be downloaded and installed, or (2) by a recovery mechanism of the boot sequence. Ex. 1004, col. 5, ll. 21–27. In manual reprogram mode, after it is determined that the main boot segment is not corrupt, the auxiliary EEPROM is erased, programmed with an image of the current boot set and the copy of the boot set in the auxiliary EEPROM is verified against the current boot set in the base EEPROM; then the system enters the “remap” mode, which is executed from the auxiliary EEPROM set. *Id.* at col. 5, ll. 35–56, Fig. 3, Steps 120–128. If the system is in the remap mode, for example, as a result of having been corrupted or a power failure, Grote discloses skipping Steps 122–128, which appears to avoid copying corrupted boot code to the auxiliary EEPROM, to force a download of a valid bootstrap firmware set. *Id.* at col. 5, ll. 14–17, Fig. 3. In either case, beginning at Step 130, Grote discloses reprogramming the base EEPROM and verifying the base EEPROM set against the image of the new code. *Id.* at Fig. 3, steps 130–138. Petitioner has not identified any disclosure in Grote of comparing the “old” code in the auxiliary EEPROM to the “new” base code to verify the boot block has not been changed.

Thus, we are persuaded by Patent Owner’s argument that Grote’s disclosure of operating from the auxiliary flash when the system is corrupt or when some other condition, such as a power failure triggers a reboot, is distinguished from the claimed apparatus in which the processor is programmed to compare the updated boot block code stored in the first of the equal sized segments with the original boot block code in the second of

the equal sized segments to verify that the updated boot block code is exactly the same.

Patent Owner also responds that, contrary to Petitioner's arguments, Grote does not disclose the equal sized memory segments recited in claim 9. Prelim. Resp. 17–22. In response to Petitioner's argument that because Grote discloses memory segments having the same address scheme, Grote suggests the two segments are of the same size (Pet. 16), Patent Owner argues that having a flash set appear at the boot address does not indicate the size or segment size of the flash set. Prelim. Resp. 16–18. According to Patent Owner, a flash set appearing at the boot address of the CPU simply lets the CPU know where the system bootstrap instructions associated with that processor are located. *Id.* at 18 (citing Ex. 1001, col. 4, ll. 53–58). Petitioner also argues that because two portions of the BIOS are stored together in Grote, a dedicated asymmetrical memory segment is not needed. Pet. 17. Patent Owner responds that Grote does not teach how its base flash set and auxiliary flash set are segmented or how data is stored in such segments, and that merely knowing the boot block code and other BIOS data are stored together in memory is insufficient to indicate whether the memory is asymmetrical or symmetrical. Prelim. Resp. 19–20.

Citing Grote's disclosure of selecting the EEPROM region to accomplish the next reboot by masking the address of one or the other EEPROM region into the address base of a central processor unit, Petitioner argues that the ability to support masking further demonstrates that each segment has the same address length, and consequently the same size. Pet. 17. Patent Owner responds that, although Grote discloses mapping the memory address space associated with the base flash set or the auxiliary

flash set to the CPU, Grote does not disclose that masking indicates the same address length for the base flash set and the auxiliary flash set, nor is the address space of the processor of the same length when either the base flash set or auxiliary flash set is mapped to such processor. Prelim. Resp. 20–21 (citing Ex. 1004, col. 3, l. 62–col. 4, l. 3).

Petitioner further argues that Grote discloses using the auxiliary flash set as a backup for the base flash set in a manner that interchanges the two flash set regions during a power failure. Pet. 17. Noting that Petitioner fails to articulate any relevance of this teaching to the base flash set or auxiliary flash set being symmetric, Patent Owner disputes that the ability to interchange to flash segments in a recovery mode so that the content of the recovery flash region is usable indicates anything about the size or disposition of the two flash regions. Prelim. Resp. 21. By way of example, Patent Owner notes that if the base flash set is 640 kilobytes and the auxiliary flash set is 1024 kilobytes, and assuming the same bootstrap data is stored in each of the base flash set in the auxiliary flash set, the two flash sets can be interchanged during a power failure because the bootstrap data is the same although the base flash set in the auxiliary flash set are of different sizes. *Id.* at 21–22.

Petitioner further argues that Grote interchangeably refers to two flash regions that are “similarly comprised” and designates either one for overseeing reboot. Pet. 17–18. Patent Owner responds that the term “similarly comprised” refers to the base flash set and auxiliary flash set being EEPROM devices, not that they are comprised of two flash segments of equal size. Prelim. Resp. 22–23. Patent Owner again notes that the ability to interchange to flash regions merely indicates the content of the

flash regions and is irrelevant to whether the two flash regions are of equal size or have segments of equal size. *Id.* at 22.

We are not persuaded by Petitioner's argument that, taken in context, Grote demonstrates a structure having two equal sized flash segments, as recited in claim 9. Pet. 18. Petitioner has identified no specific discussion in Grote concerning equal sized flash segments. Instead, Petitioner references subject matter in Grote that, as Patent Owner demonstrates, does not require symmetric memory or equal sized segments. Petitioner's arguments mirror the testimony Dr. Stefano Righi, Ex. 1010 ("Righi Decl."), at paragraph 37. Although Dr. Righi testifies that the purpose of the '265 Patent is to store the boot block and other code together in symmetrical memory, rather than asymmetrical memory, Dr. Righi points to no specific discussion in the '265 Patent concerning this issue. Righi Decl. ¶ 37. Instead Dr. Righi points to the same subject matter in the '265 Patent discussed in the Petition.

Analysis of Arguments Concerning Woodward

Petitioner argues that Woodward discloses the same general principles as those of the '265 Patent. Pet. 18. According to Petitioner, Woodward discloses asymmetrical memory storing a boot code in sector 3 and other data in differently sized sectors 0–2, and proposes a symmetrical memory structure where sector is the same size, as shown in Fig. 3 by flash ROM 14, which is divided into eight equal size sectors. *Id.* Petitioner argues that a person of ordinary skill would be motivated to combine Grote's explicit disclosure of applying its process to the bootstrap loader code (BIOS) with the symmetrical flash memory disclosed in Woodward. *Id.* at 19. As support for this argument, Petitioner cites Woodward's disclosure that it would be advantageous to develop a methodology for modifying the

Extended Industrial Standard Architecture (EISA) configuration code in a flash ROM device, without disturbing the other contents of the flash ROM, especially the boot code. *Id.* at 20 (citing Ex. 1003, col. 4, ll. 3–9).

Patent Owner disputes Petitioner’s contention that Woodward verifies the boot block code does not change after updating the flash ROM and Petitioner’s assertion that Woodward ensures that the boot block code in the flash memory is the same as the boot block in the backup memory. Prelim. Resp. 25–26. Woodward discloses that

[D]uring erase operations of the EISA configuration code, the CPU preferably reads the boot code . . . from sector 7 of the AMD flash ROM, and stores these codes in RAM. After sector 7 is erased, the boot code and . . . are automatically stored back in sector 7 of the flash ROM.

Ex. 1003, col. 4, ll. 50–55. Patent Owner notes that in Woodward there is no verification that the boot block code was not changed during the update, because the boot block code is not part of the update—instead, the boot block code that was copied to RAM from the flash ROM simply is copied back from the RAM to the flash ROM. Prelim. Resp. 25–26 (citing Ex. 1003, col. 10, ll. 40–45, 62–67). Woodward discloses checking whether the boot block code in the RAM corresponds to the boot block code copied into the flash ROM, and, if an error is detected, setting the carry flag CF and the upper half of the register to hexadecimal 84. Ex. 1003, col. 10, l. 64–col. 11, l. 3. However, as Patent Owner points out, this is not the same as verifying that the boot block code stored as part of the flash memory update (the boot block code stored in the first memory segment) matches the original boot block code (the boot block code copied into the second memory segment). Thus, because Woodward copies the original boot block code to the ROM, as opposed to verifying that the updated boot block code in the ROM is

exactly the same as the original boot block code, we are not persuaded by Petitioner's arguments that Woodward discloses comparing the boot block code in the update to the original boot block code to determine if there are any differences.

For the reasons discussed above, we are not persuaded that Petitioner has demonstrated a likelihood it will prevail in its challenge to claim 9 based on the combination of Grote and Woodward.

Claims 1–8 and 10–19 as Obvious Over Grote, Woodward, and Chuang

Claims 10–12 depend from apparatus claim 9. As discussed above, we are not persuaded that the combination of Grote and Woodward discloses an apparatus in which “said first of the equal sized segments being updated with updated code at least a portion of which includes the boot block code of the second equal sized segments.” Petitioner does not cite any disclosure of this feature in Chuang. Instead Petitioner cites Chuang as disclosing the application of write protection to flash memory segments. Pet. 33.

Therefore, we do not institute a trial on Petitioner's challenge to claims 10–12.

Independent method claim 1 is drawn to a method. Independent claim 13 is drawn to a computer program product reciting coded elements to perform substantially the same steps as those recited in claim 1. The steps in the method include comparing the second block code stored in the first writeable segment (the updated code) with the first boot block code (the original code) stored in the second writable segment to verify that the second and first boot block codes are identical. For the reasons discussed above, we are not persuaded that Petitioner has demonstrated this limitation is found in either Grote or Woodward. Petitioner does not cite any disclosure of this

feature in Chuang. Instead, Petitioner cites Chuang as disclosing the application of write protection to flash memory segments. Pet. 33. Therefore, we decline to institute a trial on this challenge to independent claims 1 and 13. Claims 2–8 depend from claim 1 and claims 14–19 depend from claim 13. Having determined that Petitioner has not demonstrated a likelihood it will succeed on its challenges to independent claims 1 and 13, we decline to institute a trial on dependent claims 2–8 and 14–19.

SUMMARY

For the reason discussed above, we are not persuaded that Petitioner has demonstrated a likelihood of success in its challenges to claims 1–19 of the '265 Patent and we decline to institute a trial.

ORDER

We decline to institute an *inter partes* review of the '265 Patent based on the challenges presented in the Petition.

PETITIONER:

Vivek Ganti
Gregory Ourada
HILL, KERTSCHER & WHARTON, LLP
vg@hkw-law.com
go@khw-law.com

PATENT OWNER:

Christopher Frerking
chris@ntknet.com