

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HTC CORPORATION and HTC AMERICA, INC.,¹
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,
Patent Owner.

Case IPR2015-01500
Patent 7,321,368 B2

Before JAMES B. ARPIN, MATTHEW R. CLEMENTS, and
SUSAN L. C. MITCHELL, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. were terminated from this proceeding. Paper 28. LG Electronics, Inc. also was terminated from this proceeding. Paper 43.

I. INTRODUCTION

HTC Corporation; HTC America, Inc.; LG Electronics, Inc.; Samsung Electronics Co., Ltd.; and Samsung Electronics America, Inc. (collectively, “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–3, 5, 7, 13–15, 17–21, and 23–25 (“the challenged claims”) of U.S. Patent No. 7,321,368 B2 (Ex. 1001, “the ’368 patent”). Paper 2 (“Pet.”). Parthenon Unified Memory Architecture LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). On January 6, 2016, we instituted an *inter partes* review of claims 1–3, 5, 7, 13–15, 17–21, and 23–25 (“the instituted claims”) of the ’368 patent on certain grounds of unpatentability alleged in the Petition. Paper 14 (“Dec. to Inst.” or “Inst. Dec.”)

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 21, “PO Resp.”), to which Petitioner filed a Reply (Paper 32, “Pet. Reply”).

We held a hearing on September 19, 2016, for this case and related Cases IPR2015-01501 and IPR2015-01502; and a transcript of that hearing is part of this record. Paper 53 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner has shown, by a preponderance of the evidence, that the instituted claims of the ’831 patent are unpatentable.

A. *Related Proceedings*

The ’368 patent is involved in several cases pending in the Eastern District of Texas. Pet. 2–3; Paper 38, 2–3. The ’368 patent also is involved in *ZTE USA, Inc. v. Parthenon Unified Memory Architecture*, Case

IPR2016-00666 (now terminated) and *Apple Inc. v. Parthenon Unified Memory Architecture*, Case IPR2016-01118 (pending). Petitioner also has filed other petitions seeking *inter partes* review of related patents. Pet. 3.

B. The '368 patent

The '368 patent, titled “Electronic System and Method for Display Using a Decoder and Arbiter to Selectively Allow Access to a Shared Memory,” issued January 22, 2008, from U.S. Patent Application No. 10/174,918, filed on June 19, 2002. Ex. 1001 at [54], [45], [21], [22]. Although the earliest application to which the '368 patent claims priority was filed August 26, 1996, Patent Owner informed us that the '368 patent expired on September 11, 2016. Paper 8 (“The Patent Owner hereby responds that the correct expiration date for U.S. Patent No. 7,321,368 is September 11, 2016.”).²

The '368 patent relates generally “to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system.” Ex. 1001, 1:42–47. At the effective filing date of the '368 patent, a conventional decoder included a dedicated memory, which represented a significant percentage of the cost of the decoder and which went unused most of the time. *Id.* at 2:28–59, 4:54–5:4, Figs. 1a–1c.

² The '368 patent states on its face that, “[s]ubject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. [§] 154(b) by 16 days” (Ex. 1001, [*]), which is consistent with PO’s representation that the patent expired on Sept. 11, 2016.

To address these and other concerns, the '368 patent discloses an electronic system in which a first device and a video and/or audio decompression and/or compression device are coupled to a shared memory through a bus having bandwidth sufficient for the video and/or audio decompression and/or compression device to operate in real time. *Id.* at 5:8–18. Figure 2 is reproduced below.

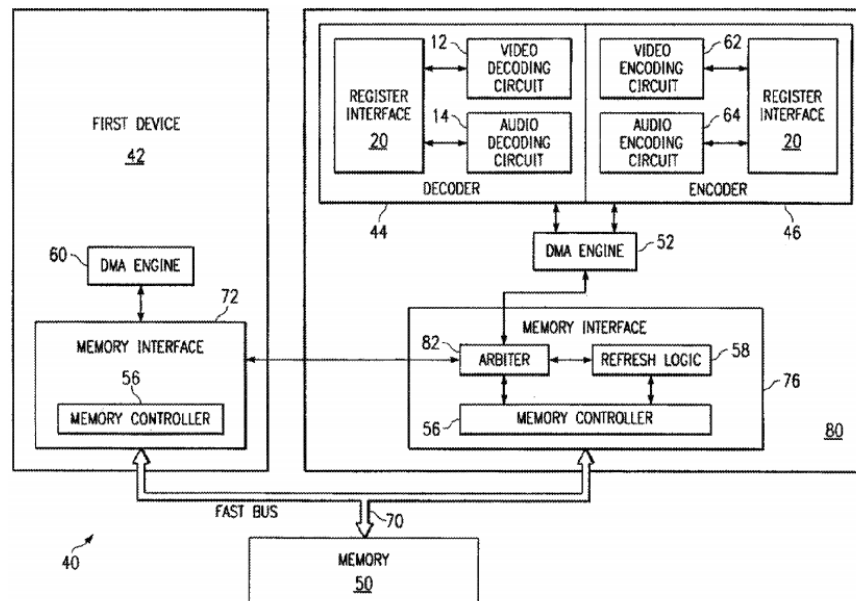


Fig. 2

Figure 2 is a block diagram of an electronic system that contains a device with a memory interface and an encoder and decoder. *Id.* at 6:17–19. “First device 42 can be a processor, a core logic chipset, a graphics accelerator, or any other device that requires access to the memory 50.” *Id.* at 6:43–46. Both first device 42 and decoder/encoder 80 have access to memory 50 through memory interfaces 72 and 76, respectively, coupled to fast bus 70. *Id.* at 6:41–43, 7:55–56. Fast bus 70 has a bandwidth of at least the bandwidth required for decoder/encoder 80 to operate in real time and, preferably, has a bandwidth of at least approximately twice the bandwidth required for decoder/encoder 80 to operate in real time. *Id.* at 8:32–38.

During operation, decoder/encoder 80, first device 42, and refresh logic 58, if it is present, request access to memory 50 through arbiter 82. *Id.* at 13:7–10. Arbiter 82 determines which of the devices gets access to memory 50. *Id.* at 13:11–13. Decoder/encoder 80 gets access to memory 50 in the first time interval, and first device 42 gets access to memory 50 in the second time interval. *Id.* at 13:14–16. Direct Memory Access (DMA) engine 52 of decoder/encoder 80 determines the priority of decoder/encoder 80 for access to memory 50 and the burst length when decoder/encoder 80 has access to memory 50. *Id.* at 13:16–20. DMA engine 60 of first device 42 determines its priority for access to memory 50 and the burst length when first device 42 has access to memory 50. *Id.* at 13:20–23.

When decoder/encoder 80 or one of the other devices generates a request to access memory 50, the request is transferred to arbiter 82, and access to memory 50 is determined based on the state of arbiter 82 and on a priority scheme. *Id.* at 13:24–53. The priority scheme can be any scheme that ensures decoder/encoder 80 gets access to memory 50 often enough to operate properly, but does not starve other devices sharing memory 50. *Id.* at 13:54–58.

C. Illustrative Claim

Of the challenged claims, claims 1, 5, 7, 13, and 20 are independent. Claims 2 and 3 depend directly from claim 1; claims 14, 15, 17–19 depend directly from claim 13; and claims 21 and 23–25 depend directly from claim 20. Claim 1 is illustrative and is reproduced below:

1. An electronic system comprising:
 - a main memory having stored therein data corresponding to images to be decoded and also decoded data corresponding to images that have previously been decoded;
 - a bus coupled to the memory;
 - a decoder coupled to the bus for receiving compressed images and for outputting data for displaying the decoded images on a display device, the decoder receiving data from the main memory corresponding to at least one previously decoded image and to a current image to be decoded and outputting decoded data corresponding to a current image to be displayed, the current image being stored in the main memory;
 - a microprocessor system coupled to the main memory, the microprocessor system storing non-image data in and retrieving data from the main memory; and
 - an arbiter circuit coupled to both the microprocessor system and the decoder for controlling the access to said main memory by the decoder and the microprocessor.

Ex. 1001, 15:57–16:9.

D. Applied References and Declarations

Petitioner relies upon the following references and declarations:

Exhibit	Reference
1003	U.S. Patent No. 5,546,547, issued Aug. 13, 1996 (“Bowes”)
1004	International Organization for Standardization, “ISO/IEC 11172-2: Information technology—Coding of moving pictures and associated audio for digital storage media at up to about 1,5 Mbit/s—Part 2: Video,” (1st ed. Aug. 1, 1993) (“MPEG”)
1005	S. Rathnam et al., “An Architectural Overview of the Programmable Multimedia Processor, TM-1,” PROC. COMPCON, IEEE Computer Society Press, Los Alamitos, CA, 1996, pp. 319–326 (1996) (“Rathnam”)
1007	U.S. Patent No. 5,774,676, issued June 30, 1998 (“Stearns”)

Pet. 5–6. Petitioner also relies upon the Declaration of Harold S. Stone, Ph.D. (“Stone Decl.”) (Ex. 1030) and the Reply Declaration of Harold S. Stone, Ph.D. (“Stone Reply Decl.”) (Ex. 1032).

Patent Owner relies upon the Declaration of Mitchell A. Thornton, Ph.D. (“Thornton Decl.”) (Ex. 2009).

E. The Instituted Grounds of Unpatentability

We instituted *inter partes* review of the ’368 patent based upon the following grounds (Dec. to Inst. 23–24):

References	Basis	Claims challenged
Bowes and MPEG	35 U.S.C. § 103(a)	1, 5, 7, 13, 15, 18, 20, 24, and 25
Bowes, MPEG, and Rathnam	35 U.S.C. § 103(a)	17, 19, and 23
Bowes, MPEG, and Stearns	35 U.S.C. § 103(a)	2, 3, 14, and 21

II. ANALYSIS

A. Claim Construction

Petitioner alleged that the ’368 patent would expire in September 2016. Pet. 10–11. Patent Owner stated that the ’368 patent would expire on September 11, 2016. Paper 8, 1. Thus, the parties agree that the ’368 patent has expired.

As a result, we construe the claims in accordance with the principles followed in district court. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b); *see Toyota Motor Corp. v. Cellport Sys., Inc.*, Case IPR2015-00633, slip op. at 8–10 (PTAB Aug. 14, 2015) (Paper 11); *cf. In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (“While claims are generally given their broadest possible scope during prosecution, the Board’s review of the claims of an expired patent is similar to that of a district court’s review.”) (internal citation omitted). Moreover,

Petitioner argues that its proposed construction will remain the same even if we apply the principles set forth in *Phillips*. Pet. 11 (stating that “the constructions proposed herein are consistent with both [the Phillips standard and the broadest reasonable interpretation standard]”).

In our Decision on Institution, we construed “decoder” to mean “hardware and/or software that translates data streams into video or audio information.” Inst. Dec. 8–9. Neither party disputes our determination or proposes additional terms for construction. Based on the record developed during this proceeding, we continue to apply this construction.

*B. Claims 1, 5, 7, 13, 15, 18, 20, 24, and 25 —
Obviousness over Bowes and MPEG*

Petitioner argues that claims 1, 5, 7, 13, 15, 18, 20, 24, and 25 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes and MPEG. Pet. 35–51. For the reasons explained below, Petitioner has established, by a preponderance of the evidence, that claims 1, 5, 7, 13, 15, 18, 20, 24, and 25 would have been obvious over Bowes and MPEG.

1. Bowes (Ex. 1003)

Bowes describes a memory bus arbiter for a computer system having a DSP co-processor. Ex. 1003, Title. According to Bowes,

In prior art computer systems, because of the high bandwidth required for real-time processing by a DSP, it has not been possible for the DSP to run off of the computer system’s DRAM in the way the CPU 10 utilizes it without adversely affecting the rest of the computer system. Thus, there has been provided a large block of SRAM 24 for use by the DSP 20. . . .

A significant disadvantage to the prior art computer architecture of FIG. 1 is the requirement of a substantial block of static random access memory 24. SRAMs are significantly more

expensive than DRAM which greatly increases the cost of computer systems which incorporate SRAM.

Id. at 2:36–48. Thus, it is an object of Bowes “to provide a mechanism and method for arbitrating the memory bus bandwidth to efficiently allow the use of a digital signal processor and a CPU over a common memory bus sharing the system’s dynamic random access memory subsystem without requiring an expensive block static random access.” *Id.* at 2:57–63.

Figure 2 of Bowes is reproduced below.

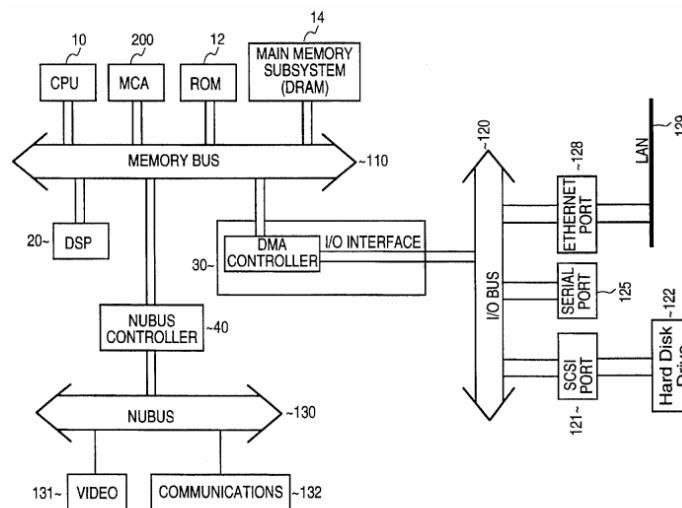


Figure 2

Figure 2 illustrates a block diagram of a computer architecture incorporating the arbitration scheme described in Bowes. *Id.* at 3:62–64. “The scheme is implemented such that the DSP is provided with sufficient bandwidth to perform real-time digital signal processing using the system’s dynamic random access memory (DRAM) and not requiring the incorporation of an expensive block of static random access memory (SRAM).” *Id.* at 4:55–60.

As shown in Figure 2, the system includes CPU 10, memory controller and arbiter (MCA) 200, main memory 14, and DSP 20. *Id.* at

Fig. 2. “Unlike prior art computer systems, the [system of Bowes] provides for the DSP 20 to reside on the system’s memory bus and operate from the computer systems’ main memory subsystem 14.” *Id.* at 6:22–26. “[T]his greatly reduces system cost by eliminating the need for an expensive block of SRAM.” *Id.* at 6:26–29. In a preferred embodiment, MCA 200 “is an application specific integrated circuit (ASIC) for arbitrating the memory bus 110 between the various bus masters subject to the constraints each imposes to provide optimal bandwidth for each, particularly the DSP which is responsible for a significant amount of real-time signal processing.” *Id.* at 6:46–52.

2. MPEG (Ex. 1004)

MPEG describes the coded representation of video for digital storage media and specifies the decoding process for the MPEG-2 standard. Ex. 1004, 1.

3. Analysis

We are persuaded by Petitioner’s arguments and cited evidence that the combination of Bowes and MPEG teaches all of the recited limitations of claims 1, 5, 7, 13, 15, 18, 20, 24, and 25. Pet. 35–51. Petitioner contends that a person of ordinary skill in the art would have found it obvious to combine Bowes and MPEG to achieve the systems, methods, and circuits recited in the challenged claims.

To the extent *Bowes* does not explicitly describe transferring and processing data in the MPEG format, it would have been obvious to combine *Bowes* with the *MPEG Standard* (Ex. 1004), in light of the knowledge of one of ordinary skill in the art in 1996, given that the ’368 patent acknowledges that MPEG was a “coding standard currently in use.” Ex. 1001 at 1:60-61. The ’368 patent describes the MPEG standards, including MPEG-1 and

MPEG-2, as being “well accepted standards for one-way communication.” *Id.* at 2:13-14. Given *Bowes*’ aim to “support a broad range of new multimedia (i.e., voice, *video* and traditional data) applications,” Ex. 1003 at 1:32-34, as well as its use of a digital signal processor (DSP 20) for “image processing,” *id.* at 6:33-35, incorporating the known MPEG standard into *Bowes*’ system would yield predictable results. Moreover, the *MPEG Standard* describes a protocol of interpolated and predicted image frames resulting in “high compression ratio while preserving good picture quality.” Ex. 1004 at 4 (§ 0.2). Because *Bowes* acknowledges DSPs “require a large amount of bandwidth to memory” for real-time processing, Ex. 1003 at 1:51-53, an ordinary artisan would have been motivated to combine the *MPEG Standard*’s highly efficient compression to address *Bowes*’ bandwidth requirement. See Ex. 1030, Stone Decl. at ¶¶ 205-208.

Pet. 35–36. We agree with this reasoning and are persuaded that a person of ordinary skill in the art would have found it obvious to incorporate the known MPEG standard into *Bowes*’ system and that doing so would have yielded predictable results, in order to achieve “high compression ratio while preserving good picture quality” in real time. See Ex. 1030 ¶¶ 205–208.

Patent Owner responds that (1) the combination of *Bowes* and MPEG does not teach “the decoder receiving data from the main memory corresponding to at least one previously decoded image” (PO Resp. 4–25); (2) *Bowes*’ MCA 200 is not an “arbiter” that controls access to the main/system memory (*id.* at 25–30); and (3) a person of ordinary skill in the art would not have been motivated to combine *Bowes* and MPEG (*id.* at 30–39). We address each argument in turn.

a. A decoder receiving a previously decoded image

i. Whether Bowes' DSP 20 is a video decoder

Patent Owner asserts that DSP 20 disclosed in Bowes is not a “video decoder” (PO Resp. 10–18), that Bowes “does not state that the DSP is suitable for video compression and decompression” (*id.* at 11), and that “a [person of ordinary skill in the art] would recognize that a DSP used for image processing is not suitable for video compression and decompression” (*id.* at 12). *See also* Tr. 62:11–65:4 (arguing “image processing” is different than video compression and decompression).

Patent Owner is correct that, although Bowes explicitly teaches the use of DSP 20 for “image signal processing” (Ex. 1003, 6:35), Bowes does not teach explicitly the use of DSP 20 for video compression and decompression. The ground of unpatentability, however, is based upon a *modification* of the teachings regarding Bowes's DSP 20 to perform video decoding according to the MPEG Standard. Pet. 35 (“To the extent Bowes does not explicitly describe transferring and processing data in the MPEG format, it would have been obvious to combine Bowes with the MPEG Standard”), 39–40. Petitioner's expert, Dr. Stone, testifies that “[a] person of ordinary skill in the art would have understood that one application of *Bowes' DSP* is video processing according to *MPEG Standard*.” Stone Decl. ¶ 207. Bowes teaches that DSP 20 “may be an off-the-shelf DSP.” Ex. 1003, 2:21–22; *see* Reply 3–4. As evidence of what would have been known to a person of ordinary skill in the art, Dr. Stone identifies the teaching in U.S. Patent No. 5,797,028, filed September 11, 1995, that, “digital system chip 112 also preferably includes *a general purpose DSP engine 206 which is programmable to perform various functions such as*

MPEG decoding.” Stone Decl. ¶ 207 (quoting Ex. 1023, 6:20–22 (emphasis added)); *see also* Stone Reply Decl. ¶ 10 (“[A] person of skill would understand Bowes to be pointing out that any available DSP could potentially be used in the system of Bowes”) (citing Exs. 1006, 1035, 1036, 2008). Petitioner also cites, albeit with respect to another ground, evidence of a commercially available prior art DSP specifically designed for decompressing MPEG video. Pet. 52 (citing Ex. 1006 (describing the Texas Instruments MVP)). Petitioner notes correctly that “neither Patent Owner nor its expert dispute that the prior art included ‘off the shelf’ DSPs capable of video compression and decompression pursuant to the *MPEG Standard* or that a skilled artisan could have implemented the *Bowes/MPEG* combination using such prior art DSPs.” Reply 2. Thus, even assuming that “image processing” does not indicate video decompression, we are, nevertheless, persuaded that “off the shelf” DSPs existed that were capable of decompressing MPEG video, and that it was within the level of ordinary skill in the art to use, in the system of Bowes, such a DSP as DSP 20 to operate in accordance with the MPEG standard.

Patent Owner also argues that DSP 20 is not suitable for video decompression because it is a floating-point DSP. PO Resp. 12–16. Those arguments are not persuasive because they are based on an exemplary implementation provided in Bowes, namely the use of the AT&T DSP3210 (see Ex. 1001, 6:28–30 (“In the *preferred embodiment implementation*, the DSP 20 is an AT&T DSP3210 which provides an internal 8K SRAM cache.” (emphasis added))). The teachings of Bowes, however, are not limited to the use of the AT&T DSP3210 as DSP 20.

ii. *Whether a person of ordinary skill in the art would have combined Bowes and MPEG by using dedicated memory*

Patent Owner also argues that, even if a person of ordinary skill in the art had combined the teachings of Bowes and MPEG, the combination would have used a dedicated memory for the decoder. PO Resp. 18–23. Patent Owner points to the local dedicated cache of the AT&T DSP3210, an exemplary embodiment of DSP 20, and argues that a person of ordinary skill in the art “would have used a larger dedicated memory with sufficient space to store an image frame and the DSP would retrieve the previously decoded image from this dedicated memory” in order to “(a) eliminate the need for the DSP to access the memory bus during the decoding process; (b) allow other devices to access the memory bus during video decoding; (c) provide faster access by the DSP to a previously decoded image; and (d) free up space in the main memory.” *Id.* at 19.

We credit the testimony of Dr. Stone, however, that a person of ordinary skill in the art would have had no reason to use a cache to hold image data because such a system would “not guarantee that you could retrieve it” (Ex. 2006, 159:22–23), and that, even if one did, the image data “will also be backed up to main memory” (*id.* at 163:22–23). *See also* Stone Reply Decl. ¶ 32 (“[I]f you stored the data in the DSP cache, you could not reliably retrieve it from the cache because it could have been evicted from the cache when you attempted to retrieve it at a later time.”). Moreover, Patent Owner’s contention that a person of ordinary skill in the art would have had reason to modify the teachings of Bowes’s DSP 20 to include a dedicated image memory is contrary to the stated purpose of Bowes, which is to eliminate a block of dedicated SRAM.

The present invention concerns a computer architecture in which a digital signal processor (DSP) operates as a true co-processor in the computer system. That is, an arbitration technique and mechanism are implemented which allows a DSP to reside on the system's CPU or memory bus and share the memory bus resources with the other potential bus masters on the memory bus. *The scheme is implemented such that the DSP is provided with sufficient bandwidth to perform real-time digital signal processing using the system's dynamic random access memory (DRAM) and not requiring the incorporation of an expensive block of static random access memory (SRAM).* DRAM is far less expensive than SRAM and the elimination of a block of SRAM greatly reduces the cost of computer systems.

Id. at 4:49–62 (emphasis added).

Patent Owner also contends that Dr. Stone confirmed that a person of ordinary skill in the art would have used dedicated memory (PO Resp. 19 (citing Ex. 2006, 134:23–142:12), but Dr. Stone's testimony merely explains when the use of shared memory is advantageous—e.g., “if I could reduce the total amount of memory or the total volume or something like that” (Ex. 2006, 140:24–141:1)—and when it may not be advantageous—e.g., if it “causes you to use more memory than if you had dedicated memory” (*id.* at 142:8–9). See *In re Nuvasive, Inc.*, No. 2015-1670, 2016 WL 7118526, at *4 (Fed. Cir. Dec. 7, 2016) (“Our recent decisions demonstrate that the PTAB knows how to [articulate a reason why a person having ordinary skill in the art would combine prior art references]. For example, in *Nike, Inc. v. Adidas AG*, we affirmed the PTAB's finding of a motivation to combine where it determined that a PHOSITA “interested in Nishida's preference to *minimize waste in the production process* would have logically consulted the well-known practice of flat-knitting, which eliminates the cutting process altogether.” (emphasis in original, internal citations omitted)). This

testimony does not undermine Petitioner’s contentions because Patent Owner provides no evidence that, in the combination of Bowes and MPEG proposed by Petitioner, the shared memory architecture always would require the use of more memory than a dedicated memory architecture. Moreover, volume of memory is not the only factor that can make shared memory advantageous; Bowes itself teaches another advantage: “DRAM is far less expensive than SRAM and the elimination of a block of SRAM greatly reduces the cost of computer systems.” Ex. 1003, 4:61–62.

Patent Owner also argues that a person of ordinary skill in the art “would not use the bandwidth on the bus.” *Id.* at 21. This argument is unavailing, however, because it is based upon “an implementation using DSP3210” (*id.*) to which Bowes is not limited, and because Bowes explicitly describes DSP 20 reading from and writing to DRAM—i.e., the recited “main memory.”

[T]he DSP will utilize the memory bus 110 [] to read a large block memory from the DRAM 14 into its internal SRAM. Another mode of operation concerns the handling of data that has already been processed by the DSP. In many cases it will be necessary to push that data back out to the DRAM so that some other parts of the computer system can utilize it. Thus, the capability of bursting data out is a second mode of operation which may be referred to further herein as a “block write”.

Ex. 1003, 7:3–12.

iii. *Whether Bowes’ DSP 20 reads the data it stores in main memory*

Patent Owner also argues that Bowes does not teach that its DSP reads the data that it stores in main memory. PO Resp. 23–25. Specifically, Patent Owner argues that Bowes teaches a “block write” operation that “pushes data from DSP 20 back to main memory 14,” but that data is stored

for use only by “some other part of the computer system to utilize.” *Id.* at 24–25 (quoting Ex. 1003, 7:2–12). As Petitioner correctly points out, however, the cited sentence in Bowes describes “many”—but not all—cases. Reply 11; Ex. 1003, 7:6–12. Moreover, Bowes does not teach that data is pushed back out to DRAM *only*, so that some other parts of the computer system can utilize it. Therefore, Patent Owner’s conclusion is not supported by the evidence.

b. Arbiter

Patent Owner argues that the proposed combination does not disclose an arbiter that controls access to the main memory because Bowes’ “MCA (200) (identified as the arbiter) arbitrates access to the memory bus (110), not the memory subsystem (14) identified by the Petition as the main/system memory.” PO Resp. 26. Patent Owner argues that controlling access to memory is not the same as merely controlling access to a peripheral bus because (1) a device may be granted access to the bus without accessing main memory; (2) a bus arbiter grant access differently than a memory arbiter; and (3) a memory arbiter is more efficient than a bus arbiter. *Id.* at 27–30.

Patent Owner’s arguments are unpersuasive because they are not commensurate with the scope of the claims, which do not recite, for example, (1) *guaranteeing* access to the memory; (2) “a memory arbiter;” or (3) controlling access to the memory or bus *most efficiently*. See *In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (stating that limitations not appearing in the claims cannot be relied upon for patentability). As Petitioner notes correctly, “claims 1, 5, and 13 do not recite how access to the memory is controlled.” Reply 13–15. As a result, we remain persuaded

by Petitioner's contention that MCA 200, by controlling access to the bus, also controls access to the main/system memory. *See, e.g.*, Pet. 41–42; *see also* Reply 12–13 (citing Stone Reply Decl. ¶¶ 46–51, 54–61).

c. Motivation to combine

Patent Owner argues that Petitioner has not articulated sufficiently a reason to combine Bowes and MPEG, and that Bowes is incompatible with Altieri. PO Resp. 30–39. Specifically, Patent Owner argues that

A [person of ordinary skill in the art (POSA)] would not have been motivated to combine Bowes with the MPEG Standard because: (1) Bowes does not disclose a video decoder; (2) at the time of filing of the '368 Patent, a POSA would not deem using a shared memory between a decoder and another device as being advantageous; (3) the Bowes' arbitration scheme is incompatible with implementation of the MPEG Standard; and (4) the Bowes' watchdog timer renders Bowes incompatible with the MPEG Standard.

Id. at 30–31. We already have addressed arguments (1) and (2) above. With respect to point (3), Patent Owner argues that “Bowes adheres to a specific state diagram (shown in Figure 3) which allows for up to 10 time slots per arbitration cycle” (*id.* at 34), and that “[t]he Bowes arbitration cycle would prevent the bus from being available to the DSP for a number of time slices (e.g., 5 of 10 time slices in the preferred embodiment of Figure 3), and would thus likely prevent the DSP from achieving the required data transfer rate due to bus unavailability” (*id.* at 37). These arguments are not persuasive.

Figure 3 of Bowes is reproduced below.

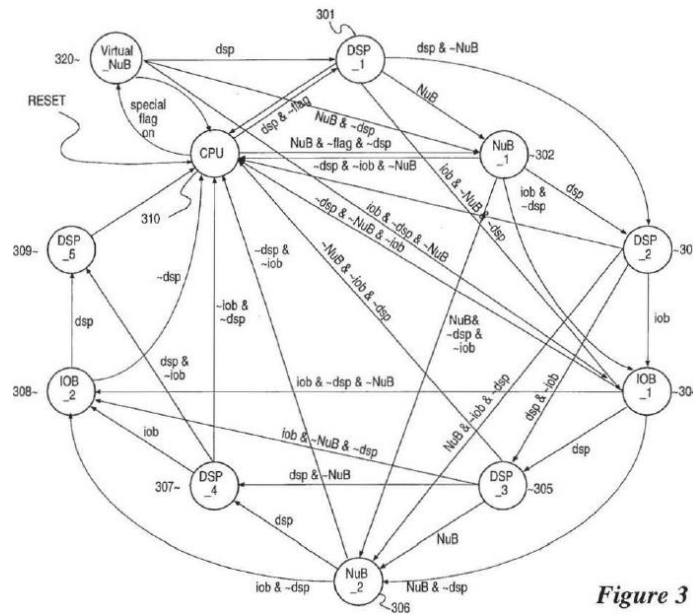


Figure 3

Ex. 1003, 3. As an initial matter, Patent Owner stops short of arguing that the arbitration cycle “would prevent” the DSP from achieving the required data transfer rate. *See* Reply 17 (arguing only that it “would *likely* prevent” the DSP from doing so, an assertion which is unsupported by expert testimony). In addition, we do not agree that the state diagram shown in Figure 3 requires stepping through all ten states. From state DSP_1, for example, the state diagram proceeds to state NuB_1 only if there is a request present from the NuBus controller (indicated in Figure 3 by the arrow labeled “NuB”). Ex. 1003, Fig. 3. If, however, there is no request present from the NuBus controller and there is a new request from the DSP (indicated by the arrow labeled “dsp & -NuB”), the state diagram proceeds to DSP_2. *Id.*; *see id.* at 8:65–9:2. Dr. Stone’s testimony is consistent with our understanding of Figure 3. Reply 17; Ex. 1032 ¶¶ 75–79. Because the arbitration scheme shown in Figure 3 could proceed directly from DSP_1 to DSP_2 to DSP_3 to DSP_4 to DSP_5 without ever entering any of the NuB

or IOB states, we disagree with Patent Owner's contention that the scheme shown in Figure 3 *necessarily* limits the DSP to only 5 of 10 time slots per arbitration cycle. Even if Patent Owner were correct about Figure 3, it is merely a preferred embodiment, and the teachings of Bowes are not limited to the preferred embodiment.

With respect to point (4), Patent Owner argues that "Bowes discloses a watchdog timer (241) that counts the number of system clocks that the DSP has owned the memory bus in a given arbitration loop before terminating the DSP's ownership of the memory bus" and that "this limitation on the DSP's access to the main memory could render a combination of Bowes with the MPEG Standard nonviable as it could prevent the DSP from decoding images in real-time." PO Resp. 37–38 (citing Ex. 1003, 9:21–38). Specifically, Patent Owner argues that "the DSP of Bowes would be unable to access previously decoded images . . . from the main memory . . . within the required time limit set by the watchdog timer (241)." *Id.* at 38.

This argument is not persuasive. Patent Owner asserts only that the limitation "could" render the combination nonviable and "could" prevent the DSP from decoding images in real-time, but does not argue that it "would" be nonviable. Patent Owner cites to paragraph 82 of the Declaration of its witness, Dr. Thornton, but that paragraph merely repeats the language in the Petition. Thornton Decl. ¶ 82. Moreover, Bowes teaches watchdog timer 241 in the context of "*Alternative DSP Operation Modes.*" Ex. 1003, 9:19 (emphasis added). Also, Petitioner counters that an entire image need not be read from main memory before the watchdog timer runs out because "the system could make multiple reads of data from the memory, each within the

time period permitted by the timer.” Reply 18 (citing Stone Reply Decl. ¶ 82). As a result, we are not persuaded that a person of ordinary skill in the art would understand Bowes’s teachings regarding watchdog timer 241 to mean that a DSP using Bowes’ arbitration scheme would not be capable of decoding video.

Finally, although not included in its list of five points, Patent Owner also argues that its assertion that combining Bowes and MPEG would not have been obvious is supported by the fact that Apple Inc., the assignee of Bowes, did not use the AT&T DSP3210 chip for processing video in its Quadra product. PO Resp. 38–39. There is no evidence, however, why Apple made the choices it made when designing the Quadra and when it made those choices. Patent Owner’s reasoning is based upon an assumption that Apple would have used the AT&T DSP3210 for video processing if the AT&T DSP3210 had been capable of video processing, but we find no support for that assumption in this record.

On the record before us, therefore, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness. *See KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

d. Dependent claims

Patent Owner does not address separately dependent claims 15, 18, 24, and 25. PO Resp. 3–39.

4. Conclusion

We are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 1, 5, 7, 13, 15, 18, 20, 24, and 25 are unpatentable as obvious over the combination of Bowes and MPEG.

*C. Claims 17, 19, and 23 — Obviousness over
Bowes, MPEG, and Rathnam*

Petitioner argues that claims 17, 19, and 23 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes, MPEG, and Rathnam. Pet. 51–55. For the reasons explained below, Petitioner has established, by a preponderance of the evidence, that claims 17, 19, and 23 would have been obvious over Bowes, MPEG, and Rathnam.

1. Rathnam (Ex. 1005)

Rathnam describes a programmable multimedia processor called TM-1. Ex. 1005, Title, Abstract. TM-1 has a high performance VLIW-CPU core with video and audio peripheral units designed to support popular multimedia applications. *Id.* at Abstract. “TM-1 easily implements popular multimedia standards such as MPEG-1 and MPEG-2, but its orientation around a powerful general-purpose CPU makes it capable of implementing a variety of multimedia algorithms, whether open or proprietary.” *Id.* at 319.

Figure 1 of Rathnam is reproduced below.

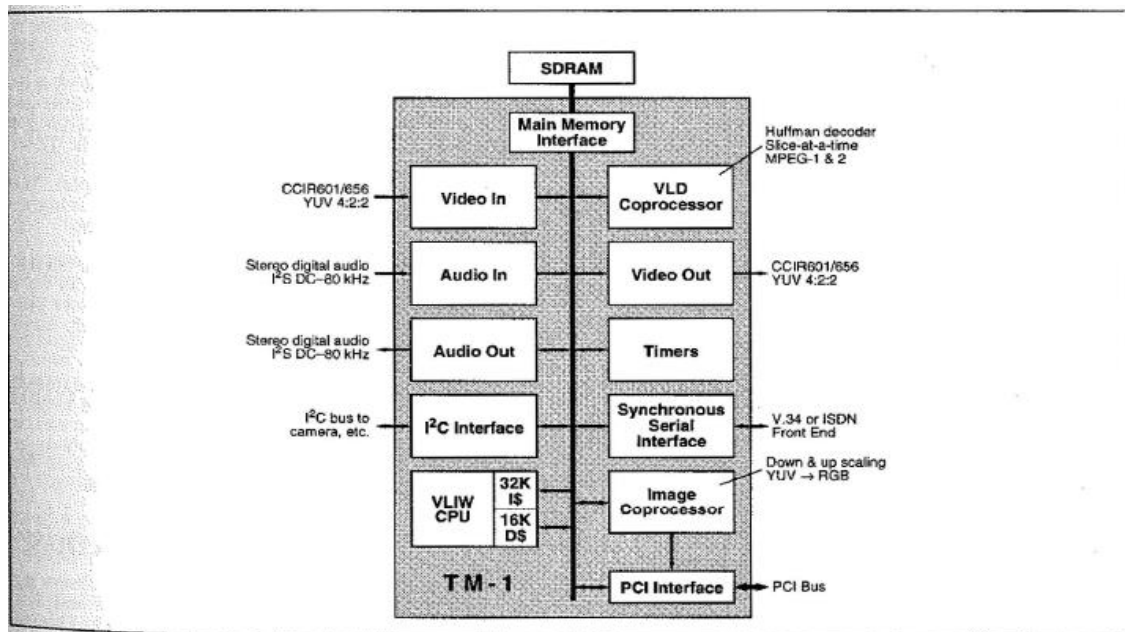


Figure 1. TM-1 block diagram.

Figure 1 shows a block diagram of TM-1. *Id.* at 320. The CPU and peripherals are time-shared and communication between units is through the SDRAM memory. *Id.* at 320–321. “The internal data bus connects all internal blocks together and provides access to internal control registers (in each on-chip peripheral units), external SDRAM, and the external PCI bus.” *Id.* at 322. “Access to the internal bus is controlled by a central arbiter, which has a request line from each potential bus master.” *Id.*

In operation, “[t]he CPU can enlist the [Image Coprocessor (ICP)] and video-in units to help with some of the straightforward, tedious tasks associated with video processing.” *Id.* at 321. “A typical mode of operation for a TM-1 system is to serve as a video-decompression engine on a PCI card in a PC.” *Id.* “Video decompression begins when the PC operating system hands the TM-1 a pointer to compressed video data in the PC’s memory” *Id.* “The TM-1 CPU fetches data from the compressed video stream via the PCI bus, decompresses frames from the video stream, and places them into local SDRAM.” *Id.* “Decompression may be aided by the VLD (variable-length decoder) unit, which implements Huffman decoding and is controlled by the TM-1 CPU.” *Id.* “The TM-1 CPU hands the VLD a pointer to a Huffman-encoded bit stream, and the VLD produces a tokenized bit stream that is very convenient for the TM-1 image decompression software to use.” *Id.* at 324.

2. Analysis

We are persuaded by Petitioner’s arguments and cited evidence that the combination of Bowes, MPEG, and Rathnam teaches each of the recited limitations of claims 17, 19, and 23. Pet. 51–55 (citing Stone Decl. ¶¶ 265–

274). Petitioner contends as follows that a person of ordinary skill in the art would have found it obvious to combine Bowes, MPEG, and Rathnam.

To the extent Patent Owner argues that *Bowes* does not disclose integrating the disclosed components on a single chip, it would have been obvious to do so in light of *Rathnam* (Ex. 1005). *Rathnam* describes a “single-chip video conferencing solution that runs all current video codecs across all common transport mechanisms.” Ex. 1005 at 19. Like *Bowes*, *Rathnam*’s chip “easily implements popular multimedia standards such as MPEG-1 and MPEG-2, but its orientation around a powerful general-purpose CPU makes it capable of implementing a variety of multimedia algorithms, whether open or proprietary.” *Id.* at 12. *Rathnam*’s single-chip implementation makes it appropriate for “low-cost, stand alone systems such as video phones to programmable, multipurpose plug-in cards for traditional computers.” *Id.* *Rathnam*’s chip “can serve as a multi-function PC enhancement vehicle.” *Id.* at 13. Like *Bowes*, *Rathnam* is designed for processing multimedia applications, but *Rathnam*’s chip “far surpasses the capabilities of fixed-function multimedia chips.” *Id.* Like *Bowes*, *Rathnam* includes “DMA-driven multimedia input/output units that operate independently and that properly format data to make processing efficient.” *Id.* The implementation of the components on a single chip, as in *Rathnam*, rather than as disparate and discrete components, as in *Bowes*, was a well-understood design choice. By the mid-1990s, single chip integration had been widely adopted and applied in multimedia processing chips. *See, e.g.*, Ex. 1006 at 1 (discussing the MVP, a video chip from Texas Instruments). In addition to enabling small packaging sizes and large-scale low-cost manufacturing, chip integration yields shorter interconnects, and thus faster communications, between electronic components. *Id.* (describing the MVP as providing “single-chip integration without slower chip-to-chip communications”). This can lead to faster, cheaper, and more capable multimedia processing chips. *Bowes* also sought to resolve these same issues. Ex. 1003 at 1:30-35, 2:42-44; Ex. 1030, Stone Dec. at ¶¶ 265-266. Accordingly, to attain these benefits, an ordinary artisan would have been motivated to apply *Rathnam*’s single-chip teachings

to Bowes. Because chip integration is a well-known technique, its use with Bowes would lead to predictable results. Thus, to the extent Bowes does not describe the integration of components on a single chip, it would have been obvious to modify Bowes in light of the well-known engineering techniques for such integration as illustrated by Rathnam. Ex. 1030, Stone Dec. at ¶¶ 265-266.

Id. at 51–53 (emphasis added). On the record before us, we agree with Petitioner and are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness. See *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Patent Owner argues that these claims are patentable based on the same reasons as the independent claims from which they depend. PO Resp. 39. As discussed above, however, we remain persuaded by Petitioner's arguments with respect to the independent claims.

3. Conclusion

We are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 17, 19, and 23 are unpatentable as obvious over the combination of Bowes, MPEG, and Rathnam.

D. Claims 2, 3, 14, and 21 — Obviousness over Bowes, MPEG, and Stearns

Petitioner argues that claims 2, 3, 14, and 21 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes, MPEG, and Stearns. Pet. 55–60. For the reasons explained below, Petitioner has established, by a preponderance of the evidence, that claims 2, 3, 14, and 21 would have been obvious over Bowes, MPEG, and Stearns.

1. Stearns (Ex. 1007)

Stearns describes a computer architecture in which MPEG accelerator functionality is integrated with a graphics accelerator. Ex. 1007, 6:14–23, Fig. 4.

2. Analysis

We are persuaded by Petitioner’s arguments and cited evidence that the combination of Bowes, MPEG, and Stearns teaches each of the recited limitations of claims 2, 3, 14, and 21. Pet. 55–60. Petitioner contends as follows that a person of ordinary skill in the art would have found it obvious to combine Bowes, MPEG, and Stearns.

To the extent Patent Owner argues that *Bowes* does not disclose directly supplying a display device with a decoded image, it would have been obvious to do so in light of the teachings of *Stearns* (Ex. 1007). See Ex. 1030, Stone Decl. at ¶¶ 275-277. *Stearns* describes embodiments in which a MPEG processor (i.e., a decoder) is directly connected to a graphics accelerator for video decompression, rather than through a PCI peripheral bus system or system memory. Ex. 1007 at FIGS. 2-3. Thus, the peripheral bus system and system memory resources that the MPEG processor would have otherwise used are freed up for alternate uses. In another embodiment, *Stearns*’ MPEG processor is simply integrated with a graphics controller. *Id.* at FIG. 4, 6:15-21. This results in, as is *Stearns*’ aim, efficient use of system resources and minimum cost. *Id.* at Abstract, 6:33-45. Accordingly, *Stearns*’ configurations “reduc[e] total system cost and mak[e] MPEG decompression more widely available even in low cost computer systems.” *Id.* at 6:40-45.

Thus, to the extent *Bowes* does not describe directly supplying a display device with a decoded image, it would have been obvious to modify *Bowes* to do so in light of *Stearns*.

Id. at 55–56 (emphasis added). On the record before us, we agree with Petitioner and are persuaded that Petitioner has provided an articulated

reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Patent Owner argues that these claims are patentable based on the same reasons as the independent claims from which they depend.

PO Resp. 40. As discussed above, however, we remain persuaded by Petitioner's arguments with respect to the independent claims.

3. Conclusion

We are persuaded that Petitioner has established, by a preponderance of the evidence that claims 2, 3, 14, and 21 are unpatentable as obvious over the combination of Bowes, MPEG, and Stearns.

E. Motion for Observations

Patent Owner also filed a Motion for Observations (Paper 36, "Obs."), to which Petitioner filed a Response (Paper 46, "Obs. Resp."). To the extent Patent Owner's Motion for Observations pertains to testimony purportedly impacting Dr. Stone's credibility, we have considered Patent Owner's observations and Petitioner's responses in rendering this Final Written Decision, and accorded Dr. Stone's testimony appropriate weight in view of Patent Owner's observations and Petitioner's response to those observations. *See* Obs. 1–2; Obs. Resp. 1–4.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has established, by a preponderance of the evidence, that claims 1–3, 5, 7, 13–15, 17–21, and 23–25 of the '368 patent under 35 U.S.C. § 103(a).

IV. ORDER

Accordingly, it is

ORDERED that claims 1–3, 5, 7, 13–15, 17–21, and 23–25 of the '368 patent are determined to be *unpatentable*;

FURTHER ORDERED that Patent Owner's Motion for Observation is taken into consideration; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2015-01500
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