

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ELBRUS INTERNATIONAL LIMITED,
Patent Owner.

Case IPR2015-01523
Patent 6,366,130

Before JUSTIN T. ARBES, JEFFREY W. ABRAHAM, and
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition seeking *inter partes* review of claims 1–3, 5–7, and 9 of U.S. Patent No. 6,366,130 B1 (Ex. 1001, “the ’130 patent”), as amended by *Inter Partes* Reexamination Certificate No. US 6,366,130 C1 (“Reexam. Cert.”). Paper 2 (“Pet.”). Elbrus International Limited (“Patent Owner”) filed a Patent Owner Preliminary Response to the Petition. Paper 8 (“Prelim. Resp.”). After considering the Petition and Preliminary Response, we determine that Petitioner has not established a reasonable likelihood of prevailing with respect to any of the challenged claims of the ’130 patent. *See* 35 U.S.C. § 314(a). Accordingly, we deny the Petition and do not institute *inter partes* review.

II. BACKGROUND

A. *Related Proceedings*

The parties identify *Cascades Computer Innovation, LLC. v. Samsung Electronics Co., Ltd.*, Case No. 1-14-cv-05691 (N.D. Ill.), currently pending, as well as pending *inter partes* review petition in Case IPR2015-01524, as also pertaining to the ’130 patent. Pet. 1–2; Paper 4, 3.

B. *The ’130 Patent*

The ’130 patent, titled “High Speed Low Power Data Transfer Scheme,” issued on April 2, 2002, with a reexamination certificate issuing on August 4, 2014. The ’130 patent is directed to a “high speed and low power [complementary metal-oxide semiconductor (CMOS)] data transfer arrangement that includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier that serves as a bus receiver.” Ex. 1001, 1:24–

28, Fig. 1. In one embodiment, the latching sense amplifier is arranged as a “cross coupled latched amplifier.” *Id.* at 1:36–38, Fig. 2.

C. Illustrative Claim

Petitioner challenges claims 1–3, 5–7, and 9. Claim 1 is the only independent claim challenged, and is reproduced below:

1. A data transfer arrangement comprising:
 - two bus drivers;
 - a voltage precharge source;
 - a differential bus coupled to the bus drivers and to the voltage precharge source; and
 - a latching sense amplifier coupled to the differential bus;wherein the latching sense amplifier comprises:
 - a first stage including a cross-coupled latch coupled to a differential data bus; and
 - an output stage coupled to an output of said first stage;wherein the output of the first stage is coupled to an input of the output stage;
- wherein the differential bus and the differential data bus are precharge to a voltage V_{pr} between V_{dd} and ground, where $V_{pr}=K \cdot V_{dd}$, and K is a precharging voltage factor.

Id. at 4:2–17.

D. References

Petitioner relies on the following references:

Ternullo, Jr. et al., U.S. Patent No. 6,052,328, filed Dec. 22, 1997, issued Apr. 18, 2000 (“Ternullo,” Ex. 1005).

Sukegawa, U.S. Patent No. 5,828,241, issued Oct. 27, 1998 (“Sukegawa,” Ex. 1006).

Hardee, U.S. Patent No. 6,249,469 B1, filed July 1, 1996, issued June 19, 2001 (“Hardee,” Ex. 1007).

E. The Asserted Grounds

Petitioner asserts the following grounds of unpatentability:

Reference(s)	Statutory Basis	Claim(s) Challenged
Ternullo	§102	1–3, 5, and 6
Ternullo and Hardee	§103	7
Ternullo and Sukegawa	§103	9

III. ANALYSIS

A. Claim Construction

Petitioner offers constructions for two terms, “latching sense amplifier” and “stage.” Pet. 9–11. Petitioner contends that “latching sense amplifier” should be construed to mean “a circuit, including a latch, that detects and amplifies signals.” *Id.* at 9. Petitioner contends that “stage” should be construed to mean “portion of a circuit.” *Id.* at 10.

Patent Owner argues that these terms are commonly used and well-known in the art, and should be given their plain and ordinary meaning. Prelim. Resp. 5–8.

In an *inter partes* review, claim terms in an unexpired patent are

interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1276–79 (Fed. Cir. 2015). We determine that no express claim construction is required for purposes of this Decision.

B. References

1. Ternullo

Ternullo discloses a “semiconductor memory device having pairs of data lines for reading and writing data signals to and from a matrix of memory cells.” Ex. 1005, 2:38–40. The device in Ternullo contains several pairs of data lines and components between the memory cells and the input/output pad. *Id.* at 3:49–52. Included among these components are data line sense amplifier (32), data line latch sense amplifier (36), and input receiver and output sense amplifier (40). *Id.* at 4:5–20, Fig. 1. Using figures and corresponding explanations in the specification, Ternullo discloses the circuitry in each component used to provide desired read and write operations. *See generally id.* at 4:5–14:26, Figs. 1–12.

2. Sukegawa

Sukegawa discloses a “signal transmission circuit which enables the distance of signal transmission . . . to be increased, while the signal delay and power consumption are reduced.” Ex. 1006, Abstract. Sukegawa teaches that “the signal is amplified and transmitted by means of the positive feedback of an intermediate amplifier circuit having input/output shared terminals.” *Id.* at 1:12–15. Sukegawa provides circuit diagrams illustrating, and corresponding descriptions in the specification describing, the specific

configuration of the various components of its transmission circuit. *See id.* at 6:35–9:50, Figs. 1–7.

3. Hardee

Hardee discloses a “sense amplifier for a very high density integrated circuit memory using CMOS technology.” Ex. 1007, Abstract. Hardee further discloses a preferred sense amplifier containing, *inter alia*, “N channel devices having their source-drain paths coupled in series.” *Id.* at 6:28–46 (referring to transistors 128, 130, 132, and 134), Fig. 5. Hardee states that these transistors “provide isolation and thereby lower the stand-by current or normal current drain of a sense amplifier where no writing operation is to occur.” *Id.* at 12:2–4.

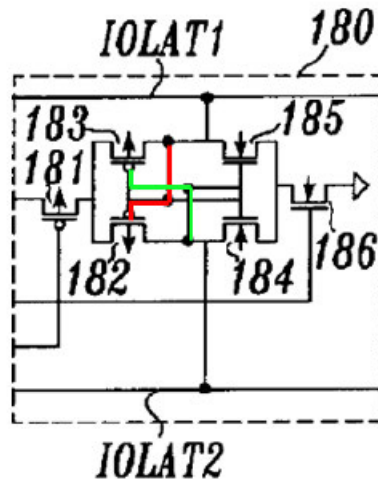
C. Analysis of Grounds of Unpatentability

1. Claims 1–3, 5, and 6

Petitioner asserts that Ternullo anticipates claims 1–3, 5, and 6. Pet. 13–43.

Independent claim 1 requires, *inter alia*, a latching sense amplifier comprising a first stage that includes a “cross-coupled latch.” Ex. 1001, 4:7–9. Petitioner contends that isolation circuit 170, latch 180, and read drivers 190 in Ternullo make up the “latching sense amplifier” recited in claim 1, and that isolation circuit 170 and latch 180 comprise the first stage of the latching sense amplifier. Pet. 20–22. Petitioner further contends that “[i]nput/output latch 180 is a cross-coupled latch because the output of a first transistor is tied to the input of a second transistor, and the output of the second transistor is tied to the input of the first transistor.” *Id.* at 23.

Petitioner relies on an annotated version of Ternullo Figure 5, reproduced below, to support its position that the first stage of the latching sense amplifier in Ternullo is a cross-coupled latch. *Id.*



Petitioner's annotated Figure 5 shows what Petitioner considers to be the first stage of the latching sense amplifier of Ternullo, including red and green lines to illustrate how the latch is cross-coupled. Petitioner notes that "[o]ne of ordinary skill in the art at the time of the alleged invention of the '130 Patent would have understood that input/output latch 180 in Fig. 5 is mistakenly drawn incorrectly," because it shows the gate of transistor 182 connected to the gate of transistor 183, and the gate of transistor 184 connected to the gate of transistor 185. *Id.* at 23 n. 7. Petitioner asserts that "Ternullo notes 'input/output latch operate[s] similarly to . . . data line latch 80 in FIG. 2' (*Ternullo* 7:63–65), and data line latch 80, as further disclosed in Ternullo Fig. 3, is drawn correctly without the transistor gates connected to each other." *Id.* (citing Ex. 1005, Fig. 3, 6:52–67; Ex. 1002 ¶ 31).

In response, Patent Owner asserts that “it is not clear that Ternullo Fig. 5 as drawn is wrong.”¹ Prelim. Resp. 15. Patent Owner contends that Petitioner fails to provide an analysis of how the circuit shown in Figure 5 would (or would not) perform, and also fails to explain why or how a person of ordinary skill in the art would have known that Figure 5 is drawn incorrectly. *Id.* at 14.

Patent Owner further asserts that Petitioner arbitrarily “corrects” Figure 5, without explaining why a person of ordinary skill in the art would have understood the disclosure of Ternullo to be “corrected” in the manner proposed by Petitioner. *Id.* at 14–15. Patent Owner acknowledges the statement in Ternullo that latch 180 in Figure 3 operates similarly to latch 80 in Figure 2, but contends that “[j]ust because two circuits might operate ‘similarly to’ each other does not mean they are wired the same.” *Id.* at 15. Patent Owner argues that in an anticipation analysis, a prior art reference must “stand on its own,” and that “[i]f it is wrong, it is wrong . . . [and i]t cannot be changed by an examiner or by a Petitioner to make it what it is not or to force it to teach what it does not teach.” *Id.* at 15–16.

Patent Owner thus argues, *inter alia*, that Ternullo fails to teach “a first stage including a cross-coupled latch coupled to a differential data bus,” and that Petitioner arbitrarily changed Figure 5 of Ternullo to create this limitation. *Id.* at 11.

¹ Patent Owner alternatively argues that if Figure 5 is drawn incorrectly, Ternullo does not enable a person of ordinary skill in the art to make or use the claimed invention, and therefore cannot anticipate claims 1–3, 5, and 6. Prelim. Resp. 16–17.

“Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim.” *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983) (citation omitted). Here, Petitioner has not demonstrated sufficiently that Ternullo discloses all elements of the claimed invention. With regard to the “cross-coupled latch” limitation, Petitioner directs us to Figure 5 of Ternullo. Pet. 20–24. Petitioner contends that a person of ordinary skill in the art would understand that Ternullo Figure 5 is drawn incorrectly, and then argues that Figure 5, as drawn “correctly,” would include a cross-coupled latch. *Id.*

Patent Owner, however, does not concede that Figure 5 is drawn incorrectly, and further argues that Petitioner and its declarant provide “no analysis of how the person of ordinary skill in the art would have chosen those two wires and not some other wires” in correcting the alleged error. Prelim. Resp. 14-15. We have reviewed the record presented, including the declaration submitted by Petitioner (Ex. 1002), and are persuaded that Petitioner has not directed us to information, from the specification of Ternullo or elsewhere, demonstrating sufficiently that a person of ordinary skill in the art would consider Petitioner’s re-drawn version of Figure 5 (as presented on page 23 of the Petition) to be the “correct” version of Figure 5. In this regard, we are persuaded by Patent Owner’s argument that just because Ternullo states that latch 180 operates similarly to latch 80 does not necessarily mean that the two latches would have been wired exactly the same way. *Id.* at 15. We additionally note that Petitioner has not directed us to any authority discussing the situation in which a party challenging the patentability of an issued patent has “corrected” alleged errors in (i.e.,

changed) a figure of an allegedly anticipatory reference, or what evidence is necessary to establish what is the “correct” redrawing of such a figure.

In view of these deficiencies, we are not persuaded that Ternullo discloses each and every limitation of independent claim 1 of the ’130 patent. Accordingly, we determine that Petitioner has not demonstrated a reasonable likelihood that independent claim 1, and therefore claims 2, 3, 5, and 6, which depend therefrom, are anticipated by Ternullo.

2. Claims 7 and 9

Petitioner contends that the subject matter of claim 7 would have been obvious over Ternullo and Hardee (Pet. 44–46), and that the subject matter of claim 9 would have been obvious over Ternullo and Sukegawa (*id.* at 46–49). Dependent claims 7 and 9 both depend from claim 1, and Petitioner does not contend that Hardee or Sukegawa cure the deficiencies identified above with regard to Ternullo. Namely, Petitioner does not contend that these references disclose a latching sense amplifier comprising a first stage that includes a “cross-coupled latch.” In view of this, Petitioner has failed to establish sufficiently that the combination of prior art references discloses each and every limitation of claims 7 and 9. For at least this reason, we determine that Petitioner has not demonstrated a reasonable likelihood that the subject matter of claims 7 and 9 would have been obvious over the cited prior art references.

IV. ORDER

For the reasons given, it is hereby
ORDERED that the Petition is denied.

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Patent 6,366,130

PETITIONER:

Steven L. Park

stevenpark@paulhastings.com

Naveen Modi

naveenmodi@paulhastings.com

PATENT OWNER:

Clifford H. Kraft

cifflaw@att.net

Joseph N. Hosteny

hosteny@hosteny.com