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Paper 8
Entered: January 29, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MAXIM INTEGRATED PRODUCTS INC.,
Petitioner,

v.

IN-DEPTH TEST LLC,
Patent Owner.

Case IPR2015-01627
Patent 6,792,373 B2

Before LINDA M. GAUDETTE, JUSTIN T. ARBES, and MICHAEL J. FITZPATRICK, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Petitioner Maxim Integrated Products Inc. filed a Petition (Paper 1, "Pet.") requesting *inter partes* review of claims 1–20 of U.S. Patent No. 6,792,373 B2 (Ex. 1001, "the '373 patent") pursuant to 35 U.S.C. § 311(a). Patent Owner In-Depth Test LLC filed a Preliminary Response (Paper 7, "Prelim. Resp.") pursuant to 35 U.S.C. § 313. We have jurisdiction under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons that follow, we have decided not to institute an *inter partes* review.

I. BACKGROUND

A. The '373 Patent[1]

The '373 patent describes a test system that executes an enhanced test process for testing components, such as "semiconductor devices on a wafer, circuit boards, packaged devices, or other electrical or optical systems," and collecting and analyzing test data. Ex. 1001, Abstract, col. 3, ll. 26–30, col. 5, ll. 18–21. Test system 100 includes tester 102 "compris[ing] any test equipment that tests components 106 and generates output data relating to the testing." *Id.* at col. 3, ll. 34–36. Tester 102 operates in conjunction with

[1] The '373 patent previously was reexamined in Reexamination Control No. 90/008,313, and all claims were confirmed. The '373 patent was challenged in Cases IPR2015-00421 and CBM2015-00060. The petitions were denied in those proceedings. The '373 patent also is being challenged in Cases IPR2015-01994 and IPR2015-01998, which are pending.

computer 108 that includes processor 110 and memory 112. *Id.* at col. 3, ll. 42–46, 59–60.

Test system 100 "uses a predetermined set of initial parameters and, if desired, information from the operator to configure the test system 100." *Id.* at col. 5, ll. 39–41. When the initial configuration process is complete, tester 102 "executes [a] test program to apply signals to connections on the components 106 and read output test data from the components 106." *Id.* at col. 6, ll. 22–25. "Each test generates at least one result for at least one of . . . components [106]." *Id.* at col. 6, ll. 32–33. The '373 patent further discloses:

> The tester 102 may perform multiple tests on each component 106 on a wafer, and each test may be repeated several times on the same component 106. Test data from the tester 102 is stored for quick access and supplemental analysis as the test data is acquired. The data may also be stored in a long-term memory for subsequent analysis and use.

Id. at col. 6, ll. 25–31. Exemplary test results may include results with statistically similar values as well as results that stray from these similar values. *Id.* at col. 6, ll. 33–37. If any of the latter results exceeds an upper or lower control limit, the tested component may be classified as a "bad part." *Id.* at col. 6, ll. 37–40. The '373 patent describes results that stray from the statistically similar values but do not exceed control limits as "outliers." *Id.* at col. 6, ll. 43–45.

Computer 108 receives the data file from tester 102 and uses supplementary data analysis element 206 to analyze the data and provide enhanced output results. *Id.* at col. 6, ll. 64–66, col. 9, ll. 17–21. Supplementary data analysis element 206 includes outlier classification element 212, which is "configured to identify and/or classify the various

outliers in the data according to selected algorithms." *Id.* at col. 14, ll. 7–14. "The outliers in the test results may be identified and analyzed for any appropriate purpose, such as to identify potentially unreliable components," "to identify various potential problems and/or improvements in the test and manufacturing processes," and "to classify the components 106 into critical/marginal/good part categories." *Id.* at col. 6, ll. 45–50, col. 14, ll. 59–61.

B. Illustrative Claims

Independent claims 1, 8, and 15 of the '373 patent recite:

> 1. A test system, comprising:
>
> a tester configured to test a component and generate test data; and
>
> a computer connected to the tester and configured to receive the test data, identify an outlier in the test data, and generate an output report including the identified outlier.
>
> 8. A data analysis system for semiconductor test data, comprising a computer system, wherein the computer system is configured to operate:
>
> a supplementary data analysis element configured to identify outliers in the semiconductor test data; and
>
> an output element configured to generate an output report including the identified outliers.
>
> 15. A method for testing semiconductors, comprising:
>
> generating test data for multiple components; and
>
> automatically identifying an outlier in the test data at run time using a computer system.

C. The Prior Art

Petitioner relies on the following prior art:

U.S. Patent No. 5,240,866, issued Aug. 31, 1993 (Ex. 1014, "Friedman");

U.S. Patent No. 5,497,381, issued Mar. 5, 1996 (Ex. 1013, "O'Donoghue");

U.S. Patent No. 6,240,329 B1, issued May 29, 2001, filed Nov. 9, 1998 (Ex. 1011, "Sun"); and

U.S. Patent No. 6,598,194 B1, issued July 22, 2003, filed Aug. 18, 2000 (Ex. 1012, "Madge").

D. The Asserted Grounds

Petitioner challenges claims 1–20 of the '373 patent on the following grounds:

Reference(s)	Basis	Claims Challenged
Sun	35 U.S.C. § 102(e)[2]	1, 2, 4, 5, 7–9, 12, and 14
Sun and O'Donoghue	35 U.S.C. § 103(a)	6, 13, 15, 16, and 18–20
Sun and Friedman	35 U.S.C. § 103(a)	3 and 10
Madge	35 U.S.C. § 102(e)	1–5, 7–12, and 14

[2] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Because the '373 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103. Also, Petitioner does not identify the particular provision of 35 U.S.C. § 102 on which it is relying for its anticipation grounds, but states that "[t]he earliest possible filing date worldwide for the application leading to the '373 Patent is May 24, 2001." Pet. 3–4. Thus, we presume that Petitioner is asserting anticipation under 35 U.S.C. § 102(e).

Reference(s)	Basis	Claims Challenged
Madge and O'Donoghue	35 U.S.C. § 103(a)	6, 13, and 15–20

E. Claim Interpretation

The Board interprets claims using the "broadest reasonable construction in light of the specification of the patent in which [they] appear[]." 37 C.F.R. § 42.100(b); *see* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015). Under this standard, we interpret claim terms using "the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the [patent] specification." *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997). We presume that claim terms have their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) ("The ordinary and customary meaning is the meaning that the term would have to a person of ordinary skill in the art in question." (internal quotation marks omitted)). A patentee, however, may rebut this presumption by acting as his own lexicographer, providing a definition of the term in the specification with "reasonable clarity, deliberateness, and precision." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). The parties provide proposed interpretations for various limitations of the claims. *See* Pet. 22–28; Prelim. Resp. 3–30. For purposes of this Decision, however, we conclude that only the term "outlier" requires interpretation.

Petitioner argues that "outlier" should be interpreted to mean "a test result that strays from a target value, but does not exceed specification limits or otherwise fail to be detected." Pet. 22–24 (citing the testimony of Jacob A. Abraham, Ph.D., Ex. 1002 ¶¶ 98–103). Patent Owner contends that the term means "a test result whose value strays from a set of test results having statistically similar values, but does not exceed control limits or otherwise fail to be detected." Prelim. Resp. 3–18. In a previous district court case, the district court interpreted the term, based on a stipulation of the parties, as "a test result that is within the upper and lower limits of the product's specifications (i.e., a test result that does not indicate a 'bad' or 'out of spec' part) but nevertheless strays from values which are statistically similar." Ex. 3001. That interpretation was adopted in Case IPR2015-00421. *See Linear Tech. Corp. v. In-Depth Test LLC*, Case IPR2015-00421 (PTAB July 21, 2015) (Paper 15).

It appears, based on their proposed interpretations, that the parties agree that the term "outlier," as used in the challenged claims, refers to a test result and that an "outlier" does not exceed certain limits or otherwise fail to be detected. The parties, however, disagree on the particular value or measurement from which a test result must stray to meet the definition of an "outlier." Petitioner contends that the test result strays from "a target value," whereas Patent Owner contends that the test result strays from "a set of test results having statistically similar values."

Upon review of the parties' arguments, we conclude that Patent Owner is correct because the Specification of the '373 patent clearly defines the term "outlier." The Specification discloses the following:

> Each test generates at least one result for at least one of the components. Referring to FIG. 9, an exemplary set of test results for a single test of multiple components comprises a first set of test results having statistically similar values and a second set of test results characterized by values that stray from the first set. Each test result may be compared to an upper test limit and a lower test limit. If a particular result for a component exceeds either limit, the component may be classified as a "bad part".
>
> Some of the test results in the second set that stray from the first set may exceed the control limits, while others do not. *For the present purposes, those test results that stray from the first set but do not exceed the control limits or otherwise fail to be detected are referred to as "outliers".*

Ex. 1001, col. 6, ll. 32–46 (emphasis added). Thus, according to the Specification, the test system may determine whether any of the second set of test results (1) exceeds an upper or lower test limit, in which case the component is considered a "bad part," or (2) strays from a first set of test results having "statistically similar values," but does not exceed control limits or otherwise fail to be detected, in which case the test result is considered an "outlier." *Id.* The above language of the Specification, in particular the portion stating that "[f]or the present purposes," certain test results are "referred to as 'outliers,'" indicates an intent by the applicant to act as his own lexicographer and explicitly define the term. *See id.*

Petitioner's arguments to the contrary are not persuasive. First, Petitioner points to another portion of the Specification stating that supplementary data analysis element 206 "may operate in any suitable manner to designate outliers, such as by comparison to selected values." *Id.* at col. 13, ll. 49–52; *see* Pet. 23. Read in context though, the cited sentence is not inconsistent with the above definition, as the immediately following

sentences refer to the calibration of sensitivity "based on selected statistical relationships for each relevant datum," where "these statistical relationships are *then* compared to a threshold or other reference point." Ex. 1001, col. 13, ll. 49–65 (emphasis added). We agree with Patent Owner that an outlier is not determined merely by comparison to a static selected value, but rather depends on some relationship to test results having statistically similar values. *See* Prelim. Resp. 12–13.

Second, Petitioner cites other statements in the Specification that "[t]he supplementary data analysis may also provide identification of critical, marginal, and good parts as defined by sensitivity parameters in a recipe configuration file," and "the outlier classification element is suitably configured to classify the components 106 into critical/marginal/good part categories, for example in conjunction with user-defined criteria." Ex. 1001, col. 14, ll. 59–col. 15, l. 1, col. 17, ll. 1–3; *see* Pet. 23. According to Petitioner, these portions indicate that the test system identifies an outlier based on "thresholds or parameters set by the user or by results of earlier tests on other like devices, regardless of any statistical analysis of the data for the devices under test." Pet. 23. As Patent Owner points out though, the cited portions pertain to part classification, which the Specification distinguishes from outlier identification. *See* Prelim. Resp. 13–14; Ex. 1001, col. 14, l. 52–col. 15, l. 67 (describing various "methods for the purpose of part and pattern classification based on identified outliers"), col. 17, ll. 1–13. The cited portions do not contradict the earlier explicit statement in the Specification describing how outliers are identified.

Third, Petitioner argues that its proposed interpretation is supported by the doctrine of claim differentiation. Pet. 23–24. Independent claim 15

recites "automatically identifying an outlier in the test data at run time using a computer system," and dependent claim 18 recites "calibrating a sensitivity for identifying the outlier in the test data using the computer system." According to Petitioner, sensitivity calibration is described in the Specification as "an example of a suitable [manner] to designate outliers," and "[t]he fact that this sensitivity calibration limitation is described as an example and appears in only dependent claims means that the threshold for calculating an outlier in the independent claims cannot require this limitation." *Id.* (citing Ex. 1001, col. 13, ll. 49–65, Fig. 4C). We are not persuaded. The step of "calibrating a sensitivity" in claim 18 further limits the "automatically identifying" step of claim 15. In other words, claim 18 requires that identification of an outlier take place, in part, by calibrating a sensitivity, but parent claim 15 does not. We see nothing in the claim language that would permit the "outlier" in claim 15 to be a test result that strays from a target value (rather than a set of test results having statistically similar values) as Petitioner suggests.

The Specification supports such a reading. The Specification describes separate steps where the system smooths the test data to assist in the identification of outliers (step 429), calculates statistics for the test data (step 430), "automatically calibrates its sensitivity to outliers based on selected statistical relationships for each relevant datum" (step 434), "define[s] relative outlier threshold limits" (step 436), and compares the output test data to "the outlier threshold limits to identify and classify the output test data as outliers" (step 438). Ex. 1001, col. 9, ll. 26–29, col. 12, ll. 31–38, col. 13, ll. 40–65, Fig. 4C. Thus, sensitivity calibration is a further limitation on the general identification of outliers as test results whose

values stray from the set of test results having statistically similar values. *See* Prelim. Resp. 14–16. The doctrine of claim differentiation does not support Petitioner's proposed interpretation.

Finally, we note a minor difference between the parties' proposed interpretations, in that Petitioner's proposed interpretation refers to an outlier as not exceeding "specification limits," whereas Patent Owner's proposed interpretation refers to "control limits." The excerpt from the Specification cited above, which explicitly defines the term "outlier," discusses "the control limits," referring to the immediately preceding discussion of the upper and lower test limits for the component being tested. Ex. 1001, col. 6, ll. 32–46. For clarity, we specify that the control limits are for the component being tested (whose test result may be designated as an outlier).

On this record, applying the broadest reasonable interpretation of the claims in light of the Specification, we interpret "outlier" to mean: a test result whose value strays from a set of test results having statistically similar values, but does not exceed the control limits specified for the tested component or otherwise fail to be detected.

II. DISCUSSION

A. Grounds Based on Sun (Claims 1–10, 12–16, and 18–20)

Petitioner, relying on the testimony of Dr. Abraham, contends that claims 1, 2, 4, 5, 7–9, 12, and 14 are anticipated by Sun under 35 U.S.C. § 102(e), claims 6, 13, 15, 16, and 18–20 are unpatentable over Sun and O'Donoghue under 35 U.S.C. § 103(a), and claims 3 and 10 are unpatentable over Sun and Friedman under 35 U.S.C. § 103(a). Pet. 28–45

(citing Ex. 1002). We are not persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted grounds for the reasons explained below.

1. Sun

Sun describes a "method for automated acceptance testing of semiconductor wafers," including "specifying a set of rules which define various device failure modes" and making a "pass/fail determination" for each semiconductor wafer being tested. Ex. 1011, col. 1, ll. 55–67. Sun discloses summary tables 300A–300D containing electrical measurements made by an electrical tester for a set of wafers 1–49. *Id.* at col. 3, ll. 1–6. Figure 3A of Sun is reproduced below.

300A

WAFER #	OUT OF SPEC	OUT OF CTRL	INVALID	50/0.9 VTN	50/0.9 IDSN	0.9N BVDSS
1	1	1	0	0.772	19.020	12.255600
1	1	2	0	0.794	18.380	8.852000
1	1	1	1	0.771	19.166	8.8965600
1	0	2	0	0.772	19.070	9.000400
1	0	1	0	0.759	19.330	8.974800
⋮	⋮	⋮	⋮	⋮	⋮	⋮
48	1	0	0	0.783	18.894	9.191600
48	0	2	0	0.777	19.128	12.212400
49	0	1	0	0.759	19.330	8.974800
49	1	2	0	0.772	19.070	9.000400
49	1	1	0	0.771	19.166	8.965600
49	1	2	0	0.794	19.380	8.852000
49	1	1	0	0.772	19.020	12.255600
AVG				0.753	19.040	9.891176
STD				0.119	1.032	1.340613
LCL				0.752	15.000	7.400000
UCL				0.850	24.000	13.600000
LSL				0.500	15.000	8.000000
USL				0.900	24.000	13.500000
VALID_LO				0.001	2.000	3.000000
VALID_HI				1.500	30.000	20.000000
% FAIL				5 %	1 %	1 %
% INVALID				0%	0%	3%
% SPREAD				16%	5%	14%

304

310

Fig. 3A

Figure 3A depicts summary table 300A showing (in the rightmost three columns) three measurements for the wafers, from which statistics are

computed (as shown in the bottom rows). *Id.* at col. 3, ll. 1–40. Summary table 300A also includes "limit values used to determine whether a wafer exhibits certain out of control, out of spec., or invalid status conditions." *Id.* at col. 3, ll. 41–44. Lower and upper control limits (LCL and UCL) "indicate the preferred range for a process," where "[t]he process is said to be in control if the measurements fall between LCL and UCL." *Id.* at col. 3, ll. 44–47. Lower and upper specification limits (LSL and USL) "indicate the required range for a process," where "[m]easurements outside of this range indicate a process that is out of spec. and will result in scrapped devices." *Id.* at col. 3, ll. 47–51. The summary tables indicate failure conditions, such as the symbol "#" for measurements that are outside LCL and UCL, and the symbol "*" for measurements that are outside LSL and USL. *Id.* at col. 4, ll. 13–25, Figs. 3B–3D.

2. Analysis

Independent claims 1, 8, and 15 recite the identification of an "outlier."[3] For each of the asserted grounds, Petitioner relies on Sun as allegedly disclosing such identification. Pet. 29–31, 41. Specifically, Petitioner argues that an "out of control" test result in Sun is an "outlier" because it is within specification limits (i.e., not a failure) but outside the LCL and UCL control thresholds, similar to the threshold determinations

[3] Claim 1 recites "a computer connected to the tester and configured to receive the test data, identify an outlier in the test data, and generate an output report including the identified outlier." Claim 8 recites "a supplementary data analysis element configured to identify outliers in the semiconductor test data." Claim 15 recites "automatically identifying an outlier in the test data at run time using a computer system."

described in the Specification of the ’373 patent. *Id.* at 30 (citing Ex. 1002 ¶ 139). Petitioner’s argument is premised on its proposed interpretation of “outlier” as being a test result that strays from *a target value*, but does not exceed specification limits or otherwise fail to be detected. As explained above, we disagree and interpret “outlier” to mean a test result whose value strays from *a set of test results having statistically similar values*, but does not exceed the control limits specified for the tested component or otherwise fail to be detected. *See supra* Section I.E. Although Sun compares test results to individual target values (LCL and UCL), Petitioner does not point to any evidence that those values are test results having statistically similar values, or even that they are based on any measured data. As Patent Owner correctly points out, Sun does not disclose how the LCL and UCL are determined, and only states that they represent the “preferred range.” *See* Prelim. Resp. 32 (citing Ex. 1011, col. 3, ll. 44–47).

Further, even if we agreed with Petitioner’s proposed interpretation of “outlier,” Petitioner’s position that an “out of control” test result in Sun must be outside the LCL-UCL range but within the LSL-USL range is incorrect based on the reference itself. Figure 3A of Sun depicts the LSL-USL range as the *same as* the LCL-UCL range for the “50/0.9 IDSN” column, and the LCL-UCL range as *outside* (not within) the LSL-USL range for the “0.9N BVDSS” column. Thus, it appears that the control and specification limits in Sun are independent of each other.

Petitioner has not shown sufficiently that Sun discloses the identification of an “outlier,” as recited in independent claims 1, 8, and 15. Accordingly, Petitioner has not demonstrated a reasonable likelihood of

prevailing on its assertion that claims 1–10, 12–16, and 18–20 are either anticipated by Sun or unpatentable over Sun and the other cited references.

B. Grounds Based on Madge (Claims 1–20)

Petitioner, relying on the testimony of Dr. Abraham, contends that claims 1–5, 7–12, and 14 are anticipated by Madge under 35 U.S.C. § 102(e), and claims 6, 13, and 15–20 are unpatentable over Madge and O'Donoghue under 35 U.S.C. § 103(a). Pet. 45–60 (citing Ex. 1002). We are not persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted grounds for the reasons explained below.

1. Madge

Madge describes a "system for determining different failure limits for various electronic characteristics of integrated circuits based on selected subsets of the integrated circuits." Ex. 1012, col. 1, ll. 6–9. According to Madge, individual integrated circuits on a wafer typically are binned as good or bad during testing, based on predetermined values for the wafer as a whole, but doing so fails to account for "differences in processing conditions across the surface of the wafer" and results in individual integrated circuits sometimes being binned improperly. *Id.* at col. 1, l. 25–col. 2, l. 14, col. 4, ll. 1–19. Madge's system takes into account the differences in processing conditions by testing a subset of integrated circuits within a particular region of the wafer. *Id.* at col. 4, l. 20–col. 7, l. 17, Figs. 4A–4B, 5A–5F. The system determines a "reference value" for an integrated circuit by "taking an average of the electrical characteristic value[s] for the nearest neighbor

integrated circuits," and then compares the tested value to the reference value to determine an "offset value." *Id.* at col. 7, ll. 18–38. The system compares the offset value to a "given amount" to determine if the integrated circuit should be binned as passing or failing. *Id.* at col. 8, ll. 29–35.

2. Analysis

For both of its asserted grounds, Petitioner relies on Madge as allegedly disclosing the identification of an "outlier," as recited in independent claims 1, 8, and 15. Pet. 45–49, 58. Petitioner cites the following disclosure from Madge:

> Although this description generally describes the process and apparatus for determining passing integrated circuits and failing integrated circuits, it is appreciated that the invention is equally applicable to assigning differing passing codes to passing integrated circuits or differing failure codes to failing integrated circuits. For example, the method and apparatus described herein can not only assign failure codes as described, but can also assign a grade of passing code, where the grade of the passing code assigned relates to the magnitude of the offset between the value of the sensed parameter for the integrated circuit and the reference value. For example, integrated circuits with relatively smaller offsets may be assigned a passing code indicating a higher passing grade, where *integrated circuits with relatively larger offsets, but not so large as to be classified as an outlier, may be assigned a passing code indicating a lower passing grade*. This may be useful, for example, in applications where differing speeds of integrated circuits are desired.

Ex. 1012, col. 9, ll. 31–48 (emphasis added); *see* Pet. 46–47. Petitioner argues that "the test data for '[integrated circuits] with relatively larger offsets'" are "outliers" as recited in the challenged claims because "they constitute acceptable (not failing) test results that are still largely offset from

the reference value, thereby 'deviat[ing] from a target value, but [] not exceed[ing] specification limits.'"[4] Pet. 13–16, 46–47 (citing Ex. 1002 ¶ 240). According to Petitioner, this should not be confused with Madge's own use of the term "outlier" as referring to a "failed or out of spec test result[]." *Id.* at 47. In other words, the claimed "outlier" that Petitioner identifies in Madge is different from what Madge calls an "outlier." Petitioner further argues that "Madge teaches that the determination of whether a test result is an outlier should be made by comparing a specific result to some norm generated by a statistical analysis of all test results in the group to which that specific result belongs," which is "the very purpose of Madge: to adjust the parameters to take into account regional variations." *Id.* (citing Ex. 1002 ¶¶ 70–72, 242).

We are not persuaded that Petitioner's analysis is sufficient to demonstrate a reasonable likelihood of prevailing for three reasons. First, Petitioner argues that Madge's reference value is a *target value* according to Petitioner's proposed interpretation of "outlier," and does not explain sufficiently how Madge identifies from test data a test result whose value strays from *a set of test results having statistically similar values*, in accordance with our interpretation above. *See id.* at 46–47; *supra* Section I.E.

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[4] Petitioner argues at other points in the Petition that "passing [integrated circuits] with larger offsets" are outliers, and that "the [waferiddq] module [in Madge] is identifying *devices* that are outside initial thresholds but within pass/fail specifications." Pet. 47, 49 (emphasis added). To the extent Petitioner is arguing that an integrated circuit itself can be an "outlier" as recited in the challenged claims, we do not agree. Our interpretation above specifies that an "outlier" is a "test result," not a device, and the claims recite identifying an outlier "in the" test data. *See supra* Section I.E.

Second, Petitioner does not explain sufficiently how Madge allegedly identifies "outlier" test results, as opposed to non-"outlier" test results. Madge determines an offset for a particular test result by comparing the test result to a reference value, and then compares the offset to a given amount to determine how the integrated circuit should be classified. Ex. 1012, col. 7, ll. 18–38, col. 8, ll. 29–35. "If the offset is greater than the given amount, then the integrated circuit is binned as failing, and if the offset is less than the given amount then the integrated circuit is binned as passing." *Id.* at col. 8, ll. 32–35. Thus, an integrated circuit is considered passing if its offset is from zero to the given amount. Within that range of offsets deemed passing, Madge discloses assigning grades of passing codes depending on the "magnitude of the offset," with integrated circuits having "relatively smaller offsets" assigned a higher passing grade and integrated circuits having "relatively larger offsets" assigned a lower passing grade. *Id.* at col. 9, ll. 31–48. No matter the grade, however, the classification is the same—the integrated circuit passes. *See* Prelim. Resp. 50–51 (arguing that part classification is different from the identification of outliers as recited in the claims). Petitioner does not explain why some test results having offsets between zero and the given amount would be considered "outliers" within the meaning of the challenged claims, but others would not. Absent further explanation as to how a person of ordinary skill in the art would have understood the disclosure of Madge, we are not persuaded that a "relatively larger" offset is a sufficient basis on which to identify an "outlier" as we interpret the term for purposes of this Decision.

Third, even if we agreed with Petitioner that test results with "relatively larger" offsets could be considered "outliers" within the meaning

of the challenged claims, Petitioner does not explain sufficiently how Madge discloses "generat[ing] an output report including the identified outlier," as recited in claim 1 and similarly recited in claim 8. Petitioner argues that Madge's output wafer map is an output report that includes identified outliers because it includes the classification (e.g., pass, fail, passing grade) for each integrated circuit. Pet. 47 (citing Ex. 1012, col. 9, ll. 14–48, Ex. 1002 ¶ 241). The alleged "outliers" according to Petitioner, however, are the test results with "relatively larger" offsets, not the passing grades assigned to those test results. *Id.* at 46–47. Thus, Petitioner has not shown sufficiently that Madge discloses the generation of an output report *including* identified outliers, as recited in independent claims 1 and 8.

Accordingly, Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 1–20 are either anticipated by Madge or unpatentable over Madge and the other cited reference.

C. Conclusion

We conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the '373 patent challenged in the Petition. Therefore, we do not institute an *inter partes* review on any of the asserted grounds as to any of the challenged claims.

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied as to all challenged claims of the '373 patent.

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