

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

LONGITUDE FLASH MEMORY SYSTEMS S.A.R.L.,
Patent Owner.

Case IPR2015-01910
Patent 6,510,488 B2

Before JUSTIN T. ARBES, GREGG I. ANDERSON, and
MICHELLE N. WORMMEESTER, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Petitioner Apple Inc. filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1, 3, 8, and 11 of U.S. Patent No. 6,510,488 B2 (Ex. 1001, “the ’488 patent”) pursuant to 35 U.S.C. § 311(a). Patent Owner Longitude Flash Memory Systems S.a.r.l. filed a Preliminary Response (Paper 9, “Prelim. Resp.”) pursuant to 35 U.S.C. § 313. We have jurisdiction under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons that follow, we have decided not to institute an *inter partes* review.

I. BACKGROUND

A. The ’488 Patent

The ’488 patent¹ describes a system for “enabling a flash memory device to employ a rapid wake-up ability, while ensuring data integrity.” Ex. 1001, col. 1, ll. 7–9. Flash memory devices require a “software translation layer that sits between the host computer’s operating system and the device low-level access routines.” *Id.* at col. 1, ll. 12–15. The translation layer handles the “mapping [of] virtual addresses into their real locations in the flash media” by using “translation tables” to convert host computer data access requests to actual flash access requests. *Id.* at col. 1, ll. 24–42. The tables may be “constructed by the software during system wake-up . . . based on control information stored within the flash device,” which can take a long time. *Id.* at col. 1, ll. 39–67. The ’488 patent

¹ The ’488 patent is asserted as a prior art reference in Case IPR2015-01911.

describes a “flash memory device [that] is able to initiate fast wake-ups when the system undergoes an orderly shut down, and reverts to regular wake-ups when the system undergoes an un-orderly shut down.” *Id.* at col. 2, ll. 37–40.

Figure 2 of the ’488 patent is reproduced below.

FIGURE 2

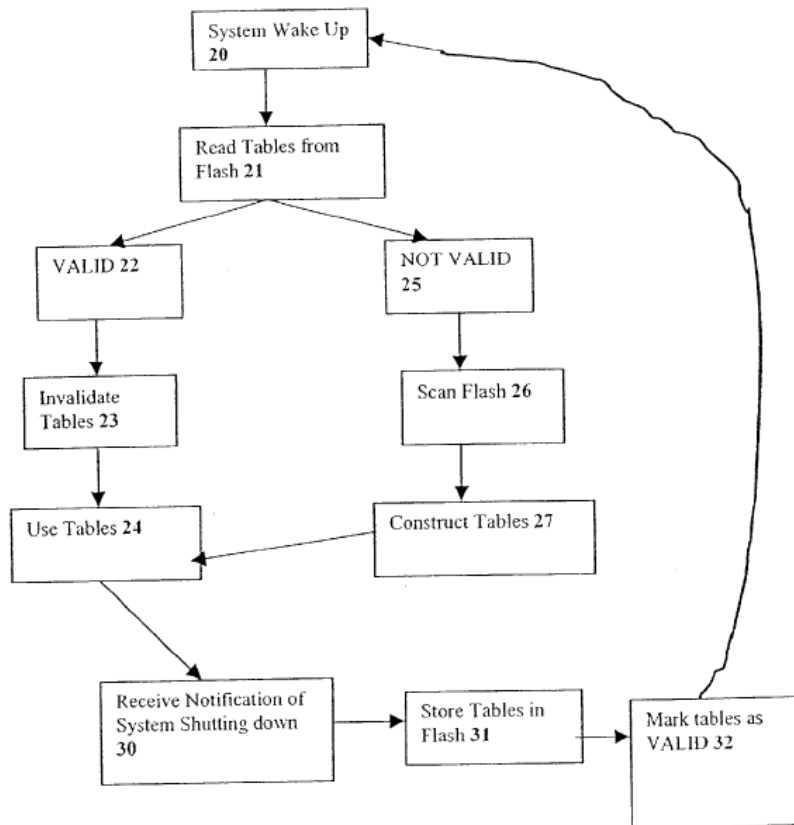


Figure 2 depicts a sequence of steps from system wake-up to shut down. During a normal shut down process, the system stores an up-to-date copy of the translation tables in the flash memory device (step 31) and marks the tables as valid (step 32). *Id.* at col. 4, ll. 36–41, 55–58. Specifically, the ’488 patent discloses marking the tables by “adding a checksum value that makes the sum of all entries equal some fixed known value or adding a validity flag to the tables.” *Id.* at col. 4, ll. 24–27. At system wake-up

(step 20), the system reads the translation tables from the flash memory device (step 21). *Id.* at col. 4, ll. 44–45. If the validity flag indicates a valid state (i.e., the translation tables are valid because of a previous normal shut down) (step 22), the system invalidates the tables “as protection against an unexpected shutdown” (step 23) and uses the tables “without having to scan the whole flash memory system” (step 24). *Id.* at col. 4, ll. 46–50.

Otherwise, if the validity flag indicates an invalid state (i.e., the translation tables are invalid because of a previous abnormal shut down) (step 25), the system scans the flash memory device (step 26), constructs updated tables (step 27), and uses them (step 24). *Id.* at col. 4, ll. 51–54.

B. Illustrative Claims

Claims 1 and 8 of the '488 patent recite:

1. A system for enabling fast wake-up of a flash memory device, such that data integrity is always maintained, comprising:

i. a hardware computing device for accessing the flash memory device;

ii. a non volatile flash memory data storage device for storing data of said hardware computing device, such that there is at least one translation table in said flash memory data storage device, for providing a translation layer with information required for converting a data access request to a flash access request;

iii. flash device low level software access routines, for providing access to content of the flash memory device;

iv. a translation layer for presenting a virtual view of said non-volatile flash memory device as a random access storage device;

v. a software mechanism selected from the group consisting of a host computer operating system and any other software program, for enabling the processing of data of said hardware computing device; and

vi. software for controlling access and use of said translation table, which enables fast wake-up of the system.

8. A method for enabling fast wake-up of a flash memory system, such that data integrity is assured, comprising the steps of:

I. When waking up:

i. Reading translation table from the flash memory system;

ii If said translation table is found to be valid

 iia.—Invalidating said table

 iib.—using said table without having to scan the whole flash memory system;

iii. Else

 iiia.—Scanning said flash memory system and constructing an updated translation table;

 iiib.—Using said table as in iib;

B. When the flash memory system is notified prior to a shutdown, storing an updated copy of said table in said flash memory system in a way that will be recognized as valid on next wake-up.

C. The Prior Art

Petitioner relies on U.S. Patent No. 5,557,777, issued Sept. 17, 1996 (Ex. 1003, “Culbert”).

D. The Asserted Grounds

Petitioner challenges claims 1, 3, 8, and 11 of the '488 patent on the following grounds:

Reference	Basis	Claims Challenged
Culbert	35 U.S.C. § 102(b) ²	1 and 3 ³
Culbert	35 U.S.C. § 103(a)	1, 3, 8, and 11

E. Claim Interpretation

The Board interprets claims using the “broadest reasonable construction in light of the specification of the patent in which [they] appear[.]” 37 C.F.R. § 42.100(b); *see In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015), *cert. granted sub nom. Cuozzo Speed Techs. LLC v. Lee*, 84 U.S.L.W. 3218 (Jan. 15, 2016) (No. 15-446). Under this standard, we interpret claim terms using “the broadest reasonable

² The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102 and 103. Because the '488 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103. Also, Petitioner asserts that Culbert “is prior art to the '488 patent under 35 U.S.C. § 102(a), (b) and (e) (pre-AIA),” but does not specify the specific provision under which its challenge is based. *See* Pet. 3, 11. Because Culbert issued more than one year before the application that issued as the '488 patent, we understand Petitioner’s challenge to be based on 35 U.S.C. § 102(b).

³ Petitioner identifies claims 1, 3, 8, and 11 as allegedly anticipated at various places in its Petition, but identifies only claims 1 and 3 in the heading on page 11 and includes substantive arguments as to claims 1 and 3 only. *See* Pet. 3, 11, 13–23. Thus, we presume the former statements to be typographical errors.

meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification.” *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997). We presume that claim terms have their ordinary and customary meaning. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016) (“Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history.”); *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (“The ordinary and customary meaning is the meaning that the term would have to a person of ordinary skill in the art in question.” (internal quotation marks omitted)). A patentee, however, may rebut this presumption by acting as his own lexicographer, providing a definition of the term in the specification with “reasonable clarity, deliberateness, and precision.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner provides a proposed interpretation for “validity flag” in claim 3, and Patent Owner responds. *See* Pet. 9–10; Prelim. Resp. 15–17. For purposes of this Decision, we conclude that no term requires interpretation at this time.

II. DISCUSSION

A. Anticipation Ground Based on Culbert (Claims 1 and 3)

Petitioner contends that claims 1 and 3 are anticipated by Culbert under 35 U.S.C. § 102(b), relying on the testimony of Darrell Long, Ph.D. Pet. 11–23 (citing Ex. 1005). We are not persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted ground for the reasons explained below.

1. Culbert

Culbert describes a power management system for a portable computer system, such as a personal digital assistant (PDA). Ex. 1003, col. 1, ll. 6–30. PDAs typically require a lengthy start up procedure, including hardware and software initialization procedures, such as “building the memory management unit (MMU) tables in system memory, enabling the MMU on the [central processing unit (CPU)], and starting the operating system.” *Id.* at col. 1, ll. 31–41. Culbert recognizes that certain start up procedures may be necessary only when the previous shut down was abnormal. *Id.* at col. 2, ll. 15–19. “If an orderly shut-down occurred previously the start-up could skip many of these steps, thereby reducing the start-up time significantly.” *Id.* at col. 2, ll. 19–22.

Figure 1 of Culbert is reproduced below.

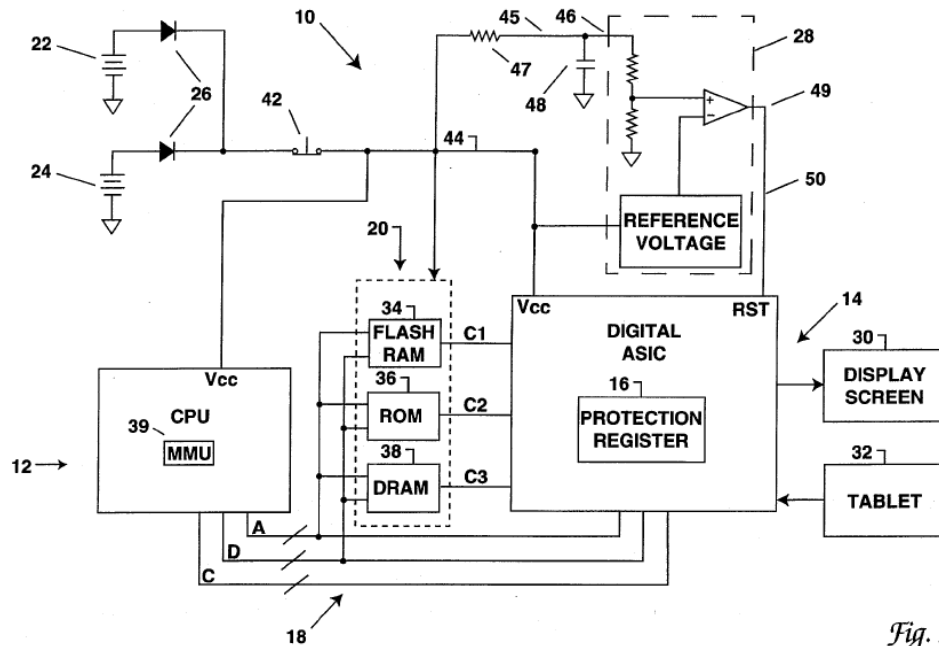


Fig. 1

Figure 1 depicts computer system 10 comprising CPU 12 with MMU 39, system controller 14 with protection register 16, and system memory 20 comprising non-volatile read/write memory 34, non-volatile read only memory (ROM) 36, and volatile read/write memory (DRAM) 38. *Id.* at col. 4, ll. 4–14. Volatile read/write memory 38 is “[t]emporary memory . . . under the control of” MMU 39. *Id.* at col. 4, ll. 31–34. Non-volatile read/write memory 34 is “flash [random-access memory (RAM)] . . . used for memory storage during a shut-down state,” and includes a “successful store register” indicating the validity of the information stored in non-volatile read/write memory 34. *Id.* at col. 4, ll. 19–39. Culbert also discloses that the protection register may be stored in non-volatile memory. *Id.* at col. 6, ll. 51–53.

During a normal shut down process, Culbert stores “critical information” in non-volatile read/write memory 34, sets the successful store register to 1 to indicate that the information was stored successfully, and sets

the protection register to 0 to indicate that a normal shut down occurred. *Id.* at col. 5, ll. 3–32, Fig. 3 (steps 64 and 68), Fig. 4 (step 86). Figure 5 of Culbert is reproduced below.

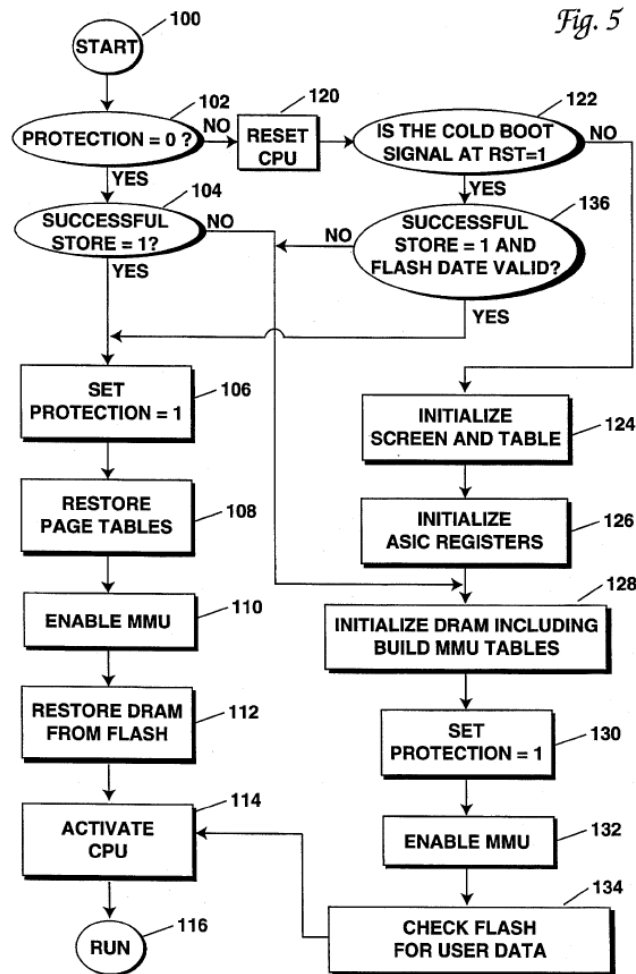


Figure 5 depicts a power-up process, where the system checks the protection register (step 102) and successful store register (step 104), and performs various actions depending on those values. *Id.* at col. 5, l. 33–col. 6, l. 22.

2. Analysis

Claim 1 recites “at least one translation table *in said flash memory data storage device*, for providing a translation layer with information required for *converting a data access request to a flash access request*”

(emphasis added). Petitioner identifies non-volatile read/write memory 34 in Culbert as a “non volatile flash memory data storage device,” and identifies the MMU tables in Culbert as “at least one translation table” stored in non-volatile read/write memory 34. Pet. 12, 14–16 (citing Ex. 1003, col. 1, ll. 38–39, col. 4, ll. 12–14, 22–24, Fig. 1). Petitioner further argues that “[p]ersons of ordinary skill would have understood that Culbert’s MMU translation table could be stored in, and indeed would have been motivated to store the table in, the flash memory 34.” *Id.* at 15.

Petitioner’s analysis does not establish a reasonable likelihood of prevailing for two reasons. First, we are not persuaded that Culbert discloses MMU tables stored in non-volatile read/write memory 34 as Petitioner contends. *See* Prelim. Resp. 19. Petitioner relies on a statement in the “Background of the Invention” section of Culbert that “[r]epresentative software start-up procedures [for a PDA] include building the memory management unit (MMU) tables in system memory, enabling the MMU on the CPU, and starting the operating system.” Ex. 1003, col. 1, ll. 38–41; *see* Pet. 12, 15. Petitioner reasons that because this portion refers to “system memory,” and system memory 20 in the disclosed embodiment includes non-volatile read/write memory 34, non-volatile read/write memory 34 must store the MMU tables. Pet. 12, 15.

When describing the exemplary embodiment of the invention, however, Culbert discloses at step 128 of Figure 5 that “the volatile read/write memory 38 is initialized, including building the MMU tables.” Ex. 1003, col. 5, ll. 58–60, col. 6, ll. 6–8. Culbert further discloses that new MMU tables “are built in the CPU,” where MMU 39 is described as “part of the CPU 12.” *Id.* at col. 3, ll. 20–26, 32–46, col. 4, ll. 32–34, Fig. 1. The

only information Culbert discloses as stored in non-volatile read/write memory 34 is the “critical” data moved to non-volatile read/write memory 34 during a normal shut down, but Culbert does not state that the “critical” data includes any MMU tables. *See id.* at col. 2, l. 65–col. 3, l. 19, col. 5, ll. 3–4; Prelim. Resp. 27. Anticipation requires that a prior art reference disclose “all of the limitations arranged or combined in the same way as recited in the claim,” *NetMoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008), but Petitioner does not point to any disclosure in Culbert of MMU tables stored in non-volatile read/write memory 34 in the context of the disclosed embodiment that Petitioner relies on for its unpatentability allegations.

Nor are Petitioner’s assertions that the MMU tables “could be” stored in non-volatile read/write memory 34, or that a person of ordinary skill in the art would have been “motivated” to store them there, sufficient to show anticipation. *See* Pet. 15. “Anticipation requires that every limitation of the claim in issue be disclosed, either expressly or under principles of inherency, in a single prior art reference,” *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1255–56 (Fed. Cir. 1989), and inherency requires a showing that the prior art “necessarily” includes the claim limitation, *MEHL/Biophile Int’l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999).

Second, even if Culbert disclosed that the MMU tables are stored in non-volatile read/write memory 34, Petitioner does not explain sufficiently how the MMU tables are for “providing a translation layer with information required for converting a data access request to a flash access request,” as recited in claim 1. *See* Pet. 14–16. We agree with Patent Owner that the

MMU tables in Culbert are used for controlling volatile read/write memory 38, not non-volatile read/write memory 34, and thus are not used to convert data access requests to “flash” access requests. See Prelim. Resp. 18–19; Ex. 1003, col. 4, ll. 31–34 (“Preferably, the temporary memory is stored as pages in the volatile read/write memory 38. Temporary memory is under the control of a memory management unit (MMU) 39, which is part of the CPU 12.”), col. 5, ll. 58–60, col. 6, ll. 6–8, 28–30. Petitioner does not point to anything in Culbert indicating that the MMU tables are used for handling requests for data stored in non-volatile read/write memory 34.

Petitioner has not shown sufficiently that Culbert discloses “at least one translation table in said flash memory data storage device, for providing a translation layer with information required for converting a data access request to a flash access request,” as recited in claim 1. Accordingly, Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claim 1, and claim 3 depending therefrom, are anticipated by Culbert.

*B. Obviousness Ground Based on Culbert
(Claims 1, 3, 8, and 11)*

Petitioner contends that claims 1, 3, 8, and 11 are unpatentable over Culbert “in view of the knowledge of persons of ordinary skill in the art at the time of the ’488 patent’s invention date” under 35 U.S.C. § 103(a), relying on the testimony of Dr. Long. Pet. 3, 23–29 (citing Ex. 1005). We are not persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted ground for the reasons explained below.

1. Claims 1 and 3

With respect to claims 1 and 3, Petitioner refers to its analysis in the anticipation ground and argues that “to the extent the Board deems certain limitations in those claims to be not anticipated by Culbert, those limitations and the claims as a whole would have been obvious to those of ordinary skill in the art at the time of the ’488 [patent] invention.” Pet. 23–24. In its anticipation ground, Petitioner contends that a person of ordinary skill in the art would have been motivated to store the MMU tables in Culbert in non-volatile read/write memory 34 because “the remaining pieces of Culbert’s system memory would be less attractive for storing the table; ROM 36 cannot be written to because it is read-only, and the volatile memory 38 would lose its information in the event of power loss.” *Id.* at 15. “Accordingly, the flash memory 34 is the most attractive location recommended by Culbert.” *Id.* Petitioner further argues that “[m]otivation would have come from Culbert’s inclusion of flash memory 34 in his system memory, and from the recognition, acknowledged by the ’488 patent itself, that an ‘obvious solution of storing the tables in flash’ . . . would have expedited the power-up of Culbert’s electronic device,” where “[e]xpeditious power-up is one of Culbert’s goals.” *Id.* at 16 (citing Ex. 1001, col. 2, l. 3, Ex. 1003, col. 2, ll. 34–36). Dr. Long repeats verbatim Petitioner’s argument in the Petition. *See id.* at 15–16; Ex. 1005 ¶¶ 57–58.

For an obviousness analysis, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). An assertion of obviousness “cannot be sustained by mere conclusory statements; instead,

there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *Id.* (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). Petitioner has not provided sufficient reasoning with a rational underpinning for why a person of ordinary skill in the art would have modified Culbert to store the MMU tables “in” non-volatile read/write memory 34, and to use the tables to provide a translation layer for “converting a data access request to a flash access request,” as recited in claim 1. As explained above, Culbert discloses that the MMU tables are used in conjunction with volatile read/write memory 38, not non-volatile read/write memory 34, and that non-volatile read/write memory 34 is used only for storing “critical” data during a normal shut down, without any disclosure that such data includes the MMU tables. *See supra* Section II.A.2; Prelim. Resp. 27–28.

Petitioner cites no other prior art reference for the missing “translation table” limitation that a person of ordinary skill in the art would have combined with Culbert, and Petitioner’s stated reasons for why a person of ordinary skill in the art would have modified Culbert are not persuasive. Petitioner’s assertion that non-volatile read/write memory 34 would be the “most attractive” location for storing the MMU tables is belied by Culbert’s disclosures that new MMU tables are “built in the CPU.” *See* Pet. 15; Ex. 1003, col. 3, ll. 20–26, 32–46. Petitioner does not address these other statements in its analysis. Also, Petitioner’s assertion that motivation to modify Culbert would have come from the fact that non-volatile read/write memory 34 is included in system memory 20 ignores the fact that system memory 20 is *optional* in Culbert. *See* Pet. 16; Prelim. Resp. 26–27; Ex. 1003, col. 4, ll. 6–7 (“[t]he computer system may also optionally include

system memory 20”). Thus, it is difficult to see why a person of ordinary skill in the art would have chosen to modify non-volatile read/write memory 34 specifically in the manner proposed by Petitioner when that memory is merely optional. Finally, assuming (without deciding) that Petitioner’s citation to the ’488 patent’s disclosure of an “obvious solution of storing the tables in the flash” is appropriate, Petitioner ignores subsequent statements in the ’488 patent explaining why doing so was problematic. *See* Pet. 16 (citing Ex. 1001, col. 2, l. 3); Prelim. Resp. 29; Ex. 1001, col. 2, ll. 6–14 (merely storing tables in the flash “will not succeed when using devices used to store data which might be changing frequently” and “[i]t is not practical to update the copy of the tables in the flash each time they change in memory”).

Based on the record presented, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claim 1, and claim 3 depending therefrom, are unpatentable over Culbert “in view of the knowledge of persons of ordinary skill in the art.” *See* Pet. 3, 23–24.

2. Claims 8 and 11

Claim 1 recites “at least one translation table in said flash memory data storage device,” and claim 8 similarly recites “[r]eading translation table from the flash memory system.” Petitioner cites steps 108–110 in Figure 5 of Culbert as allegedly teaching the limitation of claim 8. Pet. 27–28. Culbert discloses the following regarding steps 108–110: “In step 108, the page tables are restored in the MMU. Next, in step 110, the MMU is enabled.” Ex. 1003, col. 5, ll. 41–42. Petitioner does not explain sufficiently why these steps show reading any MMU tables from

non-volatile read/write memory 34. Nor are we persuaded that Culbert teaches or renders obvious storing the MMU tables in non-volatile read/write memory 34, for the reasons explained above regarding claim 1. *See supra* Sections II.A.2, II.B.1.

Based on the record presented, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claim 8, and claim 11 depending therefrom, are unpatentable over Culbert “in view of the knowledge of persons of ordinary skill in the art.” *See* Pet. 3, 24–29.

C. Conclusion

We conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the ’488 patent challenged in the Petition. Therefore, we do not institute an *inter partes* review on any of the asserted grounds as to any of the challenged claims.

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied as to all challenged claims of the ’488 patent.

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Patent 6,510,488 B2

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