

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

LONGITUDE FLASH MEMORY SYSTEMS S.A.R.L.,
Patent Owner.

Case IPR2015-01925
Patent 7,224,607 B2

Before JUSTIN T. ARBES, JO-ANNE M. KOKOSKI, and
MICHELLE N. WORMMEESTER, *Administrative Patent Judges*.

WORMMEESTER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Apple Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1, 4–10, 13, 15, 17, 18, 20–23, 25, and 27 of U.S. Patent No. 7,224,607 B2 (Ex. 1001, “the ’607 patent”). The Petition is supported by the Declaration of R. Jacob Baker, Ph.D. (Ex. 1003, “Baker Declaration”). Longitude Flash Memory Systems S.A.R.L. (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”). We have jurisdiction under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Upon consideration of the Petition, Preliminary Response, and the evidence of record, and for the reasons explained below, we determine that Petitioner has not established a reasonable likelihood that it would prevail with respect to any of the challenged claims.

B. Related Proceedings

The parties identify the following case involving the ’607 patent: *Longitude Licensing Ltd. v. Apple Inc.*, Case No. 3:14-cv-4275 (N.D. Cal., filed Sept. 23, 2014). Pet. 1; Paper 5, 1.

Petitioner further advises us that it has filed, or soon will file, petitions for *inter partes* review of twelve other patents. Pet. 1. Patent Owner identifies fifteen total petitions for *inter partes* review filed by Petitioner. Paper 5, 2.

C. The '607 Patent

The '607 patent is titled “Flash Memory Data Correction and Scrub Techniques.” In a flash memory system, memory cells are divided into blocks of cells that are simultaneously erasable. Ex. 1001, 2:45–46. A block stores at least one page of data; and a page stores at least one sector of data, the sector being an independently addressable unit of data accessed during host read and write operations. *Id.* at 2:48–53, 7:36–38. Each memory cell stores an amount of charge that represents a bit of data. *Id.* at 3:51–53. Programming, reading, or erasing one set of cells that shares a line or circuit with a second set of cells can shift the charge levels of the second set of cells, thereby corrupting the data in the second set of cells. *Id.* at 3:61–67. The '607 patent addresses this data corruption problem by describing a scrub process that restores shifting charge levels. *Id.* at 4:10–14, 4:30–34.

The scrub operation of the '607 patent may be triggered by various events, such as “[w]hen a data read, data write or erase operation occurs within a given block or other unit of the array that may disturb the charge levels[] of other units.” *Id.* at 20:13–15. After detecting a scrub trigger event, the system selects which units to scrub. *Id.* at 20:37–44, 21:20–22. Example candidates include units that share signal lines with the unit being programmed, read, or erased. *Id.* at 20:39–44. The system then reads data from the selected units and determines whether there are errors in the read data. *Id.* at 21:45–46, 22:8, 22:21–22. If there are errors, the system may defer corrective action in order to meet specific real-time operating needs. *Id.* at 22:42–46. If deferred, the system temporarily stores the read data. *Id.* at 22:54–57. Once the data are corrected, the system may rewrite the

corrected data into the original location from which the data were read or a different location. *Id.* at 23:1–4, 23:12–14.

If a block contains several pages, but data in only one or two of the pages are to be corrected, the system may use a different, designated block to temporarily store the one or two pages of corrected data, and then later consolidate the rewritten data with the uncorrected data stored in the other pages of the original block. *See id.* at 23:18–25, 32–36. For example, the system may temporarily store scrub rewrites of pages from block 2 in a designated block 3. *Id.* at 23:36–38. The system may then copy the scrub rewrites of block 2 from block 3 into an erased block 5, and also copy the remaining unchanged pages from block 2 into block 5 to consolidate the data mapped into block 2. *Id.* at 23:38–44.

D. The Challenged Claims

Petitioner challenges claims 1, 4–10, 13, 15, 17, 18, 20–23, 25, and 27 of the '607 patent. Claims 1, 7, 9, 13, and 23 are independent. Independent claim 1 is illustrative of the claimed subject matter and is reproduced below:

1. A non-volatile memory system, comprising:
 - an array of flash memory cells organized into blocks of a minimum number of memory cells that are erasable together and the blocks individually storing a plurality of units of data, and
 - a controller coupled with the memory cell array and that operates to:
 - identify when a scrub trigger event has occurred for data stored in at least one of the units of data in a first one of the blocks,
 - read the identified at least one unit of data from the first block,

correct any errors in the data read from the first block to provide corrected first block data,

write the corrected first block data as at least one unit of data to a second one of the blocks, and

thereafter copy uncorrected data units of the first block into the second block, thereby to consolidate in the second block corrected and uncorrected units of data originally of the first block.

E. Asserted Grounds of Unpatentability

Petitioner contends that the challenged claims are unpatentable based on the following grounds. Pet. 3, 16–60.

Reference(s)	Basis	Claims Challenged
So ¹	§ 103	1, 4, 13, 15, 17, 18, 20–23, 25, and 27
So and Wells ²	§ 103	5–8
So and Wong ³	§ 103	9 and 10

F. Claim Construction

We construe claims in an unexpired patent by applying the broadest reasonable interpretation in light of the specification. *See* 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015), *cert. granted sub nom. Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 890 (mem.) (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257

¹ So, U.S. Patent No. 6,151,246, issued Nov. 21, 2000 (Ex. 1005).

² Wells, U.S. Patent No. 5,740,395, issued Apr. 14, 1998 (Ex. 1019).

³ Wong, U.S. Patent No. 6,396,744 B1, issued May 28, 2002 (Ex. 1006).

(Fed. Cir. 2007). On the other hand, a “claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer” and clearly set forth a definition of the claim term in the specification. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002).

Petitioner provides proposed interpretations for various limitations of the claims, and Patent Owner responds. *See* Pet. 13–16; Prelim. Resp. 26–27. For purposes of this Decision, we conclude that no term requires interpretation.

II. ANALYSIS

A. *Obviousness over So*

Petitioner argues that claims 1, 4, 13, 15, 17, 18, 20–23, 25, and 27⁴ of the ’607 patent would have been obvious over *So*. *See* Pet. 16–32. We are unpersuaded that Petitioner’s analysis and submitted evidence have established a reasonable likelihood of Petitioner prevailing in showing the unpatentability of any of these claims.

1. *So*

So describes a refresh operation for detecting and correcting data errors in a flash memory. Ex. 1005, 1:12–15, 2:35–38, 4:17–18. The memory includes an array of rows or columns of memory cells organized into independently erasable sectors. *Id.* at 4:16–21. The array is coupled to

⁴ Petitioner identifies claims 1, 4, 13, 15, 17, 18, 20–23, 25, and 27 in its summary of the asserted grounds on page 3 of the Petition, and additionally identifies claims 7 and 8 in the heading on page 16 of the Petition. Given the substance of Petitioner’s arguments, we presume the latter to be a typographical error.

drivers and decoders that apply appropriate voltages to the memory cells for write, read, and erase operations. *Id.* at 4:27–30.

If the threshold voltage of a memory cell changes unintentionally and enters a “forbidden zone,” the data value in the memory cell also changes, thereby creating a data error. *Id.* at 1:66–2:2, 4:11–12. When the system detects an error, it marks the sector containing the error as requiring a refresh. *Id.* at 8:60–61. The refresh can be immediate, or it can be deferred until a period of inactivity in the memory. *Id.* at 8:65–9:2.

To refresh the sector containing an error, the system reads the sector and temporarily stores the read data in a buffer while the sector is erased. *Id.* at 9:6–9. The system replaces the forbidden threshold voltage with the correct threshold voltage, and then writes the corrected data back into the original sector or a different sector. *Id.* at 9:37–40, 45–49.

2. Analysis

Independent claim 1 recites a controller operable for reading a unit of data from a first block of memory cells, correcting errors in the read data, and writing the corrected data as a unit of data into a second block of memory cells. Independent claims 13 and 23 similarly recite a controller operable for reading data from a unit of a first group of memory cells, making an effort to recover data erroneously read from that unit of the first group, and writing the recovered data into a unit of a second group of memory cells. For these limitations, Petitioner directs us to where So teaches reading a sector that has been identified as requiring a refresh. Pet. 20, 25 (citing Ex. 1005, 9:6–7); *see also id.* at 30 (applying analysis of claim 1 to claim 23). In particular, So teaches reading data from that sector into a buffer, correcting the data, and then writing the corrected data from the

buffer back into the same sector or a different sector. *See* Ex. 1005, 9:33–35 (cited at Pet. 20, 21, 25), 9:48–49 (cited at Pet. 21). So also teaches writing the corrected data back into the original memory cell containing the error or a different memory cell. *Id.* at 3:5–8 (cited at Pet. 21). With respect to claim 1, Petitioner contends that So’s teaching that the corrected data may be written into “a different location” satisfies the recited step of writing the corrected data into a second block of memory cells. *See* Pet. 21. With respect to claims 13 and 23, Petitioner further contends that the recited writing steps each are “largely identical to the limitation recited in claim 1 . . . wherein the first and second groups of the instant claim[s] correspond to the first and second blocks of Claim 1.” *Id.* at 26; *see id.* at 31.

Based on the record presented, we are unpersuaded by Petitioner’s contentions. As Patent Owner points out, “nowhere in [Petitioner’s] analysis does [Petitioner] plainly state what [Petitioner] regards as a ‘block’ or a ‘unit of data.’” Prelim. Resp. 28–29; *see also id.* at 31 (“nowhere in [Petitioner’s] analysis does [Petitioner] plainly state what [Petitioner] regards as a ‘group’”). We note that the blocks in claim 1 comprise “a minimum number of memory cells that are erasable together” and “stor[e] a plurality of units of data.” Similarly, the groups in claims 13 and 23 comprise “re-programmable non-volatile memory cells” and “store a plurality of units of data.” Although So describes “floating gate transistors (memory cells) organized into independently erasable sectors,” Petitioner does not provide any explanation as to how the cited disclosures in So describe “an organization of ‘units of data’ within those sectors.” *Id.* at 29 (citing Ex. 1005, 4:21–22). In fact, Petitioner does not appear to address the recited units of data at all. *See* 35 U.S.C. § 312(a)(3) (a petition must identify,

“with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim”); 37 C.F.R. § 42.104(b) (a petition must identify “[h]ow the construed claim is unpatentable under the statutory grounds identified” and “where each element of the claim is found in the prior art,” and must explain the “relevance of the evidence to the challenge raised”); 37 C.F.R. § 42.22(a)(2) (a petition must include a “full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence”). As Petitioner does not identify specifically what it considers to be the “first one of the blocks” and “second one of the blocks,” each being “a minimum number of memory cells that are erasable together” and storing “a number of units of data,” Petitioner has not made a sufficient showing that So teaches the steps of claim 1 reciting these limitations. The same applies to the “groups” of memory cells recited in claims 13 and 23.

Further, Petitioner asserts that the corrected data in So may be “written back into . . . a different location (i.e., a second block),” but does not explain why such a location would be in a block different from the unspecified first block. See Pet. 21 (citing Ex. 1005, 3:5–8, 9:48–49, which refer only to “another memory cell” and “a different sector”); see also *id.* at 26, 31 (relying on Petitioner’s claim 1 analysis for claims 13 and 23, which similarly recite writing to a unit of “a second group of memory cells different from the first group of memory cells”). Petitioner’s asserted ground fails for this reason, as well.

In view of the foregoing, we determine that Petitioner has not established a reasonable likelihood of prevailing in showing that

independent claims 1, 13, and 23 would have been obvious over So. Claims 4, 15, 17, 18, 20–22, 25, and 27 depend from claims 1, 13, or 23.

Accordingly, we also determine that Petitioner has not established a reasonable likelihood of prevailing in showing that these dependent claims would have been obvious over So.

B. Obviousness over So and Wells

Petitioner argues that claims 5–8 of the '607 patent would have been obvious over So and Wells. *See* Pet. 32–42. We are unpersuaded that Petitioner's analysis and submitted evidence have established a reasonable likelihood of Petitioner prevailing in showing the unpatentability of any of these claims.

1. Wells

Wells describes a clean-up method for a flash memory, which entails “increasing available free memory by erasing dirty sectors on a block-by-block basis.” Ex. 1019, 1:7–9, 3:43–46. To begin the clean-up method, the system selects a focus block for clean-up. *Id.* at 2:3–4. Next, the system allocates memory within a destination block to store data. *Id.* at 2:4–6. The system then copies data from the focus block into the destination block. *Id.* at 2:6–7. Afterward, the system erases the focus block, thereby converting dirty sectors into free memory. *Id.* at 2:7–9.

A “clean-up is achieved using a finite number of states, or algorithms, which are chained together.” *Id.* at 22:59–61. As reads and writes to the flash memory occur in bursts, the system may perform clean-up as a

background process, executing each clean-up state when the host is inactive. *Id.* at 22:52–66.

2. *Claims 5 and 6*

Claims 5 and 6 depend from claim 1. As discussed above, we determine that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of claim 1 based on So. For the same reasons, we also determine that Petitioner has not established a reasonable likelihood of prevailing in showing the unpatentability of dependent claims 5 and 6 based on So and Wells.

3. *Claims 7 and 8*

Independent claim 7 recites a controller operable for reading data stored in a flash memory array, temporarily storing information about the read data, and “*thereafter* determin[ing] whether there are any errors in the [read] data” (emphasis added). For the recited reading limitation, Petitioner directs us to where So teaches reading a sector that has been identified as requiring a refresh. Pet. 38 (applying analysis of claim 1 to claim 7); see Ex. 1005, 9:6–7. For the recited temporarily storing limitation, Petitioner directs us to where So further teaches reading data from that identified sector into a buffer, correcting the data, and then writing the corrected data from the buffer back into the memory array. Pet. 38 (citing Ex. 1005, 9:32–35). Finally, for the recited determining limitation, Petitioner directs us to where So teaches detecting errors in stored data. *Id.* at 41 (citing Ex. 1005, 2:58–63). As to the sequential aspect of the recited limitations, Petitioner appears to contend that a person of ordinary skill in the art would understand that “correcting the data [in So] would first involve a determination of whether there are any errors in the data read from that sector.” *Id.*

Patent Owner asserts that “[Petitioner] fails to address the ‘thereafter’ aspect of the limitation in any meaningful detail.” Prelim. Resp. 35. We agree with Patent Owner. Although the step of correcting data in So may occur after the step of determining whether there are errors in the data, claim 7 requires that the step of determining whether there are any errors in the data occur *after* the step of temporarily storing information about the data (due to the use of the term “thereafter” in the claim). See *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1342–43 (Fed. Cir. 2001) (although not ordinarily interpreted to require a particular order, the steps of a method must be performed in sequence where the claim expressly recites an order or “implicitly require[s] that they be performed in the order written”). As discussed above, Petitioner cites disclosures in So that teach identifying a sector that requires a refresh, and then storing data from that identified sector in a buffer. See Ex. 1005, 9:6–7 (cited at Pet. 20), 9:33–35 (cited at Pet. 38, 41); see also Pet. 38 (applying analysis of claim 1 to claim 7). We note that “a sector containing a data error can be marked as requiring a refresh” in So. Ex. 1005, 8:48–50 (cited at Pet. 41); see also *id.* at 2:63–66 (“The error detection circuit detects errors in threshold voltages of memory cells storing data and in response to detecting an error, signals that a memory cell or a memory sector requires a refresh operation.”). Thus, the cited disclosures in So teach detecting a data error in a sector (determining whether there are any errors in the data) *before* storing the data from that sector in a buffer (temporarily storing information about the data).

In view of the foregoing, we determine that Petitioner has not established a reasonable likelihood of prevailing in showing that independent claim 7 would have been obvious over So and Wells. Claim 8

depends from claim 7. Accordingly, we also determine that Petitioner has not established a reasonable likelihood of prevailing in showing that this dependent claim would have been obvious over So and Wells.

C. Obviousness over So and Wong

Petitioner argues that claims 9 and 10 of the '607 patent would have been obvious over So and Wong. *See* Pet. 43–60. We are unpersuaded that Petitioner's analysis and submitted evidence have established a reasonable likelihood of Petitioner prevailing in showing the unpatentability of these claims.

1. Wong

Wong describes a refresh operation for a flash memory that includes multiple arrays of memory cells. Ex. 1006, 1:56–58, 4:9–14. The system performs the refresh operation before the threshold voltages of the memory cells have drifted (or shifted) to a level that causes a data error. *Id.* at 1:61–64. In one embodiment, the system reads data from a sector, stores the data in a refresh buffer, erases the sector, and rewrites the data from the refresh buffer back into the erased sector. *Id.* at 6:43–46. According to Wong, “re-writing eliminates any previous threshold voltage drift, and the threshold voltages remain in tight ranges around the target threshold voltage values.” *Id.* at 6:50–53.

In another embodiment, the system uses an I/O (input/output) buffer and a refresh buffer to allow for data input or output during a refresh operation. *Id.* at 6:57–59. Thus, while the system is refreshing a sector in one array, other arrays without any sectors being refreshed can be accessed through the I/O buffer. *Id.* at 6:59–62. To allow for access to the array

containing the sector being refreshed, the system can interrupt the refresh operation unless the access is to the sector being refreshed after erasing of that sector has begun. *Id.* at 6:62–66. If such erasing has begun, access can be redirected to the refresh buffer, which contains the data read from the sector being erased. *Id.* at 6:67–7:2.

2. Analysis

Independent claim 9 recites a controller operable for reading data stored in a flash memory cell array and “*thereafter* determin[ing] whether there are any errors in the [read] data” (emphasis added). For the recited reading limitation, Petitioner directs us to where So teaches reading a sector that has been identified as requiring a refresh. Pet. 51 (citing Ex. 1005, 9:6–7). For the recited determining limitation, Petitioner directs us to where So further teaches reading data from that identified sector into a buffer, correcting the data, and then writing the corrected data from the buffer back into the memory array. *Id.* at 52 (citing Ex. 1005, 9:33–35). Petitioner also directs us to where So teaches detecting errors in stored data. *Id.* (citing Ex. 1005, 2:58–63). As to the sequential aspect of the recited limitations, Petitioner appears to contend that a person of ordinary skill in the art would understand that “correcting the data [in So] would first involve a determination of whether there are any errors in the data read from that sector.” *Id.*

Based on the record presented, we are unpersuaded by Petitioner’s contentions. Claim 9 requires that the step of determining whether there are any errors in the data occur *after* the step of reading the data. Importantly, though, the disclosure in So that Petitioner relies on as allegedly teaching the reading step describes reading a sector that requires a refresh. See Ex. 1005,

9:6–7 (cited at Pet. 51). That reading takes place *after* it has been determined that the data has an error. So discloses that “a sector containing a data error can be marked as requiring a refresh.” *Id.* at 8:48–50 (cited at Pet. 52); *see also id.* at 2:63–66 (“The error detection circuit detects errors in threshold voltages of memory cells storing data and in response to detecting an error, signals that a memory cell or a memory sector requires a refresh operation.”). Thus, as argued in the Petition, Petitioner has not shown sufficiently that reading a sector that requires a refresh takes place before determining whether there are any errors in the data.

In view of the foregoing, we determine that Petitioner has not established a reasonable likelihood of prevailing in showing that independent claim 9 would have been obvious over So and Wong. Claim 10 depends from claim 9. Accordingly, we also determine that Petitioner has not established a reasonable likelihood of prevailing in showing that this dependent claim would have been obvious over So and Wong.

III. CONCLUSION

For the foregoing reasons, we are not persuaded that Petitioner has demonstrated a reasonable likelihood that it would prevail on any of the challenges to patentability of the ’607 patent set forth in the Petition.

IV. ORDER

For the reasons given, it is

ORDERED that the Petition is *denied* as to all challenged claims, and no trial is instituted.

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