

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SHARP CORPORATION
and
SHARP ELECTRONICS CORPORATION,
Petitioner,

v.

Wi-Lan Inc.,
Patent Owner.

Case IPR2016-00010
Patent 6,359,654 B1

Before JONI Y. CHANG, BRIAN J. McNAMARA, and GARTH D. BAER,
Administrative Patent Judges.

BAER, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Sharp Corporation and Sharp Electronics Corporation (collectively, “Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–5, 8, and 9 (the “challenged claims”) of U.S. Patent No. 6,359,654 B1 (Ex. 1001, “the ’654 patent”). Patent Owner Wi-LAN Inc. (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”), and a statutory disclaimer under 37 C.F.R. § 1.321(a) disclaiming claim 8 (Ex. 2004).

Pursuant to 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless “the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Because “[n]o *inter partes* review will be instituted based on disclaimed claims,” 37 C.F.R. § 42.107(e), we do not institute *inter partes* review as to claim 8. In addition, having considered the Petition and the Preliminary Response, we determine that there is not a reasonable likelihood that Petitioner would prevail in establishing that claims 1–5 and 9 of the ’645 patent are unpatentable. Therefore, we decline to institute an *inter partes* review.

I. BACKGROUND

A. RELATED PROCEEDINGS

The parties assert that the ’654 patent is involved in multiple proceedings including *Wi-LAN Inc. v. LG Electronics, Inc.*, 2-13-cv-04895 (D.N.J. 2013); *Wi-LAN USA, Inc. v. Toshiba Corp.*, 1-12-cv-23744 (S.D. Fla 2012); *Wi-LAN v. LG Electronics, Inc.*, 1-12-cv-23611 (S.D. Fla 2012); *Wi-LAN Inc. v. Sharp Corp.*, 1-15-cv-00379 (D. Del. 2015); *Wi-LAN Inc. v. VIZIO, Inc.*, 1-15-cv-00788 (D. Del. 2015); *Wi-LAN Inc. v. ON Corp US*,

Inc., 1-15-cv-00786 (D. Del. 2015); *Wi-LAN Inc. v. Sansui America, Inc.*, 1-15-cv-00787 (D. Del. 2015). Paper 4, 2; Paper 6, 2.

B. THE '654 PATENT

The '654 patent relates to displaying interlaced video on noninterlaced monitors. Ex. 1001, 1:12–15. Petitioner provides the following overview:

An interlaced system raster is one where two . . . interleaved fields are used to scan out one video frame. . . . [A]ll of the odd numbered lines are contained in one field, while the other field is made up of all the even numbered lines. . . . Each field is drawn on the screen consecutively-first one field, then the other.

Pet. 4–5 (quoting Ex. 1004, 63–64) (formatting omitted). As the '654 patent explains, “[f]or truly interlaced video the odd and even fields are from positions one half a line different (vertically) in the original image.” Ex. 1001, 5:2–4. In contrast, with noninterlaced displays like computer monitors, “each line of the display is refreshed during a scan in order from top to bottom.” Pet. 5.

The claimed method addresses problems associated with displaying interlaced fields on a noninterlaced display. The method includes an adjustment step for “correction of the positional offset of the two interlaced video fields.” See Ex. 1001, 5:13–14. The method also includes a scaling step, in which source lines are replicated, dropped, or otherwise interpolated to fit the current noninterlaced display. See *id.* at 4:51–53; see also *id.* at 1:34–36 (describing doubling each line to scale up a 240-line input to fit a 480 line display). Figure 4 of the '654 patent is reproduced below.

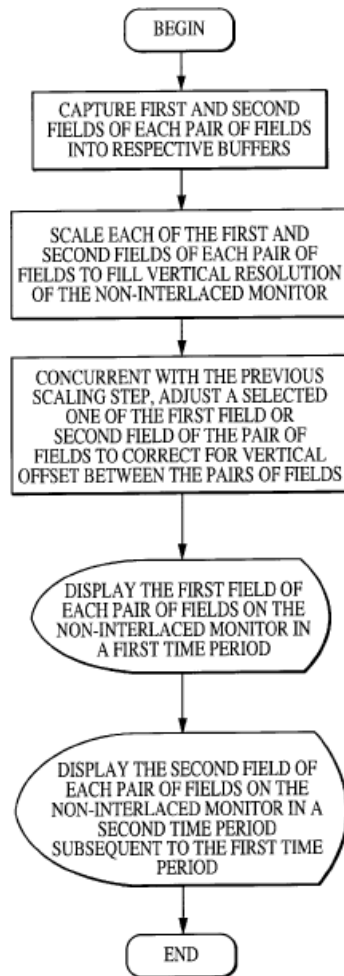


FIGURE 4

The '654 patent describes Figure 4 as “a flowchart of one embodiment of the present inventive method for displaying interlaced video data on a noninterlaced monitor.” *Id.* at 4:16–18.

C. ILLUSTRATIVE CLAIM

Of the challenged claims, only claim 1 (reproduced below) is independent.

1. A method for displaying interlaced video data on a non-interlaced monitor, the interlaced video data comprising a plurality of paired fields, each pair of fields being vertically offset relative to each other by one-half of a field line spacing

distance, each field comprising a plurality of lines of video data, the method including:

- (a) capturing a first field and a second field of each pair of fields into respective buffers;
- (b) scaling each of the first field and second field of each pair of fields to all vertical resolution of the non-interlaced monitor;
- (c) adjusting one of the first field or second field of the pair of fields to substantially correct for the vertical offset between the pairs of fields, where said adjusting is performed concurrently with said scaling;
- (d) displaying the first field of each pair of fields on the non-interlaced monitor in a first time period; and
- (e) displaying the second field of each pair of fields on the non-interlaced monitor in a second time period subsequent to the first time period.

Id. at 10:46–67.

D. ASSERTED PRIOR ART

The Petition relies on the following prior art references, as well as a supporting Declaration from Dr. Cliff Reader (Ex. 1008): U.S. Patent No. 5,181,110 (issued Jan. 19, 1993) (Ex. 1002, “Katsumata”); U.S. Patent No. 4,701,793 (issued Oct. 20, 1987) (Ex. 1003, “Hollander”); and Keith Jack, *Video Demystified – A Handbook for the Digital Engineer*, 1993 (Ex. 1004, “Jack”).

E. ASSERTED GROUNDS OF UNPATENTABILITY

Petitioner asserts the following grounds of unpatentability. Pet. 4.

References	Basis	Challenged Claim(s)
Katsumata and Hollander	§ 103(a)	1, 2, 4, 5, 8, and 9
Katsumata, Hollander, and Jack	§ 103(a)	3

II. ANALYSIS

A. CLAIM CONSTRUCTION

The Board interprets claims using the “broadest reasonable construction in light of the specification of the patent in which [they] appear[.]” 37 C.F.R. § 42.100(b). We presume a claim term carries its “ordinary and customary meaning,” which is “the meaning that the term would have to a person of ordinary skill in the art in question” at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. Concurrently

Claims 1–5 and 9 require scaling a pair of fields and adjusting one of a pair of fields, “where said adjusting is performed *concurrently* with said scaling.” Ex. 1001, 10:59–60 (emphasis added). Petitioner asserts that we should construe “concurrently” as “taking place within a common interval of time,” and cites as its only support a 1994 *IBM Dictionary of Computing*, “which defines ‘concurrent’ as ‘pertaining to processes that take place within a common interval of time during which they may have to alternately share common resources.’” Pet. 14 (quoting Ex. 1009 and recognizing that “[n]either the specification nor the prosecution history offer[s] much assistance”).

We do not agree with Petitioner’s proposed construction because it is unreasonably broad. Petitioner’s construction does not account adequately for the second part of the cited definition, which addresses the need to share common resources. *See* Ex. 1009, 133. Petitioner’s construction would leave the disputed term meaningless, as almost any two events could be characterized as concurrent simply by identifying a sufficiently long

common interval. See *Merck & Co. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) (“A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.”). For example, two minute-long processes taking place during the same week would be concurrent under Petitioner’s proffered construction, even if one ends days before the other begins.

Based on the current record and for purposes of this Decision, we construe “concurrently” consistent with the 1996 *IEEE Standard Dictionary of Electrical and Electronics Terms*: “pertaining to the occurrence of two or more activities within the same time interval, achieved either by interleaving the activities or by simultaneous execution.” Ex. 2005, 196–97. Consistent with the term’s ordinary meaning, our construction requires concurrent processes to have some overlap—one cannot complete before the other begins.

We conclude no additional express claim construction is necessary for our determination of whether to institute *inter partes* review of the challenged claims. See *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

B. ASSERTED PRIOR ART

1. Katsumata (Ex. 1002)

Katsumata discloses “a video signal processing circuit suitable for enlarging and displaying video signals,” including interlaced signals. Ex. 1002, 1:13–14, 2:63–66; see *id.* at Abstract. Katsumata’s Fig. 1 is reproduced below:

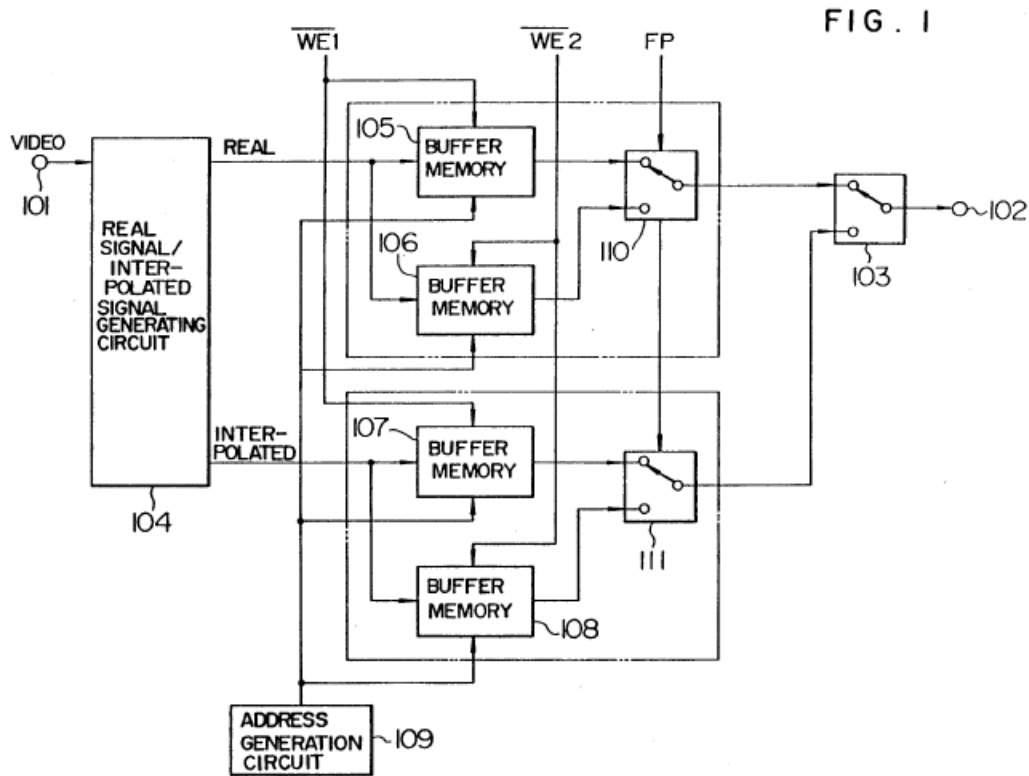
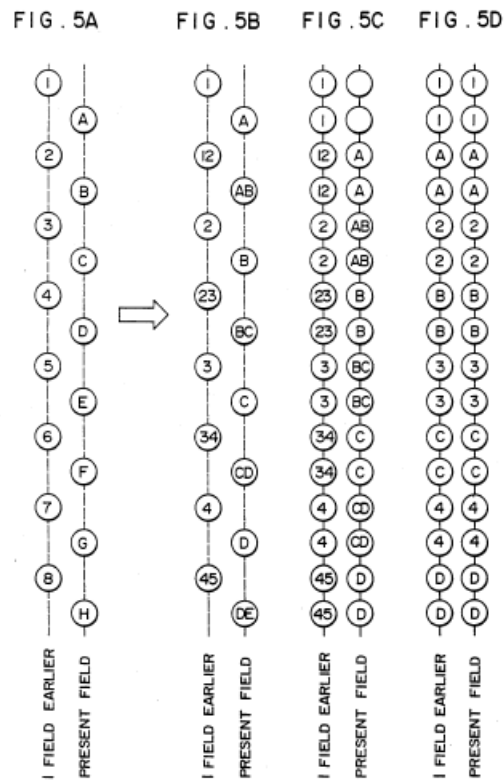


Fig. 1 is “a block diagram showing an embodiment of the invention.” *Id.* at 5:34–35. The ’654 patent describes that “[i]n FIG. 1, 101 designates an input terminal for a video signal, 102 an output terminal for an image, . . . 105 and 106 first and second buffer memories for storing the real scanning line signal, [and] 107 and 108 third and fourth buffer memories for storing the interpolated scanning line signal.” *Id.* at 6:9–18.

Katsumata’s Figs. 5A–5D are reproduced below:



The '654 patent describes Figs. 5A–5D as the “scanning line structures” that result when the disclosed interpolated scanning line preparation circuit “prepares new scanning lines from adjacent scanning line signals so as to carry out enlargement.” *Id.* at 4:37–41. Particularly relevant to this case, Fig. 5C depicts “a scanning line structure for progressive [non-interlaced] scan display.” *Id.* at 4:46–47. In addition, Katsumata discloses “repetitively read[ing]” input line signals to “effect enlargement in the vertical direction.” *Id.* at 6:53–54.

2. Hollander (Ex. 1003)

Hollander discloses techniques for video processing, including to “increase the field rate of displayed images for reducing the visibility of flicker” on interlaced television displays. Ex. 1003, 1:6–9. Particularly relevant to this case, Hollander teaches producing an output video signal in

which “[a] blank line is produced because one more line is read from the memory than was stored.” *Id.* at 4:43–45.

3. Jack (Ex. 1004)

Jack is a textbook about video processing. Pet. 4. The ’654 patent cites Jack in the Background of the Invention section for teaching video processing techniques including scaling via “line doubling” and de-interlacing via “Field Merging.” Ex. 1001, 1:37, 1:46 (citing Ex. 1004, 332–33).

C. ANALYSIS

Petitioner contends that, at the time of the invention, claims 1, 2, 4, 5, and 9 would have been obvious over Katsumata and Hollander, and claim 3 would have been obvious over Katsumata, Hollander, and Jack. Pet. 16–36. Claims 1–5 and 9 require scaling a pair of fields and adjusting one of the pair, “where said adjusting is performed *concurrently* with said scaling.” Ex. 1001, 10:59–60 (emphasis added). As outlined above, under our construction of “concurrently,” there must be some overlap in performing the adjusting and scaling steps, either by interleaving or by simultaneous execution. We find Petitioner has not made an adequate showing that the asserted references teach or suggest performing the scaling and adjusting steps “concurrently.”

Petitioner argues that “Katsumata and Hollander disclose that the scaling and the adjusting occur concurrently at read-out.” Pet. 26. According to Petitioner, combining Katsumata’s scaling with Hollander’s adjusting would result in concurrent processes because the scaling and adjusting processes both involve reading out stored input signals from memory. *See id.* at 26 (citing Ex. 1008, 35). Although Petitioner’s assertion

might suffice under its proffered construction for concurrently, it does not under ours. Petitioner has not identified any teaching in Katsumata or Hollander relating the timing of the adjusting and scaling steps to one another. *See* Pet. 26–27. Even if, as Petitioner asserts, the references disclose both scaling and adjusting in part through reading signals from memory, those teachings are not precise enough to suggest that combining the references would result in the two processes overlapping. Petitioner has not offered any explanation why it would have been obvious to one skilled in the art to perform the scaling and adjusting processes sequentially instead of concurrently (though still at read out). *See id.* at 25–27. Because claims 1–5 and 9 require scaling and adjusting “performed concurrently,” we find, on the current record, Petitioner has not set forth a reasonable likelihood of succeeding on obviousness. Accordingly, we decline to institute an *inter partes* review.

III. ORDER

Accordingly, it is:

ORDERED that the Petition is denied as to the challenged claims of the '654 patent; and

FURTHER ORDERED that no *inter partes* review is instituted.

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