

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LIMESTONE MEMORY SYSTEMS LLC,
Patent Owner.

Case IPR2016-00093
Patent 5,805,504

Before BART A. GERSTENBLITH, BARBARA A. PARVIS,
ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

GERSTENBLITH, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. *Background*

Micron Technology, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting institution of *inter partes* review of claims 1 and 2 of U.S. Patent No. 5,805,504 (Ex. 1001, “the ’504 patent”). Limestone Memory Systems LLC (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

Under 35 U.S.C. § 314(a), an *inter partes* review may be instituted only if “the information presented in the [P]etition . . . and any [Preliminary Response] . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the [P]etition.” See 37 C.F.R. § 42.108(c).

For the reasons given below, on this record, Petitioner has not established a reasonable likelihood of prevailing with respect to at least one challenged claim of the ’504 patent. Accordingly, we *deny* the Petition and decline to institute an *inter partes* review of the ’504 patent.

B. *Related Proceedings*

The parties indicate that the ’504 patent is asserted in several matters pending before the United States District Court for the Central District of California, including *Limestone Mem. Sys. LLC v. Micron Tech., Inc.*, No. 8:15-cv-00278 (C.D. Cal.), against Petitioner. Pet. 2–3; Paper 5, 2–4. Petitioner also challenges other patents assigned to Patent Owner in IPR2016-00094, IPR2016-00095, IPR2016-00096, and IPR2016-00097. Pet. 3; Paper 5, 2.

C. Real Parties-in-Interest

The Petition identifies Micron Technology, Inc. as the sole real party-in-interest. Pet. 2. Patent Owner identifies Limestone Memory Systems LLC and Acacia Research Group LLC as the real parties-in-interest. Paper 5, 1.

D. The References

Petitioner relies on the following references:

U.S. Patent No. 5,581,746, issued December 3, 1996 (Ex. 1005, “Watanabe”); and

Japanese Unexamined Patent Application Publication H4-326138, published November 16, 1992 (Ex. 1006, “Iwama”¹).

E. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1 and 2 of the ’504 patent on the following ground:

References	Basis	Claims challenged
Watanabe and Iwama	§ 103(a)	1 and 2

Petitioner supports its challenge with a Declaration by Dr. R. Jacob Baker, dated January 21, 2016 (Ex. 1003, “the Baker Declaration”).

¹ Petitioner relies upon a certified English-language translation of the Japanese Unexamined Patent Application Publication. The English translation, certification, and untranslated Japanese application were filed together as Exhibit 1006. Citations herein are to the English-language translation, which we refer to as “Iwama.”

F. The '504 Patent

The '504 patent is directed to “[a] synchronous semiconductor memory with a burst transfer mode . . . comprised of a plurality of memory cell subarrays.” Ex. 1001 [57]. The '504 patent explains that “[a] plurality of internal data buses operates with an input buffer circuit to transfer data in parallel to the subarrays. The input buffer circuit includes a shift register composed of a first and second cascade connected registers.” *Id.*

Figure 5 of the '504 patent is shown below:

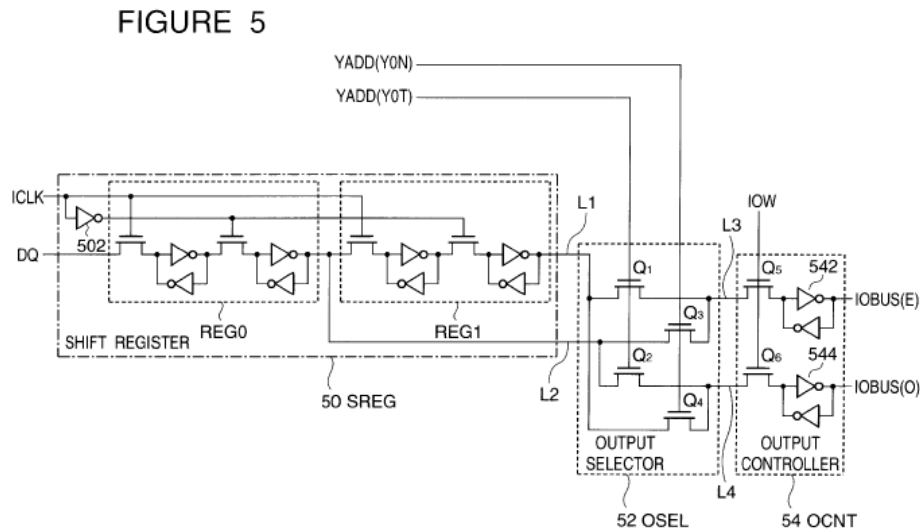


Figure 5 of the '504 patent “is a circuit diagram of the data-in buffer incorporated in the semiconductor memory shown in FIG. 4.” *Id.* at 6:51–52.

The '504 patent provides the following with respect to Figure 5:

[T]he data-in buffer 46 includes a shift register (SREG) 50 receiving the external data DQ in synchronism with the internal clock ICLK and having two parallel output lines L1 and L2, a register output selector (OSEL) 52 receiving the two parallel output lines L1 and L2, and having two parallel output lines L3 and L4, and a buffer output controller (OCNT) 54 receiving the two parallel output lines L3 and having a pair of output

connected to the internal data buses IOBUS(E) and IOBUS(O), respectively.

The shift register 50 includes a pair of cascade-connected registers REG0 and REG1 which are controlled by the internal clock ICLK and an inverted clock obtained from an output of an inverter 502 receiving the internal clock ICLK. The first register REG0 has an input receiving the external data DQ and an output connected to an input of the second register REG1 and the output line L2. The second register REG1 has an output connected to the output line L1. With this arrangement, the shift register 50 latches the external data DQ in synchronism with the internal clock ICLK, and the data latched in the shift register 50 is shifted in synchronism with the internal clock ICLK. Accordingly, the first register REG0 holds a last input data, and the second register REG1 holds the data inputted before the last input data by one cycle.

The register output selector 52 includes a first transfer gate transistor Q1 connected between the line L1 and the line L3, a second transfer gate transistor Q2 connected between the line L2 and the line L4, a third transfer gate transistor Q3 connected between the line L2 and the line L3, and a fourth transfer gate transistor Q4 connected between the line L1 and the line L4. The transfer gate transistors Q1 and Q2 are controlled by the least significant bit YADD(Y0T) of the internal column address signal YADD, and the transfer gate transistors Q3 and Q4 are controlled by an inverted signal YADD(Y0N) of the least significant bit YADD(Y0T) of the internal column address signal YADD. Thus, one of the lines L1 and L2 is distributed toward the even-numbered column address internal data bus IOBUS(E), and the other is distributed toward the odd-numbered column address internal data bus IOBUS(O).

...

The output controller 54 includes a transfer gate transistor Q5 having one end connected to the line L3, another transfer gate transistor Q6 having one end connected to the line L4, a latch 542 having an input connected to the other end of the transfer gate transistor Q5 and an output connected to the internal data bus IOBUS(E), and another latch 544 having an input connected to the other end of the transfer gate transistor Q6 and an output

connected to the internal data bus IOBUS(O). The transfer gate transistors Q5 and Q6 are controlled in common by the data-in buffer output control signal IOW. Thus, under control of the data-in buffer output control signal IOW, the output controller 54 outputs the parallel two bits of data distributed and outputted from the register output selector 52, to the internal data bus IOBUS (E) and IOBUS(O), simultaneously and in parallel, respectively.

Id. at 9:30–10:34.

G. Illustrative Claim

Claim 1 is the sole independent claim challenged in this proceeding. Claim 2 depends from claim 1. Independent claim 1 is illustrative of the claimed subject matter and is reproduced below:

1. A semiconductor memory having a burst mode transfer function, comprising:
 - a plurality of memory cell sub-arrays which are accessible in parallel and simultaneously;
 - a plurality of internal data buses for inputting and outputting data to and from said plurality of memory cell sub-arrays, in parallel; and
 - an input buffer circuit receiving an external data signals continuously and sequentially in time in synchronism with a reference clock signal, for converting said receiving serial data into a parallel data under control of an external command signal and an external address signal, so as to distribute said parallel data to said plurality of internal data buses,
 - the input buffer circuit including a shift register circuit composed of a plurality of cascade-connected registers and for latching and shifting said external data signals only in response to said reference clock signal, said cascade-connected registers outputting, in parallel, said data latched in said respective registers, and a register output selecting means receiving said data signals outputted in parallel from said cascade-connected registers, for distributing said received parallel data signals, in

parallel, to said plurality of internal data buses in accordance with said external address signal.

Ex. 1001, 16:57–17:14.

II. CLAIM CONSTRUCTION

Although Petitioner and Patent Owner present proposed constructions for several claim terms, no terms require express construction for purposes of this Decision.

III. ANALYSIS

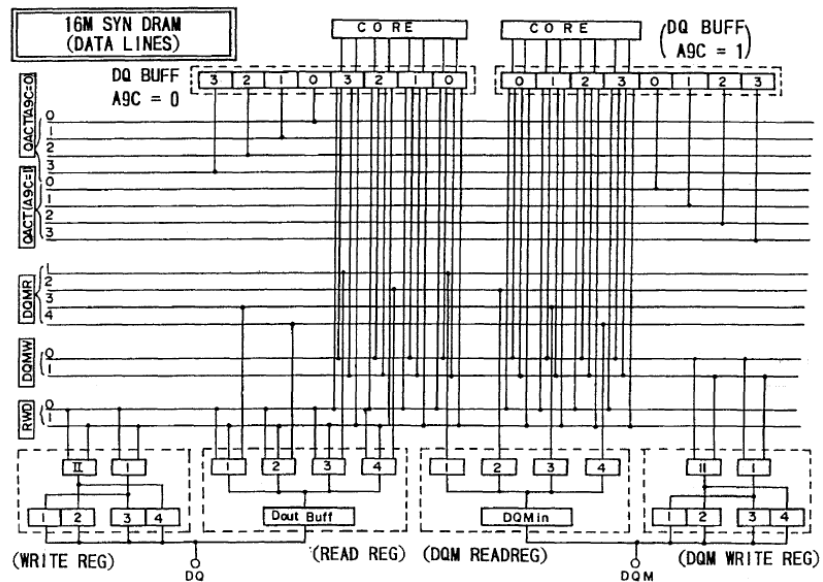
A. *Obviousness of Claims 1 and 2 over Watanabe and Iwama*

Petitioner asserts that a combination of the teachings of Watanabe and Iwama would have rendered the subject matter of claims 1 and 2 obvious to one of ordinary skill in the art at the time of the invention. Pet. 23–58. The Petition includes discussion identifying where Watanabe and Iwama allegedly teach or suggest the elements of each challenged claim. *Id.*

1. *Watanabe*

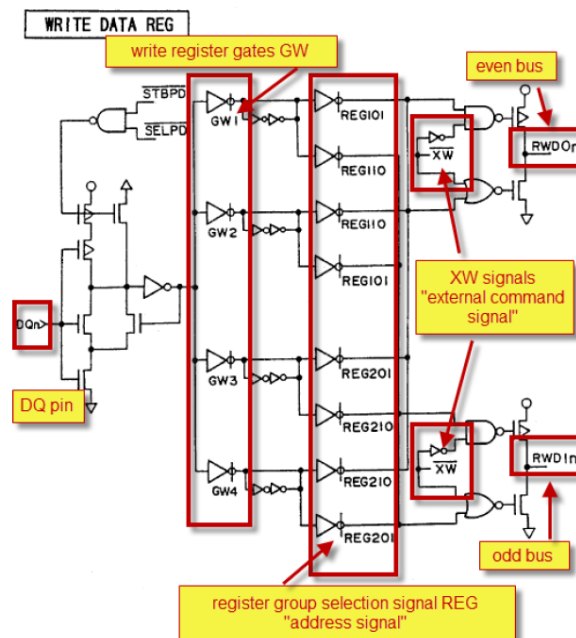
Watanabe is directed to “a synchronous LSI (large scale integrated circuit) device, and more specifically to a synchronous LSI memory device suitable for use with a high speed . . . [computer].” Ex. 1005, 1:5–8. As explained by Petitioner, “Watanabe describes a system for taking in serial data, converting that data to parallel data using a series of gates, and distributing that data in synchronism to a plurality of internal buses based on an address and clock signal after receiving a write enable signal.” Pet. 21.

Watanabe's Figure 2 is shown below:



Watanabe’s Figure 2 illustrates “a circuit diagram showing a configuration of data lines of a 16M synchronous DRAM [dynamic random access memory].” *Id.* at 3:25–26. The DRAM circuit shown in Figure 2 includes a write register circuit (“WRITE REG”). *Id.* at Fig. 2.

Watanabe's Figure 28, shown below with annotations by Petitioner, provides more detail of the WRITE REG circuit:



MICRON-1005, Watanabe at Figure 28 (annotated).

Watanabe's Figure 28 "is a circuit diagram showing a write data register circuit," annotated by Petitioner to identify a "DQ pin," "write register gates GW," "register group selection signal REG 'address signal,'" "XW signals 'external command signal,'" "even bus," and "odd bus." Pet. 20. Data received by the WRITE REG circuit is "outputted to RWD lines 2 bits by 2 bits." *Id.* at 29:25–29 (Table 15).

Watanabe teaches that "'latency' used in the specification and the drawings implies the number of clocks between when a command is inputted and when data are transferred in a synchronous device, which is widely employed in the field of the synchronous device." Ex. 1005, 6:55–59.

Watanabe states:

To achieve the above-mentioned operation, it is necessary to access to the core section within a time of two cycles. In this case, a register is required to temporarily store the data read from the core section under consideration of the latency. To cope with the latency of "4", the register requires 4 bit length at its minimum. By doing this, it is possible to prevent the interference

between the present data and the new data read by the core section during the data outputting operation.

Further, since the column address can be changed for each two cycles, only 2-bit data of the 4-bit data can be a serial data at the same column address. Accordingly, it is necessary to handle a 4-bit register as two 2-bit registers; that is, data registers of 2+2 bit configuration are required.

As shown in the read mode and write mode operation explanation of Table 15, in the read mode, two system lines between the CLK signal and the RWD lines and between the RWD lines and the data registers are operated in pipeline mode to cope with a high speed operation. Therefore, it is necessary that the read-mode register interleaves the register group two bits by two bits to transfer data from the RWD lines to the registers for each two cycles. The data are outputted from the first register in sequence.

In contrast with this, *in the write mode, it is necessary that the write-mode register interleaves the register group two bits by two bits to transfer data from the registers to the RWD lines for each two cycles.* To execute the write operation at high speed, DQM lines are used. That is, before the write data are outputted to the RWD lines, the DQM lines are write-disabled. However, immediately when the write data are outputted, the DQM lines are write-enabled, so that it is possible to execute the write operation at high speed without delaying the write operation.

FIG. 2 shows the circuit for realizing the above-mentioned operation at high speed.

Id. at 11:5–40 (emphases added).

2. Iwama

Iwama is directed to “a memory IC [integrated circuit] and aims to provide a high-speed memory IC capable of performing read and write at a high speed.” Ex. 1006 [57]. Iwama’s Figure 2 is shown below:

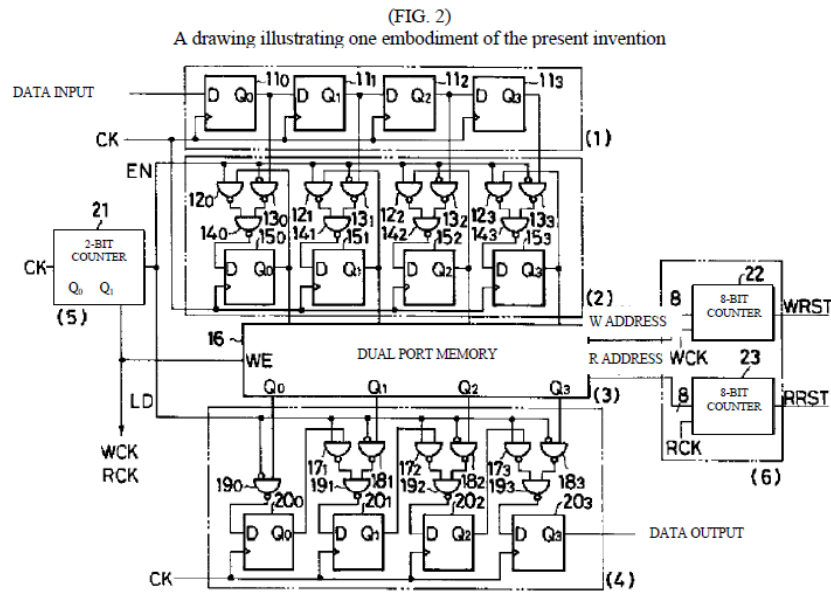


FIG. 2 . . . illustrat[es] one embodiment . . . where 11₀-11₃ are flip-flops (FF) that constitute the shift register; 12₀-12₃, 13₀-13₃, and 14₀-14₃ are NAND gates that constitute the switch part; 15₀-15₃ are flip-flops (FF) for latching data; 16 is a dual port memory that constitutes the storage part; 17₀-17₃, 18₀-18₃, and 19₀-19₃ are NAND gates that constitute the switch part; 20₀-20₃ are flip-flops (FF) that constitute the shift register; 21 is a 2-bit counter that generates various timing signals; and 22 and 23 are 8-bit counters that generate read-out addresses.

Id. ¶ 10.

Iwama explains that “FF 11₀-11₃ forms a serial-parallel conversion shift register and generates the output converted to the parallel data to the output Q₁-Q₃ by shifting the data input comprising a serial signal in response to a clock CK.” *Id.* ¶ 12. “The output Q₀-Q₃ of the serial-parallel conversion shift register sequentially is shifted one bit at a time.” *Id.* Additionally, Iwama teaches:

NAND gates 12₀-12₃, 13₀-13₃, and 14₀-14₃ and FF 15₀-15₃ forms a parallel data latch, incorporates the output Q₀-Q₃ of the serial-parallel conversion shift register to FF 15₀-15₃ at each 4 bits in response to the enable (EN) signal, and generates a

parallel data of 4-bit length to the output Q₀-Q₃ of FF 15₀-15₃ by holding the incorporated data for 3-bit period.

Id. ¶ 13.

3. *Level of Ordinary Skill in the Art*

With regard to the level of ordinary skill in the art, we determine that no express finding is necessary, on this record, and that the level of ordinary skill in the art is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

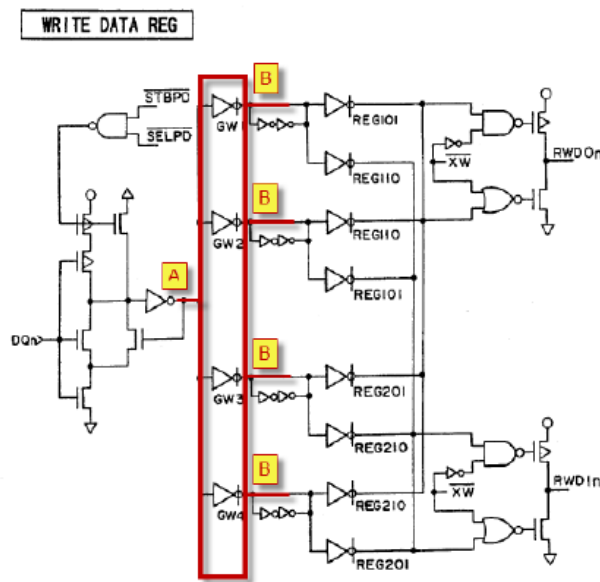
4. *Discussion*

Petitioner contends that Watanabe “discloses all the features of claims 1 and 2 except for an input buffer comprising a plurality of cascade-connected registers. Iwama discloses such an input buffer.”

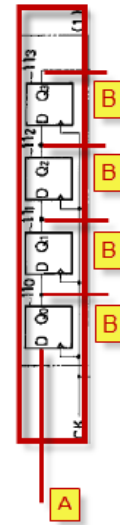
Pet. 23. Specifically, Petitioner explains that “Watanabe’s write register gates GW are not cascade-connected registers. Iwama, however, discloses cascade-connected registers for creating parallel data.” *Id.* at 37.

Petitioner’s argues that it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to substitute Iwama’s cascade-connected shift registers for Watanabe’s write register gates GW. *Id.*

Petitioner provides the following illustration of Watanabe’s Figure 28 alongside a portion of Iwama’s Figure 2, each of which includes Petitioner’s annotations, as shown below:



MICRON-1005,
Watanabe at Fig. 28 (annotated).



MICRON-1006,
Iwama at Fig. 2 (annotated).

Id. at 38. Watanabe’s Figure 28 and a portion of Iwama’s Figure 2, rotated 90°, are shown, including Petitioner’s annotations to include data input along lines “A” and output along lines “B.” *Id.*

Petitioner provides three reasons as to why one of ordinary skill in the art would have combined the teachings of Watanabe and Iwama. We discuss each.

First, Petitioner contends that Watanabe and Iwama are directed to the same function and result—“converting serial data to parallel data”—and, thus, “a person of ordinary skill in the art would have been motivated based on the nature of the problem to be solved to adapt Watanabe to include Iwama’s cascade shift registers to achieve the desired function and result.”

Id. at 25. Patent Owner asserts that Petitioner’s argument is “better characterized as [a] contention[] that the references are analogous art than as a rational underpinning for the proposed combination.” Prelim. Resp. 45 (citations omitted).

We agree with Patent Owner that Petitioner's first argument is more suited to the question of whether the references are analogous to the claimed invention, as opposed to providing a reason with a rational underpinning as to why one of ordinary skill in the art would have sought to combine the teachings therein. Accordingly, Petitioner's first proposed reason for modification, standing alone, is not persuasive on the current record.

Second, Petitioner contends that "it would have been a simple substitution of two components that would have had a predictable result – *i.e.*, a circuit that would convert serial data to parallel data." Pet. 25. Petitioner asserts that "[i]t was well within the skill of a person of ordinary skill in the art to substitute in Iwama's cascade registers for Watanabe's write register gates (GW). . . . [and that it] represent[s] a combination of known elements according to their established functions to achieve predictable results." *Id.* at 26 (citing Ex. 1003 ¶ 49). Petitioner argues that "[t]he data being treated is the same and the operation is discrete from other operations occurring in the circuit – *i.e.*, the substitution would not interference with other operations." *Id.* (citing Ex. 1003 ¶ 49).

Patent Owner contends that substituting Iwama's registers for Watanabe's GW gates would render Watanabe's circuit inoperable. Prelim. Resp. 38–43. In particular, Patent Owner argues that Iwama's registers "are arranged to receive four bits of serially provided data and output a single bit on four parallel lines utilize[ing] four sequential flip-flops 11₀-11₃ that constitute a shift register." *Id.* at 42–43 (citing Ex. 1006 ¶ 10). In contrast, Patent Owner asserts that Watanabe's GW gates "are arranged within an input buffer circuit that receives four bits of serial data and outputs the data two bits by two bits in parallel on two internal bus lines (RWD0n and

RWD1n).” *Id.* at 39 (citing Ex. 1005, 29:26–27). Patent Owner emphasizes that Watanabe requires that the four bits of data be divided into two bit chunks to accommodate the latency of its core section. *Id.* at 40. Patent Owner points to the following statement in Watanabe:

Further, since the column address can be changed for each two cycles, **only** 2-bit data of the 4-bit data can be a serial data at the same column address. Accordingly, **it is necessary** to handle a 4-bit register as two 2-bit registers; that is, data registers of 2+2 bit configuration are required.

Id. (quoting Ex. 1005, 11:15–19 (emphases added by Patent Owner)). According to Patent Owner, Watanabe’s “REG1xx and REG2xx gates illustrated in . . . figure 28 are not designed to receive or process four simultaneous data signals – which would be the result of the Petition’s proposed combination.” *Id.* (citing Ex. 1005, 12:20–23, 27:6).

As discussed above, Petitioner contends that its proposed substitution “would not interfere with other operations” and cites to paragraph 49 of the Baker Declaration for support. Pet. 26 (citing Ex. 1003 ¶ 49). Paragraph 49 of the Baker Declaration generally supports Petitioner’s argument regarding the proposed substitution, even going as far as to testify that “[s]uch a simple substitution is reflected in the figures above.” Ex. 1003 ¶ 49 (referring to the same figure, reproduced above, from page 38 of the Petition). Neither that paragraph, however, nor, from our independent review, any other testimony by Dr. Baker, supports directly Petitioner’s argument that the proposed substitution “would not interfere with other operations.” Additionally, Petitioner’s argument based on Watanabe’s Figure 28 and Iwama’s Figure 2, reproduced above, and Dr. Baker’s testimony that “[s]uch a simple substitution is reflected in the figures above,” fails to account for making any additional modifications to Watanabe, instead choosing to rely on a

picture-is-worth-a-thousand-words approach. For the reasons discussed above, Petitioner has not provided sufficient support for its argument that the substitution is so simple that it would not interfere with other operations and has not explained the other modifications that would be needed to accommodate the change. Accordingly, Petitioner's argument that this is nothing more than a simple substitution is not persuasive on the current record.

Third, Petitioner contends that "the decision to use the circuit proposed by Watanabe or the circuit proposed by Iwama is nothing more than a design choice." Pet. 27 (citing Ex. 1003 ¶¶ 50–52). Petitioner asserts that it was well known, and conventional, that cascade registers could be used to convert serial data to parallel data because "[b]oth circuits address the same problem and provide the same result – parallel data for a burst operation." *Id.* (citations omitted).

Patent Owner asserts that "[a]lthough shift registers were known structures at the time of the invention, that does not mean that it was a simple 'design choice' to use write register tri-state buffers instead of a shift register at the particular portion of Watanabe's circuit." Prelim. Resp. 47. Patent Owner points out that Watanabe "discloses a cascading shift register for other portions of the disclosed circuit relating to the timing signals – not the data – and uses that structure to generate timing pulses GW used to control the input buffer circuit." *Id.* (citing Ex. 1005, Figs. 15, 25). Patent Owner contends that "Watanabe's data circuit has a fundamentally different structure that specifically does not work with the shift register as proposed in the Petition. . . . [and t]he shift register is actually an unavailable choice," in light of Patent Owner's argument regarding inoperability. *Id.*

In light of our discussion above with respect to Petitioner's proposed substitution, we do not find Petitioner's design-choice argument persuasive. Additionally, as explained by Patent Owner, Watanabe's GW gates function in a manner conducive to Watanabe's latency goals. On this record, Petitioner has not explained sufficiently how Iwama's cascade register would similarly function to accomplish the same specific result, beyond simply converting serial data to parallel data.

Claim 2 depends from claim 1, and Petitioner relies upon the same arguments discussed above with respect to the common elements of the claims. *See, e.g.*, Pet. 49. Accordingly, we determine that, based on the record before us, Petitioner has not shown a reasonable likelihood that it would prevail in establishing the unpatentability of claims 1 and 2 as obvious over the combination of Watanabe and Iwama.

IV. CONCLUSION

For the foregoing reasons, on this record, Petitioner has not established a reasonable likelihood of prevailing with respect to claims 1 or 2 of the '504 patent.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied* as to the challenged claims of the '504 patent; and

FURTHER ORDERED that no *inter partes* review is instituted.

IPR2016-00093
Patent 5,805,504

For PETITIONER:

Jeremy Jason Lang
Justin L. Constant
WEIL, GOTSHAL & MANGES LLP
jason.lang@weil.com
justin.constant@weil.com

PATENT OWNER:

Nicholas T. Peters
Paul B. Henkelmann
FITCH EVEN TABIN & FLANNERY LLP
LimestoneIPR@fitcheven.com