

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LIMESTONE MEMORY SYSTEMS LLC,
Patent Owner.

Case IPR2016-00094
Patent 5,894,441

Before BART A. GERSTENBLITH, BARBARA A. PARVIS, and
ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. *Background*

Micron Technology, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting institution of *inter partes* review of claims 1–3 and 5–15 of U.S. Patent No. 5,894,441 (Ex. 1001, “the ’441 patent”). Limestone

Memory Systems LLC (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”).

In its Preliminary Response, Patent Owner indicates that it has disclaimed claims 1–3 and 5 under 35 U.S.C. § 253(a). Prelim. Resp. 10. As evidence of that disclaimer, Patent Owner filed an Acknowledgement Receipt. Ex. 2001. 37 C.F.R. § 42.107(e) provides: “The patent owner may file a statutory disclaimer under 35 U.S.C. 253 (a) in compliance with § 1.321(a) of this chapter, disclaiming one or more claims in the patent.” Patent Owner’s disclaimer is in compliance with 37 C.F.R. § 1.321(a). Accordingly, we decline to institute an *inter partes* review as to claims 1–3 and 5.

Furthermore, upon consideration of the Petition, and applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we deny the Petition and decline to institute an *inter partes* review of claims 6–15 of the ’441 patent.

B. Related Proceedings

The parties indicate that the ’441 patent is asserted against Petitioner in *Limestone Memory Sys. LLC v. Micron Tech., Inc.*, No. 8:15-cv-00278 (C.D. Cal.). Pet. 2; Paper 6, 2. The parties indicate that other proceedings may be related. Pet. 2–3; Paper 6, 2–3.

C. Real Parties-in-Interest

The Petition identifies Micron Technology, Inc. as the real party-in-interest. Pet. 2. Patent Owner identifies Limestone Memory Systems LLC and Acacia Research Group LLC as the real parties-in-interest. Paper 6, 1.

D. The References

Petitioner relies on the following references:

U.S. Patent No. 5,270,975, issued December 14, 1993 (Ex. 1005, “McAdams”); and

Japanese Patent Application No. H06-052696, published February 25, 1994 (Ex. 1006, “Minami”).¹

E. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 6–15 of the ’441 patent on the ground that they are unpatentable, under 35 U.S.C. § 103(a), over McAdams and Minami. Pet. 4. Petitioner supports its challenge with a declaration executed by Dr. R. Jacob Baker on October 22, 2015 (Ex. 1003).

F. The ’441 patent

The ’441 patent is directed to a “SEMICONDUCTOR MEMORY DEVICE WITH REDUNDANCY CIRCUIT.” Ex. 1001, [54]. The ’441 patent explains:

The semiconductor memory device according to this invention comprises a plurality of column selection lines, at least one redundant column selection line, a column decoder which activates one line out of the plurality of column selection lines in response to a column address a first circuit which generates a detection signal when the column address of a defect-related column selection line is supplied, and a second circuit which receives at least a part of a row address and activates the redundant column selection line in response to at least a part of the row address and the detection signal. With this arrangement, when a defect occurs in one bit, instead of replacing all of the

¹ Unless otherwise noted, citations are to the certified English-language translation, submitted as part of Exhibit 1006.

many bit lines included in the column selection line to which the defective bit line belongs, it is possible to relieve a larger number of defective bit lines using a single redundant column selection line by replacing only a part of these bit lines.

Id. at 2:13–28.

G. Illustrative Claim

Claim 6 is the remaining independent claim challenged in this proceeding. Claims 7–15 depend, directly or indirectly, from claim 6. Independent claim 6 is illustrative of the claimed subject matter and is reproduced below with emphasis on the element that is the focus of our analysis.

6. A semiconductor memory device comprising:
 - a plurality of word lines including at least first and second word lines;
 - a plurality of bit lines including at least first and second bit lines;
 - a plurality of redundant bit lines including at least first and second redundant bit lines;
 - a plurality of memory cells each of which is disposed on intersections of said word lines and bit lines;
 - a plurality of redundant memory cells each of which is disposed on intersections of said word lines and redundant bit lines;
 - a plurality of column selection lines including at least a first column selection line; said first and second bit lines being selected when said first column selection line is activated;
 - a redundant column selection line; said first and second redundant bit lines being selected when said redundant column selection line is activated;
 - a column decoder activating said first column selection line in response to a first column address when said first word line is activated; and

a column redundancy decoder activating said redundant column selection line in response to said first column address when said second word line is activated.^[2]

Ex. 1001, 13:55–14:13 (emphasis added).

II. CLAIM CONSTRUCTION

A. Legal Standard

Petitioner proposes that we construe the claim term “transfer gate” to mean “logic that transfers the logic value of a signal.” Pet. 10. For the purposes of this Decision, we are not persuaded that “transfer gate” requires express construction, because even if we were to adopt Petitioner’s proffered construction, Petitioner has not established that it is reasonably likely to succeed in showing that the challenged claims are unpatentable. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

III. ANALYSIS

A. Obviousness of Claim 6 over McAdams and Minami

Petitioner asserts that a combination of the teachings of McAdams and Minami would have rendered the subject matter of claim 6 obvious to one of ordinary skill in the art at the time of the invention. Pet. 26–44. The Petition includes discussion identifying where McAdams and Minami allegedly teach or suggest the elements of each challenged claim. *Id.*

² We refer to this limitation as “the column redundancy decoder limitation.”

1. *Principles of Law*

A claim is unpatentable, under § 103(a), if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

An invention “composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418. Instead, a determination of unpatentability on a ground of obviousness must include “‘articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.’” *Id.* (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). The obviousness evaluation “should be made explicit,” and it “can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.” *Id.*

2. *McAdams*

McAdams is directed to a semiconductor memory device and in particular to “devices which include repair circuitry for eliminating defects in memory devices.” Ex. 1005, 1:9–13. McAdams explains that “each data

block 12 is partitioned into sixteen sub-blocks 14.” *Id.* at 5:12–13.³

McAdams further explains:

Within each sub-block 14, there are 256 row or word lines R and 256 column select lines Y_s . For simplicity of illustration, only one row line R and one column select line Y_s are shown in FIG. 3. A row line is selectable based on row address information input to a one of sixteen row decoder stage 16 and a one of 256 row decoder stage 18. In each data block 12, column address decoders 20 turn on a select line Y_s to control read/-write data transfer for two columns.

Id. at 5:39–47.

3. *Minami*

Minami is directed to semiconductor memory devices providing defect rescue functions of memory cells and peripheral circuits.

Ex. 1006 ¶ 1. Minami explains:

The memory cell array is comprised of memory cells arrayed in a matrix, four regular bit lines BL_J (BL_0 , BL_1 , BL_2 , BL_3) and a spare bit line SBL, in addition to comprising four regular word lines (WL_0 , WL_1 , WL_2 , WL_3). The regular memory cells C_{ij} selected by means of the word line WL_i and the regular bit line BL_j , and the spare memory cell SC_i selected by the word line WL_i and the spare bit line SBL. The row address is input from the address lines A_0/A_0 , A_1/A_1 and one of the regular bit lines is selected by means of the column decoders CD_0 , CD_1 , CD_2 and CD_3 in correspondence with the input address.

Id. ¶ 22.

4. *Level of Ordinary Skill in the Art*

With regard to the level of ordinary skill in the art, we determine that no express finding is necessary, on this record, and that the level of ordinary skill in the art is reflected by the prior art of record. *See Okajima v.*

³ Bold omitted from reference numerals in patents throughout.

Bourdeau, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

5. *The Column Redundancy Decoder Limitation*

Regarding the last limitation recited in claim 6, i.e., the column redundancy decoder limitation, the Petition includes the following contention:

This limitation simply covers the concept of using a redundant bit line to replace only part of a column (a segment). Specifically, while the first column address and first word line activates the normal selection line, the same first column address and second word line activates the redundant column selection line. MICRON-1003, Baker Decl., Appx. A at claim [6.6].

Pet. 42 (emphasis in Petition). Regarding the first sentence, we note that Petitioner does not propose a construction for any part of the column redundancy decoder limitation. *See id.* at 10–11 (proposing a construction for only ‘transfer gate’ recited in claims 3 and 13). Petitioner’s contention regarding what the limitation purportedly “covers” (*id.* at 42) is not a proposed construction. *See* 37 C.F.R. § 42.104 (b)(3) (explaining that the Petition must set forth “[h]ow the challenged claim is to be construed”). We address Petitioner’s reliance upon Appendix A of Dr. Baker’s Declaration after considering other arguments and citations provided in the Petition.

The Petition next includes contentions relating to certain of McAdams’s teachings. For limitations recited in claim 6 that precede the column redundancy decoder limitation, the Petition includes a series of figures from McAdams that are annotated purportedly to show the limitations of claim 6. To provide context, these annotations are summarized in the table below. In the pages of the Petition identified in the table below, McAdams’s Figure 2, which illustrates a data block that is

partitioned into sixteen sub-blocks 14 (Ex. 1005, 5:12–13), is reproduced on the left-hand side of the page. *See, e.g.*, Pet. 34. McAdams’s Figure 3, which illustrates a partial view of a sub-block (*id.* at 4:31–32), is reproduced twice on the right-hand side of the page. *See, e.g.*, Pet. 34.

Element of Claim 6 (recited in full)	Contentions in the Petition
a column redundancy decoder activating said redundant column selection line	Petitioner asserts that a first redundant column select line Y _{RS} is annotated in gold. Pet. 39.
in response to said first column address ⁴	Petitioner asserts that the first column selection line is annotated in navy blue. Pet. 37–38. Petitioner asserts that the first word line is in the top sub-block and is annotated in red. Pet. 33–34.
when said second word line is activated	Petitioner asserts that the second word line is in the bottom sub-block and is annotated in purple. Pet. 34.

Regarding the column redundancy decoder limitation, the Petition includes the following contention based on McAdams:

McAdams discloses column repair decoder circuits that are “each connected to a repair column and each programmable with column and row address information corresponding to a section of an array column containing a defective memory cell. With this programming, memory cells in a segment of a repair column can replace memory cells in a segment of an array column containing a defective memory cell.” *Id.* at 3:51-58. The redundant column select lines “[are] capable of replacing multiple defective column portions with multiple redundant

⁴ Although Petitioner does not annotate a particular element corresponding to “said first column address,” we note that “said first column address derives antecedent basis from the following: “activating said first column selection line in response to a first column address when said first word line is activated.”

column portions which are enabled by the same redundant column select line.” *Id.* at 3:12-16. In other words, depending on the row address (first or second word line), activation of the redundant selection line will occur, *e.g.*, if the column and second word line address correspond to a defective cell.

Pet. 43.

The indication that each decoder is programmable “with column and row address information corresponding to a section of an array column containing a defective memory cell” (*id.*), does not by itself indicate that the redundant column selection line is activated in response to the first column address (which is the same address that activates the first column selection line) when “said second word line is activated,” as recited in claim 6. Additionally, the final sentence, shown above in the block quote, of Petitioner’s contention is ambiguous because it refers to “first or second word line” and “if the column,” without specifying which one. Further, the final sentence is not supported sufficiently by the immediately preceding citations and does not include its own evidentiary citation.

The Petition also includes the following contention:

As shown in Figure 5, the output of the fusible comparator decoders 40 (which detects a defective cell by using the row and column address) is provided to the Y_{RS} enable logic 50 that is then provided to the redundant column decoder that activates the redundant column selection lines if the address (*e.g.*, first column address and second word line) matches a defective cell. *Id.* at 7:57-8:7, 8:44-61 (“When one decoder in a group SS_i outputs a logic high signal the select enable logic circuit 50 for that group outputs a logic high signal, corresponding to the associated redundant select line Y_{RSi} . With appropriate addressing provided to the decoders 40 and 42, each select enable logic circuit 50 **provides a logic-high signal to one redundant select line Y_{RS} in each data block.**”).

Pet. 43–44.

The reference to “appropriate addressing” (*id.*) alone is vague, and does not indicate that the redundant column selection line is activated in response to the first column address when the second word line is activated, as recited in claim 6. We are not persuaded that these additional contentions resolve the deficiency noted above.

The Petition apparently acknowledges the deficiency, stating the following: “[w]hat McAdams does not explicitly disclose is whether activating the column redundancy decoder occurs when a word line is activated.” *Id.* at 44. The Petition purportedly addresses the deficiency as follows: “this would have been obvious to a person of ordinary skill in the art in view of the disclosures in Minami for the same reasons discussed with reference to the previous limitation.” *Id.* (citing Section 10.2.6 claim [6.5]; Ex. 1003 Appx. A at claim [6.6]). The reference to “the previous limitation” does not provide sufficient specificity as to which of Petitioner’s previous contentions purportedly relate to the column redundancy decoder limitation and specifically why this limitation would have been obvious.

Accordingly, we determine that the Petition does not show sufficiently that the combination of McAdams and Minami teaches the column redundancy decoder limitation.

As noted above, Petitioner also relies on the Declaration of Dr. Baker and, in particular, Appendix A thereto. We determine that Petitioner’s reliance on Appendix A of Dr. Baker’s Declaration does not resolve the deficiency in the Petition for the following reasons.

First, Appendix A includes many references to other contentions and does not provide sufficient specificity with respect to the column redundancy decoder limitation. The portion of Appendix A of the

Declaration of Dr. Baker cited in the Petition that pertains to the column redundancy decoder limitation is five pages, beginning with the page shown below.

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MICRON-1003 ("Baker Decl.")

441 Patent - Claim 6	Ground #2: Rendered Obvious by McAdams in view of Minami						
	Minami discloses that the column decoder activates a column selection line (Y_S) in response to column address data when the word line is activated, as it would have been obvious that McAdams could have used the conventional row-then-column approach exemplified in Minami.						
[6.6] a column redundancy decoder activating said redundant column selection line in response to said first column address when said second word line is activated.	The following table is a summary of the function of the circuit described in claims [6.0]-[8.0], and [14.0], and disclosed by McAdams. A row address is first provided that activates the relevant word line. Then, a column address is provided. Based on the row address and column address, either a normal column selection line is activated or a redundant column selection line is activated. <table> <tr> <td></td><td>In response to <u>first</u> column address:</td></tr> <tr> <td>In response to <u>first</u> row address, the <u>first</u> word line is activated.</td><td>(First bit line) Column Decoder activates <u>first</u> column selection line</td></tr> <tr> <td>In response to <u>second</u> row address, the <u>second</u> word line is activated.</td><td>(Second bit line DEFECTIVE) Column Redundancy Decoder activates said <u>redundant</u> column selection line</td></tr> </table> McAdams discloses column repair decoder circuits that are "each connected to a repair column and each programmable with column and row address information corresponding to a section of an array column containing a defective memory cell. With this programming, <u>memory cells in a segment of a repair column can replace memory cells in a segment of an array column containing a defective</u>		In response to <u>first</u> column address:	In response to <u>first</u> row address, the <u>first</u> word line is activated.	(First bit line) Column Decoder activates <u>first</u> column selection line	In response to <u>second</u> row address, the <u>second</u> word line is activated.	(Second bit line DEFECTIVE) Column Redundancy Decoder activates said <u>redundant</u> column selection line
	In response to <u>first</u> column address:						
In response to <u>first</u> row address, the <u>first</u> word line is activated.	(First bit line) Column Decoder activates <u>first</u> column selection line						
In response to <u>second</u> row address, the <u>second</u> word line is activated.	(Second bit line DEFECTIVE) Column Redundancy Decoder activates said <u>redundant</u> column selection line						

A-44

MICRON-1003.084

Ex. 1003, Appx. A.

As shown above, this portion of Appendix A begins with a reference to McAdams's teachings regarding claims 6 through 8 and claim 14. Additionally, as can be seen above, the contentions with respect to "[i]n response to second row address, the second word line is activated," do not include evidentiary citations and apparently rely on arguments directed to other elements of claims 6, 7, 8, and 14. The contentions pertaining to other elements of claims 6, 7, 8, and 14 are found on pages A-24 through A-54 and A-70 through A-72. "A brief must make all arguments accessible to the

judges, rather than ask them to play archeologist with the record.” *DeSilva v. DiLeonardi*, 181 F.3d 865, 866–67 (7th Cir. 1999). With respect to other elements of claims 6, 7, 8, and 14, Appendix A does not specify sufficiently which of the other contentions relate to the column redundancy decoder limitation and does not provide enough context to determine whether any other contentions relate to the column redundancy decoder limitation.

Second, the portion of Appendix A that pertains to the column redundancy decoder limitation includes conclusory statements regarding the knowledge of one of ordinary skill in the art. *See, e.g.*, Ex. 1003, Appx. A-47, A-48. “Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.” *See* 37 C.F.R. § 42.65(a).

We further find that the portion of Appendix A that pertains to the column redundancy decoder limitation includes evidentiary citations that are similar to those specified in the Petition. For the reasons discussed above, that evidence is not persuasive to show sufficiently that the combination of McAdams and Minami teaches the column redundancy decoder limitation.

Accordingly, we determine that Petitioner has not shown sufficiently that the combination of McAdams and Minami teaches the column redundancy decoder limitation.

6. *Reasoning to Support Conclusion of Obviousness*

The Petition includes the following contention: “[o]ne of ordinary skill in the art would have been motivated to combine McAdams and Minami” because they “address the same problem” and “adopt similar solutions.” Pet. 27 (citing Ex. 1003 ¶¶ 71–79; Ex. 1005, 3:3–7; Ex. 1006 ¶ 17). The Petition includes further contentions pertaining to the

similarity of the problems and solutions of McAdams and Minami, as well as general interoperability of components used in the circuits. *Id.* (citing Ex. 1003 ¶¶ 75, 76; Ex. 1005, 3:3–7, 3:12–16, 6:27–30; Ex. 1006 ¶¶ 17, 22, 23, 28, 29 Abstract.).

Although the similarities of McAdams and Minami are considerations, as well as interoperability of components, in this case, we are not persuaded that these alone are sufficient to show what teachings Petitioner contends should be combined or modified and, without more, do not provide an articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

The Petition includes the following additional contention “one of ordinary skill in the art would also have found the combination of McAdams and Minami to be merely a simple substitution of prior art elements according to known methods that would yield predictable results.” *Id.* at 28. The Petition includes the following more specific contention: “Y_{RS} enable logic” of McAdams “could be substituted for or modified to include the NMOS transistors T₀–T₃ described in Minami” (also referred to as transfer gates). *Id.* at 28–29 (citing Ex. 1005, 8:48–61; Ex. 1006 ¶ 23; Ex. 1003 ¶ 77). According to the Petition, the proposed substitution would improve redundancy and lower power consumption. *Id.* at 29 (citing Ex. 1003 ¶ 78).

The Petition includes citations to the Declaration of Dr. Baker. We have reviewed Dr. Baker’s testimony (Ex. 1003 ¶¶ 71–79), which is similar to the contentions in the Petition.

Patent Owner contends that “[t]he Y_{RS} enable logic 50 in McAdams applies to multiple memory array blocks” (Prelim. Resp. 25), whereas

“Minami’s transistors T_0 – T_3 and column decoders CD_0 – CD_3 are wired to individual wordlines in a single memory array” (*id.* at 27 (citation omitted)). In particular, Patent Owner points to McAdams’s teaching that “all of the decoders 40 in a particular group SS_i are wired to turn on the same redundant select line Y_{RSi} ($i=1,N$) **in all of the data blocks.**” *Id.* at 25–26 (citing Ex. 1005, 8:8–16) (emphasis in Preliminary Response). Patent Owner provides annotations to Figure 5 to show how one Y_{RS} enable logic block (shown in red) connects to four data blocks. *Id.* at 26. Additionally, Patent Owner points to Minami’s teaching that “[t]he regular memory cells C_{ij} selected by means of the word line WL_i and the regular bit line BL_j , and the spare memory cell SC_i selected by the word line and the spare bit line SBL .” *Id.* at 27 (citing Ex. 1006 ¶ 22); *see also id.* (illustrating an annotated Figure 1 of Minami).

Upon review of the contentions in the Petition, and the evidence cited therein, including the testimony of Dr. Baker, as well as the contentions in the Preliminary Response, we are not persuaded that the Petition demonstrates sufficiently that the combination of the teachings discussed above is nothing more than a simple substitution. We also do not find that Petitioner’s contentions are sufficient to show what additional teachings Petitioner contends should be combined or modified so as to demonstrate that every element, arranged as recited in claim 6, would have been obvious over the combined teachings of McAdams and Minami.

Petitioner additionally contends that one of ordinary skill in the art would have been motivated to combine the teachings of McAdams and Minami because the result would improve redundancy in McAdams, which would result in lower power consumption. Pet. 29 (citing Ex. 1003 ¶ 78).

McAdams, however, already teaches the concept of redundancy and the Petition does not specify sufficiently how redundancy would be improved. The Petition includes a citation to Dr. Baker's Declaration, who also testifies that redundancy is improved without sufficient further specificity. Dr. Baker does not disclose sufficiently the underlying facts or data on which his opinion is based. *See* 37 C.F.R. § 42.65(a). Accordingly, we determine that Petitioner does not provide sufficiently an articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

7. *Summary*

Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claim 6 of the '441 patent is unpatentable.

B. *Obviousness of Claims 7–15 over McAdams and Minami*

Petitioner asserts that a combination of the teachings of McAdams and Minami would have rendered the subject matter of claims 7–15 obvious to one of ordinary skill in the art at the time of the invention. Pet. 44–60. Each of claims 7–15 depends, directly or indirectly, from independent claim 6. Accordingly, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claims 7–15 of the '441 patent are unpatentable.

IV. ORDER

For the foregoing reasons, it is:

ORDERED that the Petition is *denied* and no *inter partes* review is instituted.

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Patent 5,894,441

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