

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION,
SAMSUNG ELECTRONICS, CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC., and
SAMSUNG SEMICONDUCTOR, INC.,
Petitioner,

v.

RAYTHEON COMPANY,
Patent Owner.

Case IPR2016-00209¹
Patent 5,591,678

Before JO-ANNE M. KOKOSKI, JENNIFER MEYER CHAGNON, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Case IPR2016-00962 has been joined with the instant proceeding.

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–18 of U.S. Patent No. 5,591,678 (Ex. 1001, “the ’678 patent”) are unpatentable.

A. Procedural History

Sony Corporation (“Petitioner”) filed a Petition (Paper 2, “Pet.”) for *inter partes* review of claims 1–18 (“the challenged claims”) of the ’678 patent. Petitioner included a Declaration of Dr. Richard A. Blanchard (Ex. 1002) to support its positions. Raytheon Company (“Patent Owner”) timely filed a Preliminary Response (Paper 10, “Prelim. Resp.”).

Pursuant to 35 U.S.C. § 314(a), on March 29, 2016, we instituted an *inter partes* review of the challenged claims to determine whether claims 1–4, 6, 7, 10, and 11 are unpatentable under 35 U.S.C. § 102 as anticipated by Liu;² whether claims 2–4 and 11 are unpatentable under 35 U.S.C. § 103 as obvious in view of Liu and Black;³ whether claims 5 and 12–16 are unpatentable under 35 U.S.C. § 103 as obvious in view of Liu and Riseman;⁴ whether claim 8 is unpatentable under 35 U.S.C. § 103 as obvious in view of Liu and Oldham;⁵ whether claim 10 is unpatentable under 35 U.S.C. § 103 as obvious in view of Liu and Wen;⁶ whether claim 9 is unpatentable under

² U.S. Patent No. 4,422,091, issued Dec. 20, 1983 (Ex. 1003).

³ U.S. Patent No. 4,426,768, issued Jan. 24, 1984 (Ex. 1007).

⁴ U.S. Patent No. 4,106,050, issued Aug. 8, 1978 (Ex. 1009).

⁵ U.S. Patent No. 4,681,718, issued July 21, 1987 (Ex. 1005).

⁶ U.S. Patent No. 3,846,198, issued Nov. 5, 1974 (Ex. 1004).

35 U.S.C. § 103 as obvious in view of Liu, Wen, and Ying;⁷ whether claim 17 is unpatentable under 35 U.S.C. § 103 as obvious in view of Liu, Riseman, and Kusunoki;⁸ and whether claim 18 is unpatentable under 35 U.S.C. § 103 as obvious in view of Liu, Riseman, and Oldham. Paper 12 (“Inst. Dec.”).

Subsequent to institution, Patent Owner filed a Patent Owner Response (Paper 36,⁹ “PO Resp.”), along with a Declaration of Dr. Eugene A. Fitzgerald (Ex. 2001¹⁰) to support its positions. Petitioner filed a Reply (Paper 27, Paper 28 (redacted version), “Pet. Reply”) to the Patent Owner Response. After Petitioner’s Reply was filed, institution was granted in *Samsung Electronics, Co. v. Raytheon Co.*, Case IPR2016-00962, and that proceeding was joined with the instant proceeding. See Paper 29. An oral hearing was held on October 13, 2016. A transcript of the hearing is included in the record. Paper 44 (“Tr.”).

⁷ U.S. Patent No. 3,864,819, issued Feb. 11, 1975 (Ex. 1006).

⁸ JP App. Pub. No. 3-108776, published May 8, 1991. Kusunoki is a Japanese-language reference (Ex. 1014). Citations to Kusunoki herein are to the certified English translation submitted by Petitioner (Ex. 1008).

⁹ Pursuant to our telephonic authorization, Patent Owner filed a Corrected Patent Owner Response (Paper 36) that corrects specific citations to Dr. Fitzgerald’s Declaration. A red-line version was filed as Exhibit 2030. Paper 36 replaces the originally filed Patent Owner Response (Paper 22), and all citations herein are to the corrected version.

¹⁰ Exhibit numbers 2001–2003 were re-used by Patent Owner at the time of filing the Patent Owner Response. We note this is in violation of 37 C.F.R. § 42.63(c). For clarity, citations herein to Exhibits 2001–2003 are to the documents filed on June 15, 2016.

B. Related Proceedings

The '678 patent has been asserted in *Raytheon Co. v. Samsung Electronics Co.*, No. 2:15-cv-00341 (E.D. Tex.), and *Raytheon Co. v. Sony Kabushiki Kaisha*, No. 2:15-cv-00342 (E.D. Tex.). Paper 5, 2; Pet. 1. Petitioner Sony also has challenged the '678 patent in *Sony Corp. v. Raytheon Co.*, Case IPR2015-01201 (“the 1201 IPR”). Pet. 1–2; Paper 5, 2. The '678 patent also has been challenged in *Samsung Electronics, Co. v. Raytheon Co.*, Case IPR2016-00739, which currently is pending.

C. The '678 Patent

The '678 patent, titled “Process of Manufacturing a Microelectric Device Using a Removable Support Substrate and Etch-Stop,” relates to a method of fabricating a microelectronic device, in which the microelectronic device is moved from one support to another during fabrication. Ex. 1001, 1:12–13. According to the '678 patent, “[t]he invention permits microelectronic devices to be prepared using well-established, inexpensive thin-film deposition, etching, and patterning techniques, and then to be further processed singly or in combination with other such devices, into more complex devices.” *Id.* at 2:9–14.

Figure 1 of the '678 patent is reproduced below.

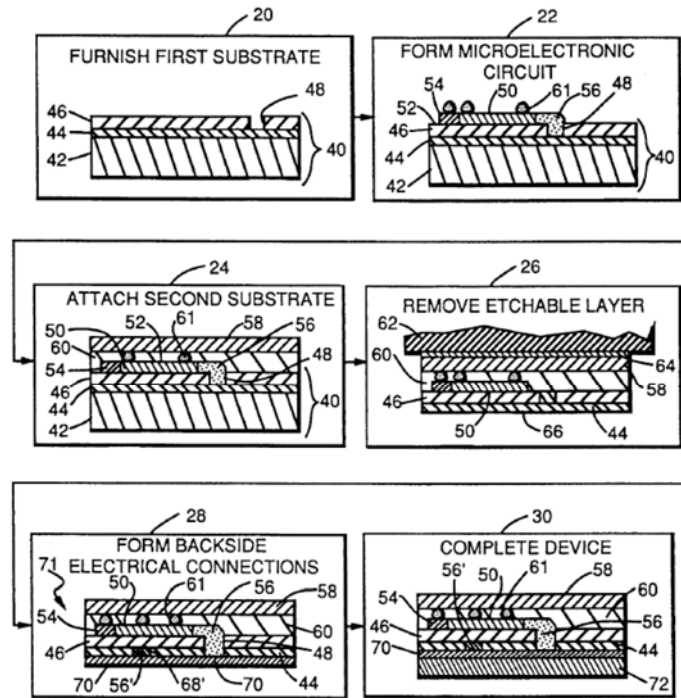


FIG. 1.

Figure 1 is a process flow diagram of the method of the '678 patent, schematically illustrating each stage of fabrication of a microelectronic device formed in accordance with the method. *Id.* at 3:48–50. As shown in box 20, first substrate 40 is provided, the first substrate including etchable layer 42, etch-stop layer 44, and wafer layer 46. *Id.* at 3:65–4:2. As noted in the '678 patent, “[s]uch substrates can be purchased commercially,” or “prepared by applying well-known microelectronic techniques.” *Id.* at 4:2, 4:22–23. In a preferred embodiment, etchable layer 42 is a layer of bulk silicon, etch-stop layer 44 is a layer of silicon dioxide, and wafer layer 46 is a layer of single crystal silicon. *Id.* at 4:3–15.

Microelectronic circuit element 50 is formed in wafer layer 46, as shown in box 22. *Id.* at 4:37–52. The '678 patent notes that “the present invention is not limited to any particular circuit element 50,” and, for

example, “can include many active devices such as transistors,” or “may be simply a patterned electrical conductor layer that is used as an interconnect between other layers of structure in a stacked three-dimensional device.”

Id. at 4:55–56, 4:47–51.

Second substrate 58 is attached to the structure, as shown in box 24. *Id.* at 5:14–44. Second substrate 58 may comprise, for example, silicon or aluminum oxide, and optionally may include a microelectronic device deposited therein. *Id.* at 5:18–25. Etchable layer 42 is removed by etching, as shown in box 26. *Id.* at 5:45–6:9. The entire structure may be attached temporarily to base 62, which may be a piece of aluminum oxide (particularly, sapphire), to protect the structure against etch attack. *Id.* at 5:47–49. As described in the ’678 patent, the “etchant is chosen so that it attacks the etchable layer 42 relatively rapidly, but the etch-stop layer 44 relatively slowly or not at all.” *Id.* at 5:52–54.

“Back-side electrical connections are formed through the [exposed] etch-stop layer 44 (for direct back-side interconnects 56’) and through the etch stop layer 44 and the wafer layer [46] to the microelectronic circuit element 50 (for indirect front-side interconnects [56]),” as shown in box 28. *Id.* at 6:10–14. The connections are formed by patterning etch-stop layer 44 using well-known patterning techniques. *Id.* at 6:14–17. Electrical conductor layer 70 may be deposited over etch-stop layer 44 and back side electrical connections 56, 56’. *Id.* at 6:44–49.

As shown in box 30 of Figure 1, final structure 71 may be joined with another microelectronic device 72, to form a three-dimensional structure comprising structures 71, 72. *Id.* at 6:50–58, Fig. 2.

D. Illustrative Claims

Of the challenged claims, claims 1, 11, and 13 are independent. Claims 2–10 depend, directly or indirectly, from claim 1; claim 12 depends from claim 11; and claims 14–18 depend, directly or indirectly, from claim 13. Claims 1, 6, and 7 of the ‘678 patent, reproduced below, are illustrative of the challenged claims:

1. A method of fabricating a microelectronic device, comprising the steps of:

furnishing a first substrate having an etchable layer, an etch-stop layer overlying the etchable layer, and a wafer overlying the etch-stop layer;

forming a microelectronic circuit element in the exposed side of the wafer of the first substrate opposite to the side overlying the etch-stop layer;

attaching the wafer of the first substrate to a second substrate; and

etching away the etchable layer of the first substrate down to the etch-stop layer.

Ex. 1001, 8:5–16.

6. The method of claim 1, wherein the second substrate contains a second microelectronic circuit element.

Id. at 8:32–33.

7. The method of claim 6, wherein the step of attaching includes the step of

making an electrical contact from the microelectronic circuit element on the wafer of the first substrate to the second microelectronic circuit element on the second substrate.

Id. at 8:34–39.

II. ANALYSIS

A. Claim Construction

The '678 patent is expired. When interpreting claims of an expired patent, our analysis is similar to that of a district court. *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012); *see also Black & Decker, Inc. v. Positec USA, Inc.*, RW, 646 Fed. App. 1019, 1024 (Fed. Cir. 2016) (holding that in an *inter partes* review, “[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc)”). Specifically, claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313–17. However, there is no presumption of validity, and we do not apply a rule of construction with an aim to preserve the validity of claims.

The parties’ dispute requires construction of several terms, which we address below. No issue in this Decision requires express construction of any other claim terms. *See, e.g., Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

1. “furnishing”

Patent Owner argues that the claims use the terms “furnishing” and “forming” to represent different steps of the claimed method. PO Resp. 13. According to Patent Owner, “furnishing” should be construed to mean “to

supply or provide something *that already exists.*” *Id.* at 13 (emphasis added). Patent Owner cites to Webster’s Third New International Dictionary (1993), which defines “furnish” as “to provide or supply with what is needed.” PO Resp. 13; Ex. 2022, 6. Patent Owner asserts that “forming” should be construed to mean “to assemble or put together.” PO Resp. 13. We need not construe “forming” for purposes of this Decision, but provide Patent Owner’s argument as a comparison to its proposed construction of “furnishing.”

Regarding the construction of “furnishing,” Petitioner argues that “the multi-layer substrates of the claims of the ‘678 [patent] *always* need to be manufactured,” at some point. Pet. Reply 4 (citing Ex. 1019 (deposition of Dr. Fitzgerald), 43:16–44:4). Even the first substrate as described in the Specification of the ‘678 patent must be formed, in Patent Owner’s use of the word, at some point. *See* Ex. 1001, 4:2 (“[s]uch substrates can be purchased commercially,” where they must presumably be formed), 4:22–36 (discussing preparation of first substrate 40 “by applying well-known microelectronic techniques”); Pet. Reply 4–5. In other words, even in the ‘678 patent, there is a point in time before substrate 40 *exists*.

Based on the evidence in the complete record now before us, we are not persuaded that the claimed “furnishing” step requires disclosure of the existence of a pre-existing three-layer substrate separate and apart from a disclosure that a three-layer substrate is being supplied for some intended purpose. No further express construction of furnishing is required for purposes of this Decision.

2. “wafer”

According to Patent Owner, the “term ‘wafer’ is explicitly used in the ’678 Patent to represent the top layer in the furnished substrate.” PO Resp. 11. Patent Owner also argues that the “wafer layer of the furnished substrate itself does not initially contain microelectronic circuit elements.” *Id.* Thus, according to Patent Owner, the term “wafer” should be construed to mean “a portion of the first substrate in or on which the microelectronic circuit element is formed.” *Id.* (citing Ex. 2001 ¶ 58). Patent Owner’s arguments attempting to distinguish the claims from the cited references, however, also incorporate the requirement that the wafer layer does not initially contain microelectronic circuit elements. *See, e.g., id.* at 22–23 (arguing that Liu does not disclose the claimed wafer layer because layers 6 and 8 include microelectronic circuit elements).

We are not persuaded that the term “wafer” is so limited. In describing the details of the first substrate and the preparation thereof (with regard to box 20 of Figure 1), the Specification states that “wafer layer 45 may also be or include an interconnect material such as a metal or other structure as may be appropriate for a particular application.” Ex. 1001, 4:16–18; *see* Pet. Reply 6–7. This description is counter to Patent Owner’s assertion that the ’678 patent requires that the wafer “does not initially contain microelectronic circuit elements.” In fact, the Specification states that the term “microelectronic circuit element” is “to be interpreted broadly, and can include active devices and passive structure. For example, the microelectronic circuit element . . . may be simply a patterned electrical conductor layer that is used as an interconnect between other layers of structure.” Ex. 1001, 4:45–51; *see* Pet. Reply 6–7. While we recognize this

description is in reference to the types of microelectronic circuit elements that may be formed in the “forming” step, we find it instructive as to the question of what may or may not be included in the furnished wafer, which the Specification expressly states “may also be or include an interconnect material such as a metal or other structure.” Ex. 1001, 4:16–18.

Based on the evidence in the complete record now before us, we are not persuaded that the Specification supports limiting the claim language “wafer” to a layer that does not initially contain microelectronic circuit elements, as Patent Owner advocates. No further express construction of the term is required for purposes of this Decision.

3. “*overlying*”

Patent Owner asserts that “overlying” should be construed to mean “lying on,” according to the Specification of the ’678 patent. PO Resp. 12–13 (citing Ex. 1001, Fig. 1). Based on Patent Owner’s arguments attempting to distinguish the claims from the cited references, we understand Patent Owner to mean that one layer “overlying” another layer requires *direct* contact with the layer upon which it overlies. *See id.* at 23–24. In its Reply, Petitioner argues that “‘overlying’ simply means ‘lying over’—it does not require direct contact.” Pet. Reply 10. We agree that the plain and ordinary meaning of overlie does not include a requirement of direct contact. *See Overlie Definition*, MERRIAM-WEBSTER.COM, <http://www.merriam-webster.com/dictionary/overlie> (last visited Nov. 21, 2016) (defining “overlie” as “to lie over or upon”). Accordingly, we construe *overlying*, in accordance with its plain and ordinary meaning, as *lying over or upon*.

B. Principles of Law — Anticipation and Obviousness

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference.

See Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Although the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *accord In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In that regard, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). The level of ordinary skill in the art may be reflected by the prior art of record. *See*

Okajima v. Bourdeau, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978). Further, while objective indicia of nonobviousness must always be considered when present, such objective indicia “do not necessarily control the obviousness determination.” *Merck & Cie v. Gnosis S.P.A.*, 808 F.3d 829, 837 (Fed. Cir. 2015), *cert. denied*, No. 16-125, 2016 WL 4014485 (U.S. Oct. 11, 2016) (citing *In re Cyclobenzaprine Hydrochloride Extended–Release Capsule Patent Litig.*, 676 F.3d 1063, 1075–76 (Fed. Cir. 2012); *Bristol–Myers Squibb Co. v. Teva Pharm. USA, Inc.*, 752 F.3d 967, 977 (Fed.Cir.2014)).

We analyze the asserted grounds of unpatentability in accordance with those principles.

C. Anticipation by Liu

Petitioner asserts that claims 1–4, 6, 7, 10, and 11 are unpatentable under 35 U.S.C. § 102 as being anticipated by Liu. Pet. 3, 20–33. Patent Owner argues that Liu does not disclose all the steps of the claimed methods. PO Resp. 16–31. We have reviewed the entire record before us, including the parties’ contentions and supporting evidence presented during this trial. For the reasons explained below, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1–4, 6, 7, 10, and 11 are unpatentable.

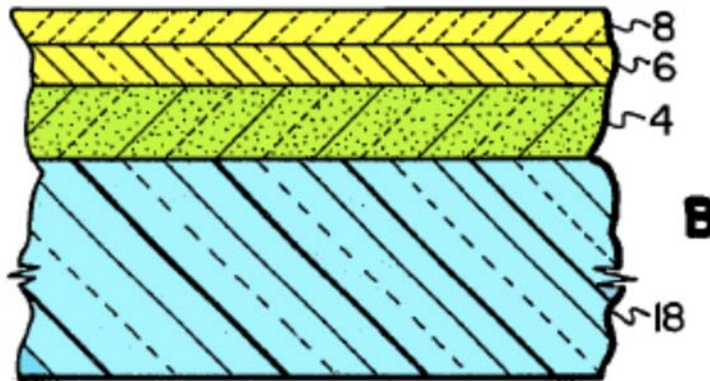
Claim 1

Petitioner’s Contentions

Claim 1 recites a “method of fabricating a microelectronic device.” Ex. 1001, 8:5–6. Liu describes an imaging charge coupled device (CCD)

and a fabrication method thereof. Ex. 1003, Abstract; see Pet. 20–21 (citing Ex. 1003, Abstract, 1:11–13; Ex. 1002 ¶ 83).

Petitioner relies on substrate 18, window layer 4, and absorber and channel layers 6, 8 of Liu as disclosing the claimed etchable layer, etch-stop layer, and wafer, respectively. Pet. 21–22. Petitioner provides an annotated version of Figure 2B of Liu, reproduced below (*id.* at 21).

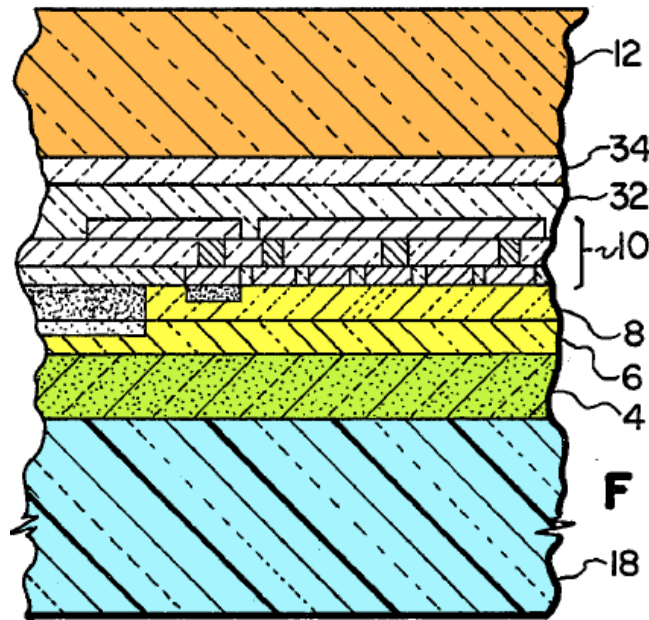


Petitioner’s annotated figure illustrates the portions of Liu’s device that Petitioner points to as corresponding to the claimed etchable layer (highlighted in blue), etch-stop layer (highlighted in green), and wafer (highlighted in yellow). *Id.* at 21–22 (citing Ex. 1003, 2:26–34, 3:63–4:19, 4:53–58, Fig. 2B; Ex. 1002 ¶¶ 69, 84–87, 89; Ex. 1001, 2:53–56, 4:16–18). Petitioner asserts that absorber layer 6 and channel layer 8 are a wafer “because they are used in the formation of the microelectronic circuits.” *Id.* at 22.

Petitioner further relies on CCD circuit 10 that is fabricated on channel layer 8 as disclosing the claimed “microelectronic circuit element” being “form[ed] . . . in the exposed side of the wafer of the first substrate opposite to the side overlying the etch-stop layer.” *Id.* at 22–24 (citing Ex. 1003, 3:23–33, 4:7–27, Fig. 2C; Ex. 1002 ¶¶ 90–93; Ex. 1001, 4:37–43).

As described in Liu, CCD circuit 10 includes ohmic contacts 20, channel isolation 22, barrier gates 24, vias 28, and interconnects 30. Ex. 1003, 4:21–27, Fig. 2F; see Pet. 23.

Petitioner relies on support 12 of Liu as disclosing the claimed “second substrate.” Pet. 24. Petitioner provides an annotated version of Figure 2F of Liu, reproduced below (*id.*).



Petitioner’s annotated figure illustrates a second substrate (highlighted in orange) attached to the wafer (highlighted in yellow). *Id.* (citing Ex. 1003, 3:34–35, 4:7–19, 4:29–46, Fig. 2F; Ex. 1002 ¶¶ 91, 94–97).

Finally, Petitioner relies on Liu’s disclosure of etching away substrate 18 (highlighted in blue, above) using a selective etchant that removes substrate 18 without removing window layer 4 (highlighted in green, above) (see Ex. 1003, Fig. 2G) for the claimed step of “etching away the etchable layer of the first substrate down to the etch-stop layer.” Pet. 25 (citing Ex. 1003, 3:65–4:19, 4:53–58, Figs. 2F, 2G; Ex. 1002 ¶¶ 98–101).

Patent Owner's Contentions and Our Analysis

Patent Owner argues that several features of claim 1 are missing from Liu. PO Resp. 16–25. We address each of Patent Owner's contentions in turn.

“furnishing a substrate”

Patent Owner argues that Liu does not disclose furnishing a three-layer substrate, as claimed, because Liu “first furnishes a *single layer* substrate” 18 (PO Resp. 16 (citing Ex. 1003, 3:63–68, Fig. 2A)) and, *then*, deposits three liquid phase epitaxial (LPE) layers 4, 6, 8 on top of substrate 18 (*id.* at 17 (citing Ex. 1003, 2:7–9, Fig. 2B)). *See id.* at 16–20. Patent Owner argues that “[t]hese additional layers comprise the imaging CCD—and *cannot* be a part of the **furnished** substrate, which is only a single layer.” *Id.* (citing Ex. 2001 ¶¶ 55–57, 62–64, 83–89). Patent Owner argues also that “Petitioner and Dr. Blanchard conflate the ‘furnishing’ and ‘forming’ steps to argue that layers 4, 6, and 8, which are *formed* on the single layer GaAs substrate in Liu’s Step B, are somehow part of Liu’s *furnished* GaAs substrate.” *Id.* at 18. Patent Owner also focuses on the fact that layers 4, 6, and 8, which Petitioner maps to the certain layers of the furnished substrate, are all part of the CCD imager itself formed *on* substrate 18, and are not *part of* substrate 18 shown in Figure 2A. *Id.* at 19.

Based on our construction of “furnishing,” discussed above (*see supra* section II.A.1), we are not persuaded that the only substrate that is furnished in Liu is that shown in Figure 2A, as asserted by Patent Owner. In mapping Liu to the claims, Petitioner relies on Figure 2B as disclosing the claimed furnished substrate. Pet. 21–22. Whether Figure 2A includes a single layer or multiple layers is, thus, irrelevant in determining if Liu anticipates the

claims. In addition, whether Liu describes steps prior to the configuration of Figure 2B also is irrelevant to whether it is furnished or not, within the meaning of the claims.

Further, regardless of the words Liu uses to describe the layers of its device, Liu can still anticipate the claims if it discloses each and every limitation therein. *In re Gleave*, 560 F.3d at 1334 (“[A] reference need not satisfy an *ipsissimis verbis* test.”). We agree with Petitioner’s mapping of the layers of Figure 2B of Liu to the substrate in the furnishing step of claim 1. As discussed above, substrate 18 of Liu is etched away using a selective etchant that removes substrate 18 without removing window layer 4, thus these layers disclose an etchable layer and etch-stop layer respectively. *See* Ex. 1003, 3:65–4:19, 4:53–58, Figs. 2F, 2G. Further, we are persuaded that absorber and channel layers 6, 8 disclose a wafer, as discussed in more detail below.

“wafer”

Patent Owner argues that Liu does not disclose a “wafer,” as claimed. PO Resp. 20–23. According to Patent Owner, “Liu refers to its ***entire device*** as its multi-layered wafer, which is inconsistent with the ’678 Patent’s use of the term as a single portion of material.” *Id.* at 20. Again, however, regardless of the particular language used in Liu, Liu can still anticipate the claims if it discloses each and every limitation therein. *See In re Gleave*, 560 F.3d at 1334 (“[A] reference need not satisfy an *ipsissimis verbis* test.”).

Patent Owner further argues that “Liu’s layers 6 and 8 are not the wafer claimed in the ’678 patent, or even part of the wafer, because even though they comprise semiconductor material, these layers *comprise* part of the device circuitry (*e.g.* they are part of the CCD).” PO Resp. 21 (citing

Ex. 2001 ¶¶ 70–71). Patent Owner also argues that Petitioner’s definition of wafer as being “used in the formation of microelectronic circuits” “is inconsistent with the term’s use in the ’678 Patent,” because “[t]he ’678 Patent requires its wafer to be the top portion of the furnished substrate.” *Id.* (citing Ex. 2001 ¶¶ 59–60; Ex. 1001, claims 1, 11, 13). Patent Owner continues that “[w]hile a microelectronic circuit element is formed *into or on top of* the top wafer, the ’678 Patent’s wafer layer does not exclusively consist of microelectronic elements as do Liu’s layers 6 and 8.” *Id.* (citing Ex. 2001 ¶¶ 59–60, 70).

In this regard, Patent Owner also argues that the claims of the ’678 patent “require that, initially, the wafer must not have circuit elements within it,” and that “forming the microelectronic circuit element in the wafer takes place *after* furnishing the substrate with a wafer layer.” *Id.* at 22. As previously discussed in our construction of “wafer” (*see supra* section II.A.2), however, the claimed wafer is not limited to a layer that does not initially contain microelectronic circuit elements.

The other limitation placed on the term “wafer” in the claims is that “microelectronic circuit elements [are formed] in the exposed side of the wafer” Ex. 1001, 8:10–12; *see* Pet. Reply 7. Petitioner, however, does not rely on any microelectronic circuit element present in layer 6 or 8 in Figure 2B also to describe the later formed microelectronic circuit elements, but instead relies on CCD circuit 10 that is fabricated on channel layer 8, as we have previously discussed. *See* Pet. 22–24; Ex. 1003, Fig. 2C. Accordingly, we are persuaded that absorber and channel layers 6, 8 of Liu disclose the claimed wafer.

“wafer layer *overlying* an etch-stop layer”

Patent Owner argues that “Liu’s CCD layers, even if they were considered a part of the initial substrate (which they are not), still do not teach the etch-stop and wafer substrate layers in the ’678 Patent because Liu’s CCD layers do not satisfy the challenged claims’ requirements that layers ‘overl[ie]’ each other.” PO Resp. 23 (citing Ex. 2001 ¶¶ 90–92). In this regard, Patent Owner argues that channel layer 8 of Liu does not “overlie” layer 4 (which Petitioner relies upon as the claimed etch-stop layer), because absorber layer 6 is between these layers. *Id.* at 24. This argument is not persuasive for two reasons. First, Petitioner relies on both absorber layer 6 *and* channel layer 8 as disclosing the claimed wafer layer. Second, as previously discussed in our construction of “overlying” (see *supra* section II.A.3), the claims do not require direct contact of the layers for one layer to be overlying another layer.

Patent Owner also argues that substrate 18 does not overlie any layer in the Liu device. PO Resp. 24. This argument is not persuasive because, as discussed above, Petitioner relies on substrate 18 only to disclose the claimed etchable layer, and not to disclose the claimed wafer.

Accordingly we are persuaded that Liu discloses the claimed wafer layer overlying an etch-stop layer.

“forming a microelectronic circuit element in the exposed side of the wafer”

Patent Owner argues that Liu does not disclose forming a microelectronic circuit element in the exposed side of the wafer. PO Resp. 25. Patent Owner’s arguments in this regard are premised on its arguments that channel layer 8 does not disclose the claimed wafer.

However, as discussed above, we are not persuaded by this argument, and agree with Petitioner that absorber and channel layers 6, 8 of Liu disclose the claimed wafer. We also agree with Petitioner that formation of Liu's CCD circuit 10 discloses the claimed forming step.

Conclusion

For the reasons discussed, we agree with Petitioner's above-described mapping of Liu to claim 1, and are persuaded that Petitioner has shown, by a preponderance of the evidence, that Liu anticipates independent claim 1.

Claims 2–4

Claim 2 depends from claim 1, and further recites “patterning the etch-stop layer.” Ex. 1001, 8:17–19. Regarding claim 2, Petitioner points to the disclosure in Liu that “access to CCD device circuit 10 can be provided by etching through the thin LPE layers down to interconnect pads 16.” Pet. 26 (citing Ex. 1003, 4:59–61). “[T]he etchant can be confined to the periphery of the device to provide a border supporting interconnect pads 16.” Ex. 1003, 4:64–66; Pet. 26. Petitioner further asserts that claim 2 of the '678 patent “does not limit the ‘patterning’ . . . to any particular location on the device.” Pet. 26 (citing Ex. 1002 ¶ 108).

Claim 3 and 4 depend from claim 2, and further recite “after the step of patterning, . . . forming an electrical connection to the microelectronic circuit element through the patterned etch-stop layer and through the wafer,” and “after the step of patterning, . . . forming an electrical connection to the wafer through the patterned etch-stop layer,” respectively. Ex. 1001, 8:20–28. Regarding claim 3, Petitioner points to the disclosure in Liu that “[p]ads 16 are extensions of CCD circuit 10,” upon which Petitioner relies to

disclose the claimed microelectronic circuit element. Pet. 27; Ex. 1003, 3:59–60. According to Petitioner, the “connections are through the etch-stop layer and through the wafer, because the etch-stop layer and wafer have been removed around the periphery of the device to provide external access to the microelectronic circuit element.” Pet. 27; *see also* Ex. 1003, 3:56–59 (“[T]he area of semiconductor layers 4, 6, and 8 is less than the area of support 12 thus providing a ledge or border upon which interconnect pads 16 are positioned.”). Regarding claim 4, Petitioner points to Figure 2C of Liu, which shows, for example, ohmic contact 20 (which is a portion of CCD circuit 10) extending into channel layer 8. Pet. 28 (citing Ex. 1002 ¶ 117).

Patent Owner argues that Liu does not disclose patterning the etch-stop layer. PO Resp. 25–31. According to Patent Owner, the purpose of patterning and forming an electrical connection to the microelectronic circuit element through the etch-stop layer is to “permit access to the microelectronic circuit element from the back side,” or in other words “to provide an avenue to access circuitry that has been deposited on the wafer layer of the furnished substrate.” *Id.* at 26 (citing Ex. 1001, 2:28–33; Ex. 2001 ¶¶ 96–98). Patent Owner also argues that, unlike the ’678 patent which “permit[s] access to the full area of the transferred region from the backside of the transferred layer,” Liu “cannot bring connections through any region of the device,” but allows only etching and contact around the periphery. *Id.* at 30 (citing Ex. 2001 ¶¶ 101–105). We note, however, that the claims do not include limitations directed to these features described in the ’678 Specification on which the Patent Owner relies (e.g., the claims do not require access at any particular location on the device). Instead, the

claims merely require patterning and electrical contact through the etch-stop layer and wafer.

Patent Owner also points to the Specification of the '678 patent, which indicates “etch-stop layer 44 is patterned . . . to precisely identify the location to be penetrated.” *Id.* at 27 (citing Ex. 1001, 6:15–19). According to Patent Owner, “Liu does not describe *any* patterning to the window layer 4 that Blanchard opines is an etch-stop layer.” *Id.* (Ex. 2001 ¶ 99). Instead, according to Patent Owner, “Liu merely describes *removing* the layers 4, 6, and 8 through etching (confined to the periphery of the device in the embodiment shown).” *Id.* at 28 (citing Ex. 1003, 4:59–66; Ex. 2001 ¶ 99). In its Reply, Petitioner cites to Dr. Fitzgerald’s deposition testimony and other record evidence to confirm that, in the relevant timeframe, the etching of the periphery of the device would have been accomplished by using an etch-resistant coating over the portion that should not be etched, and then exposing the surface to an etchant, or in other words by “patterning.” Pet. Reply 12 (citing Ex. 1019, 59:12–60:25; Ex. 2003, 5:35–43; Ex 2015 14).

Patent Owner further argues that a “novel feature of the methods claimed in the '678 Patent is the ability to decrease the footprint of the microelectronic device by permitting access to the full area of the transferred region from the backside of the transferred layer.” PO Resp. 30 (citing Ex. 2001 ¶¶ 101–102). “Liu, on the other hand, cannot bring connections through any region of the device,” but only describes “etching the periphery of layers 4, 6, and 8.” *Id.* (citing Ex. 2001 ¶¶ 101–105). We agree with Petitioner, however, that “nothing in the '678 patent requires that the electrical connections be made through the layers in the center of the device,

rather than at the periphery as shown in . . . Liu.” Pet. 28 (citing Ex. 1002 ¶ 112).

Based on the evidence in the record before us, we are persuaded that Liu’s removal of window layer 4 (which Petitioner maps to the claimed etch-stop layer) and absorber layer 6 and channel layer 8 (which Petitioner maps to the claimed wafer), via etching, to provide electrical contact to CCD circuit layer 10 (which Petitioner maps to the claimed microelectronic circuit element) through the portions of the aforementioned layers that have been removed, meets the limitations recited in claims 2–4.

Claims 6, 7, 10, and 11

We also have reviewed Petitioner’s contentions and supporting evidence regarding claims 6, 7, 10, and 11. See Pet. 2–33 (citing Ex. 1003, Abstract, 1:11–13, 2:28–32, 3:23–50, 3:56–4:46, 4:53–66, Figs. 1, 2B, 2C; Ex. 1002 ¶¶ 118–124, 126–139; Ex. 1001, 2:28–33, 6:15–19). We agree with Petitioner’s mapping of Liu to these claims, and adopt it as our own. Patent Owner does not present additional arguments for these claims, beyond those already discussed above with respect to claim 1. We, thus, are persuaded that Petitioner has demonstrated, by a preponderance of the evidence, that Liu discloses all steps of claims 6, 7, 10, and 11.

Conclusion

For the reasons discussed, we are persuaded that Petitioner has shown, by a preponderance of the evidence, that Liu anticipates claims 1–4, 6, 7, 10, and 11.

D. Obviousness Based, at Least in Part, on Liu

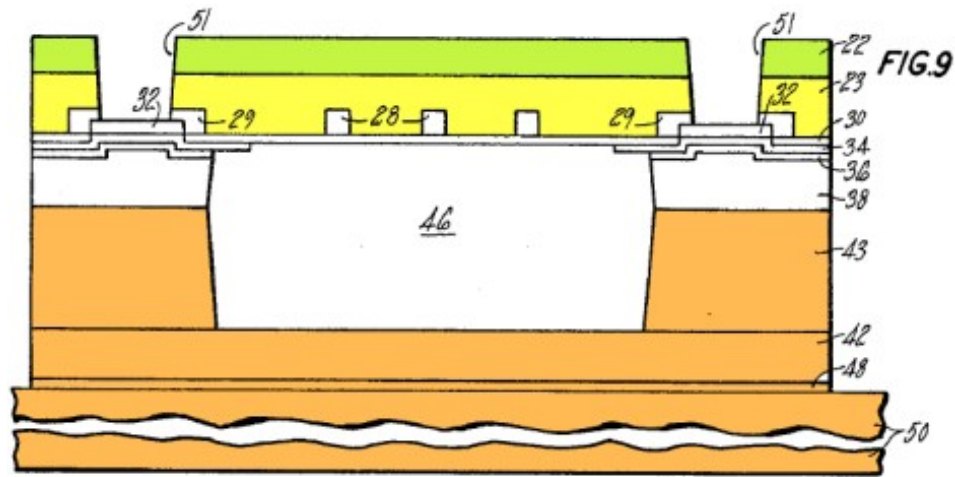
Petitioner makes the following assertion regarding alleged obviousness of the claims of the '678 patent: that claims 2–4, and 11 would have been obvious in view of Liu and Black (Pet. 3, 33–36); that claims 5 and 12–16 would have been obvious in view of Liu and Riseman (*id.* at 3, 36–49); that claim 8 would have been obvious in view of the combination of Liu and Oldham (*id.* at 3, 49–50); that claim 18 would have been obvious in view of the combination of Liu, Riseman, and Oldham (*id.* at 3, 57–58); that claim 10 would have been obvious in view of Liu and Wen (*id.* at 3, 50–52); that claim 9 would have been obvious in view of Liu, Wen, and Ying (*id.* at 3, 52–54); and that claim 17 would have been obvious in view of Liu, Wen, and Kusunoki (*id.* at 3, 54–57). Patent Owner argues that the cited references do not teach all features of the claims, and that one of skill in the art would not combine the references in the manner asserted by Petitioner. PO Resp. 31–42. Patent Owner also argues that secondary considerations support a finding of nonobviousness. *Id.* at 42–49.

We first address Petitioner's mapping of the cited art to the claims, and the presented reasoning for combining the references. We then address Patent Owner's evidence regarding objective indicia of nonobviousness.

1. Obviousness of Claims 2–4 and 11 in View of Liu and Black

Black relates to a method for making a plurality of thin pressure sensors by processing a wafer to provide a plurality of electronic devices. Ex. 1007, Abstract. As described in Black, electrical contact to the devices is provided through holes 51. *Id.* at Abstract, 3:37–42, 6:17–28, Fig. 9.

Holes 51 are shown in Figure 9, an annotated version of which is reproduced below (Pet. 35).



Petitioner's annotated figure illustrates a second substrate (highlighted in orange) attached to the wafer (highlighted in yellow), with holes 51 formed through the etch stop layer (highlighted in green) and the wafer. *See* Pet. 16–17 (citing Ex. 1007, 2:39–60, 3:1–7, 5:22–28, 6:15–28, Figs. 1, 9; Ex. 1002 ¶¶ 142–147).

Claims 2–4 and 11 recite patterning the etch-stop layer and/or forming an electrical connection to the microelectronic circuit element through the etch-stop layer and/or wafer. *See* Ex. 1001, 8:17–28, 9:7–9. Petitioner argues that Liu discloses patterning and an electrical connection through the etch-stop layer and wafer around the border of the device, and that Black discloses such patterning and connection inward from the edge of the device. Pet. 33 (citing Ex. 1007, Fig. 9; Ex. 1002 ¶¶ 103–117, 149, 150; Ex. 1001, Fig. 4). Petitioner provides declaration testimony that one of skill in the art would have recognized the benefits of placing the electrical contacts of Liu inward from the edge of the device, such as the ability to provide more contacts, the ability to reach contacts near the center of the device, or to

provide protection from damage to the contacts. Ex. 1002 ¶ 152; *see* Pet. 34. Petitioner further asserts that to do so would have “no unpredictable results.” Pet. 34; *see* Ex. 1002 ¶ 153.

Patent Owner argues that one of skill in the art would not combine Liu and Black because Liu involves a *light* sensor, while Black involves a *pressure* sensor, and, thus, the references are non-analogous art. PO Resp. 33–34. We agree with Petitioner, however, that both Liu and Black are in the more general field of “microelectronic devices,” the same field as the ’678 patent, and are, thus, analogous art. Pet. Reply 14–16 (citing Ex. 1001, 1:11 (“This invention relates to microelectronic devices.”); Ex. 1019, 49:9–19 (Dr. Fitzgerald confirming the relevant art is microelectronic processing); Ex. 1003, 1:11–22; Ex. 1007, 1:7–10, 2:39–42); *see also Wyers v. Master Lock Co.*, 616 F.3d 1231, 1238 (Fed. Cir. 2010) (“The Supreme Court’s decision in *KSR* . . . directs us to construe the scope of analogous art broadly.”).

Patent Owner also argues that the resulting device of Petitioner’s combination would be inoperable, and, thus, there is no motivation to combine the references. PO Resp. 34–35. Specifically, Patent Owner argues that Black’s pressure sensor “must have a structurally-compromised layer that can bend under pressure,” and a person of ordinary skill “would not combine Black with Liu because it results in a structure that would break during manufacture.” *Id.* (citing Ex. 2001 ¶¶ 112–114; Ex. 1007, 3:58–60). Petitioner, however, does not argue that Black’s structure must be bodily incorporated into Liu. *See* Pet. Reply 16. Instead, Petitioner relies on Black to “show the known use of patterning to form contacts through an etch-stop layer, inward from the edge of the layer, and directly to a relevant

microelectronic circuit element.” *Id.* (citing Pet. 33–34). We agree with Petitioner that the “use of [such] patterning does not require that Black’s flexible layer be incorporated into Liu.” *Id.*; *see also In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (“It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements.” (citing *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (noting that the criterion for obviousness is not whether the references can be combined physically, but whether the claimed invention is rendered obvious by the teachings of the prior art as a whole))).

Patent Owner also argues that neither Liu nor Black teaches patterning of an etch-stop layer to allow access to circuitry beneath the layer. PO Resp. 35 (citing Ex. 2001 ¶¶ 115–116). We have already addressed this argument with respect to Liu (*see supra* II.C, discussion of claims 2–4). With respect to Black, Figure 9 of Black clearly shows that holes 51 through etch-stop layer 22 and layer 23 “expose[] the aluminum bonding pads 32 to permit . . . bonding of conductors (not shown) to the aluminum bonding pads 32.” Ex. 1007, 6:25–28; *see* Pet. Reply 16–17; Ex. 1002 ¶ 160.

Finally, Patent Owner argues that claims 3, 4, and 11 are further patentable because “neither reference teaches forming vias through the etch-stop layer.” PO Resp. 35–36 (citing Ex. 2001 ¶¶ 117–120). The claims, however, do not recite “vias,” but instead require only “electrical connection,” which, as discussed above, we are persuaded is taught by Petitioner’s combination of Liu and Black.

Given the evidence on this record, we are persuaded that Petitioner has shown that the combination of Liu and Black teaches or suggests all of

the limitations of claims 2–4 and 11, and has articulated sufficient reasoning why it would have been obvious to combine these references in the proposed manner.

2. Obviousness of Claims 5 and 12–16 in View of Liu and Riseman

Claims 5 and 12 depend from claims 1 and 11, respectively, and further recite that “the etchable layer is silicon, the etch-stop layer is silicon dioxide, and the wafer is single-crystal silicon.” Ex. 1001, 8:29–31, 9:10–12. Independent claim 13 recites limitations similar to claim 1, and additionally includes the same specific materials recited in claims 5 and 12 for the etchable layer, the etch-stop layer, and the wafer, respectively. *Id.* at 9:13–26.

As discussed by Petitioner, Riseman “describes an integrated circuit structure, and like Liu, discloses a substrate that includes an etchable layer, an etch-stop layer, and a wafer.” Pet. 37 (citing Ex. 1009, 4:50–57, 5:45–51; Ex. 1002 ¶ 172). Petitioner provides an annotated version of Figure 5 of Riseman, reproduced below (*id.*).

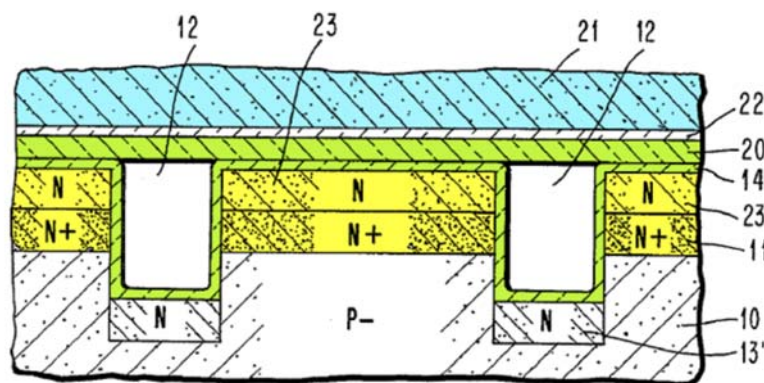


FIG. 5

Petitioner’s annotated figure illustrates the portions of the Riseman device that Petitioner points to as corresponding to an etchable layer (highlighted in

blue), an etch-stop layer (highlighted in green), and a wafer (highlighted in yellow). *Id.* (citing Ex. 1009, 4:50–57, 5:45–57, 6:4–5; Ex. 1002 ¶ 172–175, 190). Petitioner further asserts that, in Riseman, the etchable layer is silicon, the etch-stop layer is silicon dioxide, and the wafer is single-crystal silicon. *Id.* (citing Ex. 1009, 4:50–57, 5:45–57; Ex. 1002 ¶ 173, 174, 190).

According to Petitioner, “[i]t would have been obvious to use Riseman’s single crystal silicon substrate and wafer, and SiO₂ etch-stop layer, in the process flow disclosed in Liu, and doing so would have had no unpredictable results.” *Id.* at 43 (citing Ex. 1002 ¶ 191); *see also id.* at 40–41 (citing Ex. 1003, 1:15–21, 3:9–20; Ex. 1002 ¶¶ 184–187) (discussing reasons one of skill in the art would have used a Si/SiO₂ semiconductor/insulator combination in Liu).

Claims 14–16 depend from claim 13, and recite patterning the etch-stop layer and forming an electrical connection to the microelectronic circuit element through the etch-stop layer and/or wafer. Ex. 1001, 10:1–12.

As discussed above with respect to claims 2–4, Petitioner asserts that Liu discloses patterning the etch-stop layer and wafer around the border of the device. Petitioner similarly relies on this disclosure to meet the limitations of claims 14–16. Pet. 46 (citing *id.* at 25–27; Ex. 1003, 4:59–66; Ex. 1002 ¶ 204). Petitioner also asserts that Riseman discloses such patterning and connection inward from the edge of the device, relying on openings 25 of Riseman. *Id.* at 46–47 (citing Ex. 1009, 6:67–7:1, Fig. 7; Ex. 1002 ¶¶ 204–205). Petitioner provides declaration testimony that one of skill in the art would have recognized the benefits of placing the electrical contacts of Liu inward from the edge of the device, such as the ability to provide more contacts, the ability to reach contacts near the center of the device, or to

provide protection from damage to the contacts. Ex. 1002 ¶ 188; *see* Pet. 47. Petitioner further asserts that to do so would “not have had any unpredictable results.” Pet. 47; *see* Ex. 1002 ¶ 206.

Patent Owner argues that “neither Liu nor Riseman discloses a first substrate in which the etchable layer is silicon, the etch-stop layer is silicon dioxide, and the wafer is single-crystal silicon.” PO Resp. 36 (citing Ex. 2001 ¶ 123). In this regard, Patent Owner notes that Liu teaches the use of III-V semiconductor materials, not silicon (*id.* (citing Ex. 2001 ¶ 124)), and Riseman includes an “SiN insulating layer between the Si and SiO₂, but fails to disclose the ’678 Patent’s three-layered substrate” (*id.* at 37 (citing Ex. 2001 ¶ 125)). As discussed above, however, Petitioner relies on Liu to teach the three-layered substrate and on Riseman to teach the use of the specific silicon-based materials. Thus, Patent Owner’s argument is not persuasive in this regard. *See In re Keller*, 642 F.2d 413, 426 (CCPA 1981) (holding that nonobviousness cannot be established by attacking references individually where the ground of unpatentability is based upon the teachings of a combination of references).

Patent Owner also argues that one of skill in the art “would not combine Liu with Riseman because these references describe different solutions to different problems in the microelectronic fabrication industry.” PO Resp. 37 (citing Ex. 2001 ¶ 126). Patent Owner further argues that “Liu explicitly teaches away from the use of silicon and SiO₂ because these materials ‘hamper’ the performance of CCD devices.” *Id.* (citing Ex. 1003, 1:17–22; Ex. 2001 ¶¶ 126–28). Patent Owner also asserts that Petitioner’s stated motivation (i.e., semiconductor isolation) is “improper.” *Id.* at 38 (citing Ex. 2001 ¶ 129).

As discussed by Petitioner, “Liu already teaches that its CCD can be implemented in ‘other semiconductors,’” and recognizes that CCD devices are *typically* implemented in silicon. Pet. Reply 17 (citing Ex. 1003, 5:9–10, 1:16–17). Although Liu notes that silicon can hamper performance, as Patent Owner asserts to support its teaching away argument, Liu indicates this is only for “some specific applications.” Ex. 1003, 1:18–19; see Pet. Reply 17. We agree with Petitioner that “[w]hen the vast majority of devices [at the time] were made with silicon, Liu’s reference to silicon would not have convinced anyone to avoid it except for certain specific applications.” See Pet. Reply 18; Ex. 1002 ¶ 187; Ex. 2001 ¶ 48; Ex. 2016,¹¹ 2.

Patent Owner also disagrees with Petitioner’s characterization of Riseman’s N⁺ region 11 and silicon pockets 23 as a wafer. PO Resp. 38–39. This argument, however, is premised on Patent Owner’s proposed constructions of the terms “wafer” and “overlying,” which we do not adopt, as previously discussed. See *supra* sections II.A.2, II.A.3. Further, as discussed above, Petitioner relies on Liu to teach the three-layered substrate and on Riseman to teach the use of the specific silicon-based materials; the particular structure of Riseman is not the basis of Petitioner’s obviousness assertion. In any event, as noted by Petitioner, the SiN insulating layer shown in Riseman is described as optional. Pet. Reply 18 (citing Ex. 1009, 5:59–6:5; Ex. 1002 ¶ 175).

Patent Owner also argues that Riseman’s interconnected elements are on the second substrate, not the first substrate, as claimed. PO Resp. 39

¹¹ Gordon E. Moore, *Cramming More Components onto Integrated Circuits*, 86 PROCEEDINGS OF THE IEEE 82–85 (January 1998).

(citing Ex. 2001 ¶ 133). Again, Petitioner relies on Riseman to teach the use of specific silicon-based materials; the particular structure of Riseman is not the basis of Petitioner's obviousness assertion.

Given the evidence on this record, we are persuaded that Petitioner has shown that the combination of Liu and Riseman teaches or suggests all of the limitations of claims 5 and 12–16, and has articulated sufficient reasoning why it would have been obvious to combine these references in the proposed manner.

3. Obviousness of Claim 8 in View of Liu and Oldham, and Claim 18 in view of Liu, Riseman, and Oldham

Claims 8 and 18 depend from claims 1 and 13, respectively, and further recite “placing a layer of epoxy between the second substrate and the wafer portion of the first substrate, and degassing and curing the epoxy.” Ex. 1001, 8:41–45, 10:20–24. For this limitation, Petitioner points to the disclosure in Liu that channel layer 8 with CCD circuit layer 10 (i.e., the claimed wafer portion with its microelectronic circuit elements) is bonded to support 12 (i.e., the claimed second substrate) by sealing layer 14, which may be an epoxy. Pet. 49 (citing Ex. 1003, 3:33–52; Ex. 1002 ¶ 219); *see id.* at 58. Petitioner relies on Oldham as teaching that “the use of an epoxy molding compound with both degassing and curing” was a common practice at the time of the invention. *Id.* at 49–50 (citing Ex. 1005, 3:30–43; Ex. 1002 ¶¶ 220–221); *see id.* at 58. Petitioner further asserts “[i]t would have been obvious to apply steps known to be useful for epoxies . . . to the epoxy of Liu, and there would not have been any unpredictable results.” *Id.* at 50; *see* Ex. 1002 ¶ 223; Pet. 58; *see also* Ex. 1019, 12:20–13:1 (Dr. Fitzgerald admitting that degassing and curing epoxy were standard

steps during the relevant time frame). We agree with Petitioner's assertions regarding these claims.

Patent Owner argues that Oldham does not cure Liu's and Riseman's alleged deficiencies, and also that Oldham is cumulative of other epoxy art considered by the Examiner during prosecution. PO Resp. 39–40, 42. As discussed above, we are persuaded that Liu discloses all the steps of independent claim 1, and that the combination of Liu and Riseman teaches all the steps of independent claim 13. Further, even if Oldham was cumulative of epoxy art considered by the Examiner during prosecution with respect to dependent claims 8 and 18, there is no evidence in the record that Liu, upon which Petitioner relies primarily in challenging the independent claims, was considered by the Examiner.

Given the evidence on this record, we are persuaded that Petitioner has shown that the combination of Liu and Oldham teaches or suggests all of the limitations of claim 8 and that the combination of Liu, Riseman, and Oldham teaches or suggests all of the limitations of claim 18, and that Petitioner has articulated sufficient reasoning why it would have been obvious to combine these references in the proposed manner.

4. Obviousness of Claim 10 in View of Liu and Wen

Claim 10 depends from claim 1, and further recites “contacting the etchable layer to a liquid etchant that attacks the etchable layer rapidly and the etch-stop layer slowly.” Ex. 1001, 8:50–54. Petitioner asserts that Liu discloses such a liquid etchant (Pet. 50 (citing Ex. 1003, 4:53–58; Ex. 1002 ¶¶ 101, 130–131)), while Wen expressly discusses contacting the etchable layer with a liquid etchant that attacks the etchable layer rapidly and the etch-stop layer slowly (*id.* at 50–51 (citing Ex. 1004, 3:67–4:3, 4:11–14,

4:36–40; Ex. 1002 ¶¶ 240–241, 243)). Petitioner further asserts that it “would have been obvious to use known etchants with these known characteristics, as disclosed in Wen, with the process of Liu, without any unpredictable results.” *Id.* at 51–52 (citing Ex. 1002 ¶¶ 235–237). We agree with Petitioner’s assertions regarding claim 10.

Patent Owner argues only that Wen does not does not cure Liu’s alleged deficiencies. PO Resp. 40. As discussed above, we are persuaded that Liu discloses all the steps of independent claim 1. Given the evidence on this record, we are persuaded that Petitioner has shown that the combination of Liu and Wen teaches or suggests all of the limitations of claim 10, and has articulated sufficient reasoning why it would have been obvious to combine these references in the proposed manner.

5. Obviousness of Claim 9 in View of Liu, Wen, and Ying

Claim 9 depends from claim 1, and further recites, “after the step of attaching and before the step of etching, . . . fixing the second substrate to an etching support that is resistant to attack by an etchant.” Ex. 1001, 8:46–49. Petitioner relies on Wen and Ying as teaching this claim element. Pet. 52–54. Wen relates to a method of making semiconductor devices and teaches the use of an etching support. Ex. 1004, 1:36–38, 3:60–62; *see* Ex. 1002 ¶¶ 249–250. Ying relates to the fabrication of small semiconductor devices, and teaches, prior to etching a semiconductor wafer, attaching the wafer to a substrate such as sapphire, which is not capable of being attacked by an etching solution. Ex. 1006, 1:8–11, 3:12–4:28; *see* Ex. 1002 ¶¶ 257–258. Petitioner asserts that “a person of skill in the art would have needed to hold the device [of Liu] while performing etching, and would not have wanted the structure holding the device to be dissolved, as taught by Ying.” Pet. 54

(citing Ex. 1002 ¶ 259). Petitioner further asserts that “[u]sing the structures disclosed in Wen and Ying with the method . . . disclosed in Liu would result in no unpredictable results.” *Id.* We agree with Petitioner’s assertions regarding claim 9.

Patent Owner argues only that Wen and Ying do not cure Liu’s alleged deficiencies. PO Resp. 40–41. As discussed above, we are persuaded that Liu discloses all the steps of independent claim 1. Given the evidence on this record, we are persuaded that Petitioner has shown that the combination of Liu, Wen, and Ying teaches or suggests all of the limitations of claim 9, and has articulated sufficient reasoning why it would have been obvious to combine these references in the proposed manner.

6. Obviousness of Claim 17 in View of Liu, Riseman, and Kusunoki

Claim 17 depends from claim 13, and further recites particular thicknesses for the layers of the device. *See* Ex. 1001, 10:13–18. Petitioner relies on Kusunoki as teaching this claim feature. Pet. 54–57. Kusunoki relates to methods of manufacturing multi-layer semiconductor devices. Ex. 1008, 2. In particular, Petitioner asserts that Kusunoki teaches a wafer (i.e., epitaxial layer (for forming circuit elements)) with a thickness of 5000 Å, an etchable layer (*see, e.g., id.* at Fig. 1A) with a thickness of 500–600 microns, and a SiO₂ layer with a thickness of 1000 to 10,000 Å. Pet. 56 (citing Ex. 1008, 11–12; Ex. 1002 ¶¶ 272–274). Petitioner asserts that these values correspond to the claimed thickness ranges in claim 17. *Id.* (citing Ex. 1002 ¶¶ 272–274). Petitioner further asserts that “a person of ordinary skill could easily have determined acceptable thicknesses for these layers . . . , and Kusunoki and Riseman show that the claimed thicknesses

were not unusual.” *Id.* at 57 (citing Ex. 1002 ¶ 276). Thus, according to Petitioner, “[i]t would have been obvious to one of skill in the art to combine the teachings of Kusunoki regarding these thicknesses, with the teachings of Liu and Riseman regarding the methods for forming microelectronic circuits, with no unpredictable results.” *Id.* (citing Ex. 1002 ¶ 278).

Patent Owner argues that Kusunoki does not cure the alleged deficiencies of the Liu/Riseman combination. PO Resp. 41. As discussed above, we are persuaded that the combination of Liu and Riseman teaches all the steps of independent claim 13.

Patent Owner also argues that Kusunoki does not disclose a *bonded* silicon wafer with the dimensions recited in claim 17. *Id.* As discussed above, however, Petitioner relies on Liu to teach the three-layered substrate, and on Kusunoki to show that the thicknesses recited in claim 17 were known. *See* Pet. Reply 20. Thus, Patent Owner’s argument is not persuasive in this regard. *See In re Keller*, 642 F.2d at 426 (holding that nonobviousness cannot be established by attacking references individually where the ground of unpatentability is based upon the teachings of a combination of references).

Patent Owner also argues that one of skill in the art would not combine the references in the manner asserted by Petitioner. PO Resp. 41–42. Patent Owner argues that, because Liu does not disclose any thickness limitations, one of skill in the art would not seek to limit the substrate thickness with a narrowing reference (i.e., one which teaches specific thicknesses), and that the only reason to do so is hindsight bias. *Id.* We agree with Petitioner, however, that “anyone who implements Liu’s invention needs to pick a substrate thickness” and that “Kusunoki shows that

the thicknesses of claim 17 were known.” Pet. Reply 20. Further, as noted by Petitioner, the Specification of the ’678 patent acknowledges that the claimed thicknesses “are not critical, and may be varied as necessary.” See Ex. 1001, 4:13–14.

Given the evidence on this record, we are persuaded that Petitioner has shown that the combination of Liu, Riseman, and Kusunoki teaches or suggests all of the limitations of claim 17, and has articulated sufficient reasoning why it would have been obvious to combine these references in the proposed manner.

7. Secondary Considerations

Patent Owner argues that secondary considerations, including industry praise, failure of others, and commercial success, heavily weigh against a finding that the claims of the ’678 patent are obvious. See PO Resp. 43–49. We discuss each of Patent Owner’s objective indicia of nonobviousness in turn.

Industry Praise

Patent Owner presents evidence of purported industry praise. PO Resp. 43–45. In particular, Patent Owner presents evidence that back-illuminated (“BSI”) technology has received industry praise. *Id.* For example, Patent Owner cites to a Sony news release, dated June 11, 2008, which praises BSI technology as delivering “an even higher quality image experience.” *Id.* at 44 (citing Ex. 2026¹²). Patent Owner also points to another Sony news release, dated August 20, 2012, in which “Sony lauded

¹² Sony Global – News Release, *Sony Develops Back-Illuminated CMOS Image Sensor, Realizing High Picture Quality, Nearly Twofold Sensitivity And Low Noise* (June 11, 2008).

what it believed was a ‘unique, newly-developed “stacked structure”’ ‘which combine superior image quality and advanced functionality with compact size.’” *Id.* (citing Ex. 2027¹³). Patent Owner also points to other evidence that purports to demonstrate that “[o]ther competitors, like OmniVision, also praised the breakthroughs offered by BSI technology.” *Id.* (citing Ex. 2028,¹⁴ 5; Ex. 2029,¹⁵ 9; Ex. 2010¹⁶). Patent Owner further argues that “[i]t took Petitioner [Sony] and OmniVision years before they were able to practice the patented process that Raytheon had been commercializing for over a decade.” *Id.* at 45.

We agree with Petitioner, however, that the “alleged praise is directed to the advantages of BSI sensors [generally] as compared to front-side illuminated sensors,” rather than to sensors formed by the claimed process. Pet. Reply 21. For example, the OmniVision presentation (Ex. 2029), upon which Patent Owner relies, indicates that although BSI sensors “have been used for many years in highest performance applications,” such as astronomy, military, and scientific applications, these “devices were expensive due to fragility and processing costs.” Ex. 2029, 6. The OmniVision presentation indicates that OmniVision’s “breakthrough [is] the ability to mass produce very small, cost effective BSI pixels for high performance products,” rather than implementation of a BSI sensor

¹³ Sony Global – News Release, *Sony Develops “Exmor RS,” The World’s First Stacked CMOS Image Sensor* (Aug. 20, 2012).

¹⁴ OmniVision, *OmniBSI™ Technology Backgrounder* (June 22, 2009).

¹⁵ OmniVision, *OmniBSI™ Technology*, Slide Presentation.

¹⁶ OmniVisionTech YouTube Video, *OmniVision’s Backside Illumination (BSI) Explained* (also available at <https://www.youtube.com/watch?v=fyg1DCVLqzg>).

generally. *Id.* In fact, the OmniVision technology does even not use the silicon on insulator (SOI) wafers to implement its BSI sensors, which is the technology discussed in the '678 patent. *See* Ex. 2029, 9–10; Ex. 2001 ¶ 41 (Dr. Fitzgerald discussing that the preferred embodiments of the '678 patent use SOI substrates). Further still, Liu, upon which all the obviousness grounds are based, itself teaches a BSI sensor, and advantages thereof. Ex. 1003, at [54], 2:50–54; *see* Pet. Reply 21–23.

Accordingly, we assign the evidence of industry praise little weight in our overall obviousness analysis.

Failure of Others

Patent Owner presents evidence of purported failure of others. PO Resp. 45–46. Patent Owner argues that “[n]o one except Raytheon could commercialize BSI structure until the late 2000’s.” *Id.* at 45 (citing Ex. 2010; Exs. 2026–2029). Petitioner argues that Patent Owner does not present any evidence that others have failed, but “merely assumes that others were trying to make BSI devices, assumes that these devices were never made, and then assumes that the (assumed) inability to make [such] devices was related to the non-obviousness of the '678 patent method.” Pet. Reply 23; *see id.* at 23–25.

We agree with Petitioner that any actual evidence of failure of others is lacking. Patent Owner’s only evidence for failure of others is that Sony and OmniVision did not come out with their products until the mid-2000s. There is no evidence in the record, however, that they were attempting to do so. Also, the OmniVision materials recognize that the technology was available earlier, but was not commercially viable, except in, for example, astronomy and military applications, which are the industries in which

Raytheon asserts it was able to commercially exploit its process. *See, e.g.*, Ex. 2029, 6; Ex. 2008 ¶ 5.

Patent Owner also points to the age of the references cited in this *inter partes* review, and argues that “[t]he Federal Circuit has recently held that an extended gap in time between the ‘background of useful knowledge’ and the patent at issue is evidence that the ‘claimed invention was not obvious to try.’” PO Resp. 45–46 (citing *Leo Pharm. Prods., Ltd. v. Rea*, 726 F.3d 1346, 1356 (Fed. Cir. 2013)). However, the Federal Circuit also has held that “[a]bsent a showing of long-felt need or the failure of others, the mere passage of time without the claimed invention is not evidence of nonobviousness.” *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1325 (Fed. Cir. 2004).

The record evidence does not support a finding of failure of others. Thus, we assign Patent Owner’s evidence of failure of others little weight in our overall obviousness analysis.

Commercial Success

Patent Owner also presents evidence of purported commercial success. PO Resp. 46–49. In particular, Patent Owner proffers declaration testimony of Mr. John J. Drab, Senior Principle Engineer at Raytheon, that “Raytheon identified a commercial opportunity for the process disclosed in the ’678 Patent [as part of its business] in fabricating high-resolution sensors for government defense work and space programs.” Ex. 2008 ¶ 5 (citing Ex. 2009¹⁷); PO Resp. 47. According to Patent Owner, the BepiColombo

¹⁷ R. E. Mills et al., *Advanced staring Si PIN visible sensor chip assembly for Bepi-Colombo mission to Mercury*, 7439 PROC. OF SPIE 74390A-1 – 9 (2009).

space telescope uses a sensor manufactured by the methods of claims 1–3, 6, 7, 10–14, and 17 of the '678 patent. PO Resp. 47–48 (citing Ex. 2009, 1). Patent Owner asserts that “[t]his microelectronic device is a high–resolution, stacked, visible-range sensor” (*id.* at 48 (citing Ex. 2009, 2)), the features of which “align with the advantages explicitly described in the '678 Patent’s specification” (*id.* (citing Ex. 1001, 2:5–9, 2:29–42, 2:59–3:5)). Patent Owner also asserts that the '678 patent “won Raytheon other lucrative contracts from the United States Air Force.” *Id.* at 49 (citing Ex. 2008 ¶ 8).

Patent Owner proffers no analysis comparing the claims to the BepiColombo sensor’s manufacturing process, beyond Patent Owner’s conclusory allegation that the sensor chip used in the BepiColombo space telescope embodies the claims of the '678 patent. We recognize the Federal Circuit’s guidance that “[w]hen the patentee has presented undisputed evidence that its product is the invention disclosed in the challenged claims, it is error for the Board to find to the contrary without further explanation.” *PPC Broadband, Inc. v. Corning Optical Commc’ns RC, LLC*, 815 F.3d 734, 747 (Fed. Cir. 2016). In any event, in this case, there is evidence that any commercial success was due to unclaimed features of device. *See Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1312 (Fed. Cir. 2006) (holding that evidence that commercial success was due to unclaimed or non-novel features of device “clearly rebuts the presumption that [the product’s] success was due to the claimed and novel features”).

The description of the sensor chip assembly in the BepiColombo space telescope article, upon which Patent Owner relies to show commercial success, describes technology beyond that covered by the '678 patent. As described in the '678 patent, “techniques such as indium bumps [are used] to

form the interconnections between the stacked devices.” Ex. 1001, 2:41–42; *see also id.* at 3:10–12 (“interconnections between the two microelectronic circuit elements are made at this point, as by using an indium-bump technique/epoxy technique”). However, the BepiColombo space telescope article describes that the oxide bond interconnect solution used in sensor chip thereof “eliminate[s] the need for indium bumps altogether,” which *avoids the disadvantages thereof*, such as the need for epoxy. Ex. 2009, 3; *see* Ex. 1021 (Deposition of Mr. Drab), 29:6–38:6, 52:23–56:2. We, therefore, are not persuaded that Patent Owner’s evidence of commercial success is attributed primarily to the claimed process, but instead is attributed, at least in part, to the “novel interconnect solution.” Ex. 2009, 9; Pet. Reply 26–27. This is particularly true given that the BepiColombo space telescope project was happening over ten years after the issue date of the ’678 patent.

We, thus, assign the evidence of commercial success little weight in our overall obviousness analysis.

8. Conclusion on Obviousness

We have considered the entirety of the evidence, both Petitioner’s evidence of obviousness and Patent Owner’s evidence regarding objective indicia of nonobviousness. On balance, we determine that a preponderance of the evidence supports the following conclusions:

Claims 2–4 and 11 of the ’678 patent would have been obvious over the combined teachings of Liu and Black;

Claims 5, 12, and 13–16 of the ’678 patent would have been obvious over the combined teachings of Liu and Riseman;

Claim 8 of the '678 patent would have been obvious over the combined teachings of Liu and Oldham;

Claim 18 of the '678 patent would have been obvious over the combined teachings of Liu, Riseman, and Oldham;

Claim 10 of the '678 patent would have been obvious over the combined teachings of Liu and Wen;

Claim 9 of the '678 patent would have been obvious over the combined teachings of Liu, Wen, and Ying; and

Claim 17 of the '678 patent would have been obvious over the combined teachings of Liu, Riseman, and Kusunoki.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1–4, 6, 7, 10, and 11 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Liu; that claims 2–4 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Liu and Black; that claims 5 and 12–16 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Liu and Riseman; that claim 8 is unpatentable under 35 U.S.C. § 103(a) as obvious in view of Liu and Oldham; that claim 10 is unpatentable under 35 U.S.C. § 103(a) as obvious in view of Liu and Wen; that claim 9 is unpatentable under 35 U.S.C. § 103(a) as obvious in view of Liu, Wen, and Ying; that claim 17 is unpatentable under 35 U.S.C. § 103(a) as obvious in view of Liu, Riseman, and Kusunoki; and that claim 18 is unpatentable under 35 U.S.C. § 103(a) as obvious in view of Liu, Riseman, and Oldham.

IV. MOTIONS TO SEAL

The Board granted the parties' Motion for Entry of a Modified Protective Order on October 11, 2016. Paper 39; *see* attachment to Paper 30 (protective order). There are two Motions to Seal pending in this proceeding. Paper 30 (Petitioner's Motion); Paper 37 (Patent Owner's Motion). Neither motion is opposed. Paper 30, 3; Paper 37, 3. Except where a party requests sealing a document in its entirety, redacted public versions of the documents sought to be sealed have been filed. *See* Paper 30.

There is a strong public policy that favors making information filed in an *inter partes* review open to the public. *Garmin Int'l, Inc. v. Cuozzo Speed Techs. LLC*, Case IPR2012-00001, slip op. at 1–2 (PTAB Mar. 14, 2013) (Paper 34). The standard for granting a motion to seal is good cause. 37 C.F.R. § 42.54. That standard includes showing that the information addressed in the motion to seal is truly confidential, and that such confidentiality outweighs the strong public interest in having the record open to the public. *See Garmin*, slip op. at 2–3.

We have considered the arguments presented by the parties and determine that good cause has been established for sealing the documents identified in the Motions to Seal. Specifically, the parties demonstrate that the information sought to be sealed reflects information covered by The International Traffic in Arms Regulations ("ITAR") (*see* 22 C.F.R. Parts 120–130) and/or is Patent Owner's confidential information. Paper 30; Paper 37.

Accordingly, we grant the parties' Motions to Seal. The record will be maintained undisturbed pending the outcome of any appeal taken from

this Decision. At the conclusion of any appeal, or if no appeal is taken, the documents may be made public. See *Trial Practice Guide*, 77 Fed. Reg. 48,756, 48,761 (Aug. 14, 2012). Further, either party may file a motion to expunge sealed documents from the record pursuant to 37 C.F.R. § 42.56. Any such motion will be decided after the conclusion of any appeal or the expiration of the time period for appealing.

V. ORDER

Accordingly, it is

ORDERED that claims 1–18 of U.S. Patent No. 5,591,678 are held *unpatentable*;

FURTHER ORDERED that Petitioner’s Motion to Seal (Paper 30) is *granted*;

FURTHER ORDERED that Patent Owner’s Motion to Seal (Paper 37) is *granted*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 5,591,678

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