

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
and
QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC.,
GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN
MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES DRESDEN
MODULE TWO LLC & CO. KG,
Petitioner,

v.

DSS TECHNOLOGY MANAGEMENT, INC.,
Patent Owner.

Case IPR2016-00288¹
Patent 6,784,552 B2

Before BRYAN F. MOORE, BRIAN J. McNAMARA, and
MINN CHUNG, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Case IPR2016-01314 has been joined with this proceeding.

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Intel Corporation, Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, and Globalfoundries Dresden Module Two LLC & Co. KG (collectively, “Petitioner”) challenge the patentability of claims 8–12 (the “challenged claims”) of U.S. Patent No. 6,784,552 B2 (Ex. 1101, “the ’552 patent”), owned by DSS Technology Management, Inc. (“Patent Owner”). The Board has jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). With respect to the grounds instituted in this trial, we have considered the papers submitted by the parties and the evidence cited therein. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 8–12 of the ’552 patent are unpatentable.

A. Procedural History

On December 8, 2015, Intel Corporation filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 8–12 of the ’552 patent. Patent Owner filed a Preliminary Response (Paper 7, “Prelim. Resp.”). On June 8, 2016, we instituted an *inter partes* review of claims 8–12 of the ’552

patent based on the ground that the challenged claims are anticipated by Heath.² Paper 11 (“Dec. on Inst.”), 28.

After institution, Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, and Globalfoundries Dresden Module Two LLC & Co. KG (collectively, “Qualcomm”) filed a petition requesting *inter partes* review of claims 8–12 of the ’552 patent on the same grounds asserted by Intel Corporation, accompanied by a timely motion seeking joinder with this proceeding. IPR2016-01314, Papers 3 (petition), 4 (motion for joinder).³ Patent Owner did not oppose the joinder. We instituted an *inter partes* review and joined it with the present proceeding. Papers 18, 19.

On September 7, 2016, Patent Owner filed a Patent Owner Response (Paper 20, “PO Resp.”) that contained no citations to evidence and no argument, other than noting that, in contrast to the standard applied in reaching a decision to institute (i.e., a reasonable likelihood Petitioner will prevail on its challenge to patentability of a claim), the standard for reaching a final decision is whether the Petitioner proved unpatentability by a preponderance of the evidence. PO Resp. 2. Patent Owner then stated that it “defers to the Board to make this determination based on its impartial analysis of the prior art and Petitioners’ arguments.” *Id.*

² Ex. 1103, U.S. Patent No. 4,686,000 (Aug. 11, 1987) (“Heath”).

³ Because Qualcomm’s petition in IPR2016-01314 is identical in all substantive aspects to the Petition in this proceeding (*see* Paper 18, 8), we cite only to the Petition throughout this Final Written Decision.

In its Reply (Paper 21, “Pet. Reply”) filed on December 7, 2016, Petitioner stated that Patent Owner has not cross-examined Petitioner’s expert, John C. Bravman, Ph.D., or provided any testimony that contradicts Dr. Bravman’s testimony, and that the challenged claims should be found unpatentable. Pet. Reply 1–2.

No hearing was held because we determined oral argument is not necessary to render a final written decision in this proceeding. See Paper 24, 2.

B. Related Proceedings

According to the parties, the ’552 patent is the subject of the following patent infringement cases: *DSS Tech. Mgmt., Inc. v. Intel Corp.*, Case No. 6:15-cv-130-JRG (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. Samsung Elec. Co., Ltd.*, Case No. 6:15-cv-690 (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. SK Hynix, Inc.*, Case No. 6:15-cv-691 (E.D. Tex.); and *DSS Tech. Mgmt., Inc. v. Qualcomm, Inc.*, Case No. 6:15-cv-692 (E.D. Tex.). Pet. 7; Paper 6, 2–3.

In related proceedings before the Board, we instituted *inter partes* reviews of claims 1–7 of the ’552 patent in IPR2016-00287 and IPR2016-01311.⁴ The ’552 patent is also the subject of an instituted trial proceeding *Samsung Elec. Co., Ltd. v. DSS Tech. Mgmt., Inc.*, Case IPR2016-00782. Additionally, we instituted *inter partes* reviews of claims of U.S. Patent

⁴ Case IPR2016-01311 has been joined with IPR2016-00287.

No. 5,965,924 in *Intel Corp. v. DSS Tech. Mgmt., Inc.*, Cases IPR2016-00289, IPR2016-00290, IPR2016-01312, and IPR2016-01313.⁵

II. THE '552 PATENT

A. Described Invention

The '552 patent describes a process of semiconductor device fabrication and a structure of a semiconductor device having “substantially rectangular” lateral insulating spacers adjacent to gate electrodes. Ex. 1101, Abstract. The '552 patent defines the term “substantially rectangular” to mean that “a side of the spacer has an angle relative to the substrate surface of more than 85°.” *Id.* at col. 8, ll. 40–42.

Figure 4(D) of the '552 patent is reproduced below.

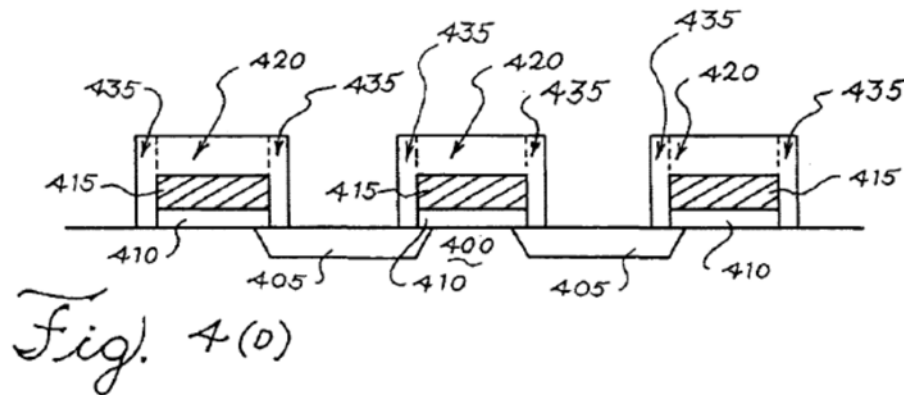


Figure 4(D) illustrates a cross-sectional view of a series of gates 415 (also called conducting layers or polysilicon layers) completely encapsulated in insulating material 420, e.g., TEOS (tetraethyl orthosilicate glass), where spacers or spacer portions 435 of the insulating material adjacent to the gates

⁵ Cases IPR2016-01312 and IPR2016-01313 have been joined with IPR2016-00290 and IPR2016-00289, respectively.

have substantially rectangular profiles. *Id.* at col. 9, ll. 9–13; col. 11, ll. 40–46. As shown in Figure 4(D), gates 415 are insulated from sources or drains 405 by insulating dielectric layers 410. *See id.* at col. 10, ll. 49–50. The '552 patent describes a process of making high quality contacts to the sources or drains, such as “self-aligned” contacts, by etching structures over substrate 400 and sources or drains 405. *Id.* at col. 7, ll. 19–22; col. 8, ll. 4–6.

Figure 4(I) of the '552 patent is reproduced below.

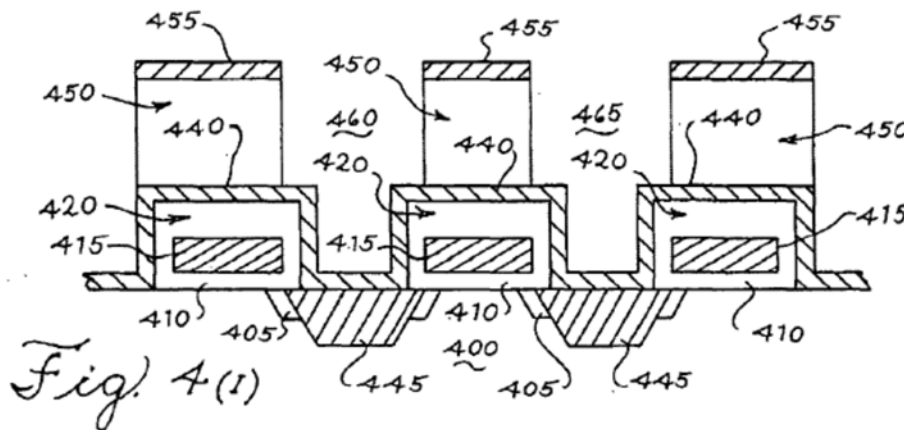


Figure 4(I) illustrates additional structures deposited and etched over the structure described in Figure 4(D), such as second dielectric layer 440 (called etch stop layer), blanket layer 450, and photoresist mask layer 455. *Id.* at col. 9, ll. 33–39; col. 11, ll. 63–65; col. 12, ll. 34–42. According to the '552 patent, etch stop layer 440, e.g., silicon nitride layer 440, depicted in Figure 4(I) is distinct or different from the underlying TEOS insulating layer. *Id.* at col. 12, ll. 10–11. The etch stop layer protects the underlying

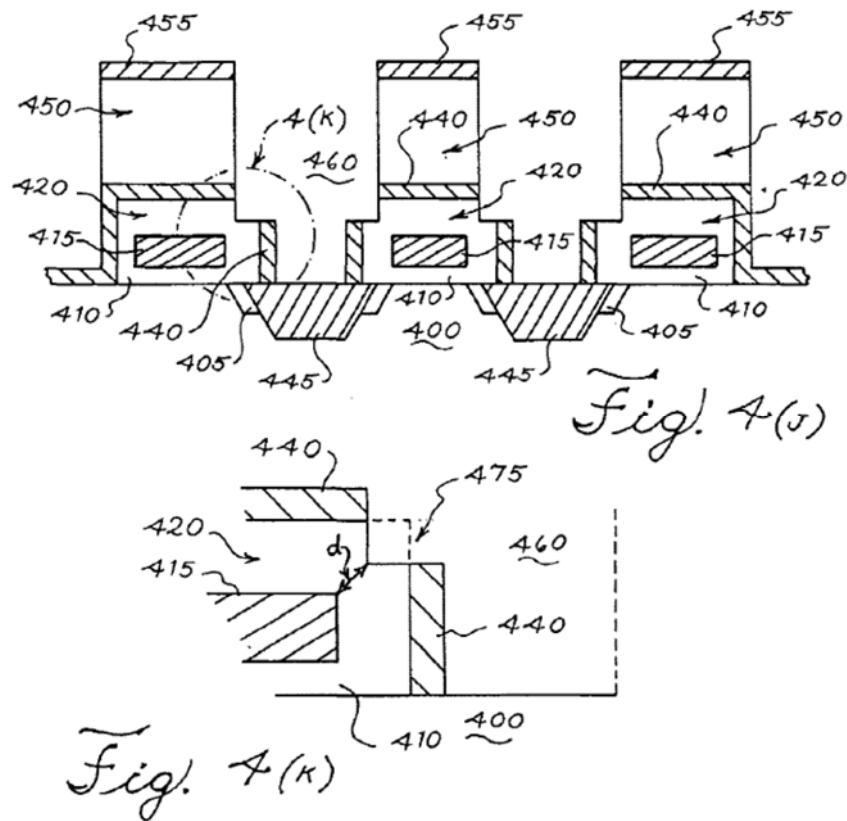
TEOS layer when blanket layer 450 made of BPTEOS⁶ is etched away to create contact openings 460 and 465 above source or drain 445. *See id.* at col. 12, ll. 36–42; col. 4, ll. 41–59.

A second etch is then performed to remove etch stop layer 440 covering source or drain 445 in contact openings 460 and 465. *Id.* at col. 12, ll. 48–52; col. 7, ll. 43–45. The '552 patent describes that the second etch is “almost completely anisotropic,” which means that the etchant etches in the vertical direction, or perpendicular relative to the substrate surface. *Id.* at col. 7, ll. 45–48; col. 12, ll. 55–58. Hence, the etch removes the etch stop material covering the area of the contact openings or contact regions 460 and 465, but does not significantly etch the etch stop material adjacent to the spacer portions 435.⁷ *Id.* at col. 7, ll. 53–55; col. 12, ll. 58–61.

⁶ BPTEOS is an acronym for borophosphosilicate tetraethyl orthosilicate glass. *See* Ex. 1101, col. 11, ll. 6–7.

⁷ As discussed above, spacer portions 435 are illustrated in Figure 4(D) and the accompanying text. *See* Ex. 1101, col. 11, ll. 40–46, Fig. 4(D).

Figures 4(J) and 4(K) of the '552 patent are reproduced below.



Figures 4(J) and 4(K) illustrate the structure of the semiconductor device of the '552 patent after the second etch for removing the etch stop layer from the contact regions 460 and 465 is completed. As shown in Figures 4(J) and 4(K), due to the anisotropic or vertical nature of the second etch, only a small portion, i.e., portion 475, of the TEOS spacer portion 435 is removed during the etch. *Id.* at col. 13, ll. 6–9. Of primary significance, according to the '552 patent, the spacer portion 435 of the TEOS insulating layer 420 retains its substantially rectangular profile, in contrast to the conventional prior art method which transforms a substantially rectangular spacer into a sloped spacer. *Id.* at col. 13, ll. 9–10; col. 7, ll. 48–51; col. 5, ll. 4–14.

B. Illustrative Claim

Claim 8 is illustrative of the challenged claims and is reproduced below with the key limitation (the “angle limitation”) emphasized in *italics*:

8. A structure, comprising:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer;

(e) a blanket layer over the etch stop material; and

(f) an opening through a first part of the etch stop material to the first electrically conductive material,

wherein a side of the electrically insulative spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.

III. CLAIM CONSTRUCTION

As acknowledged by the parties, the ’552 patent has expired. Pet. 28; Prelim. Resp. 14. Thus, we construe the claims in accordance with the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See *In re CSB-Sys. Int’l, Inc.*, 832 F.3d 1335, 1341 (Fed. Cir. 2016) (“[W]hen an expired patent is subject to reexamination, the traditional *Phillips* construction standard attaches.”) (citing *In re Rambus*, 694 F.3d 42, 46 (Fed. Cir. 2012)); *Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed.

App’x 1019, 1024 (Fed. Cir. 2016) (holding that in an *inter partes* review, “[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in [*Phillips*]”).

In the Decision on Institution, applying the *Phillips* standard, we preliminarily interpreted the “angle limitation” set forth above—i.e., the limitation reciting “a side of the electrically insulative spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°”⁸—to mean “a side of the electrically insulative spacer has an angle relative to the substrate surface that is greater than 85° and less than or equal to 90°.” Dec. on Inst. 8–14. Importantly, we were unpersuaded by Patent Owner’s argument that the angle of a side of the insulating spacer must be obtained “through the use of a low selectivity etch” (Prelim. Resp. 15–19) and determined that the challenged claims do not require the use of a low selectivity etch. Dec. on Inst. 8–12.

⁸ Claim 1 includes essentially the same limitation, the only difference being that claim 1 recites “insulating spacer” instead of “electrically insulative spacer” recited in claim 8. Tracking the language of the claims, the ’552 patent uses the terms “insulating spacer” and “insulative spacer” interchangeably throughout the written description. See, e.g., Ex. 1101, col. 6, ll. 13–65; see also *id.* at col. 13, ll. 55–62 (using “the spacer portions of the insulating material” and “the spacer portions [of] insulative material” interchangeably). The parties also appear to use the terms “insulating spacer” and “insulative spacer” interchangeably in the Petition and the Preliminary Response. See, e.g., Pet. 28–29; Prelim. Resp. 15–16, 19. Upon considering the complete record, we deem the terms “insulating spacer” and “insulative spacer” to be interchangeable and to have no meaningful difference in their meaning in the context of the ’552 patent.

The parties do not present additional claim construction arguments in their Patent Owner Response and Petitioner Reply. Upon considering the complete record, we discern no reason to deviate from our construction, which was adopted from the parties' agreed construction at the district court (Dec. on Inst. 14 (citing Ex. 1124 (Dist. Ct. Claim Construction Order), 7–8)), and maintain our construction of the “angle limitation” to mean “a side of the electrically insulative spacer has an angle relative to the substrate surface that is greater than 85° and less than or equal to 90°.”

No other claim terms need to be construed expressly for purposes of this Final Written Decision. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (explaining that “claim terms need only be construed ‘to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

IV. ANALYSIS OF PETITIONER’S PRIOR ART CHALLENGES

As previously discussed, the Patent Owner Response does not contain any substantive argument or citations to evidence. Although it remains Petitioner’s burden to prove unpatentability by a preponderance of the evidence, in our Scheduling Order, we cautioned Patent Owner that “any arguments for patentability not raised in the response will be deemed waived.” *See* Paper 12, 4–5. Patent Owner elected not to respond substantively and, instead, “defers to the Board” to determine whether Petitioner has demonstrated the challenged claims are unpatentable by a preponderance of the evidence. PO Resp. 2. Under the particular

circumstance of this case, for purposes of this Final Written Decision, we exercise our discretion to consider Patent Owner's substantive patentability arguments in its Preliminary Response in reaching a decision as set forth below. *See* 37 C.F.R. § 42.5(a).

A. Anticipation by Heath

Petitioner asserts that claims 8–12 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Heath. Pet. 34–47. Petitioner provides detailed explanations and specific citations to Heath indicating where in the reference the claimed features are disclosed. *Id.* In addition, Petitioner relies upon the Declaration of John C. Bravman, Ph.D. (“Bravman Decl.,” Ex. 1102) to support its position. *Id.* Upon review of all of the parties' papers and supporting evidence discussed in those papers, we are persuaded that Petitioner has demonstrated, by a preponderance of evidence, that claims 8–12 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Heath.

1. Principles of Law

A claim is unpatentable under 35 U.S.C. § 102 only if a single prior art reference expressly or inherently describes each and every limitation set forth in the claim. *See Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005); *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987). Further, a reference cannot anticipate “unless [it] discloses within the four corners of the document not only all of the limitations claimed[,] but also all of the limitations arranged or combined in the same way as recited in the claim.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be

arranged in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). We analyze this asserted ground based on anticipation with the principles identified above in mind.

2. Overview of Heath

Heath describes a process for forming a self-aligned contact window in a semiconductor device, such as an integrated circuit. Ex. 1103, Abstract. Heath describes a two-step etching process which comprises the steps of first etching a dielectric layer down to a silicon nitride etch stop layer, and then etching the etch stop, leaving a “stick” of the etch stop material on the vertical sidewall of the layer to be protected. *Id.*

Figure 8B of Heath is reproduced below.

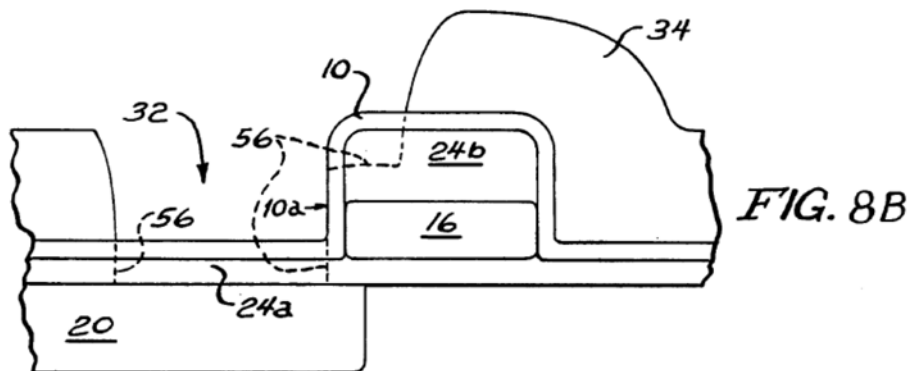


Figure 8B depicts a cross-sectional view of a semiconductor structure after the first etching step, including gate electrode 16 insulated from contact window 32 and source or drain 20 by silicon nitride layer 10. *See id.* at col. 9, ll. 50–67. In the second etching step, etch stop layer 10 is removed to open contact window 32 to source or drain 20. Heath describes that, because

the nitride removal is anisotropic, vertical “stick” 10a of nitride layer 10 will remain on the side of gate electrode 16 so that no electrical short occurs between the gate electrode and the contact window or the source or drain region. *Id.* at col. 10, ll. 1–11.

3. Discussion

a. Claim 8

Petitioner asserts that the embodiment depicted in Figure 8C of Heath discloses every limitation of claim 8. Pet. 34. According to Petitioner, Heath is directed to the same problem as the ’552 patent—i.e., avoiding a short-circuit between the contact and the gate electrode—and describes solving the problem in the same way—that is, through the use of a non-conductive sidewall spacer with vertical sides. *Id.* at 25 (citing Ex. 1103, Abstract; Ex. 1102 ¶ 60). Petitioner references Figure 8C of Heath and asserts that Heath discloses a transistor structure consisting of the same components arranged in the same way as the invention of the ’552 patent. *Id.* at 25–26 (identifying various components depicted in Fig. 8C and citing Ex. 1103, Abstract, Fig. 8C, col. 5, ll. 26–30, col. 10, ll. 2–13; Ex. 1102 ¶¶ 61, 62).

Figure 8C of Heath is reproduced below.

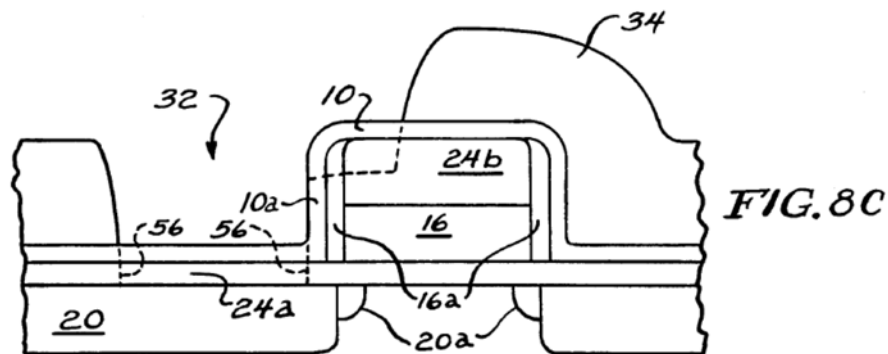


Figure 8C above depicts a cross-sectional view of a semiconductor structure at the same stage of processing as Figure 8B (reproduced in Overview of Heath section above) combined with the addition of a sidewall spacer 16a. Ex. 1103, col. 10, ll. 14–19. Referencing Figure 8C, Petitioner provides detailed explanations and specific citations to Heath indicating where in the reference each limitation of claim 8 is disclosed. Pet. 34–43. For the reasons discussed below, we are persuaded that Heath discloses each limitation of independent claim 8 as arranged in the claim.

i. Preamble and Elements (a), (b), (c), (d), (e), and (f)

Beginning with the preamble of claim 8, Petitioner cites Heath’s disclosure of a transistor structure in Figure 8C as disclosing a “structure” recited in claim 8. *Id.* at 34 (citing Ex. 1103, col. 10, ll. 33–35, Fig. 8C; Ex. 1102 ¶ 78). We agree with Petitioner that Figure 8C of Heath discloses a “structure” recited in claim 8 because, as noted by Petitioner, Heath describes methods to “produce a *transistor structure* which has source/drain implants like those shown in FIG. 8C.” *Id.* (quoting Ex. 1103, col. 10, ll. 33–35); *see also id.* at 25–26 (Petitioner arguing that Figure 8C of Heath discloses a transistor structure consisting of the same components arranged in the same way as the invention of the ’552 patent). As discussed above, both the ’552 patent and Heath describe a process of forming a self-aligned contact structure in a semiconductor device. Ex. 1101, Abstract, col. 7, ll. 19–22, col. 8, ll. 4–6 (“The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts.”); Ex. 1103, Abstract.

Petitioner next addresses the limitations recited in the body of claim 8. Claim 8 numbers from (a) to (f) the elements recited in the body of the claim and recites the numbered elements as follows: (a) a first electrically conductive material formed in and/or on a surface of a substrate; (b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate; (c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material; (d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer; (e) a blanket layer over the etch stop material; and (f) an opening through a first part of the etch stop material to the first electrically conductive material.

Claim 8 recites two distinct “electrically conductive material” elements formed on a substrate: “(a) a first electrically conductive material formed in and/or on a surface of a substrate” and “(b) . . . a second electrically conductive material formed on the substrate.” Petitioner asserts that Figures 2 and 8C of Heath disclose both of these “electrically conductive material” limitations. Pet. 34–37.

Petitioner asserts that source/drain 20 depicted in Figure 8C discloses “(a) a first electrically conductive material formed in and/or on a surface of a substrate,” as recited in claim 8. *Id.* at 34–36 (citing Ex. 1103, col. 8, ll. 2–5; col. 9, ll. 50–55; Figs. 2–7, 8C), 35 n.7 (citing Ex. 1103, col. 7, ll. 36–41, 56–58; Figs. 2–7). Citing the testimony of Dr. Bravman, Petitioner argues that sources and/or drains are known in the art to be electrically conductive diffusion regions of a transistor structure. *Id.* at 36 (citing Ex. 1102 ¶ 79).

Petitioner further argues that Figures 2 and 3 of Heath and their accompanying text disclose source/drain 20 as a diffusion region, which is formed on substrate 12 by arsenic, boron or phosphorous implantation. *Id.* at 35 n.7 (citing Ex. 1103, col. 7, ll. 36–41, 56–58; Figs. 2–7; Ex. 1102 ¶ 79 n.5), 36 (citing Ex. 1103, col. 8, ll. 2–5).

Petitioner also asserts that gate electrode 16 depicted in Figure 8C discloses “a second electrically conductive material formed on the substrate,” as recited in element (b) of claim 8. *Id.* at 36–37 (citing Ex. 1103, col. 7, ll. 36–38; col. 8, ll. 8–11; col. 9, ll. 44–47, 50–52; Figs. 2, 8C). Petitioner notes that Heath discloses gate electrode 16 is made of doped polysilicon, which Petitioner argues, citing the testimony of Dr. Bravman, a person of ordinary skill in the art would understand to be electrically conductive in a transistor structure. *Id.* at 36–37 (citing Ex. 1103, col. 8, ll. 8–11; Ex. 1102 ¶ 80). Petitioner further argues that Figure 2 of Heath shows gate electrodes 14 and 16 are formed on substrate 12 as part of the same process of forming the structure depicted in Figure 8C. *Id.* at 37 (citing Ex. 1103, col. 7, ll. 36–38, Fig. 2).

We agree with Petitioner that source/drain 20 shown in Figures 2 and 8C is a diffusion region formed on substrate 12 because, as noted by Petitioner, Heath discloses that

FIG. 2 illustrates a layer 10 operable as an etch stop and a *substrate 12* having poly gate electrodes 14 and 16 over a relatively thin gate oxide 18. Between the gate electrodes but *in the substrate* is an arsenic, phosphorous or boron implant 20 which acts as a transistor *source or drain*.

Id. at 35 n.7 (quoting Ex. 1103, col. 7, ll. 36–41). We also agree that Figures 2 and 8C disclose gate electrode 16 formed on substrate 12 because, as cited by Petitioner, Heath discloses that “FIG. 2 illustrates a layer 10 operable as an etch stop and a *substrate 12* having poly *gate electrodes 14 and 16* over a relatively thin gate oxide 18” (*id.* at 37 (quoting Ex. 1103, col. 7, ll. 36–38)), “FIGS. 8A, 8B and 8C relate to establishing a contact window to a source/drain region next to a *gate electrode* or field-shield electrode 16 . . .” (*id.* at 36 (quoting Ex. 1103, col. 9, ll. 44–47)), and “FIGS. 8A and 8B show a *gate electrode 16* and an active area 20 *in the substrate* to the left of gate electrode 16” (*id.* (quoting Ex. 1103, col. 9, ll. 50–52) (emphases added)). In addition, we are persuaded that Figures 2 and 8C are part of the same disclosure in Heath because both figures illustrate the process of forming a self-aligned contact window in a semiconductor device. See Ex. 1103, col. 2, ll. 28–32 (“FIG. 2 shows an illustrative semiconductor structure near the completion of processing according to the invented process applied illustratively for establishing a *self-aligned contact window* to a gate electrode or field-shield electrode edge.” (emphasis added)), col. 11, ll. 11–13 (“As a result of the process described with reference to FIGS. 8 and 9, *the contact window* to the active area will be *self-aligned*, i.e., it will be protected from shorting to an element nearby to which contact is not to be made.” (emphases added)).

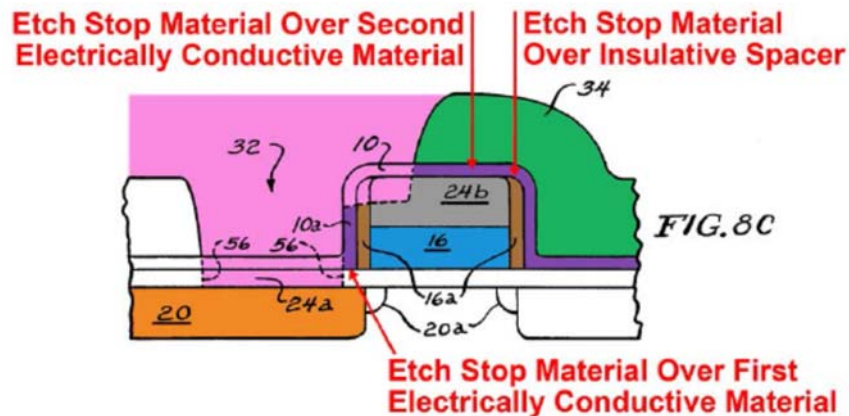
We credit Dr. Bravman’s testimony and are persuaded that sources and/or drains are known in the art to be electrically conductive diffusion regions of a transistor structure, and that polysilicon used to form gate electrode 16 of Heath is an electrically conductive material. See Ex. 1102

as recited in claim 8. *Id.* at 38–39. Petitioner identifies sidewall spacer 16a shown in Figure 8C (annotated in brown above) as the claimed “electrically insulative spacer,” and argues that sidewall spacer 16a is in contact window 32, i.e., the claimed “contact opening,” which is adjacent to gate electrode 16, the claimed “second electrically conductive material.” *Id.* (citing Ex. 1103, col. 10, ll. 12–27; Fig. 8C). Citing the testimony of Dr. Bravman, Petitioner argues that sidewall spacer 16a is an electrically insulative spacer because it is made of insulative oxide. *Id.* at 39 (citing Ex. 1103, col. 10, ll. 23–25; Ex. 1102 ¶ 82).

We are persuaded by Petitioner’s argument that sidewall spacer 16a is “in” contact window 32 because Figure 8C shows, as indicated by dotted line 56, a portion of sidewall spacer 16a has been removed to create an opening and form contact window 32. As noted by Petitioner, sidewall spacer 16a is made of oxide. *Id.* at 38–39 (quoting Ex. 1103, col. 10, ll. 12–27 (“spacer 16a is formed illustratively of *oxide*”)). We credit Dr. Bravman’s testimony and are persuaded that oxide is an insulator because both Heath and the ’552 patent describe oxide as an insulating material. *See, e.g.,* Ex. 1101, col. 10, ll. 50–52 (“The polysilicon layer 415 overlays an *insulating* dielectric layer 410 such as doped or undoped silicon dioxide. The dielectric layer 410 may comprise a single *oxide*, or several layers formed by various methods.” (emphases added)); Ex. 1103, col. 5, ll. 26–31 (“These and several other objects and advantages are obtained by providing a self-aligned contact process . . . protecting the tops of these elements with an *insulating oxide*” (emphasis added)). Therefore, we are persuaded that Heath discloses “(c) an electrically insulative spacer in the contact

opening adjacent to the second electrically conductive material,” as recited in claim 8.

Petitioner provides a further annotated version of Figure 8C, which is reproduced below.



Further Annotated Figure 8C in Petition

Pet. 39. Referencing Further Annotated Figure 8C shown above, Petitioner asserts that Figure 8C discloses “(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer,” as recited in claim 8. *Id.* at 39–40. Petitioner identifies etch stop layer 10 shown in Figure 8C (annotated in purple in Further Annotated Figure 8C above) as the claimed “etch stop material” and argues that, as shown in Figure 8C, etch stop layer 10 is formed over sidewall spacer 16a (i.e., the claimed “electrically insulative spacer”) as well as source/drain 20 (i.e., the claimed “first electrically conductive material”) and gate electrode 16 (i.e., the claimed “second electrically conductive material”). *Id.* at 39 (citing Ex. 1103, Fig. 8C; Ex. 1102 ¶ 83). Citing the testimony of Dr. Bravman, Petitioner argues that Heath discloses etch stop

layer 10 is made of a different material—specifically, silicon nitride—from the sidewall spacer 16a, which is formed of oxide. *Id.* at 39–40 (quoting Ex. 1103, col. 5, ll. 38–39 (“The *etch stop* preferably is *silicon nitride*.”), col. 10, ll. 12–27 (“*spacer 16a* is formed illustratively of *oxide*”)) (citing Ex. 1102 ¶ 84; Ex. 1103, Abstract; col. 9, ll. 2–4, 66–67).

We are persuaded by Petitioner’s argument because, as identified by Petitioner referencing Further Annotated Figure 8C reproduced above, Figure 8C plainly shows etch stop layer 10 is formed over sidewall spacer 16a as well as source/drain 20 and gate electrode 16. In addition, we credit Dr. Bravman’s testimony and are persuaded that silicon nitride which comprises etch stop layer 10 is a different material from oxide that makes up sidewall spacer 16a. Therefore, we are persuaded that Heath discloses “(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer,” as recited in claim 8.

Petitioner next asserts Figure 8C of Heath discloses “(e) a blanket layer over the etch stop material,” as recited in claim 8. *Id.* at 40–41. Petitioner presents another annotated Figure 8C (not reproduced herein) and identifies dielectric layer 34 (annotated in green) as the claimed “blanket layer” and argues that, as shown in Figure 8C, dielectric layer 34 is formed over etch stop layer 10, i.e., the claimed “etch stop material.” *Id.* at 41 (citing Ex. 1103, col. 7, ll. 48–50, Fig. 8C).

Upon reviewing Figure 8C and the structures or geometries evidently shown in the figure, we are persuaded that Heath discloses dielectric layer 34 is formed over etch stop layer 10. As noted by Petitioner, Heath also

discloses that “[a] very thick BPSG (borophosphosilicate glass) *dielectric* 34 covers the layer 10 except in contact windows 30 and 32.” *Id.* (quoting Ex. 1103, col. 7, ll. 48–50). Hence, we are persuaded that Heath discloses “(e) a blanket layer over the etch stop material,” as recited in claim 8.

Petitioner further asserts that Figure 8C of Heath also discloses “(f) an opening through a first part of the etch stop material to the first electrically conductive material,” as recited in claim 8. *Id.* at 37–38. As discussed above with respect to element (b), Petitioner has shown that contact window 32 depicted in Figure 8C discloses “a contact opening.” Petitioner argues Figure 8C shows that the contact opening passes through a first part of etch stop layer 10 (i.e., the claimed “etch stop material”) and through oxide layers 24a and 24b to source/drain 20 (i.e., the claimed “first electrically conductive material”). *Id.* (citing Ex. 1103, col. 10, ll. 1–11, 58–59, col. 10, l. 68–col. 11, l. 1, Fig. 8C).

We are persuaded by Petitioner’s argument because it is consistent with the disclosure in Heath’s Figures 8A, 8B, 8C and their accompanying text, which describe in detail the process of forming contact window 32 by etching away materials along the dotted lines 56, through a portion of etch stop layer 10 and through oxide layers 24a and 24b, and creating an opening that extends down to source/drain 20. Ex. 1103, Figs. 8A–C, col. 6, l. 67–col. 7, l. 3, col. 9, l. 50–col. 11, l. 15. Petitioner’s cited evidence is part of this disclosure. On the complete record, we are persuaded that Heath discloses “(f) an opening through a first part of the etch stop material to the first electrically conductive material,” as recited in claim 8.

Patent Owner does not dispute specifically Petitioner's contention that Heath discloses the preamble and numbered elements (a), (b), (c), (d), (e) and (f) of claim 8. Upon considering the complete record, we determine Petitioner has demonstrated that Heath discloses the preamble and elements (a), (b), (c), (d), (e), and (f) of claim 8.

ii. The "Angle Limitation"

The last limitation of claim 8, the "angle limitation," recites "a side of the electrically insulative spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°." Petitioner asserts that Figure 8C of Heath also discloses the "angle limitation" recited in claim 8. Pet. 41–43. According to Petitioner, Heath discloses a sidewall spacer 16a with a side that is at a right angle relative to the substrate surface because Heath describes the sidewall spacers as being "vertical" with respect to the substrate. *Id.* at 41–43 (citing Ex. 1103, Abstract; col. 11, ll. 1–10; Fig. 8C). Pointing to Figure 8C of Heath, Petitioner argues Heath describes that the entire side of the sidewall spacer is at a 90° angle relative to the substrate surface, and, therefore, the sidewall spacer meets the "angle limitation" regardless of where along the side of the sidewall spacer—be it near the bottom or near the top of the spacer—the angle is measured relative to the substrate surface. *Id.* at 42–43.

Patent Owner asserts that Heath does not disclose the "angle limitation" recited in claim 8 because Heath does not describe using a low selectivity etch to obtain substantially rectangular insulating spacers. Prelim. Resp. 26–30. Patent Owner further asserts that Heath is merely

cumulative of the prior art structure disclosed in the Background of the Invention section of the '552 patent and that the vertical sidewall in Figure 8C of Heath relied upon by Petitioner is the same as the prior art “vertical sidewall” that is shown in Figure 1(B) of the '552 patent. *Id.* at 26–29.

Patent Owner contends that both figures do not show actual etching effects and that Heath’s use of a selective etch process will result in a final structure with a sloped spacer, not a spacer with a substantially rectangular profile required by claim 8. *Id.* at 27–29. According to Patent Owner, the '552 patent improves upon the vertical sidewall spacers present in the background prior art discussed in the '552 patent in that the claimed invention uses a low selectivity etch instead of a selective etch process. *See id.* at 29–30.

Patent Owner’s “low selectivity etch” argument primarily turns on the claim construction of the “angle limitation” and is, therefore, unpersuasive because we do not agree with Patent Owner’s proposed construction of the term requiring the use of a low selectivity etch. As discussed in Section III.A. (Claim Construction) above, we determine neither the “angle limitation” nor any other term in the challenged claims requires the use of a low selectivity etch for the reasons explained in our Decision on Institution. Dec. on Inst. 8–12.

With respect to Patent Owner’s argument based on the prior art structure described in the Background of the Invention section of the '552 patent, we are not persuaded vertical sidewall spacers are present in Figure 1(B) of the '552 patent because, other than pointing to Figure 1(B), Patent Owner provides no further explanation or supporting evidence to show why the dielectric spacer 150 depicted in Figure 1(B) has a vertical sidewall

relative to the substrate surface. Nor do we discern any disclosure in the '552 patent that describes an insulating spacer depicted in Figure 1(B) as having a vertical sidewall. Rather, the '552 patent describes in detail that the prior art process of forming contact regions transforms a substantially rectangular spacer into a sloped spacer. See Ex. 1101, col. 4, l. 26–col. 6, l. 12; Figs. 2(A), 2(B), 3. Patent Owner provides no explanation or supporting evidence why the illustration in Figure 1(B) departs from this description and, instead, discloses insulating spacers with a vertical sidewall relative to the substrate surface.

In addition, although Figure 1(B) of the '552 patent may not show actual etching effects because sloped spacers are shown in more detailed illustration of prior art structures depicted in Figures 2(B) and 3, we are not persuaded that Figure 8C of Heath does not show actual etching effects or that Heath's use of a selective etch process will result in a final structure with a sloped spacer. According to Petitioner, Heath describes, contrary to Patent Owner's contention, etching "anisotropic[ally]" in a vertical direction to maintain the vertical sidewalls of the lateral spacer. Pet. 26 (quoting Ex. 1103, col. 10, ll. 2–11 ("[T]he part of layer 10 between dashed lines 56 is removed leaving a *vertical stick 10a* of layer 10 Some oxide 24 will remain on the top of gate electrode 16 even after the etch exposes the source/drain region 20 within the contact window, and *because the nitride removal is anisotropic* [i.e., it can etch vertically], *the 'stick' 10a will remain on the side, so no short to electrode 16 can occur.*")) (citing Ex. 1103, Abstract; Ex. 1102 ¶ 62). As shown in Figure 8C, because the *vertical* "stick" 10a remains on the sidewall of the insulating spacer 16a after the

anisotropic etching of the etch stop layer 10, the insulating spacer has a vertical side relative to the substrate surface. Thus, Petitioner has shown that Heath describes an anisotropic etching process for the etch stop layer that results in insulating spacers with a side that has a vertical profile or is at a right angle relative to the substrate surface.

As discussed in Section III.A. above, we construe the “angle limitation” to mean “a side of the electrically insulative spacer has an angle relative to the substrate surface that is greater than 85° and less than or equal to 90°.” We are persuaded that Heath discloses the “angle limitation” under this construction because the vertical side of oxide spacer 16a “has an angle relative to the substrate surface that is greater than 85° and less than or equal to 90°,” as recited in claim 8.

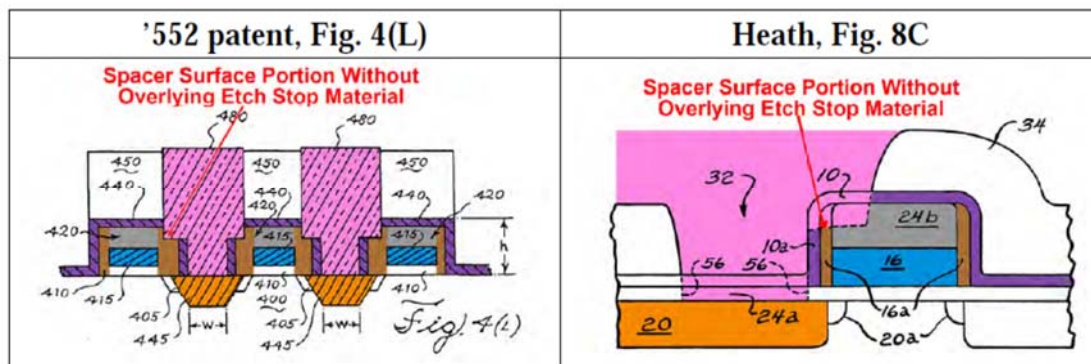
iii. Conclusion

Therefore, based on the complete record, we find that Petitioner has shown Heath discloses each limitation of independent claim 8 as arranged in the claim. Accordingly, upon considering all of the evidence of record, we determine that Petitioner has demonstrated, by a preponderance of evidence, that claim 8 is unpatentable under 35 U.S.C. § 102(b) as anticipated by Heath.

b. Dependent Claims 9–12

For claims 9–12, which depend directly or indirectly from claim 8, Petitioner provides detailed explanations and specific citations to Heath indicating where in the reference the additionally recited limitations of the dependent claims are disclosed. Pet. 43–47.

Claim 9 depends from claim 8 and further recites “the electrically insulative spacer has a surface portion without overlying etch stop material.” Comparing Figure 8C of Heath to Figure 4(L) of the ’552 patent, Petitioner asserts that Heath discloses sidewall spacer 16a (i.e., the claimed “electrically insulative spacer”) that has a surface portion that is not covered by etch stop layer 10 (i.e., the claimed “etch stop material”), similar to the insulating spacer described in Figure 4(L) of the ’552 patent. Pet. 44. The figure below is Petitioner’s comparison of Figure 4(L) of the ’552 patent on the left and Figure 8C of Heath on the right.



Petitioner’s Comparison of
Fig. 4(L) of the ’552 Patent to Fig. 8C of Heath

Id. Petitioner argues that the portion of the sidewall spacer 16a indicated by the red arrow in Petitioner-annotated Figure 8C above does not have etch stop material overlying it because that portion of the etch stop layer 10 has been removed via the etching process in order to create contact window 32. *Id.* (citing Ex. 1103, col. 10, ll. 1–3; Ex. 1102 ¶ 90). Hence, Petitioner asserts that Heath discloses “the electrically insulative spacer has a surface

portion without overlying etch stop material,” as recited in claim 9. *Id.* at 43–44.

Claim 10 depends from claim 9 and additionally recites “the electrically insulative spacer surface portion without overlying etch stop material comprises a surface portion most distant from the substrate.” Petitioner presents another comparison of Figure 8C of Heath and Figure 4(L) of the ’552 patent (not reproduced herein) and argues that the surface portion of sidewall spacer 16a identified in connection with Petitioner’s discussion of claim 9 above is the portion of the oxide spacer that is farthest away or most distant from the substrate surface, similar to the structure described in Figure 4(L) of the ’552 patent. *Id.* at 44–45 (citing Ex. 1102 ¶ 91). Thus, Petitioner asserts that Heath discloses “the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate,” as recited in claim 10. *Id.*

Based on the foregoing and upon reviewing Figure 8C and the structures or geometries evidently shown in the figure, we are persuaded that Petitioner has cited sufficient disclosure from Heath to show Heath discloses the limitations recited in claims 9 and 10.

Claim 11 depends from claim 8 and further recites “further comprising a second insulating layer on the etch stop layer and over the conductive layer.” Petitioner presents another annotated Figure 8C (not reproduced herein) and identifies dielectric layer 34 (annotated in green) as the claimed “second insulating layer.” Pet. 45–46. According to Petitioner, as shown in Figure 8C, Heath discloses oxide layer 24b (i.e., a first

insulating layer) and dielectric layer 34 (the claimed “second insulating layer”), which is formed on etch stop layer 10 (the claimed “etch stop layer”) and over gate electrode 16 (the claimed “conductive layer”). *Id.* at 45. Petitioner argues that, as shown in Figure 8C, dielectric layer 34 is formed by depositing borophosphosilicate glass (“BPSG”) on etch stop layer 10 and over gate electrode 16. *Id.* at 45–46 (citing Ex. 1103, col. 7, ll. 48–50, Fig. 8C). Citing the testimony of Dr. Bravman, Petitioner argues that BPSG is an insulator. *Id.* (citing Ex. 1102 ¶ 92).

Upon reviewing Figure 8C and the structures or geometries evidently shown in the figure, we credit Dr. Bravman’s testimony and are persuaded that Heath discloses “a second insulating layer on the etch stop layer and over the conductive layer,” as recited in claim 11.⁹

Claim 12 depends from claim 11 and additionally recites “further comprising a second conductive material in the contact region.” Petitioner asserts that this claimed “second conductive material in the contact region” refers to the electrically conductive material that is placed into the contact opening, thus forming the contact, as shown in Figure 4(L) of the ’552 patent. Pet. 46–47 (citing Ex. 1101, col. 13, ll. 43–45; Fig. 4(L)). Petitioner asserts that Heath discloses “a second conductive material in the contact

⁹ Although Petitioner does not address the apparent ambiguity in claim 11 as to whether “the conductive layer” recited in claim 11 refers to the “first electrically conductive material” or the “second electrically conductive material” of base claim 8, we note that, as shown in Figures 8A–8C, dielectric layer 34 is formed over both source/drain 20 (the claimed “first electrically conductive material”) and gate electrode 16 (the claimed “second electrically conductive material”).

region,” as recited in claim 12, because Heath describes that contact window 32 can be filled with metal to form a contact. *Id.* at 47 (citing Ex. 1103, col. 11, ll. 50–51; col. 12, ll. 8–9, 42–43; Ex. 1102 ¶ 93).

Figure 4(L) of the '552 patent is reproduced below.

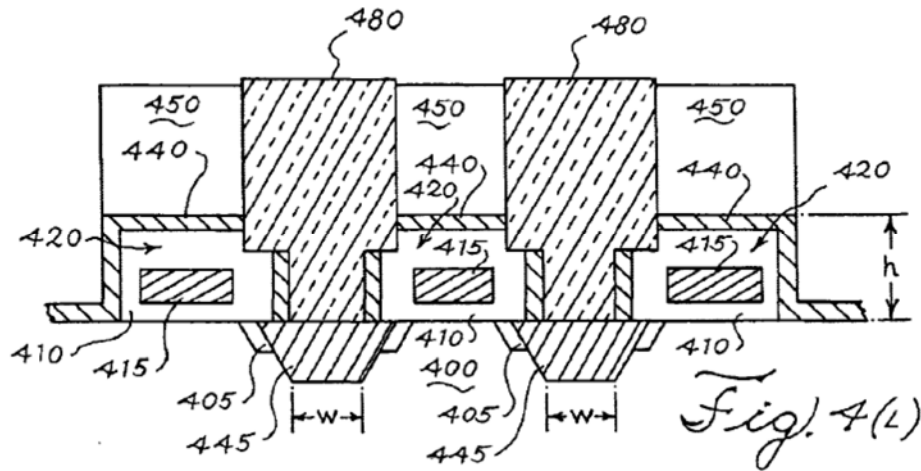


Figure 4(L) illustrates the structure of the semiconductor device of the '552 patent after conductive contacts 480 have been deposited in contact openings 460. Ex. 1101, col. 13, ll. 43–45. The '552 patent describes that, once contact openings are formed by the process of fabrication depicted in Figures 4(A) to 4(K), the only material deposited in the contact openings is conductive contacts. *See id.* at col. 13, l. 43–col. 14, l. 9. Furthermore, the '552 patent describes providing high quality contacts between a conductive material in the contact region and a device region, such as source or drain 445, as one of the primary goals of the described invention. *See id.* at col. 7, ll. 20–23 (SUMMARY OF THE INVENTION), Abstract. In view of these disclosures in the Specification, we are persuaded that “a second conductive material in the contact region” recited in claim 12 encompasses electrically conductive material that is placed into the contact opening to form a contact.

Hence, we agree with Petitioner that Heath's contact window 32 filled with metal to form a contact constitutes "a second conductive material in the contact region," as recited in claim 12.

Patent Owner does not respond separately, with specificity, to Petitioner's challenge to dependent claims 9–12 beyond Patent Owner's arguments advanced with respect to claim 8 discussed above. Upon considering the complete record, we determine that Petitioner has demonstrated, by a preponderance of evidence, that claims 9–12 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Heath.

V. CONCLUSION

Petitioner has met its burden of proof, by a preponderance of the evidence, in showing that claims 8–12 of the '552 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by Heath.

VI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 8–12 of the '552 patent are *unpatentable*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 6,784,552 B2

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