

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

INNOVATIVE MEMORY SYSTEMS, INC.,
Patent Owner.

Case IPR2016-00320
Patent 6,169,503 B1

Before KARL D. EASTHOM, JAMES B. ARPIN, and
KEVIN W. CHERRY, *Administrative Patent Judges*.

Opinion for the Board filed by *Administrative Patent Judge* EASTHOM.

Opinion Concurring by *Administrative Patent Judge* ARPIN.

EASTHOM, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
AFTER REHEARING
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1 and 8–10 of U.S. Patent No. 6,169,503 B1 (“the ’503 patent,” Ex. 1001). Pet. 1. Innovative Memory Systems, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 8 (“Prelim. Resp.”).

We instituted trial for claims 1 and 8–10 (the “challenged claims”). Paper 10 (“Institution Decision” or “Inst. Dec.”). Patent Owner then disclaimed claim 1 and filed a Response. Paper 23 (“PO Resp.”), 2 n.1. Petitioner followed with a Reply. Paper 25 (“Pet. Reply”). The record includes a transcript of the Oral Hearing. Paper 39 (“Tr.”).

We issued a First Final Written Decision. Paper 40 (“1st FWD”). Subsequently, Patent Owner filed a Request for Rehearing. Paper 41 (“Rehearing Request” or “Reh’g Req.”). Based on the Rehearing Request, the Board withdrew the First Final Written Decision as set forth in the Decision on Rehearing. Paper 42 (Withdrawal of Final Written Decision and Authorization of Sur-Reply) (“Rehearing Decision” or “Reh’g Dec.”). As set forth in the Rehearing Decision, we granted Patent Owner’s request for additional briefing in the form of a Sur-Reply (Paper 43). *See* Reh’g Dec. 5–6; Sur-Reply.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision After Rehearing issues pursuant to 35 U.S.C. § 318(a). After reconsidering the record in light of Patent Owner’s Sur-Reply and Rehearing Request, we determine Petitioner has shown by a preponderance of the evidence that claims 8–10 of the ’503 patent are unpatentable.

A. Related Matters

According to the parties, a co-pending lawsuit involves the '503 patent and other patents owned by Patent Owner: *Innovative Memory Sys., Inc. v. Micron Tech., Inc.*, 14-cv-1480 (D. Del. 2014). *See* Pet. 2; Paper 6, 1.

Petitioner filed petitions challenging the patentability of certain subsets of claims in patents involved in the Delaware litigation: (1) U.S. Patent No. 7,045,849 (Case IPR2016-00322); (2) U.S. Patent No. 7,495,953 B2 (Case IPR2016-00323); (3) U.S. Patent No. 7,886,212 B2 (Case IPR2016-00324) (institution denied); (4) U.S. Patent No. 7,000,063 B2 (Case IPR2016-00325) (institution denied); (5) U.S. Patent No. 6,324,537 B1 (Case IPR2016-00326) (terminated, adverse judgment requested by patent owner); (6) U.S. Patent No. 7,085,159 B2 (Case IPR2016-00327) (terminated, adverse judgment requested by patent owner); and (7) U.S. Patent No. 6,901,498 B2 (Case IPR2016-00330). *See* Pet. 2–3; Paper 6, 1.

B. The '503 Patent

The '503 patent describes analog-to-digital converters (“ADCs”). Ex. 1001, Abstract. An ADC converts an analog signal, such as a voltage, to a digital value. *Id.* at 1:14–17. For example, an analog audio or image signal may be converted into digital form by quantizing digital samples of the signal as represented by a number of bits. *See id.* at 1:14–42.

Instead of using comparators, in order to obtain relatively higher speed, lower power, and smaller circuit areas, the '503 patent describes using a plurality of transistors having different threshold voltages (referred to alternatively as memory or reference cells) that conduct at such different threshold voltages in response to an analog input voltage. *Id.* at 2:24–63.

These threshold voltages may be within read only memories (ROMs) or within programmable transistors. *See id.* at 2:60–63, 3:6–16.

The ROMs or transistors may be arranged in different types of arrays. *Id.* at 2:60–3:23. For example, “transistors having programmable threshold voltages . . . may be in an array including multiple rows and columns of memory cells.” *Id.* at 3:14–16. However, “[o]ther array configurations are possible.” *Id.* at 4:39–40. In one embodiment, “ADC 300 uses a row of reference cells.” *Id.* at 4:37.

Figure 5B, reproduced below, depicts a disclosed embodiment having multiple rows of memory cells or programmable transistors in ADC 500:

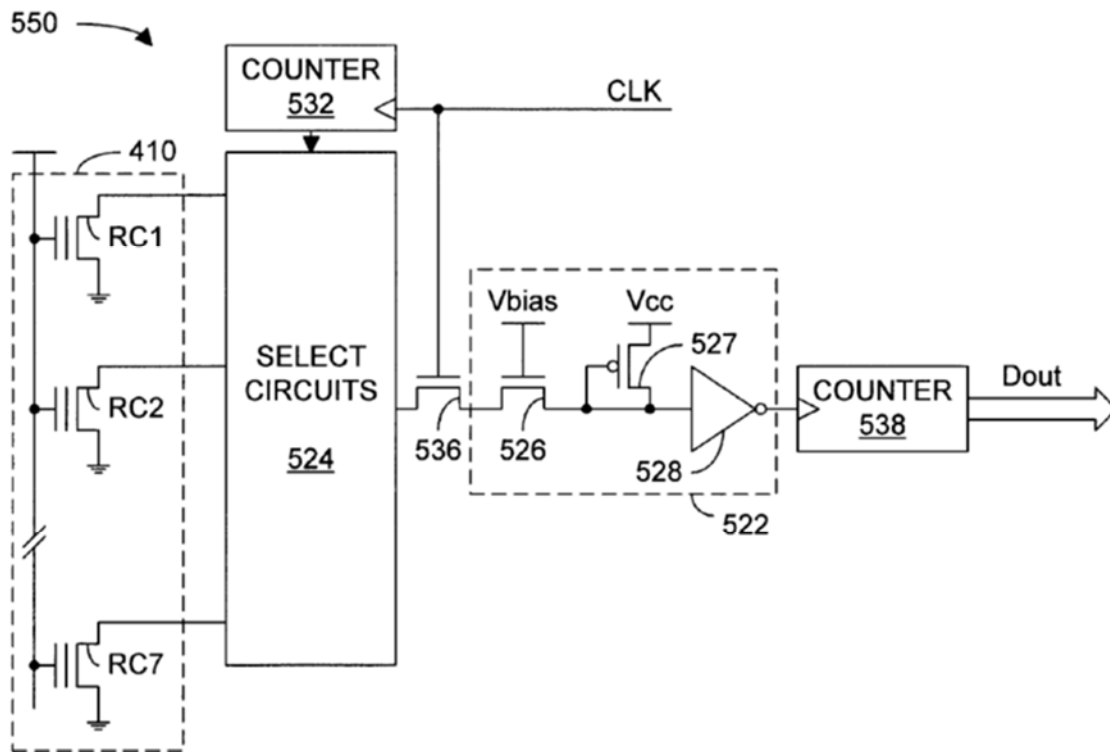


FIG. 5B

With respect to Figure 5B, to convert an analog signal A_{in} into a signal in digital format D_{out} , “sense circuit 522 generates a pulse for each

reference cell RC1 to RC7 that conducts. Counter 538 counts pulses from sense circuit 522 and outputs the resulting count as signal Dout.” Ex. 1001, 7:5–8.

Figures 5A and 5B show that Ain connects to all of the rows, such that embodiments represented by those figures use all the rows simultaneously in a specific digital conversion. The Specification also describes modifying embodiments including those represented by Figures 5A and 5B, such that “[i]nstead of simultaneously applying analog input voltage Ain to all of the reference cells associate with a conversion, the ADC applies signal Ain only to [sic] reference cell (or one row of reference cells) at a time.” *See id.* at 7:11–14. At least one such embodiment includes a row decoder to select successive rows. *See id.* at 7:14–16. In an embodiment that selects successive rows, “signal CSEL initially has a value that selects one of the rows associated with the desired conversion, and circuit 740 determines the conductivity states of the reference cells in the current row. . . . The control circuit continues to change signal CSEL until a row is found in which some reference cells conduct and others don’t conduct.” *Id.* at 10:14–23 (discussing Figure 7A and AADAC 700).¹

¹ AADAC refers to a dual converter (which uses the same reference cells) for both an analog to digital and digital to analog conversion. *See* Ex. 1001, 9:32–51.

C. Illustrative Claims

Independent challenged claims 8 and 9, and dependent claim 10, remain in the trial. Claims 8 and 9 follow:

8. A converter comprising:

an array of reference cells, the reference cells having a plurality of threshold voltages;

a sense circuit coupled to the array; and

an encoder coupled to the sense circuit, wherein the encoder generates a multi-bit digital output signal that represents a value that depends on which of the reference cells conduct when an analog input signal is applied to a set of reference cells, wherein the encoder comprises a counter coupled to count pulses from the sense circuit, the multi-bit digital output signal being a count of the number of reference cells that conduct.

9. A converter comprising:

an array of reference cells, the reference cells having a plurality of threshold voltages, wherein the array contains a plurality of rows;

a sense circuit coupled to the array; and

an encoder coupled to the sense circuit, wherein the encoder generates a multi-bit digital output signal that represents a value that depends on which of the reference cells conduct when an analog input signal is applied to a set of reference cells; and

a row decoder coupled to the array, the row decoder selecting a row of reference cells to which the analog signal is applied.

Ex. 1001, 11:20–32, 12:20–33, 12:34–47.

D. Grounds of Unpatentability

We instituted trial on claims 1 and 8–10 of the '503 patent, challenged on alleged grounds of obviousness under 35 U.S.C. § 103(a). Patent Owner subsequently disclaimed claim 1. PO Resp. 2 n.2. The grounds remaining in the trial follow:

References	Claim(s) Challenged
Seligson ² and Bucklen ³	8
Seligson, Bucklen, and Yonemaru ⁴	8
Seligson and Yonemaru	9 and 10

See Pet. 3–4; Inst. Dec. 6, 27–28.

Petitioner relies on the Declaration of R. Jacob Baker, Ph.D (Ex. 1003, the “Baker Declaration”) and the Reply Declaration of R. Jacob Baker, Ph.D (Ex. 1030, the “Baker Reply Declaration”). Patent Owner relies on the Declaration of Vijay K. Madisetti, Ph.D (Ex. 2001, the “Madisetti Declaration”).

II. ANALYSIS

A. Claim Interpretation

The claims of an unexpired patent must be interpreted using the broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest

² U.S. Patent No. 5,376,935 (issued Dec. 27, 1994) (Ex. 1005).

³ U.S. Patent No. 4,591,825 (issued May 27, 1986) (Ex. 1007).

⁴ U.S. Patent No. 5,187,483 (issued Feb. 16, 1993) (Ex 1006).

reasonable interpretation standard under 37 C.F.R. § 42.100(b)). Under this standard, absent any special definitions, claim terms or phrases carry their ordinary and customary meaning, as would be understood by one of ordinary skill in the art, in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Most of the claim terms do not require express construction because they do not raise a controversy. See *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that “only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy” and noting that “the stage at which the claims are construed may vary with the issues, their complexity, the potentially dispositive nature of the construction, and other considerations of the particular case”).

1) “selecting a row”

Claim 9 recites “a row decoder coupled to the array, the row decoder *selecting a row* of reference cells to which the analog signal is applied.” (Emphasis added). Focusing partly on the indefinite article “a,” Petitioner contends that “selecting a row” means selecting “one or more rows.” Pet. Reply 5 (emphasis added) (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000)). Patent Owner disagrees and argues that claim 9 “require[s] that the row decoder selectively apply the analog input signal to a particular row of reference cells, i.e., depending on the range of the analog signal.” PO Resp. 29. Patent Owner similarly contends that “the row decoder recited in claim 9 selects from the plurality of rows of reference cells a single row of reference cells that is to receive the analog input signal.” *Id.* at 27.

Addressing the indefinite article “a” in a claim (as recited in claim 9), *KCJ Corp.*, 223 F.3d at 1356, supports Petitioner’s argument as follows:

This court has repeatedly emphasized that an indefinite article “a” or “an” in patent parlance carries the meaning of “one or more” in open-ended claims containing the transitional phrase “comprising.” See *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 . . . (Fed. Cir.1999); *Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 . . . (Fed. Cir.1997); *North Am. Vaccine, Inc. v. American Cyanamid Co.*, 7 F.3d 1571, 1575–76 . . . Fed. Cir.1993); see also Robert C. Faber, *Landis on Mechanics of Patent Claim Drafting* 531 (3d ed. 1990). Unless the claim is specific as to the number of elements, the article “a” receives a singular interpretation only in rare circumstances when the patentee evinces a clear intent to so limit the article. See *Abtox*, 122 F.3d at 1023 Under this conventional rule, the claim limitation “a,” without more, requires at least one.

. . . .

Moreover, standing alone, a disclosure of a preferred or exemplary embodiment encompassing a singular element does not disclaim a plural embodiment. “[A]lthough the specifications may well indicate that certain embodiments are preferred, particular embodiments appearing in a specification will not be read into the claims when the claim language is broader than such embodiments.” *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 . . . (Fed. Cir. 1994). Thus, as the rule dictates, when the claim language or context calls for further inquiry, this court consults the written description *for a clear intent to limit the invention to a singular embodiment*.

Id. (emphasis added).

Claim 9 does not recite “selecting a [single] row.” Accordingly, in line with the “conventional rule,” “selecting a row” means “selecting at least one row.” See *KCJ Corp.*, 223 F.3d at 1356. *KCJ Corp.* also shows that absent a clear disclaimer (or lexicographic definition), Patent Owner’s

argument that “the embodiments disclosed in the ‘503 Patent . . . select[] . . . a single row of reference cells” fails to support Patent Owner’s narrow reading of claim 9. *See* PO Resp. 27; 223 F.3d at 1356.

Furthermore, prior to the “selecting a row” phrase, claim 9 recites “when an analog input signal is applied to *a set of reference cells*” (emphasis added). Specifically, claim 9 recites

an encoder coupled to the sense circuit, wherein the encoder generates a multi-bit digital output signal that represents a value that depends on which of the reference cells conduct *when an analog input signal is applied to a set of reference cells*; and

a row decoder coupled to the array, the row decoder *selecting a row of reference cells to which the analog signal is applied*.

(Emphases added).

In context, the “set of reference cells” includes (at least one of) “a row of reference cells.” Given that claim 9 recites “*when an analog signal is applied to a set of reference cells*” (emphasis added), the language implies that “selecting a row of reference cells to which *the* analog signal is applied” (emphasis added) includes one or more rows of the set.⁵ In other words, “the analog signal” refers back to “when *an analog signal is applied to a set of reference cells*.” As discussed in the next section, this latter phrase indicates the whole “set of reference cells” has an analog signal applied to it in order to generate the digital output signal.

⁵ Apparatus claim 9, drawn to a converter, does not require the “analog signal,” thereby rendering the phrases “selecting a row of reference cells to which the analog signal is applied” and “to which the analog signal is applied” statements of intended use.

Figures 3, 4, 5A, and 5B clearly show all of the rows (and the whole set of reference cells) connected to *Ain*. The Specification states “[t]he set of threshold voltage[s] in the conversion array controls the conversion or conversions implemented.” Ex. 1001, 2:63–65.

Therefore, and as explained more fully in the next section, claim 9 reasonably includes a row decoder that selects one or more rows that have an applied analog signal.

The Specification explains that

transistors having programmable threshold voltages . . . may be in an array including multiple rows and columns of memory cells. In one embodiment, the transistors are in a conversion array having multiple rows, where each row contains transistors with a sequence of threshold voltages that defines a different conversion. A conventional row decoder *can select a row accessed from the conversion array during a conversion and thereby select from among multiple conversions implemented in the converter.*

Ex. 1001, 3:14–23 (emphases added).

As the foregoing quotation and other portions of the Specification show, the row decoder selects a row or rows to perform a specific type of conversion (for example, linear or non-linear conversions). *See id.* at 2:66. As noted above, the entire set in an array can be used for any given type of conversion: “The set of threshold voltage[s] in the conversion array controls the conversion or conversions implemented.” *See id.* at 2:63–65; *cf. id.* at 4:39–42 (describing other embodiments that “do not require simultaneous application of the same control gate voltage to all reference cells”).

Describing a particular embodiment associated with Figure 7A, the Specification explains that “*multiplexer 714 selects analog input signal Ain,*

and row decoder 712 selects from array 710 a row identified by a conversion select signal CSEL and applies a signal Vrow from multiplexer 714 to the selected row.” *Id.* at 9:33–34. Patent Owner relies on Figure 7A and contends “[r]ow decoder 712 further prevents Ain from being applied to any other row of reference cells.” PO Resp. 9 (citing Ex. 1001, 9:32–39; Ex. 2001 ¶¶ 61–64). Dr. Madisetti makes a similar statement. See Ex. 2001 ¶ 64.

Even if the embodiment of Figure 7A supports Patent Owner’s construction of selecting a single row, it provides insufficient basis to *limit* the plain language of claim 9 of selecting a row. The Specification supports the plain meaning of claim 9 in several ways. For example, the Specification narrowly refers to selecting “only” a “row of reference cells” in the “conversion array including a column of reference cells,” as follows:

Another alternative to ADC has a conversion array including a *column* of reference cells that are associated with a conversion. Instead of simultaneously applying analog input voltage Ain to all of the reference cells associate with a conversion, the ADC applies signal Ain *only to* [sic] reference cell (or *row of reference cells*) to which signal Ain is applied. *For this embodiment*, bias and select circuits include a row decoder to select *the* reference cell (or *row of reference cells*) to which signal Ain is applied.

Ex. 1001, 7:11–17 (emphases added).

This Specification language that describes an embodiment that selects “*the . . . row*,” which refers back to “*only* [sic a] . . . row,” suggests that claim 9 recites broader language. In particular, claim 9 recites “when an analog signal is applied to a *set* of reference cells” and “*a* row to which the

analog signal is applied” (which refers back to “an analog signal” in the first clause).

Further supporting the broader construction of claim 9, Petitioner provides persuasive evidence that typical row decoders select “one or more rows.” Pet. Reply 7 (citing Ex. 1029, 29; 1030 ¶¶ 21–23). Petitioner points out that “the Summary of Invention expressly states that the ‘503 [p]atent employs ‘[a] **conventional row decoder** [to] select a row accessed from the conversion array.’” *Id.* at 6 (quoting Ex. 1001, 3:16–23 (emphasis by Petitioner)). Dr. Baker persuasively demonstrates that conventional row decoders commonly select a location in an array, which may include one or more rows, thereby supporting the broader construction. *See* Ex. 1030 ¶¶ 21–24 (citing Ex. 1003, 3:16–23; Ex. 1029, 29; 1031, 54–55).

Dr. Madisetti does not disagree, and, if anything, agrees that the claims cover conventional converters. For example, Dr. Madisetti testifies “[t]he claims of the ‘503 Patent generally cover converters in which the multi-bit digital output signal depends on which reference cells conduct *when an analog input signal is applied to a set of the reference cells.*” Ex. 2001 ¶ 60 (emphasis added). Dr. Madisetti also summarizes embodiments in the Specification and concludes that claim 9 “claims a converter in which a row decoder selects a particular row of reference cells.” *Id.* ¶ 63; *see* PO Resp. 8 (citing Ex. 2001 ¶¶ 60–63). This testimony does not contradict Petitioner or Dr. Baker, because Petitioner’s claim construction (i.e., “one or more rows” or equivalently “at least one row”) includes selecting only a single (“particular”) row. Moreover, claim 9 does not recite selecting a “particular” row, contrary to Dr. Madisetti’s testimony.

Claim 12 depends from claim 9 via intervening claim 10. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d. 1576, 1582 (Fed. Cir. 1996) (When construing claims, “[f]irst, we look to the words of the claims themselves, *both asserted and unasserted*, to define the scope of the patented invention.” (Emphasis added.)). Claim 10 recites, in pertinent part, “the converter of claim 9, further comprising . . . a conversion select signal that selects from among a plurality of conversions that the converter implements.” Claim 12 recites “[t]he converter of claim 10, wherein *at least one* conversion in the plurality of conversions corresponds to *multiple rows in the array*.” (Emphases added.)

As Petitioner argues, claim 9 must be broader than claim 12 by virtue of the dependency of claim 12. *See* Pet. Reply 7–8. Claim 12 also appears to be broad enough to embrace a converter that either is capable of selecting all of the rows simultaneously or selecting one row at a time. *See id.* at 8 (“Tracking claim 12, the Specification describes embodiments in which the conversions involve multiple rows. ‘In an alternative embodiment of ADDAC 700, **multiple rows of array 710 contain reference cells for a single conversion.**’” (quoting Ex. 1001, 10:4–6, citing *id.* at 10:4–13) (emphasis by Petitioner)) & n.2 (arguing claim 12 lacks necessary recited structure for the sequential conversion: “column lines and sense circuitry”). The cited passage explains that “[u]sing multiple rows for a conversion allows higher resolution analog signals and more bits in digital signals.” Ex. 1001, 10:6–8.

In any event, even if dependent claim 12 requires sequential selection of rows, that would imply (by virtue of claim dependency) that claim 9 does not. As noted above, the Specification generally describes embodiments

associated with Figures 3, 4, 5A, and 5B and other embodiments that do not select rows for connection to Ain (i.e., Ain connects to all of the rows). See Ex. 1001, 7:11–14. As discussed further in the next section, modified embodiments, including modified versions of Figures 5A and 5B, may include a row decoder to select a row to which to apply signal Ain, but in contrast to claim 9, the Specification uses narrow language to make clear a row decoder applies Ain “*only to . . . one row . . . at a time.*” See *id.* at 7:14–15.

Claims 9 and 12 appear to cover (but not necessarily require) the sequential row selection noted above by Petitioner. See Ex. 1001, 10:4–12. The Specification indicates that, in one sequential row selection embodiment, “signal CSEL initially has a value that *selects one of the rows* associated with the desired conversion.” Ex. 1001, 10:14–16 (emphasis added). “If all of the reference cells in *the selected row* conduct or do not conduct, control circuitry (not shown) changes signal CSEL to *select another row* corresponding to the desired conversion.” *Id.* at 10:17–21 (emphases added). In other words, this alternative embodiment narrowly describes “*selecting one of the rows*” and then successively “*select[ing] another row.*” *Id.* at 10:14–21. Therefore, although claim 12 may correspond to this narrow successive row selection embodiment, this shows that claim 9 embraces broader subject matter of a *conventional recited row decoder that does not include a row select signal* (i.e., CSEL as disclosed and noted above). For the additional and similar reasons explained above, claim 9 employs broader selecting language (i.e., “selecting *a* row”) than the CSEL embodiment (i.e., “selects *one* of the rows” (*id.* at 10:14–21)). See *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir.

2004) (“a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment”).

It follows that the disclosed embodiments do not overcome the plain and ordinary meaning of “selecting a row.” See *KCJ Corp.*, 223 F.3d at 1356 (“indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more,’”; “particular embodiments appearing in a specification will not be read into the claims when the claim language is broader than such embodiments”; and “when the claim language or context calls for further inquiry, this court consults the written description for a clear intent to limit the invention to a singular embodiment”). As explained above, claim 9 employs a conventional row decoder that typically includes selecting plural rows. And claim 9 does not recite what narrower dependent claims 10 and 12 recite, namely, a “terminal for a conversion select signal,” which implies circuitry in claims 10 and 12 for selecting successive single rows using the row decoder.

In other words, the Specification does not show, by implication or expressly, the requisite intent to disavow or redefine clearly the plain and ordinary meaning of “selecting a row” (or “row decoder”). See *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (“To act as its own lexicographer, a patentee must ‘clearly set forth a definition of the disputed claim term’ other than its plain and ordinary meaning.”) (quoting *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1365 (Fed. Cir. 2002)). “It is not enough for a patentee to simply disclose a single embodiment or use a word in the same manner in all embodiments, the patentee must ‘clearly express an intent’ to redefine the term.” *Thorner*, 669

at 1365 (quoting *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1381 (Fed. Cir. 2008)).

Based on the foregoing discussion, Petitioner shows persuasively that the broadest reasonable interpretation of “selecting a row” is “selecting at least one row.”

2) “the row decoder selecting a row of reference cells to which the analog signal is applied.”

Patent Owner contends “selecting a row of reference cells to which the analog signal is applied” “*requires* that the row decoder select a row of reference cells *to receive* the analog input signal.” Reh’g Req. 5 (emphasis added). As Patent Owner correctly notes, in the First Final Written Decision, we determined “[c]laim 9 ‘simply requires’ ‘that any rows that are selected – whether one or more than one – have an analog signal applied to them.’” Reh’g Req. 5 (quoting 1st FWD 31; Pet. Reply 7). By its plain terms “is applied” is not restricted either to “to be applied,” as Patent Owner urges, or to “already is applied,” as our First Final Written Decision determines. In other words, the plain meaning includes both options.

Nevertheless, Patent Owner contends “[t]he Specification nowhere states that Ain is applied, at any time, to all rows.” See Reh’g Req. 5. To the contrary, the Specification, as noted above and in the First Final Written Decision, discloses multiple embodiments where that occurs. See 1st FWD 10 (“Figures 3, 4, 5A, and 5B [of the ’503 patent] clearly show all of the rows (and the whole set of reference cells) connected to Ain.”)

In its Sur-Reply, Patent Owner contends no embodiments include row encoders with rows already having Ain connected, as follows:

There is not a single embodiment disclosed in the specification *wherein a row decoder selects a row from the array that already has the analog signal applied to it*. A “construction which excludes the preferred embodiment is ‘rarely, if ever correct.’” *PPC Broadband, Inc. v. Corning Optical Communications RF, LLC*, 815 F.3d 747, 755 (Fed. Cir. 2016), quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996). In this case, *Petitioner’s claim construction does not read on any embodiment disclosed in the specification*.

Sur-Reply 2 (emphasis added).

Although Patent Owner focuses on Petitioner’s alleged claim construction, the adopted claim construction does not exclude any embodiments. Rather, as noted above, “is applied to” includes “already applied to” and “to be applied to.” We indicated clearly, as we stated in our First Final Written Decision that claim 9 encompasses both options. For example, as we stated, “[c]laim 9 neither precludes selecting a particular row to provide an output nor requires selecting a particular row to receive the analog signal under the broadest reasonable claim construction.” 1st FWD 32; *see also* FWD 34 (discussing “Patent Owner’s narrower claim construction”); Inst. Dec. 23 (indicating both options apply: “[A]ccording to Petitioner’s showing on this preliminary record, using Yonemaru’s encoder and select switches to select different rows of programmable transistors in Seligson’s circuit would have been obvious for the purpose of expanding comparisons and sensing different analog ranges, while providing a known array configuration for utilizing available chip space.”); *infra* Section III (Motion to Exclude, citing PO Resp. 27 and determining Patent Owner was aware of both options.).

Furthermore, even if Patent Owner’s construction reads on an embodiment, as noted above, embodiments typically do not narrow the plain meaning of claim terms.⁶ See *SuperGuide Corp.*, 358 F.3d at 875 (“a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment”). As indicated above, claim 9 recites broader subject matter than the embodiments it covers. The plain meaning of “is applied to” simply is not limited to “to be applied to” (i.e., in the future). And as discussed in the preceding section, prior to the “selecting a row” phrase, claim 9 recites “generat[ing] digital output signal . . . when an analog input signal is applied to a set of reference cells.” Specifically, claim 9 recites

an encoder coupled to the sense circuit, wherein the encoder *generates a multi-bit digital output signal* that represents a value that depends on which of the reference cells conduct *when an analog input signal is applied to a set of reference cells*; and

a row decoder coupled to the array, the row decoder *selecting a row of reference cells to which the analog signal is applied*.

(Emphases added).

⁶ Patent Owner asserts in its Rehearing Request that we mischaracterized aspects of Figure 7A to support our claim construction. Reh’g Req. 6–7. Nevertheless, we stated “[e]ven if the embodiment of Figure 7A somehow were to support Patent Owner’s proposed claim construction, the Specification also tracks the broader construction of claim 9,” and relied on the broader teachings of the Specification and the language of claim 9, as we do here. See 1st FWD 12, Section II.A.1. In this Final Written Decision After Rehearing, we clarify that we do not rely on any reasoning related to biasing or noise that Patent Owner alleges we mischaracterized with respect to interpreting Figure 7A. See Reh’g Req. 6–7.

The phrase “selecting a row of reference cells to which *the* analog signal is applied” (emphasis added) refers back to “generat[ing] a . . . digital output signal when *an analog signal* is applied to *a set of reference cells*.” This latter phrase not only shows the whole “set of reference cells” (for a given conversion type) has an analog signal applied thereto, it also shows the row decoder selects one or more rows of that set (dedicated to the specific type of conversion such as linear, non-linear, etc.) to generate the digital output—an output the encoder generates with Ain already connected as an input to one or more rows.

Immediately after discussing embodiments of Figures 5A and 5B, which depict all of the array rows connected to Ain (*see, e.g.*, Figure 5B above), the Specification describes an alternative embodiment as follows:

Another alternative to ADC has a conversion array including a column of reference cells that are associated with a conversion. *Instead of simultaneously applying analog input voltage Ain to all of the reference cells* associated with a conversion, the ADC applies signal Ain only to reference cell (or one row of reference cells) at a time. *For this embodiment, bias and select circuits include a row decoder* to select the reference cell (or row of reference cells) to which signal Ain is applied.

Ex. 1001, 7:9–17 (emphases added).

Contrary to the description above, claim 9 does not recite bias and select circuits that “include a row decoder,” or applying Ain “only” to “one row of reference cells at a time.” Because the Specification states that “*select circuits include a row decoder . . . to which signal Ain is applied*” (*id.*), this also implies a select circuit may include a row decoder to select rows in general, including for the purpose of selecting a row or rows already connected to Ain, in order to generate the digital output related to that row,

as claim 9 recites. Figures 5A and 5B, discussed above (and in the First Final Written Decision), each disclose select circuits 524 that select rows that already have Ain connected thereto. *See supra* Section IB; 1st FWD Section IB.

Patent Owner cites the passage above and quotes a part of it, arguing no embodiments that have Ain connected to all the rows include row decoders. Sur-Reply 2. But that argument ignores the clear language noted above that select circuits may include row decoders and the fact that Figures 5A and 5B include select circuits. *See* Ex. 1001, 7:9–17; Sur-Reply (quoting Ex. 1001, 7:11–7).

Further supporting the broader reading, as discussed above in the preceding section, Petitioner points out that “the Summary of Invention expressly states that the ‘503 [p]atent employs ‘[a] **conventional row decoder** [to] select a row accessed from the conversion array.’” *Id.* at 6 (quoting Ex. 1001, 3:16–23 (emphasis by Petitioner)). This general row selection does not specify using the row decoder only to connect to input Ain, and therefore, further supports the finding that modified embodiments of at least Figures 5A and 5B contemplate using a row decoder in a select circuit, such as select circuit 524 (*see* Figure 5B above), for the purpose of selecting rows that have Ain already applied to them in order to determine the digital output pertaining to the selected row—as claim 9 recites.

Finally, the Specification specifically informs the artisan of ordinary skill not to limit the plain language of the claims to any specific embodiments and to recognize that different features of different embodiments may be combined:

Although the invention has been described with reference to particular embodiments, the description is only an example of the invention's application and should not be taken as a limitation. Various adaptations and combinations of features of the embodiments disclosed are within the scope of the invention as defined by the following claims.

Ex. 1001, 11:13–18.

Based on the foregoing discussion, the plain meaning of “the row decoder selecting a row of reference cells to which the analog signal is applied” includes “the row decoder selecting one or more rows of reference cells to receive the analog input signal, or selecting one or more rows that already have the analog signal.”

3) “counter . . . to count pulses”

Claim 8 recites “a counter coupled to count pulses from the sense circuit, the multi-bit digital output signal being a count of the number of reference cells that conduct.” In its Petition, Petitioner argues that the claim 8 phrase, “a counter coupled to count pulses from the sense circuit,” should be construed as “a counter that counts changes in current or voltage from a circuit that indicates whether a given reference cell is conducting.” Pet. 19.

In its Preliminary Response, Patent Owner asserts that no construction is necessary and contends that Petitioner’s claim construction “attempts to add unnecessary verbiage to . . . a clear and unambiguous claim term that would be readily understood by one of ordinary skill in the art.” Prelim. Resp. 15. As a preliminary matter, we determined that “[n]o need exists to construe the term” for purposes of institution. Inst. Dec. 13.

In its Response, Patent Owner contends that “[o]ne of ordinary skill in the art would understand that a ‘counter’ is something that uses *sequential*

logic to count *individual pulses*, not a transition detection circuit that uses combinational logic to locate the transition point from which the ultimate count may be determined.” PO Resp. 41 n.7 (emphases added). Patent Owner does not contend that this “understand[ing]” corresponds to the broadest reasonable construction of the term “counter.” See PO Resp. at 41–42. Rather, Patent Owner, relying on Dr. Madisetti’s deposition testimony and the Madisetti Declaration, asserts that “counters are used for counting the number of occurrences of an event, such as, in the context of the ‘503 Patent, the individual pulses generated by the sense circuit.” PO Resp. 39 (citing Ex. 2003, 257; Ex. 2001 ¶ 151). At the cited paragraph, Dr. Madisetti testifies that “[a] counter circuit is a specific type of sequential circuit that goes through a prescribed sequence of states upon the application of input pulses.” Ex. 2001 ¶ 151. Neither Dr. Madisetti nor Patent Owner explicitly proffers a plain and ordinary meaning or the broadest reasonable construction.

On the other hand, Petitioner replies that “the claim language does not limit a ‘counter’ to one that ‘counts pulses’ in some special way, such as one that ‘**sequentially** count[s] pulses.’” Pet. Reply 27. Petitioner also argues that the Specification specifically describes sequentially counting, thereby indicating that claim 8 embraces broader subject matter. *Id.* at 27–28 (citing Ex. 1001, 6:11–15). The language of the Specification supports Petitioner’s argument. Spanning the cited passage, the Specification states

a clock signal causes counter 532 to *sequentially* count up from zero. When the count in counter 532 crosses the boundary between the addresses of conductive reference cells and the addresses of non-conductive references cells, a transition in the

output signal from inverter 528 cases latch 534 to register the count signal from counter 532.

Ex. 1001, 6:11–19 (emphasis added).

Petitioner also contends that “the extrinsic evidence is clear that there are other types of ‘counters’ that do not use ‘sequential logic.’” Pet. Reply 29 (citing Ex. 1032, 3; 1033, 4). Petitioner provides a trade dictionary definition that states “[l]ess frequently, a counter is an accumulator.” *Id.* (citing Ex. 1033, 4). Another cited trade dictionary definition supports Petitioner and defines a counter as “[a] device such as a register or storage location used to represent the number of occurrences of an event.” Pet. Reply 29 (citing Ex. 1032, 3). A slightly more restrictive definition in the former trade dictionary also supports Petitioner’s argument, as it defines a counter as “a circuit that produces one output pulse each time it receives some predetermined number of input pulses.” Ex. 1033, 4 (emphasis added). In other words, the latter-defined counter outputs a pulse based on a group of input pulses—i.e., it “counts” pulses in groups, instead of necessarily counting pulses one by one.⁷

As noted above, Patent Owner provides evidence that a counter includes a sequential counter. PO Resp. 39 (citing Ex. 2003, 212, 257, 267;

⁷ In relevant context, Exhibit 1033 defines a counter according to this latter definition as follows:

(A) A device, capable of changing from one to the next of a sequence of distinguishable states upon each receipt of an input signal. Note: One specific type is a circuit that produces one output pulse each time it receives some predetermined number of input pulses. The same term may also be applied to several such circuits connected in cascade to provide digital counting.

Ex. 1033, 4.

Ex. 2001 ¶ 151) (arguing “[c]ounters are used for counting the number of occurrences of an event, such as, in the context of the ‘503 Patent, the individual pulses generated by the sense circuit”). Petitioner characterizes Patent Owner’s evidence as follows:

Patent Owner’s extrinsic evidence certainly suggests that counters which use sequential logic are a common type of counter. That does not mean, however, that “counter” in the [’]503 [p]atent claims should be limited to this specific type of counter when the industry definition and understanding of “counter” covers much more than “sequential” counters.

Id. (footnote omitted, discussing Ex. 2003, 212) (emphasis added).⁸

As Petitioner persuasively argues, claim 8 does not require the counter explicitly to count each sensed pulse individually. Rather, claim 8 more generally requires “a counter coupled to count pulses from the sense circuit.” Neither party addresses how the phrase “to count” impacts the phrase “counter . . . to count pulses.” Tracking Patent Owner’s argument that claim 8 requires a sequential (one by one) counter, one meaning of “count” includes “to name or list (the units of a group or collection) one by one in order to determine a total; to number.” *See* Ex. 3001 (THE AMERICAN HERITAGE DICTIONARY, 303 (1975)). On the other hand, tracking Petitioner’s arguments, “count” also means “[t]o recite numerals in ascending order or enumerate items by units or groups <count by *tens*>” or “[t]he act of enumerating or calculating.” *Id.* (latter emphasis added).

⁸ Patent Owner’s cited evidence, including that relied upon by Dr. Madisetti, refers to a counter as “essentially a register that goes through a predetermined sequence of states upon the application of input pulses.” PO Resp. 39 (citing Ex. 2001 ¶ 151; Ex. 2003, 267); Ex. 2001 ¶ 151 (citing Ex. 2003, 267).

Another source generally includes both of those definitions and states that “count” means “to say the names of numbers one after the other in order, or to calculate the number of units in a group.” Ex. 3002.⁹ The latter source also indicates that the verb “count” broadly means “calculate,” which supports Petitioner’s position. *Id.*

Therefore, the phrase “to count,” which broadly means “to calculate,” further limits the claimed pulse “counter.” See Ex. 3001; Ex. 3002. Based on the foregoing discussion, the record evidence shows that the plain and ordinary meaning of a “counter . . . to count pulses” means an “accumulator, circuit, or device that calculates the number of pulses.”

The Specification does not deviate clearly from the plain and ordinary meaning that includes an accumulator as a calculator of sensed pulses. Sequential address counter 532 tracks addresses and does not correspond clearly to the claimed pulse counter (Ex. 1001, 6:11–15), and the Specification does not limit the plain meaning of a counter to a sequential counter or even describe pulse counter 538 clearly as a sequential counter. See Ex. 1001, 6:56–7:8 (stating “counter 538 counts pulses from sense circuit 522,” showing counter 538 merely as a box in Fig. 5B, but describing counter 532, as “sequentially count[ing]”). “To act as its own lexicographer, a patentee must ‘clearly set forth a definition of the disputed claim term’ other than its plain and ordinary meaning.” *Thorner*, 669 F.3d at 1365 (quoting *CCS Fitness*, 288 F.3d at 1365). “It is not enough for a patentee to simply disclose a single embodiment or use a word in the same manner in all

⁹ Obtained at dictionary.cambridge.org/us/dictionary/English/count CAMBRIDGE DICTIONARY (last visited Apr. 19, 2017).

embodiments, the patentee must ‘clearly express an intent’ to redefine the term.” *Id.* (quoting *Helmsderfer*, 527 F.3d at 1381); *see also SuperGuide*, 358 F.3d at 875 (“a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment”).

Moreover, the Specification generally states the following:

Embodiments of ADCs that sequentially determine the conductivity of reference cells can be *implemented in a variety of ways*. For example, *counter 532 in ADC 500 can be replaced with circuitry that performs a binary search for the boundary between conducting and on-conducting reference cells*. An exemplary binary search starts at a central address . . . and *increases or decreases the address depending on whether the reference cell at the current address conducts*.

Id. at 6:39–47 (emphases added).

This passage, although not referring specifically to a pulse counter, such as counter 538, generally suggests using different types of counters or circuits for performing sequential counting functions to determine the number of reference cells that conduct. The ’503 patent at other places describes several counter embodiments for using different counter options to determine the specific number of reference cells that conduct. *See id.* at 5:38–7:8. Although one embodiment uses “[c]ounter 538 to count pulses from sense circuit 522,” as noted above, the Specification does not state unequivocally or clearly that counter 538 *sequentially* counts the pulses in that embodiment, let alone state that it must do so. *See id.* at 7:7–8 (“[S]ense circuit 522 generates a pulse for each reference cell RC1 to RC7 that conducts. Counter 538 counts pulses from sense circuit 522 and outputs the resulting count as signal Dout.”).

Even if the Specification implicitly describes counter 538 as a sequential counter (*see id.* at Fig. 5B, 7:1–15), given the broad nature of known counters as discussed above, and given that the Specification describes determining the number of conducting cells in “a variety of ways,” including by replacing counters with other functional counting circuitry, the Specification broadly contemplates using generic counters. *See id.* at 5:38–7:8. Furthermore, notwithstanding the description of using different counter circuitry to determine the number of conducting cells (*id.*), claim 8 does not require that relationship explicitly—it does not require the claimed invention to do anything with counted pulses. That is, claim 8 broadly recites “a counter coupled to count pulses from the sense circuit, the multi-bit digital output signal being a count of the number of reference cells that conduct.” Claim 8 does not define an explicit relationship between the multi-bit digital output signal (“a count”) and “a counter to . . . count pulses.” This claim breadth further implies that a “counter . . . to count pulses” as recited in claim 8 covers broader subject matter than any implied description of a sequential counter to count pulses that the Specification describes as determining the number of conducting reference cells. *See SuperGuide Corp.* 358 F.3d at 875 (quoted above).

Even if some implied relationship exists in claim 8, the output being “a count” signifies a sum (an accumulation), tracking the plain meaning. *See Ex. 3001* (a “count” is “a number reached by counting,” or “a reckoning, an accounting”). Note that this output of “a count” would not be superfluous to the construction of “a counter . . . to count pulses,” because the “count” must be output, and also, output as a “multi-bit digital output signal” (representing the number of conducting cells), whereas the counter merely

accumulates (or stores), at most, a calculated count of pulses (which may or may not relate to the number of conducting cells). *See, e.g.*, Ex. 1032, 3 (“counter” is “[a] device such as a register or storage location used to represent the number of occurrences of an event”).

Accordingly, in light of the Specification, the broadest reasonable interpretation of the phrase “a counter . . . to count pulses” tracks the plain meaning of its words (including the plain trade meaning), and means an “accumulator, circuit, or device that calculates the number of pulses.”

3) Remaining Terms

No other terms require explicit construction. *See, e.g., Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (only those claim terms or phrases that are in controversy need to be construed, and only to the extent necessary to resolve the controversy).

B. Alleged Obviousness of Claims 9 and 10 Based on Seligson and Yonemaru

Petitioner contends that the combination of Seligson and Yonemaru would have rendered claims 9 and 10 obvious. Pet. 49–56. To support its contentions, Petitioner provides explanations as to how the prior art discloses or suggests all of the claim limitations. *Id.* As noted above, Petitioner initially relies upon the Baker Declaration (Ex. 1003) to support its positions.

1) Seligson

Seligson discloses an ADC with programmable floating gate transistors. Ex. 1005, Abstract. Figure 4 of Seligson, as annotated by Patent Owner, is reproduced below:

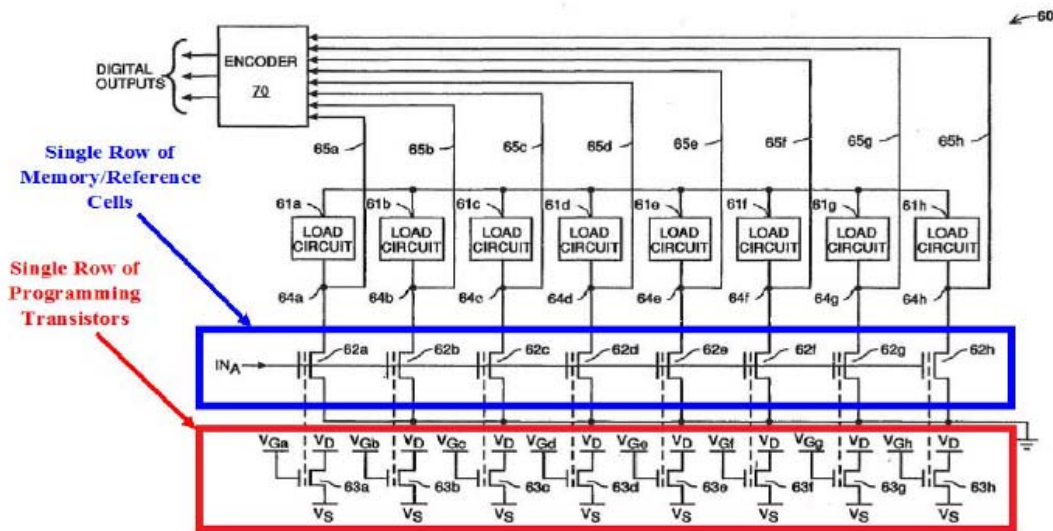
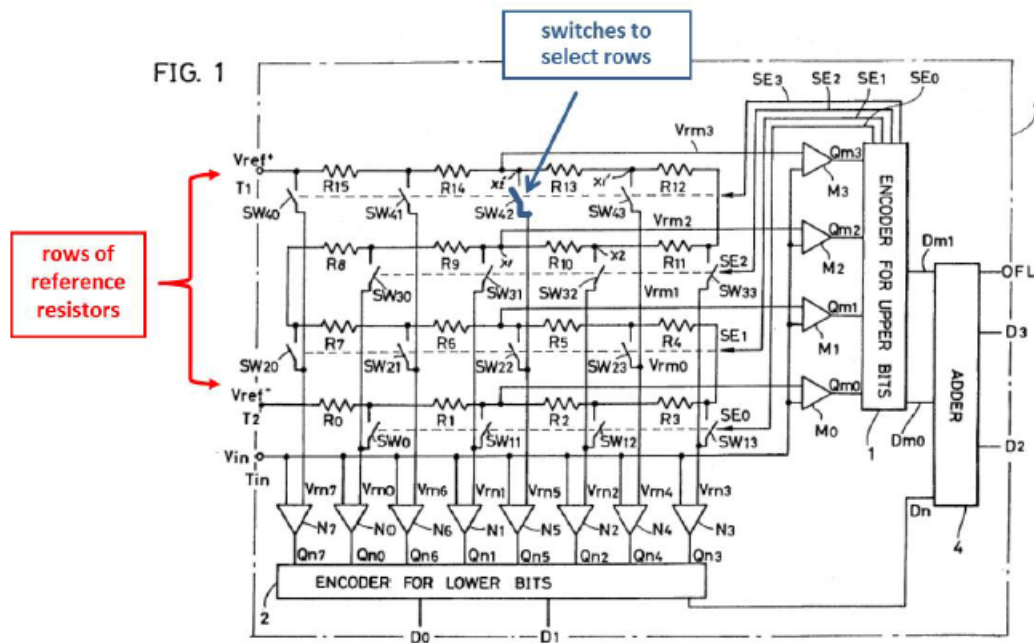


FIG. 4
Seligson Figure 4 (Annotated)

Prelim. Resp. 25. Figure 4 depicts a schematic view of Seligson's ADC, which includes a row of floating gate transistors 62a through 62h having gates connected to analog signal IN_A. Ex. 1005, 7:48–56. The transistors comprise a row of reference cells that convert analog signal IN_A to a digital signal. *Id.* at 7:52–56, Fig. 4. Floating gate programming transistors 63a–63h serve to program reference voltages in floating gate transistors 62a–62h. *Id.* at 8:22–52.

2) Yonemaru

Yonemaru discloses an ADC. Ex. 1006, Fig. 1. Figure 1 of Yonemaru, as annotated by Petitioner, is reproduced below:



Pet. 27. Figure 1 of Yonemaru represents an ADC employing a multiple row array of resistors each of which provide reference voltages for comparison to analog signal V_{in} . The upper bit encoder controls selector switches SE_0 – SE_2 to select a row of resistors for comparison of different proportions of V_{ref} to V_{in} as determined by selected resistors (i.e., resistor dividers). See Ex. 1006, 5:52–6:19, Fig. 1. Yonemaru teaches its “serial-to-parallel type A/D converter” (see *supra* Fig. 1) creates “a compact semiconductor circuit,” as compared to “a flash A/D converter” for which “the number of comparators increases exponentially as the number of bits increases” to obtain a desired resolution. Ex. 1001, 1:20–30. “[H]igh speed” converters include both types, flash and serial-to-parallel. *Id.* at 1:18–19.

3) Analysis

Claim 9 recites “an array of reference cells . . . wherein the array contains a plurality of rows.” Petitioner contends that Seligson discloses a row of reference cells at Figure 4 and also discloses an array of reference transistors as background art. Pet. 50 (citing Ex. 1005, 1:33–53 and the disclosure of “MOS” (metal oxide semiconductor) transistors). Petitioner contends that “Yonemaru teaches that the purpose of multiple rows is to provide for conversion of different ranges of analog values.” *Id.* at 51 (citing Ex. 1006, 6:20–37). Petitioner reasons that “[i]t would have been obvious in light of Yonemaru to add additional rows of the exemplary row within the Seligson array to likewise sense different ranges of analog values.” *Id.*

According to Petitioner, “[t]his would result in a multi-row arrangement of the floating gate transistors, *i.e.*, memory cells, and hence an array of memory cells that contain the first plurality of memory cells (a row within that array).” *Id.* Petitioner also contends that Seligson and Yonemaru involve the same field of endeavor (ADCs), and that “one of ordinary skill in the art would have been motivated to consider well-known architectures such as Yonemaru in combination with Seligson, *e.g.*, to decrease the size of the converter.” *Id.* at 28–29 (citing Ex. 1003 ¶ 99). Petitioner further contends that “the combination is simply arranging the Seligson elements according to a known technique, that is, arranging the reference cells of Seligson into a serial-to-parallel arrangement as in Yonemaru, and the results would have been understood as predictable.” *Id.* at 29 (citing Ex. 1003 ¶ 100).

With respect to a row decoder for selecting a row, Petitioner contends that Seligson teaches “a row of reference cells that accept the analog signal on their gates,” and “the encoder and switches of Yonemaru would connect the respective row to the analog signal (the gates in that row to the analog signal),” depending on the range of the signal in order to sense multiple analog ranges. *See* Pet. 53–54. Petitioner reasons that “it would have been obvious to combine Seligson and Yonemaru so that Seligson could sense multiple analog ranges.” *Id.* at 54 (referring to Section 8.5 of the Petition for “motivations to combine”).

Petitioner adds the following row decoder analysis:

Thus, by Yonemaru disclosing [a] row decoder (the encoder that generates the SE signals for the SW switches), which connects a respective row to the analog-to-digital path, and by Seligson disclosing a row of reference cells that accept the analog signal on their gates, Seligson in view of Yonemaru discloses a row decoder coupled to the array, the row decoder selecting a row of reference cells to which the analog signal is applied.

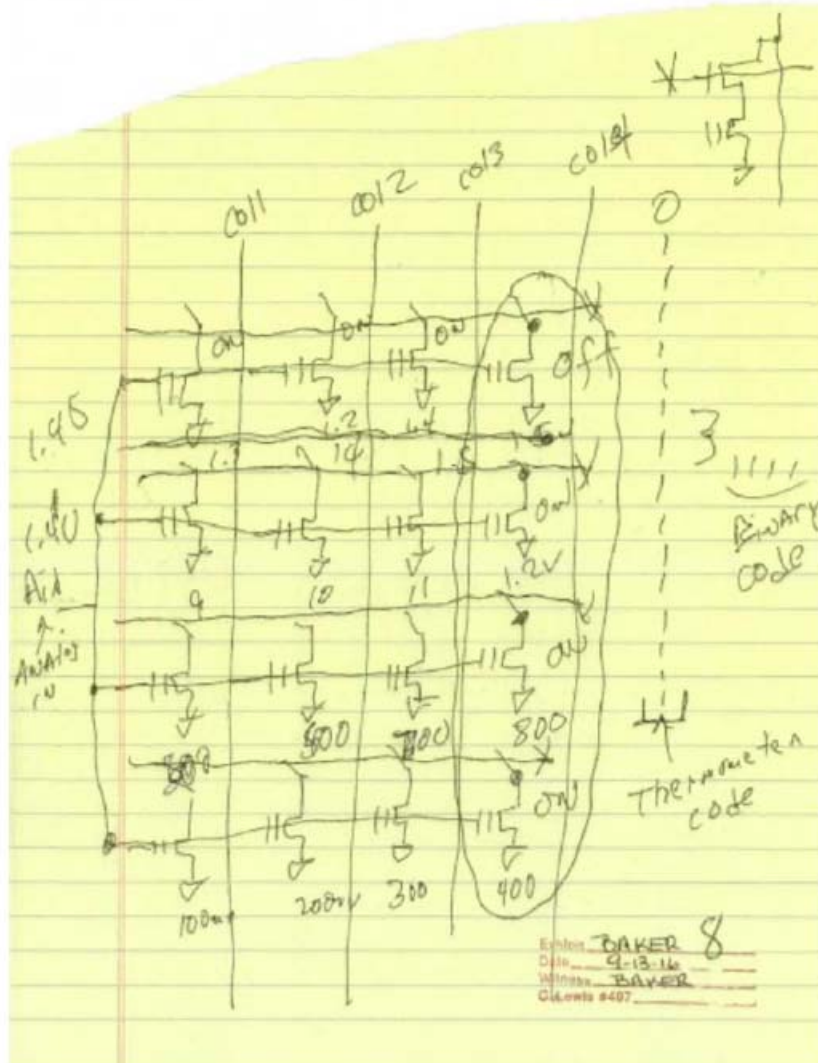
Pet. 54–55.

In response, Patent Owner contends that

it is abundantly clear that the combination proposed by Petitioner, relying upon its expert, R. Jacob Baker, Ph.D., is the rearrangement of Seligson’s one-pass parallel converter using floating-gate transistors into the architecture of Yonemaru’s two-pass serial-to-parallel converter.

PO Resp. 23. Further addressing the combination, Patent Owner explains that, “during his deposition, Dr. Baker made the drawing shown below, purporting to show the asserted combination.” *Id.* at 24 (citing Ex. 2004, 63–64).

Dr. Baker's deposition drawing, which Patent Owner includes in its Response, follows:



PO Resp. 24 (reproducing Dr. Baker's deposition drawing). This deposition drawing shows reference transistors, which Seligson teaches (see Ex. 1005, Fig. 4)) combined into an array of 4 rows via switches (which Yonemaru teaches (Ex. 1006, Fig. 1)).

Patent Owner addresses the deposition drawing as follows:

As Dr. Baker has described it, his drawing purports to show the modification using a 4-bit output implementation. He rearranged 16 of Seligson's elements (which consist of reference transistors and programming transistors) into a four row array, with each row containing four floating-gate transistors. The control gate of each of the reference transistors receives the analog input voltage, *Ain* (corresponding to *Vin* in Figure 1 of Yonemaru). As he initially described it, the converter depicted by Dr. Baker's drawing also includes four column lines (Col 1 – Col 4). Each transistor has an associated switch that is connected to its output terminal. *In each row, the output terminals of the four transistors in that row may be selectively coupled to their respective column lines by means of their associated switches.* Dr. Baker further describes an encoder (not shown in the drawing) coupled to receive the outputs of the last transistor in each row, as well as the outputs of the column lines. . . .

According to Dr. Baker's explanation, in operation, the analog input signal *Ain*, which is to be converted into binary code, is applied *at all times* to the control gates of *all* the transistors in the array. . . .

Id. at 25–26 (citing Ex. 2004, 35–48) (first emphasis added).

Based on this drawing, Patent Owner argues “the combination of Seligson and Yonemaru” does not result in “the analog signal being selectively connected to the gates of the transistors *in a particular row.*” *Id.* at 29 (emphasis added). Patent Owner similarly argues “[i]t is clear from the embodiments disclosed in the '503 [p]atent that are within the scope of this claim that at any given time, *the row decoder* recited in claim 9 selects from the plurality of rows of reference cells a single row of reference cells *that is to receive the analog input signal.*” *Id.* at 27 (emphases added).

As discussed above, claim 9 recites “selecting a row,” which requires “selecting at least one row,” instead of selecting a particular row. *See supra*

Section II.A.1 (Claim Construction). Therefore, Patent Owner’s arguments largely turn on claim construction and are not persuasive. Claim 9 also recites “a row decoder coupled to the array, the row decoder selecting a row of reference cells to which the analog signal is applied.” As Petitioner argues, and in line with the adopted claim construction, claim 9 includes a reading such “that any rows that are selected—whether one or more than one—have an analog signal applied to them.” See Pet. Reply 7 (interpreting the disputed selecting phrase in claim 9), 9 (asserting the combination satisfies the phrase under Patent Owner’s and Petitioner’s construction).

Patent Owner characterizes Petitioner’s reading of claim 9 (onto the combined circuit) as merely showing that Yonemaru’s row decoder (part of the encoder which provides SE signals (Ex. 1005, Fig. 1)), as combined with Seligson, picks a specific row to provide an *output* for that row. See PO Resp. 26–27; Pet. Reply 9–10 (citing Pet. 54). In other words, similar to the passage quoted above, Patent Owner characterizes Petitioner’s showing as follows:

The row selected by the encoder is the first row, going from bottom to top, in which the transistor at the end of the row is in an “off” state. Id. The encoder initiates the second pass by causing the switches of the selected row, and only that row, to close so that the outputs of the transistors in the selected row are connected to their respective column lines.

PO Resp. 26 (emphases added).

As indicated above, we adopt a combination of Patent Owner’s and Petitioner’s proposed claim construction as the broadest reasonable interpretation of the claim. See *supra* Section II.A.2. Under this construction, claim 9 includes a reading whereby a row decoder selects one

or more rows of the set of reference cells that have an applied analog signal. *See id.* The combined encoder satisfies the disputed phrase in claim 9, because it includes a row decoder that selects one or more rows connected to the input analog signal, according to Petitioner’s showing and the adopted claim construction. *See* Pet. 54–55, Pet. Reply 7 (citing Ex. 1030 ¶¶ 21–23)); Ex. 1005, Fig. 4; Ex. 1006, Fig. 1.

Patent Owner concedes that the combined decoder selects “a row to which the analog signal is applied,” because, as noted, Patent Owner concedes the analog signal is applied to all of the rows of reference cells in the combination in order to connect to the outputs of reference cells. *See* PO Resp. 27–30, 30 (“The only selection made by the ‘decoder’ in the converter of the proposed modification is the selection of the row of transistors whose *outputs* are to be connected to the column lines, i.e., the outputs to be provided to the encoder in the second pass.”). As described above, the ’503 patent supports the plain meaning of claim 9 and includes selecting a row already connected to an input signal. *Supra* Section II.A.2.

Patent Owner’s related claim construction argument, namely, that claim 9 requires “select[ing] the row of reference cells *to receive the analog input signal*,” is not persuasive for similar reasons. *Id.* at 30 (emphasis added). Claim 9 neither precludes selecting a particular row to provide an output nor requires selecting a particular row to receive the analog signal under the broadest reasonable claim construction. *See supra* Section II.A.2.

In Yonemaru, the decoder selects switches SW not only to select reference resistors in rows from set R0–R16, but that selection also provides different comparator N₀–N₇ inputs from selected rows of Vref inputs that depend upon the rows of selected reference resistors R0–R16. *See* Ex. 1006,

Fig. 1; Pet. 53–54 (citing comparators and row decoder signals for selecting rows). Therefore, Petitioner shows persuasively that the combination suggests the disputed claim 9 limitation under the adopted claim construction—a row decoder selecting at least one row of reference cells (transistors in Seligson) that have the analog input signal applied thereto—in order to save converter space and to convert different analog ranges into digital signals based on the row arrangement in a predictable fashion. *See* Pet. 26–29 (discussing Yonemaru’s two pass architecture, a coarse adjustment, and a fine adjustment, with rows reducing the footprint of comparators (citing Ex. 1003 ¶¶ 100–101)), 37–39 (Yonemaru teaches rows for different ranges of analog values), 47–54 (describing Yonemaru’s two stages rendering multiple rows in Seligson obvious, with each row providing a different sensing range); Ex. 1003 ¶¶ 91–92 (Yonemaru’s two pass converter reduces footprint).

Moreover, Petitioner shows that the combination renders claims 9 and 10 unpatentable for obviousness under both Patent Owner’s and Petitioner’s proposed claim constructions. Seligson’s transistors include reference voltages and inputs, which function similarly to the reference resistors and inputs in Yonemaru, and Yonemaru discloses select switches ultimately to provide different selected rows of voltage references for comparisons. *See* Ex. 1005, Fig. 4; Ex. 1006, Fig. 1; Inst. Dec. 23; Ex. 1030 ¶¶ 27–31.

Petitioner explains that Yonemaru’s “SW switches select rows within the resistor array depending on the value of the upper bits, *i.e.*, depending on the range of the analog signal.” Pet. 38 (citing Ex. 1006, 5:52–6:37); *see also* Pet. 53–54 (similar showing). Petitioner shows persuasively that modifying Yonemaru’s decoder and select switches to select at least one row of

programmable reference transistors in Seligson's circuit to attach an input voltage to a row would have been obvious for the purpose of sensing different analog ranges, while providing a known array configuration for utilizing available chip space. *See* Pet. 28–29, 37–39, 49–54.¹⁰

Petitioner adds that combining Yonemaru's switching and row arrangement with Seligson amounts to rearranging parts. *See* Pet. 28–29. As explained above, Yonemaru discloses switching V_{ref} (an input voltage) across different reference resistors to compare those reduced reference voltages to V_{in} (another input voltage), with both of those voltages ultimately provided as inputs at comparators N_0 – N_7 in Yonemaru's Figure 1. *See* Ex. 1006, Abstract, Fig. 1. Seligson's circuit similarly compares an analog voltage input to a row of reference cells that have programmed reference voltages to form a digital output. *See* Ex. 1005, Fig. 4. Seligson does not show any switches, including a switch for connecting input signal IN_A to input gates 62a–62h, but an artisan of ordinary skill would have recognized using some type of switch to control operation of the circuit. *See* Ex. 1005, Fig. 4; Ex. 1003, 70 (A-23) (explaining Seligson's row includes cells conduct “*during application* of the analog voltage (IN_A)” (emphasis added)).

Expanding Seligson's circuit from one long row to multiple shorter rows to save converter footprint space in light of Yonemaru's row and switch technique suggests switching the voltage to be compared, the analog input reference, into a row, similar to switching Yonemaru's compared

¹⁰ Various portions of the Petition refer to similar showings with respect to claims 1 and 8. *See, e.g.*, Pet. 52.

voltage input V_{ref} into a row, in order to obtain a digital output having expanded ranges. See Ex. 1006, Fig. 1; Pet. 53–54 (discussing row selection and comparators in Yonemaru); Ex. 1003, 67 (A-20), ¶¶ 91, 99 (rows reduce footprint and provide more sensing ranges).

In other words, Petitioner shows persuasively that Seligson and Yonemaru would have suggested employing Yonemaru's decoder to control switches SW (via signals SE) to connect an input voltage to a selected row of reference cells and thereby satisfy Patent Owner's narrower claim construction. See Pet. 53–54 (discussing Yonemaru's Figure 1). Stated another way, Yonemaru teaches using switches SW to select input reference voltages V_{ref} (via selected rows of reference resistors) to cause the comparators to compare V_{ref} to the analog input signal V_{in} , thereby effectively switching compared input (V_{in} and V_{ref}) values into the encoder to create digital outputs. See Ex. 1006, Fig. 1, Abstract, 6:11–49.

In its Sur-Reply, advancing its narrower claim construction of selecting rows to which to apply the input signal, Patent Owner contends

there would be no reason why one of ordinary skill in the art would *want* to add the pass transistors to Dr. Baker's serial-to-parallel converter. To do so would result in unwanted redundancy. As originally described by Dr. Baker, the Yonemaru switches in the Seligson/Yonemaru converter already select the rows to be connected *to the column lines*. Adding pass transistors to selectively connect the rows *to the analog input signal* merely duplicates the functionality already being performed by the switches that connect the selected rows to the column lines. Moreover, as can be seen in the figures included in Dr. Baker's Reply Declaration, adding this set of pass transistors would increase the footprint of the converter initially described by Dr. Baker. Ex. 1030.015, .020. Reduction in footprint was a primary motivation offered by Dr. Baker in the

first instance for arranging Seligson's transistors into Yonemaru's serial-to-parallel converter. Ex. 1003,044-.045, ¶¶ 99–100. In short, the only reason for adding this duplicative set of switches as Dr. Baker now suggests is to meet the limitations of the claim, using improper hindsight.

Sur-Reply 7.

These arguments are not persuasive. As discussed above, Yonemaru employs switches for two functions, connecting one input Vref and also connecting rows for an output. See Ex. 1006, Fig. 1. Dr. Baker's testimony, based on the teachings of Yonemaru and Seligson, represent Dr. Baker's view of different modifications of the combined teachings, including using switches to connect a row of memory cells to a voltage signal input, and also memory cells to a column, in order to measure the output pertaining to a selected row and column. See, e.g., Ex. 1030 ¶¶ 32–33 (figure showing switches/transistors and five rows of memory cells), 35 (“As shown above in the full figure, the same row signal that connects the row to the columns can also be used to turn on the ‘switch[es]’ to connect the row to the analog signal.”); Ex. 1003 ¶ 99; Ex. 1030 ¶¶ 29–41 (explaining how the original Baker Declaration and teachings in Yonemaru and Seligson convey the proposed modification, including a coarse conversion and a fine conversion circuit as portrayed in the Baker Reply Declaration).

Petitioner concedes Dr. Baker's modification involves some additional transistors. See Reply Br. 13. Nevertheless, Dr. Baker testifies that providing more rows expands the ranges of signals to be sensed and at the same time, generally reduces the overall footprint as compared to one long single row. See Ex. 1003 ¶¶ 91, 99; Ex. 1030 ¶¶ 40–41, 47 (folding approach reduces footprint as compared to a long single row).

Also, Dr. Baker testifies that applying A_{in} to one row at time as the combination of Yonemaru and Seligson suggests decreases load and power requirements, and increases speed, relative to one long row. *See* Ex. 1030 ¶ 41. Patent Owner also persuasively argues that in addition to using the row and column configuration to reduce a footprint, the row configuration allows for shared sensing and load circuitry and reduced encoder sizes. *See* Pet. Reply 17 (noting a single row of 256 transistors requires 256 load/sensing circuits as compared to 16 for a 16 x 16 array); Ex. 1030 ¶¶ 36, 41, 48; Ex. 1003 ¶¶ 91, 99.

As Patent Owner notes, Dr. Baker testified in his deposition that “adding a switch is something that even someone way below the skill required for ordinary skill in the art . . . would know how to implement if one wanted to only connect the analog input to one row.” *Id.* at 6–7 (citing Ex. 2013, 12). Patent Owner faults Dr. Baker’s reasoning because it does not provide a rationale for connecting the analog input to a row. This line of argument essentially reduces to the assertion that an artisan of ordinary skill would apply a switch to an output, but not recognize the same or a similar result would occur by applying a switch to the input. As noted above, Yonemaru discloses switches for applying voltage input V_{ref} to a comparator as an input, and Seligson at least suggests a switch of some sort to connect IN_A to the transistor inputs. Ex. 1006, Fig. 1; Ex. 1005, Fig. 4; Ex. 1003, 70 (A-23), 98 (A-51).

And as indicated above, Yonemaru’s row and switch (SW) teachings support Dr. Baker and provide a reason, as they suggest a relatively simple way of connecting Seligson’s analog input IN_A to Seligson’s row of reference cell inputs (gates), to obtain the predictable result of providing

analog to digital conversion for different voltage ranges while saving converter footprint space. *See* Ex. 1006, Fig. 1, 6:50–7–9 (selecting resistors R8–R15); Pet. 54 (arguing “the switches of Yonemaru would connect the respective row to the analog signal (the gates of the transistors in that row to the analog signal) depending on the range of the analog signal”); Pet. Reply 12, 14, 20 (citing Ex. 1030 ¶¶ 29–37) (reproducing circuits from Baker Reply Declaration representing the combination as suggested by the references)). Modifying Seligson’s single row array into multiple rows to save converter space for large arrays, in view of Yonemaru’s row switching technique, readily suggests using switches on the only controllable non-programming voltage input in Seligson, IN_A , in order to apply it to a selected row of reference cells for comparison purposes depending on the voltage range of the voltage input.¹¹ *See* Pet. 54; Pet. Reply 12, 14, 20; Ex. 1030 ¶¶ 32, 31–39 (showing a multiple row array, with each row using “Seligson cell[s]” and a Yonemaru “switch”).

As noted, Dr. Baker testifies in his Reply Declaration and during his deposition that using switches to select one input per row reduces the capacitive loading (thereby increasing speed and reducing power requirements). Ex. 1030 ¶ 41 (reducing the capacitance by selecting a single row at a time increases speed); Ex. 2013, 14:23–15:2 (“I think I said there could be a switch added . . . so that the analog signal is only applied to one row at a time. One might want to do that to reduce capacitive loading on the

¹¹ Seligson’s reference cells (i.e., transistors) have pre-set threshold voltages and require time to program with reference input programming voltage pulses V_G . *See* Ex. 1005, 4:40–59, 8:22–53, Figs. 2B, 4. They also must be erased to be reprogrammed. *See id.* at 8:45–52.

analog input signals I discussed in my second declaration.”); Ex. 1030 ¶ 27 (citing his original declaration (Ex. 1003, 98 (A-51)); Ex. 1003, 98 (A-51) (“Applying this teaching to Seligson would result in multiple rows of the exemplary row of Seligson reference cells shown in Fig. 4 of Seligson, and the switches of Yonemaru would connect the respective row to the analog signal (the gates of the transistors in that row to the analog signal).”)

In its Response, Patent Owner argues a lack of motivation to combine the references. For example, Patent Owner argues that Yonemaru only uses multiple rows “to provide a more refined conversion” of “the exact same analog signal” evaluated in the first, coarse step of the process. See PO Resp. 33. Therefore, according to Patent Owner and Dr. Madisetti, the combination of Seligson and Yonemaru “does not expand comparison or sense different voltages.” *Id.* at 33 (quoting Ex. 2001 ¶ 100).

Petitioner appears to concede that the combination does not expand the number of comparisons otherwise available in a single, long row or with respect to another parallel converter. See Pet. Reply 21 Pet. Reply 21 (“motivation does not require that the different ranges expand the overall range **relative** to the flash device”) (citing Ex. 1028, 99:14–21 (different rows may provide different ranges)). In other words, Petitioner simply shows for a given number of columns in an array, increasing the number of rows expands the available comparisons. For example, in addition to citing the reduced capacitance, power requirements, and footprint as noted above, Petitioner provides argument supported by persuasive evidence that in the first and second passes of Yonemaru’s serial-to-parallel (or two-pass) converter, “the multiple row arrangement allows for sensing different values (e.g., Row1: 0–1V; Row2: 1–2V). This expands the available conversions.”

Pet. Reply 21 (citing Ex. 1030 ¶ 40).¹² Petitioner also explains that “Dr. Madisetti admits the obvious: one row of cells with thresholds from 100 to 400 millivolts and another row with thresholds of 500 to 800 represents different ranges.” *Id.* (citing Ex. 1028, 99:14–21). Petitioner, citing Dr. Baker, provides example switch circuits in its Reply based on the combination that persuasively evidence the concept of multiple rows translating to multiple ranges. *Id.* at 32; Ex. 1030 ¶¶ 30–31, 39–40.

The record supports Petitioner’s argument. Simply put, adding more cell rows provides different voltage ranges for each row added (at least for a given number of columns), as Yonemaru teaches and Dr. Baker explains. *See* Ex. 1030 ¶¶ 30–31, 39–40 (circuits with analog input switches showing rows with different ranges). And as noted, adding rows reduces the “footprint” as compared to a single row, including by allowing for shared sensing circuitry and lines, and a smaller encoder. *See* Ex. 1030 ¶¶ 46–48 (“folding approach” as “[t]he practical way” that reduces footprint and reduces sensing loads and amplifiers); Ex. 1003 ¶ 91 (adding rows as Yonemaru suggests “reduces the footprint,” and “allows selectiv[e] use [of] the rows . . . depending on the value of the analog signal”); Ex. 1001, 10:6–8

¹² The parties refer to “serial-to parallel” architectures, like that of Yonemaru, as requiring multiple passes, typically two passes (i.e., coarse and fine). *See* Ex. 2001 ¶ 53; Pet. Reply 22 & n. 11, 24. Dr. Madisetti testifies serial-to-parallel (including two-pass) converters are slower but use fewer comparators (i.e., reduced circuit size) as compared to flash (parallel or single row) converters. Ex. 2001 ¶¶ 54–55. As discussed above, Seligson does not use comparators and instead uses floating gate and programming transistors. *Id.* ¶ 56.

(“Using multiple rows for a conversion allows higher resolution analog signals and more bits in digital signals.”).

Dr. Baker also testifies, in reply to Patent Owner, that it was common knowledge that single chips carried different and multiple voltages, so that “it is common sense to select a conversion that has a range in which the voltage will fall, e.g., 1–2 volts for the roughly 1.6 volt signal. This requires less power as a single pass because it utilizes a fraction of the overall converter (1 pass and only 1 row of transistors).” See Ex. 1030 ¶ 40; Pet. Reply 13–13 (reducing driver size). In other words, by using the two pass technique and a minimal number of rows corresponding to expected voltage ranges, as Yonemaru teaches, a skilled artisan would have recognized that relative to one long single row, using a number of rows having transistors within each row for fine tuning would have reduced power requirements and the footprint. See Pet. Reply 13 (citing Ex. 1030 ¶¶ 34–35, 37, 41).

Patent Owner also contends that speed and footprint amount to trade-offs that dictate toward selecting speed: “Any reduction in footprint of the converter, however, would have been insubstantial and would not have justified the loss of speed of the converter as a result of changing from a one-pass parallel converter to a two-pass serial-to-parallel converter.” PO Resp. 31. Patent Owner contends that the large reduction in footprint for two-pass, serial-to-parallel converters using *comparators*, which was well-known in the relevant art, does not transfer to the modification of using Seligson’s programmable *transistors* in that two-pass architecture (which Yonemaru employs). *Id.* at 32–33; see Ex. 1030 ¶¶ 45–49 (describing known benefits for folding arrays including reduced footprint, circuit and load sharing, and capacitance reduction).

Patent Owner also contends Petitioner’s proposed modification “would not have been a ‘simple’ matter.” *Id.* at 34. In support of the latter argument, Patent Owner points out that

Yonemaru employed two sets of comparators, one dedicated to the first pass for the upper bits and one dedicated to the second pass for the lower bits. In Dr. Baker’s design, the transistors at the end of each row are used in both passes, i.e., they are shared for both passes. The sharing of comparison elements in a two-pass serial-to-parallel converter is nowhere taught by the asserted prior art references.

PO Resp. 34–35. Patent Owner points out other differences between Dr. “Baker’s design” and Yonemaru’s encoder. *See id.* at 35.

These arguments are not persuasive. As Petitioner persuasively points out, Patent Owner’s characterization of a minimal footprint savings as outweighed by speed with respect to Seligson’s transistors, modified to be in a two pass architecture, as Yonemaru teaches, fails to consider larger arrays suggested by the combination. *See* Pet Reply 15–17. Petitioner’s arguments and supporting evidence show a substantial reduction in footprint when considering large arrays, which were common at the time. For example, Petitioner provides the example of a 256 (8-bit, 16 row x 16 column) array of Seligson transistor cells, and compares that array to a simple, column array using 256 cells arranged in a long single row. *See id.* at 16–17 (citing Ex. 1030 ¶¶ 45–49; Ex. 2021, 23). As noted above, Petitioner contends persuasively that the footprint reduction also includes fewer load and sensing circuits and traces via sharing (i.e., based on the number of columns). *See id.* at 17 (citing Ex. 1030 ¶ 48 (“If the array is folded into 16 x 16, then only 16 loads and sense amplifiers are needed.”)).

Patent Owner acknowledges some footprint reduction, even when employing transistors, such as those of Seligson, in a multiple-row array. Patent Owner frames the issue, however, as “[t]he reduction in size has to be enough to make the sacrifice in performance worth it.” PO Resp. 33. This argument tacitly acknowledges trade-offs, for example, a speed “performance” sacrifice necessarily would be “worth it” when size is a significant concern or design constraint (e.g., designing a small converter to fit into a tight space such as a space craft). See Pet. Reply 19 (“The point . . . is that the benefits of two-pass converters, e.g., footprint savings, often outweigh the impact on speed.”); see also Pet. Reply 18 (citing *In re Urbanski*, 809 F.3d 1237, 1244 (Fed. Cir. 2016) (finding motivation to combine reference “even if that meant foregoing the benefit taught by [the primary reference]”)). The apt comparison does not involve a comparison between two types of parallel converters, because both satisfy claims 9 and 10.

Petitioner also points out that Dr. Madisetti acknowledges that choosing converter architectures requires considering trade-offs, and provides evidence that high speed may come at a cost of accuracy (e.g., resolution) in parallel or flash converters that employ comparators. See *id.* & n.10 (arguing “Dr. Madisetti himself is an editor of a textbook which states that parallel converters are typically used only for very high speed low resolution applications.”) (citing Ex. 1008, 76; Ex. 1019, 30; quoting and discussing Ex. 1028, 57:9–60:3, 62:24–63:5)¹³; Ex. 1019, 30 (“flash A/D

¹³ Responding to Petitioner’s statement that “[f]or a higher speed analog/digital converter, person of ordinary skill in the art would consider a flash architecture,” Dr. Madisetti’s testifies “maybe not. I mean, it depends

converters are typically used only for very high speed low resolution applications”).¹⁴ Finally, as indicated above, replying to Patent Owner’s arguments, Petitioner also shows persuasively that some speed loss may be mitigated in a two-pass architecture via capacitive load reduction by successively selecting one row of transistors during the second pass for the fine conversion. See Pet. Reply 13 (citing Ex. 1030 ¶ 41), 25 (citing Ex. 1031, 24–26). Supporting this argument, at the cited paragraph, Dr. Baker testifies

one of ordinary skill in the art would have been motivated to apply the analog signal to as few transistors as possible, e.g., as few rows as possible, if speed was a consideration. This is because increasing the number of transistors to which the signal is applied increases the capacitance load for the signal. With a larger load, it takes longer to turn on the respective transistors.

Ex. 1030 ¶ 41.

Regarding Patent Owner’s argument that the modification would not have been simple, Petitioner persuasively responds that

on the application and the type of tradeoffs that they are evaluating in that context.” Ex. 1028, 62:23–63:4.

¹⁴ The textbook edited by Dr. Madisetti shows a circuit using parallel comparators and states “[t]he flash A/D, also known as a parallel A/D, is the highest speed architecture for A/D conversion since maximum parallelism is used.” Ex. 1019, 29–30. (“The speed of the converter is limited by the time delay through a comparator and the encoding logic. The speed is gained at the expense of accuracy . . .”). Dr. Baker’s textbook makes similar statements. See Ex. 1031, 192–193. The textbook also describes “two-step Flash” converters, which are similar in architecture to Yonemaru’s two-step converters (i.e., using coarse and fine grain adjustments), which minimizes the number of comparators as compared to parallel or flash converters. See *id.* at 195–199; Pet. Reply 24 (citing Ex. 1031, 192–201); Ex. 2001 ¶¶ 54–55.

Dr. Baker's adaptation of Seligson into a serial-to-parallel architecture is well within the ordinary level of skill in the art. That ordinary skill level includes at least an undergraduate degree in, for example, electrical engineering and 2–3 years of experience in the design of memory devices (or a graduate degree with less design experience).

Pet. Reply 22–23 (citing Ex. 1031, 20 (quoting and characterizing Dr. Baker's textbook as "offered at the senior/first-year graduate level")). Petitioner also points out "Dr. Madisetti taught different ADC architectures to his undergraduate students (including serial-to-parallel architectures), and confirms that pass transistors (or switches) are within the ordinary level of skill." *Id.* at 23 n.13 (citing Ex. 1028, 9:15–10:22, 17:6–18:3). The record shows that artisans of ordinary skill readily would have been able to employ switches in a serial-to-parallel architecture, as Yonemaru suggests, to reference cell gates, such as Seligson's transistors. Petitioner's summary of basic concepts and the skill level is persuasive. *See* Pet. Reply 22–24 (citing Ex. 1003 ¶¶ 19, 33–40; Ex. 1008; Ex. 1028, 9:15–10:22, 17:6–18:3; Ex. 1030 ¶ 51; Ex. 2001 ¶ 68).

Patent Owner's arguments that each of Yonemaru and Seligson discloses something different than the modification proposed by Petitioner do not address Petitioner's showing related to what the combination fairly teaches or suggests and narrowly focuses on circuit elements not involved in the combination, such as Yonemaru's comparators. *See* PO Resp. 35. For example, Patent Owner argues that Yonemaru's circuit uses all eight comparator outputs in the second pass without selecting them, whereas Petitioner's proposed combination only uses four transistors in the second pass, but must select them. *See id.* This comparison is not apt. For

example, as described above, Seligson's four transistor elements in a row function as a combination of resistor rows and comparators, and similar to the combination, Yonemaru's circuit selects resistor rows and voltage inputs to apply to comparators. In addition, Patent Owner's arguments impermissibly attack the references individually and assume bodily incorporation of components not required in the claims. *See id.*; Pet. Reply 21 (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Patent Owner's argument and related arguments that "an expert such as Dr. Baker can combine or modify prior art references so as to render the resultant combination obvious," does not challenge Dr. Baker's ability to opine about what an artisan of ordinary skill would have recognized from the combined teachings. *See* PO Resp. 35–36; *Duramed Pharmaceuticals, Inc. v. Watson Lab's, Inc.*, 413 F.3d App'x 289, 296 (Fed. Cir. 2010) (error to reject testimony of one who "was not a person of ordinary skill, but extraordinary skill," because "a person of extraordinary skill may opine on the knowledge of this hypothetical person") (citing *Moore v. Wesbar Corp.*, 701 F.2d 1247, 1253 (7th Cir.1983)) ("not selected for publication"). In any event, Patent Owner's arguments fail to overcome Dr. Baker's testimony (and Petitioner's showing) that persons of ordinary skill would have been able (and motivated) to combine the switch selection and row teachings of Yonemaru with Seligson's transistors to arrive at claim 9. *See* PO Resp. 35–36; Ex. 2013, 12:2–6 ("But adding a switch is something that even someone way below the skill required for ordinary skill in the art, as we defined in the declarations, would know how to implement if one wanted to only connect the analog input to one row."); Pet. Reply 22–24 (showing requisite skill level involved and citing Ex. 1003 ¶¶ 19, 33–40; Ex. 1008; Ex. 1028, 9:15–

10:22, 17:6-18:3; Ex. 1030 ¶ 51; Ex. 2001 ¶ 68); *see also* Ex. 1003 ¶ 21 (“My opinion below explains how a person of ordinary skill in the art would have understood the technology described in the references I have identified herein around the 1998 time period I was a person of at least ordinary skill in the art in 1998.”).

Patent Owner adds that Dr. Baker refers to the deposition drawing as “quite slick” (*see* PO Resp. 36), but in context, Dr. Baker merely responds to Patent Owner’s questioning and request to “draw out what you are referring to” on what appears to be a single sheet of paper. Ex. 2004, 35:14–15; PO Resp. 35–36 (citing Ex. 2004, 50).¹⁵ As noted above, Patent Owner argues that the sketch does not show all of the recited limitations (according to Patent Owner’s construction), cutting against the argument that providing the sketch shows extraordinary ability.¹⁶

¹⁵ In context, Dr. Baker testifies to “be[ing] able to line things up” as “quite slick,” after being asked if he “want[s] another piece of paper” and stating “I can do it with this [paper], no problem.” Ex. 2004, 13–22. Referring to a single page sketch as “slick” lacks sufficient context for an accurate characterization, but sketching aspects of the proposed combination on the spot during a deposition tends to support Petitioner’s showing that artisans of ordinary skill readily could have arrived at the invention based on the teachings of Seligson and Yonemaru. *See* Ex. 2004, 50. A couple questions later, during related questioning, Dr. Baker lends some context, and testifies that his modification tracks “the same way as seen in Figure 1 of Yonemaru. . . . And then you take the signals exactly as seen in Yonemaru and feed them back to activate the row.” *Id.* at 51:5–10.

¹⁶ Patent Owner’s Motions for Observation (Papers 30 and 32) and Petitioner’s Response to Patent Owner’s Motion for Observation (Paper 34) lend context to the Patent Owner Response, and we considered the Papers in addressing obviousness and in addressing the Motion to Exclude (discussed *infra*). We also have considered Patent Owner’s citations to Dr. Madisetti’s

As Petitioner argues, a showing of obviousness does not require bodily incorporation, so that contrary to Patent Owner's arguments, Dr. Baker does not necessarily have to show all of the specific circuit details involved in the combination in order to provide evidence of obviousness, either via a sketch during his deposition or otherwise in his Reply Declaration. See Pet. Reply 21–22. The '503 patent does not provide specific details as to how to apply *Ain* to a particular row, thereby indicating further that skilled artisans readily would have been able to use a switch to connect a signal to a gate. See Ex. 1001, Figs. 7A, 7B (showing row decoder boxes and CSEL signal).¹⁷ And “[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art.” See *Keller*, 642 F.2d at 425. For similar reasons, using the same reference cell transistors of Seligson for two passes merely combines teachings in a predictable fashion by placing reference cells in rows similar to Yonemaru's resistors.

With respect to claim 10, Petitioner contends that Yonemaru discloses terminals that output address signals SE0–3 to select conversions to connect appropriate rows through row decoder switches. Pet. 55–56. As set forth

Deposition for similar context. See Paper 32; Ex. 2015 (citing Ex. 1028).

¹⁷ Even if describing the biasing of unselected lines so they do not conduct constitutes some level of detail associated with Figure 7A, the Specification does not describe details of a row decoder circuit (apart from its use of signal CSEL) that selectively connects *Ain* to only a single row. See Ex. 1001, 9:18–31, Fig. 7A, 7B; *supra* Section II.A.1.

and summarized above with respect to similar reasons and findings supporting obviousness with respect to independent claim 9, Petitioner shows persuasively that it would have been obvious in view of Yonemaru to provide selective rows in Seligson's array for the purpose of altering or expanding the input voltage ranges to be converted while also minimizing the footprint. *See id.* and discussion *supra*. Petitioner also shows persuasively that selecting different conversions using Yonemaru's technique would have been obvious in order to allow appropriate selections for implementing a desired digital conversion of multiple analog ranges. *See id.* at 54–56. Patent Owner does not present and thereby waives arguments directed to claim 10. *See* Paper 11, 3 (“**The patent owner is cautioned that any arguments for patentability not raised in the response will be deemed waived.**”).

Based on foregoing discussion, Petitioner shows by a preponderance of evidence that the combination of the teachings of Seligson and Yonemaru would have rendered claims 9 and 10 obvious.

*C. Alleged Obviousness of Claim 8 Based on
Seligson and Bucklen, or Seligson, Yonemaru, and Bucklen*

1) Bucklen

Bucklen discloses an ADC and coding technique. Ex. 1007, Abstract. Regarding the coding, Bucklen teaches modifying a conventional “Gray” code using a “novel binary encoding technique.” *Id.* As background, Bucklen characterizes a prior art adding technique that employs an adder to count outputs as “not a simple matter.” *Id.* at 1:33–35. Bucklen also notes that with respect to thermometer codes, “[t]he desired output can be obtained as the sum of individual comparator outputs.” *Id.* at 1:27–28.

Bucklen also discloses converting an analog signal “in conventional fashion to an array of comparators, from which are obtained an array of output signals having a transition from ones to zeroes at the array position corresponding to the analog signal magnitude.” *Id.* at Abstract. In conventional higher resolution detection systems, “[o]nce the transition is located, it is converted to a desired digital code in a read-only circuit.” *Id.* at 1:38–40. Bucklen’s encoding technique improves upon prior art conversion techniques. *See id.* at 1:41–2:45.

2) Analysis

Similar to its showing with respect to claims 9 and 10, Petitioner asserts that Seligson discloses most of the limitations of claim 8. *See Pet.* 40–49. To the extent that Seligson does not disclose a multi-row array of memory cells or reference cells, Petitioner relies on the combination of the teachings of Seligson and Bucklen, or Seligson, Yonemaru, and Bucklen. *Pet.* 40–49.¹⁸

¹⁸ Petitioner adds Yonemaru in the event an “array” as recited in claim 8 requires more than one row and in case Seligson itself does not disclose or suggest a multi-row array as background art. *See Pet.* 46. In the Institution Decision, we determined that an array is broad enough to include one or more rows, an issue that largely involved (now disclaimed) claim 1. *See Inst. Dec.* 7–11. To the extent necessary to resolve an issue here (which neither party has raised), after further review of the record and based on a preponderance of evidence, we maintain that preliminary claim construction largely for the reasons advanced in the Institution Decision. *See id.* We also maintain our findings in the Institution Decision, which largely track our findings and reasoning herein, that it would have been obvious in view of Yonemaru to employ an array having multiple rows (assuming *arguendo* a narrow construction of an array that requires multiple rows (i.e., more than one)). *See, e.g., Pet.* 21–22, 54; *Ex.* 1003 ¶ 91 (multiple row array arrangement would have been a predictable rearrangement of cells, resulting

Petitioner's showing is persuasive. Claim 8 (reproduced above) largely recites known DAC subject matter, including an array, a sense circuit, an encoder, a counter, and a row decoder, as evidenced by the applied prior art, and as discussed generally above (with the exception of the counter) in connection with claims 9 and 10. *See* Pet. 40–49.

The only remaining dispute with respect to claim 8 on this record centers on the following “counter” phrase in claim 8: “wherein the encoder comprises *a counter coupled to count pulses* from the sense circuit, the multi-bit digital output signal being a count of the number of reference cells that conduct.” (Emphasis added.) Petitioner relies on Bucklen to teach the counter and its function of counting, as recited in the encoder of claim 8, contending it would have been obvious to implement the technique in an encoder such as that of Seligson (or as modified by Yonemaru) in order to convert the analog signal to a digital value in a predictable fashion. *See* Pet. 43–45. According to Petitioner, Bucklen discloses encoding circuitry that counts logical outputs and converts a thermometer code to binary form via an adder as a single pulse counter or as a zero to one transition counter. *See* Pet. 25, 43–45; Ex. 1007, 1:27–35 (prior art single pulse counter), 2:40–45 (one-to-zero transition counter).

Petitioner, citing the Baker Declaration, contends that Bucklen teaches an improved coding technique (via a one-to-zero transition counter) and discloses prior art adding techniques (via a prior art single pulse counter). *See* Pet. 44 & n. 15 (citing Ex. 1003 ¶¶ 84–88; Ex. 1007, 5:17–6:5). Petitioner contends that using either of these known counting techniques

in footprint reduction and the ability to sense multiple analog ranges).

would have been obvious to employ, where Bucklen generates a multi-bit digital thermometer code and Seligson's encoder accepts such a code, and "wherein [after the modification,] the encoder comprises a counter coupled to count pulses from the sense circuit, the multi-bit digital output signal being a count of the number of reference cells that conduct." See Pet. 45. Dr. Baker testifies that Figure 3 of Bucklen represents an "example of . . . an adder." Ex. 1003 ¶ 87.

To further support its showing, Petitioner cites to the Baker Declaration for the proposition that "the conversion of thermometer to binary code requires only counting or adding the number of logical 1s (or logical 0s)." Pet. 9 (citing Ex. 1003 ¶39; Ex. 1009, 2:33–34). At the cited paragraph, Dr. Baker cites Exhibit 1009 (EP 0 221 238 B1) as evidence to support the proposition that counting was well-known, and also cites Bucklen's prior art adder as an example adder that counts pulses. See Ex. 1003 ¶ 39 (citing Ex. 1009, 238, 2:33–35; Ex. 1007, 1:6–40).

Patent Owner replies that Bucklen's one-to-zero transition detector is not a counter. See PO Resp. 39. According to Patent Owner,

[t]he encoding circuitry taught and disclosed by Bucklen does not employ a sequential circuit to count individual pulses. Instead, it uses the outputs of the AND gates to provide an output code that identifies the particular comparator at which the transition from a logical 1 to a logical 0 occurred.

Id.

Patent Owner's argument with respect to Bucklen's improved, transition detector amounts to a claim construction argument that is not persuasive. Per the adopted claim construction, claim 8 does not require "a sequential circuit to count individual pulses." See *supra* Section II.A.2.

Patent Owner concedes that Bucklen's transition detector efficiently aggregates the "ultimate count":

While the sum, or total count of 1s in the comparator outputs, may be determined as a result of locating the transition point from logical 1 to logical 0, locating that transition point does not involve the use of a counter to count. *In other words, obtaining "the count" by locating the transition point is not the same as using a counter "to count" the pulses, as is required by claim 8 of the [']503 Patent.* In fact, as acknowledged by Dr. Baker in his deposition, the technique described by Bucklen for locating the transition point from 1 to 0 is different than, and *a far more efficient way of, determining the ultimate count than counting the number of individual 1s in the comparator outputs.*

See PO Resp. 40–41 (emphases added).

Patent Owner also concedes that Bucklen's prior art pulse counter satisfies its narrow claim construction. See *id.* at 41. Patent Owner contends, however, that Bucklen teaches away from using that prior art counter (i.e., a pulse counter that counts individual pulses) because of the "difficulty" in using it, and Bucklen otherwise teaches the above-noted improved transition detector as a "more efficient means of obtaining the count." See *id.* Petitioner replies that Bucklen only teaches that pulse counters (under the narrow construction) of the prior art suffer from an accuracy problem—i.e., that they are difficult to implement if accuracy is a concern. See Pet. Reply 25–26; Pet. 44 n.15; Ex. 1003 ¶¶ 84–88.

Regarding this prior art pulse counter, Bucklen states that "the desired digital output can be obtained as the sum of the individual comparator outputs." Ex. 1007, 1:27–28. Nevertheless, as Patent Owner points out, Bucklen also states that using such an "adder . . . is *not a simple matter* . . . and *virtually all higher-resolution* parallel analog-to-digital converters built

today rely on the detection of a single transition” method. *Id.* at 1:33–38 (emphases added). But, as Petitioner persuasively argues, describing the known, single pulse count method as “not a simple matter” and describing better “higher-resolution” alternatives for parallel converters does not amount to teaching away. See Pet. Reply 25–26 (stating just because “better alternatives” may exist in the prior art “does not mean that an inferior combination is inapt for obviousness purposes” (quoting *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012))).

“A reference that ‘merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into’ the claimed invention does not teach away.” *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1383 (Fed. Cir. 2017) (quoting *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013))) (also reasoning “Finseth does not say or imply that text descriptions are ‘unreliable,’ ‘misleading,’ ‘wrong, or ‘inaccurate,’ which might lead one of ordinary skill in the art to discard text descriptions completely”). The “mere disclosure of alternative designs does not teach away.” *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004).

Claim 8 does not specify or require any degree of resolution, and Bucklen refers to 256 comparators with respect to higher resolution converters. See Ex. 1007, 1:28–33, 4:1–5 (256 comparators, 8 bit resolution); Ex. 1003 ¶¶ 33–38 (indicating resolution increases as the number of quantization levels and bits increase); Reply Br. 15–16 (discussing bits relative to reference cells). Dr. Baker testifies that Bucklen’s description of prior art counters as not a simple matter involved a problem with errors in counting. See Ex. 1003 ¶ 86 & n.8. Petitioner

emphasizes that “this ‘simple’ statement [in Bucklen] was made in regards to the system’s susceptibility to errors resulting from faulty transitions” and that “the proposed combination of these elements in the references . . . would merely *result in a less accurate system (i.e., one that is ‘somewhat inferior’ in regards to accuracy).*” Pet. Reply 26 (emphasis added; citing *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007)).¹⁹

By arguing that the count is less accurate, Petitioner raises an issue with *Meiresonne*’s reasoning that such a teaching “*might* lead one of ordinary skill in the art to discard” the single pulse counter “completely.” See *Meiresonne*, 849 F.3d at 1383. But, as explained above in the claim construction section, claim 8 does not require the pulse counter to do anything with the pulse count. See *supra* Section II.A.2. It also does not require, as just noted above, higher resolution (*e.g.*, around 256 comparators, or 8 bits resolution). See Ex. 1007, 1:28–38, 4:1–5. In light of Bucklen’s disclosure, Dr. Baker’s testimony about accuracy is interpreted as directed to a problem associated with higher resolution (*i.e.*, the more bits, the more accurately the digital representation represents the analog input, but the harder to implement in a counter).²⁰ See *id.*; Ex. 1003 ¶ 86 & n.8. It follows

¹⁹ Petitioner’s quotation marks around “somewhat inferior” apparently refer to its earlier quotation of *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994). See Pet. Reply 25 (arguing [a] reference . . . does not teach away when it merely describes an article “as somewhat inferior to some other product for the same use”).

²⁰ Bucklen’s method improves the accuracy (decreases errors) caused by using the Gray code in known transitional (zero-to-one) counters. See Ex. 1007, 2:40–45.

that Bucklen does not teach away from using a well-known, single pulse counter according to the “the path . . . taken” in claim 8, because claim 8 does not require a high degree (or any degree) of resolution. See *Meiresonne*, 849 F.3d 1379 (quoting *Galderma Labs*, 737 F.3d at 738) (“A reference teaches away ‘when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken’ in the claim.”). Rather, Bucklen at most suggests that skilled artisans might have been led away from the well-known pulse counter in high resolution applications, but otherwise suggests they would have used such a well-known, single pulse counter in order to count single pulses accurately and easily in low resolution applications.²¹ See Ex. 1007, 1:28–38.

Based on the foregoing discussion, Petitioner shows that each of the logical adding and counting techniques described in Bucklen (i.e., the prior art single pulse counter and the zero-to-one transition counter) were well-known for converting thermometer codes. Notwithstanding Patent Owner’s arguments, Petitioner shows that artisans of ordinary skill would have been aware that these well-known techniques would have been effective as a form of counting pulses, in order to convert thermometer or similar codes in a modified encoder. See Ex. 1003 ¶¶ 85–88.

²¹ With respect to this teaching away analysis involving resolution and the single pulse counter, the combination of the teachings of Seligson and Bucklen does not require the above-discussed rationale advanced by Petitioner (as discussed above in connection with claim 9 and based on Yonemaru’s multiple rows) that using more rows (more resolution) would have saved footprint space especially for larger arrays. See also *supra* note 18 (discussing Yonemaru’s array teachings).

Based on the foregoing discussion, Petitioner has demonstrated by a preponderance of evidence that the combination of the teachings of Seligson and Bucklen, or Seligson, Yonemaru, and Bucklen, would have rendered claim 8 obvious.

III. MOTION TO EXCLUDE

Patent Owner moves to exclude paragraphs 24, 31–41, and 51–53 of the Baker Reply Declaration (Ex. 1030). Paper 31 (“Motion” or “Mot.”). Petitioner opposes the Motion. Paper 35 (“Opposition” or “Opp.”). Patent Owner replies to the Opposition. Paper 36. As movant, Patent Owner has the burden to establish that it is entitled to the requested relief. See 37 C.F.R. § 42.20(c).

Patent Owner’s Sur-Reply further contends that Petitioner shifted to a new claim construction by construing “selecting a row to which the analog signal is applied” to include selecting rows already connected to an analog signal (i.e., selecting rows to connect to the output). See Sur-Reply 1–3; *supra* Section II.A.2. But the Sur-Reply granted Patent Owner an opportunity to reply to new theories regarding allegedly new circuits in the Baker Reply Declaration upon which Petitioner contends Patent Owner’s *narrower* claim construction reads (i.e., selecting rows to connect to the input). See Reh’g Dec. 5. Patent Owner does not seek to exclude this allegedly new construction in its Motion, and it not clear why Patent Owner raises it now. Although Patent Owner cites to the Reply in its Rehearing Request, Patent Owner also does not characterize it as a new claim construction in its Rehearing Request. See Reh’g Req. 5 (arguing “the Board adopted Petitioner’s claim construction” (citing Pet. Reply 7)).

In any case, the record does not support Patent Owner’s argument that Petitioner restricted its initial showing to selecting rows to connect to an input. Petitioner did not construe “to which the analog signal is applied” explicitly in its Petition. Patent Owner correctly notes, however, that the Petition does allege it would have been obvious to use switches to connect a row to the input voltage (analog signal). See Pet. 54; Sur-Reply 1–2.

However, Patent Owner’s Sur-Reply notes that Dr. Baker also applied the broader reading that includes selecting rows to apply to an output: “[t]he only specific explanation [Dr. Baker] provided in his original Declaration was the use of the Yonemaru switches to select the *output* of the selected rows to the column lines.” Sur-Reply 5, 4 (citing Ex. 1003 ¶ 92); *see also id.* at 6 (“The only details and particularity [Dr. Baker] offered in his original Declaration, and again at his deposition, was how the Yonemaru switches connected the selected row to the column line.”); Mot. 5 (“Dr. Baker, only disclosed selecting a row of transistors whose *outputs* were connected to the column lines”). And, in the Institution Decision, without construing the phrase explicitly, we indicated the broader plain meaning that includes both selection options (input and output) applies, because we did not restrict the trial to the obviousness of connecting either the input or the output to the rows: “[A]ccording to Petitioner’s showing on this preliminary record, using Yonemaru’s encoder and select switches to select different rows of programmable transistors in Seligson’s circuit would have been obvious for the purpose of expanding comparisons and sensing different analog ranges, while providing a known array configuration for utilizing available chip space.” Inst. Dec. 23 (citing Pet. 28–29, 37–39, 49–54).

Therefore, Patent Owner had notice that the phrase would be read in the manner indicated. Patent Owner acted responsive to that notice by arguing for a narrower reading of the phrase in its Response: “It is clear from the embodiments disclosed in the ‘503 Patent that are within the scope of this claim that at any given time, the row decoder recited in claim 9 selects from the plurality of rows of reference cells a single row of reference cells that is to receive the analog input signal.” PO Resp. 27. On the next page, Patent Owner quoted the preliminary finding in the Institution Decision (quoted in the preceding paragraph) and indicated its awareness of the panel’s broader reading of the phrase, stating “[t]he issue, however, is not whether the combined references teach merely selecting rows, *regardless of the purpose*, but rather whether those combined references teach selecting the row of reference to which the analog input signal is applied, as required by claim 9.” *Id.* (emphasis added).

With respect to the interpretation Patent Owner advances, Patent Owner contends Dr. Baker originally provided no “detail” about how to connect input Ain to a rows:

He suggests that what he now describes in his Reply Declaration is what he meant in his original Declaration when he stated that “the switches of Yonemaru would connect the respective row to the analog signal (the gates of the transistors in that row to the analog signal).” Ex. 1030.017, ¶ 35. His original Declaration, however, is wholly lacking in any of the detail and particularity that he now includes in his Reply Declaration.

Sur-Reply 6.

Dr. Baker provided more detail in response to Patent Owner’s arguments urging a narrower claim construction and contending Petitioner failed to show how the combination arrived at that narrow construction. *See*

PO Resp. 26–29; Sur-Reply 4 (similarly alleging “Baker’s original Declaration *set forth no specificity* whatsoever as to how the switches of Yonemaru would connect the row to the analog signal” (emphasis added)).

The decision on this Motion only is relevant under Patent Owner’s narrower claim construction of “the row decoder selecting a row of reference cells to which the analog signal is applied.” If a broader construction applies (we determine it does), the Motion is moot, because the paragraphs sought to be excluded pertain to the narrower claim construction advanced by Patent Owner.

Assuming the narrower construction applies, Patent Owner contends that the cited paragraphs of the Baker Reply Declaration improperly raise new issues in reply to Patent Owner’s Response and, therefore, are not relevant under Fed. Rule Evid. 401 and prejudicial under Fed. Rule Evid. 403. Motion 1–2. Patent Owner’s contentions regarding relevance and prejudice under Fed. Rule Evid. 401 and 403 as a vehicle for a motion to exclude presuppose improperly that the Reply is beyond its proper scope in replying to the Response. To the extent the Baker Reply Declaration may exceed the proper scope of a reply, Patent Owner could have raised this question separately by seeking to file a paper limited to that scope issue. *See, e.g., Apple, Inc. v. Papst Licensing GHMG & Co.*, Case IPR2016-01839 (PTAB Nov. 30, 2017) (Paper 27). In other words, as Petitioner notes, motions to exclude evidence are not the proper vehicle to address the scope of a reply. *See Opp. 1, 5* (citing *Motorola Mobility LLC v. Intellectual Ventures I LLC*, IPR2014-00501, slip op. at 31 (PTAB Sept. 9, 2015) (Paper 48)). Patent Owner’s unauthorized Motion is improper.

Assuming the Motion is proper, as discussed further below, Petitioner argues persuasively that Dr. Baker merely replies to arguments made by Patent Owner. See Opp. 1–3. Patent Owner asserts the following basis for striking the Baker Reply Declaration: “Patent Owner has no further opportunity to submit any other paper to the Board that can substantively address the new evidence and theories raised by Dr. Baker.” Mot. 2. During the Oral Hearing, we queried Patent Owner and Petitioner about how to provide an opportunity for Patent Owner to address and alleviate Patent Owner’s stated concerns regarding the alleged new arguments and evidence in the Reply and Baker Reply Declaration, including discussing the possibility of additional briefing and evidence by Patent Owner. In response to a copy of an email that this panel did not receive until Patent Owner attached it to a declaration (Ex. 2016) with its Rehearing Request, we granted Patent Owner a Sur-Reply of seven pages (after incorrectly determining in the First Final Written Decision that Patent Owner declined the opportunity to seek additional briefing—the reason for withdrawing the First Final Written Decision). See Tr. 52:3–57:14; Reh’g Req. 5.²²

To afford Patent Owner an opportunity to be heard, even though Patent Owner did not request further briefing or evidence in its Rehearing Request as we noted in our Rehearing Decision, we granted Patent Owner a

²² During the Oral Hearing, after Patent Owner indicated it needed more time to decide how to respond to the Baker Reply Declaration and Reply, we instructed Patent Owner to confer with Petitioner and contact the Board via email to inform the Board of Patent Owner’s intention regarding additional briefing or other options. See Tr. 57:3–14. Patent Owner provides declaration evidence that it contacted the Board via email after the Oral Hearing regarding its concerns. See Reh’g Dec. 4 & n.2.

Sur-Reply. *See* Reh’g Dec. 5. As noted, Patent Owner’s Motion indicates that further briefing would provide it an opportunity it needed to be heard. *See* Mot. 2 (“Patent Owner has no further opportunity to submit any other paper to the Board that can substantively address the new evidence and theories raised by Dr. Baker.”). Patent Owner also indicates in its Motion that having its expert “analyze and opine” regarding the allegedly new evidence would have provided Patent Owner a full and fair opportunity to respond. *See id.* On the other hand, Patent Owner’s Sur-Reply states “a sur-reply limited to seven pages of additional briefing, with no additional expert declaration, renders hollow the opportunity now being afforded to Patent Owner to respond to Dr. Baker’s new assertions of unpatentability.” Sur-Reply 1.

Nevertheless, although Patent Owner sought relief in its email (Ex. 2016, App’x A) prior to its Rehearing Request, Patent Owner did not renew that email request (for additional briefing or an opportunity to provide declaration evidence) in its Rehearing Request. *See* Reh’g Dec. 4 (citing Reh’g Req. 1–4). Patent Owner also did not request an opportunity to provide further declaration evidence or seek extra pages after we granted the Sur-Reply. Patent Owner had the opportunity to allow its expert to analyze the Baker Reply Declaration to aid in preparing the Sur-Reply. And we do not dismiss any of the arguments Patent Owner made in its Sur-Reply as being mere attorney arguments. We accept them as if Patent Owner’s expert had endorsed them. Patent Owner also did not request a Sur-Reply until *after* the hearing. Although Petitioner ultimately has the burden of proof, we

did not grant Petitioner further briefing to respond to the Sur-Reply.²³ In addition, Patent Owner devotes roughly half of its Sur-Reply asserting that the broader claim construction creates a new issue. Sur-Reply 1–4 (“New Claim Construction”). Patent Owner also presents passages that resemble or restate arguments made in its Motion. *See id.* at 4 (“Notwithstanding this wholly conclusory statement, Baker’s original Declaration set forth no specificity whatsoever as to *how* the switches of Yonemaru would connect the row *to the analog signal*.”) Yet, the purpose for the Sur-Reply was to afford Patent Owner an opportunity to respond to the allegedly new circuits set forth in specific paragraphs of the Baker Reply Declaration. *See* Motion 4; Reh’g Dec. 5.

Under these circumstances, Patent Owner received an opportunity to be heard regarding the allegedly new circuits set forth in specific paragraphs of the Baker Reply Declaration. No more was required. Accordingly, Patent Owner’s Motion is *denied*. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1081 (Fed. Cir. 2015) (“With no Board denial of concrete, focused requests before us, we are not prepared to find that [the appellant] was denied a meaningful opportunity to respond.”)²⁴; Opp. 15 (“Patent

²³ In the copy of the email attached to Exhibit 2016 by Patent Owner, Patent Owner presented Petitioner’s position, part of which follows: “Should the Board grant Patent Owner’s request to file a sur-reply, Petitioner respectfully requests a deposition of Patent Owner’s expert and a responsive brief to the sur-reply.” Ex. 2016, App’x A, 2. Although Patent Owner prepared a contingent schedule in the event we decided to grant Petitioner’s contingent request for deposition testimony, Patent Owner opposed any request by Petitioner to file a “sur-sur-reply brief.” *Id.* at 1.

²⁴ *See also Securus Techs., Inc. v. Global Tel*Link Corp.*, 685 F. App’x. 979, 2017 WL 1458867, *4 (Fed. Cir. Apr. 25, 2017) (nonprecedential)

Owner also could have, but did not, request a sur-reply.” (citing *Belden*, 805 F.3d at 1081)).²⁵

We alternatively deny the Motion for the following substantive reasons. Patent Owner fails to meet its burden of showing that the Baker Reply Declaration does not reply properly to Patent Owner’s Response. (Also, to the extent the Baker Reply Declaration may exceed the proper scope of a reply, Patent Owner responded in the Sur-Reply, as noted above.)

Specifically, Patent Owner contends that Dr. Baker provided a “single conclusory statement” without “further disclosure whatsoever as to how the switches of Yonemaru connect the analog input signal to the row selected by the row decoder.” Mot. 3–4 (citing Ex. 1003 ¶ 98). According to Patent Owner, “there was no suggestion, for example, either in [Dr. Baker’s] Original Declaration or his deposition, that it would have been necessary for one of ordinary skill in the art to add missing circuitry not disclosed by Seligson and Yonemaru.” Mot. 4.

The record does not support Patent Owner’s argument. Patent Owner appears to allege that the additional circuitry may be “pass transistors.” Mot. 8. Nevertheless, as Patent Owner notes, Dr. Baker refers to these

(“Moreover, it is incumbent upon the party complaining of some procedural violation—such as the inclusion of improper rebuttal in a reply brief—to first raise the issue below. . . . Securus presents no evidence that it availed itself of the procedures for filing a sur-reply, a motion to strike, or a conference call to challenge this allegedly improper argument.”) (citing *Belden*, 805 F.3d at 1081)

²⁵ Petitioner filed the Opposition prior to Patent Owner’s email. Nonetheless, the argument applies to the extent Patent Owner waited to request further briefing and did not renew its request to supply further evidence.

allegedly new pass transistors as “Yonemaru switches.” *Id.* (citing Ex. 1030 ¶¶ 19–20, 39); Opp. 7 n.2 (“Patent Owner recognizes that Dr. Baker is relying on ‘Yonemaru switches’ for the allegedly new ‘pass transistors.’”); Ex. 1003, 98 (A.51) (“the switches of Yonemaru would connect the respective row [of Seligson’s reference cell gates] to the analog signal”); Pet. 54–55 (same). The Petition tracks that original testimony and proposes using the “encoder and switches of Yonemaru” to “connect[] a respective row to the analog-to-digital signal path” that includes Seligson’s “gates.” See Pet. 54–55. According to Patent Owner, however, “[t]he new figures and accompanying explanation that Dr. Baker includes in his Reply Declaration show how the same row signal that connects the row to the column lines can be used to turn on the pass transistors to connect the row to the analog input signal.” Mot. 9. According further to Patent Owner, this allegedly new evidence of proposed circuits and new rationale “includes significant detail that could readily have been included in his Original Declaration.” *Id.*

These arguments fail to show an improper Reply, which clarifies various ways in terms of circuitry to implement one aspect of the original ground in response to Patent Owner’s arguments that Petitioner provided insufficient detail with respect to Patent Owner’s narrow claim construction that it raised in the Patent Owner Response. As background, Petitioner shows persuasively that Patent Owner’s Motion attempts to cabin Petitioner’s showing by limiting it to Dr. Baker’s deposition sketch (made in response to Patent Owner’s questions), but “Patent Owner did not ask Dr. Baker whether the combination also teaches applying the analog signal to only a single row.” See Opp. 4. In other words, as Petitioner contends,

the deposition sketch only shows an example of the combined teachings of Yonemaru and Seligson, and does not even show the row decoder at issue. *See* Opp. 14 (citing Ex. 2004, 35:14–17, 44:13–25). In any event, the deposition sketch does not limit the showing in the Petition as outlined above (even if the sketch provides a handy reference point).

Petitioner also argues persuasively that “Patent Owner concedes that the alleged ‘new evidence’ at issue relates to whether the Seligson/Yonemaru combination renders obvious the ‘row decoder’ limitation under its new construction.” *Id.* “Patent Owner construed ‘row decoder’ in its Response, bringing this issue to the forefront. Thus, Petitioner is well within its rights to reply directly to this argument.” *Id.* at 6.

As Patent Owner acknowledges in its Motion, the Baker Declaration and the Petition refer explicitly to “the switches of Yonemaru” to be used in Seligson, which Dr. Baker shows with specificity in the new circuits provided in the Baker Reply Declaration (to implement selecting a row):

Dr. Baker stated: Applying [Yonemaru’s] teaching to Seligson would result in multiple rows of the exemplary row of Seligson reference cells shown in Fig. 4 of Seligson, and *the switches of Yonemaru would connect the respective row to the analog signal (the gates of the transistors in that row to the analog signal)*. Mot. 6 (quoting Ex. 1003.098 (A-51) and Pet. 54 (first emphasis added, second emphasis by Patent Owner)); *see* Pet. 54–55 (advancing materially the same showing).

As Petitioner argues, “[i]n the context of the combination, this statement [in the Baker Declaration and Petition, *see* Ex. 1003, 98 (A-51), Pet. 54] is referring to one or more rows, just as ‘a row’ of claim 9 refers to

one or more rows.” Opp. 6 n.1. Moreover, Dr. Baker provides the circuits in response to Patent Owner’s argument that the combination does not suggest “that the row decoder selects a row that is to be connected to the analog input signal.” See Mot. 6 (arguing “it was clear from Dr. Baker’s Original Declaration (as well as the Petition) that both he and Petitioner understood this language to mean that the row decoder selects a row that is to be connected to the analog input signal”).

In other words, as Petitioner contends, Patent Owner criticized Dr. Baker’s deposition drawing and also argued that it would not have been obvious to apply Yonemaru’s switch teachings to select a single row to connect it to an analog input signal *according to Patent Owner’s new narrow claim construction*, and Dr. Baker replied by showing details to support part of its original showing that it would have been obvious to arrive at the narrow alternative of selecting a row to which to apply the input. See Opp. at 1–4, 9–11 (arguing that Dr. Baker replies to show the normal meaning of “row decoder” and to implement Yonemaru’s switch teachings). As Petitioner persuasively argues,

[s]uch evidence that responds to Patent Owner’s criticism is proper because it confirms Petitioner’s *prima facie* case through elaboration. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1071, 1079 (Fed. Cir. 2015) (“Evidence admitted in rebuttal to respond to the patent owner’s criticisms will commonly confirm the *prima facie* case. That does not make it necessary to the *prima facie* case.”). That Patent Owner disagrees that Yonemaru teaches such “pass transistors” . . . is of no moment.

Id. at 12. Petitioner adds a related and valid point; the Reply evidence and argument are “relevant to the Petition (namely, an argument that Petitioner indisputably made in the original Petition) and [are] not prejudicial to Patent

Owner (it has been on notice of the argument since the Petition was filed).”
Id.

Therefore, Petitioner rebuts Patent Owner’s allegations and shows paragraph 24 of the Baker Reply Declaration properly responds to Patent Owner’s new assertion of an alleged special meaning for a “row decoder” (which relates to selecting a row), and also shows that “paragraphs 31–41 of Dr. Baker’s Reply Declaration simply elaborate on Dr. Baker’s original declaration” (with respect to the row decoder and implementing Yonemaru switches as pass transistors). *See id.* at 8–12. Petitioner also provides persuasive rebuttal and shows that Dr. Baker properly responds in paragraphs 51–53 by providing proper evidence of the ordinary skill level in the art to “rebut Patent Owner’s allegation that the Seligson/Yonemaru combination is beyond this level.” *See id.* at 12–13 (“Dr. Baker elaborated on his original opinion to demonstrate the knowledge required for this combination has been taught to undergraduate students before the priority date of the [’]503 [p]atent, including the use of ‘pass transistors’ relevant to Patent Owner’s new ‘row decoder’ construction.”).

Patent Owner also seeks to exclude Exhibits 1031 and 1035 “submitted support of the new unpatentability rationale offered by Dr. Baker in his Reply Declaration.” Mot. 15. As discussed above, however, we find that Dr. Baker’s rationale properly replies to Patent Owner’s Response.

Finally, as noted above, by being granted a Sur-Reply, Patent Owner had an opportunity to respond to theories it contends were improper as beyond the scope of its Response.

Based on the foregoing discussion, Patent Owner fails to meet its burden on the Motion. Accordingly, the Motion is *denied*.

IV. CONCLUSION

Petitioner shows by a preponderance of the evidence that claims 8–10 are unpatentable for obviousness, as follows: 1) claim 8 based on the combination of Seligson and Bucklen, or Seligson, Yonemaru, and Bucklen; and 2) claim 9 based on the combination of Seligson and Yonemaru.

V. ORDER

In consideration of the foregoing, it is hereby
ORDERED that claims 8–10 of the '503 patent are unpatentable;
FURTHER ORDERED that Patent Owner's Motion to Exclude is
denied; and

FURTHER ORDERED that, because this Final Written Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

INNOVATIVE MEMORY SYSTEMS, INC.,
Patent Owner.

Case IPR2016-00320
Patent 6,169,503 B1

Before KARL D. EASTHOM, JAMES B. ARPIN, and
KEVIN W. CHERRY, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*, concurring.

I concur in the majority’s decision determining that Petitioner shows, by a preponderance of evidence, that claims 8–10 of the ’503 patent would have been obvious, and denying Patent Owner’s Motion to Exclude (“Mot.” or “Motion”). I write separately regarding Patent Owner’s and our shared responsibility regarding the missed email request for a sur-reply.

In its Rehearing Request, Patent Owner challenged the alternative reason for denying the Motion, namely, our determination that Patent Owner had decided not to pursue additional briefing remedies Patent Owner alluded

to in its Motion. See 1st FWD 54–55 (citing Mot. 2). The First Final Written Decision explained the background underlying Patent Owner’s request as follows:

In its Motion, Patent Owner asserts the following basis for striking the Baker Reply Declaration: “*Patent Owner has no further opportunity to submit any other paper to the Board that can substantively address the new evidence and theories raised by Dr. Baker.*” Mot. 2. During the Oral Hearing, we queried Patent Owner and Petitioner about how to provide an opportunity for Patent Owner to address and alleviate Patent Owner’s stated concerns regarding the alleged new arguments and evidence in the Reply and Baker Reply Declaration, including discussing the possibility of additional briefing and evidence by Patent Owner. Patent Owner declined the opportunity. See Tr. 52:3–57:14.

Because Patent Owner chose not to avail itself of an opportunity to seek to respond to what it asserts are new argument and evidence, and its Motion indicates that such an opportunity would have been sufficient (Mot. 2), Patent Owner’s Motion is denied. See Belden Inc. v. Berk-Tek LLC, 805 F.3d 1064, 1081 (Fed. Cir. 2015) (“With no Board denial of concrete, focused requests before us, we are not prepared to find that [the appellant] was denied a meaningful opportunity to respond.”); Opp. 15 (“Patent Owner also could have, but did not, request a sur-reply.”) (citing Belden, 805 F.3d at 1081).

1st FWD 54–55 (footnote omitted) (emphases added); see Majority op. at 66 n.22.

In its Rehearing Request, filed 30 days after the First Final Written Decision issued, Patent Owner shows that, contrary to the quote from the First Final Written Decision, Patent Owner did attempt to contact the Board with a post-hearing email to avail itself of an opportunity to respond with additional briefing. See Reh’g Req. 3–4 (citing Ex. 2016; Ex. 2017). We have acknowledged this in our Final Written Decision.

Patent Owner provides declaration testimony that it sent a post-hearing email (specifically on Monday, March 27, 2017) following the Thursday (March 23, 2017) oral hearing, regarding a possible sur-reply and followed up once thereafter to confirm whether someone at the Board received the email. *See* Reh’g Req. 3; Ex. 2016; Ex. 2017. Patent Owner attaches a copy of the email (which includes Petitioner as a recipient) as an appendix to Exhibit 2016. *See* Ex. 2016, App’x.

Due to circumstances unknown, Patent Owner’s email requesting additional briefing only reached us after Patent Owner filed its Rehearing Request providing us with a copy of the email. In its Rehearing Request, Patent Owner requests that we modify and correct the First Final Written Decision to reflect that “Patent Owner did specifically request an opportunity to submit a sur-reply to address the new evidence and arguments raised in the Baker Reply Declaration, *and that Patent Owner has been denied that opportunity.*” Reh’g Req. 4 (emphasis added). Regarding Patent Owner’s request that we correct the record to show that “Patent Owner has been denied th[e] opportunity” (*id.*) for additional briefing, this we cannot do. Although we did not grant the request at the time it was made; we could not *deny* a request that we did not receive; and, ultimately, we granted a Sur-Reply to Patent Owner.

Although Patent Owner submitted an email request for briefing, it knew that we had not responded to that request, and it was aware of the impending statutory deadline for issuing the Final Written Decision. Patent Owner investigated the status of its email request within a week after submitting it, but apparently did not investigate the status further or attempt to renew its request or to seek a response to it prior to the statutory deadline

for issuance of our Final Written Decision. As we noted above, we did not learn of Patent Owner's attempted email request until one month *after* the mailing of our First Final Written Decision. *See id.*; Ex. 2016, App'x A; Ex. 3003.

Regarding its investigation of the status of its request, Patent Owner's counsel states that a call was placed to the Board "on or about April 3, 2017" (Reh'g Req. 3) by an associate, who testifies he spoke to an unnamed paralegal at the Board, who told the associate the Board had received the email request on March 27, 2017. Ex. 2016 ¶¶ 8, 9; Ex. 2017 ¶¶ 6, 7; *see* Reh'g Req. 3–4 ("Patent Owner was advised [by a paralegal at the Board] that the Board had received the email."). Based on the associate's testimony, it appears the paralegal either misspoke when confirming receipt of the email or in some way mishandled the email, as the paralegal staff later could not find it. *See* Ex. 3003. Without knowing to whom the associate spoke, we cannot confirm whether the email request actually was received and, if so, determine why it was not forwarded to us. In any event, apparently, Patent Owner made no further attempt to investigate or to contact us regarding the status of the email request before the issuance of the First Final Written Decision two months later on June 5, 2017. As noted above, the next communication with the Board regarding the email request was the Request for Rehearing, filed July 5, 2017.

Despite the Board's possible failure to route properly Patent Owner's email request to us, Patent Owner must bear some degree of responsibility for the email request going unanswered until *after* the statutory deadline passed. We note that, not only did Patent Owner request to file a sur-reply in its email, but it specified other steps to be taken on specific dates prior to

the statutory deadline for issuance of the Final Written Decision. Ex. 2016, App'x. Patent Owner apparently allowed each of those dates to pass without further attempts to learn the status of its request. Patent Owner also stated in its email request that Petitioner opposed the request, and, consequently, was aware that there was a possibility that, assuming that we received the request, we might be persuaded by Petitioner's arguments, which Patent Owner set forth in its email, and deny the request. Patent Owner was seeking the opposed sur-reply and had the greatest interest in learning our decision on its request, yet it allowed over three months (i.e., from April 3, 2017, until July 5, 2017) to pass before taking additional steps to obtain our response to its email request.²⁶

Finally, Patent Owner knew that it had the opportunity to request a sur-reply at the time of Petitioner's Reply, but chose not to address the issue until the Oral Hearing in response to questions from us. *See* Mot. 2; Opp. 15; Tr. 54:12–20; *see also Belden*, 805 F.3d at 1081 (“Thus, if the petitioner submits a new expert declaration with its Reply, the patent owner can respond in multiple ways. It can cross-examine the expert and move to file observations on the cross-examination. It can move to exclude the declaration. It can dispute the substance of the declaration at oral hearing before the Board. *It can move for permission to submit a surreply responding to the declaration's contents.* And it can request the Board waive or suspend a regulation that Patent Owner believes impairs its

²⁶ It also is not clear why Patent Owner chose to wait until the filing deadline for a request for rehearing to inquire regarding its email request when it was apparent from the First Final Written Decision that we had not received the request. *See* 1st FWD 54–55 (quoted above).

opportunity to respond to the declaration. The options are not mutually exclusive.” (emphasis added)). By waiting until the hearing to make its request for a sur-reply, however, Patent Owner placed a burden on the Board to evaluate a request for and potentially to consider additional briefing in the limited period of time between the Oral Hearing and the statutory deadline for issuance of the Final Written Decision. Further, by this delay, Patent Owner forfeited the opportunity to argue the content of any sur-reply at the Oral Hearing. The unnecessary expenditure of additional resources by the parties and the Board due to the preparation and subsequent withdrawal of the First Final Written Decision could have been avoided if the email – assuming it was received – had been handled properly by the Board and if Patent Owner had followed-up diligently on the status of its email request or made the request at an earlier point in the *inter partes* review.

As noted by the majority, the arguments presented in the Sur-Reply have been considered fully in the instant Final Written Decision After Rehearing.