

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

INNOVATIVE MEMORY SYSTEMS, INC.,
Patent Owner.

Case IPR2016-00325
Patent 7,000,063 B2

Before KARL D. EASTHOM, JAMES B. ARPIN, and
KEVIN W. CHERRY, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

DECISION

Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”), filed a Petition requesting an *inter partes* review of claims 42–44 of U.S. Patent No. 7,000,063 B2 (Ex. 1001, “the ’063 patent”) under 35 U.S.C. §§ 311–319. Paper 1 (“Petition” or “Pet.”). Innovative Memory Systems, Inc. (“Patent Owner”), filed a Preliminary Response. Paper 9 (“Prelim. Resp.”). Under 35 U.S.C. § 314, an *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons set forth below, we deny institution of an *inter partes* review of any of claims 42–44 of the ’063 patent.

A. Related Proceedings

According to the parties, the ’849 patent is involved in, at least, the following lawsuit: *Innovative Memory Sys., Inc. v. Micron Tech., Inc.*, 14-cv-1480 (D. Del. 2014). Pet. 2; Paper 7, 1.

Petitioner filed a number of other petitions challenging the patentability of certain subsets of claims in the following patents owned by Patent Owner: (1) U.S. Patent No. 6,169,503 B1 (Case IPR2016-00320); (2) U.S. Patent No. 7,045,849 B2 (Case IPR2016-00322); (3) U.S. Patent No. 7,495,953 B2 (Case IPR2016-00323); (4) U.S. Patent No. 7,886,212 B2 (Case IPR2016-00324); (5) U.S. Patent No. 6,324,537 B1 (Case IPR2016-00326); (6) U.S. Patent No. 7,085,159 B2 (Case IPR2016-00327); and (7) U.S. Patent No. 6,901,498 B2 (Case IPR2016-00330). *See* Pet. 2–3; Paper 7, 1.

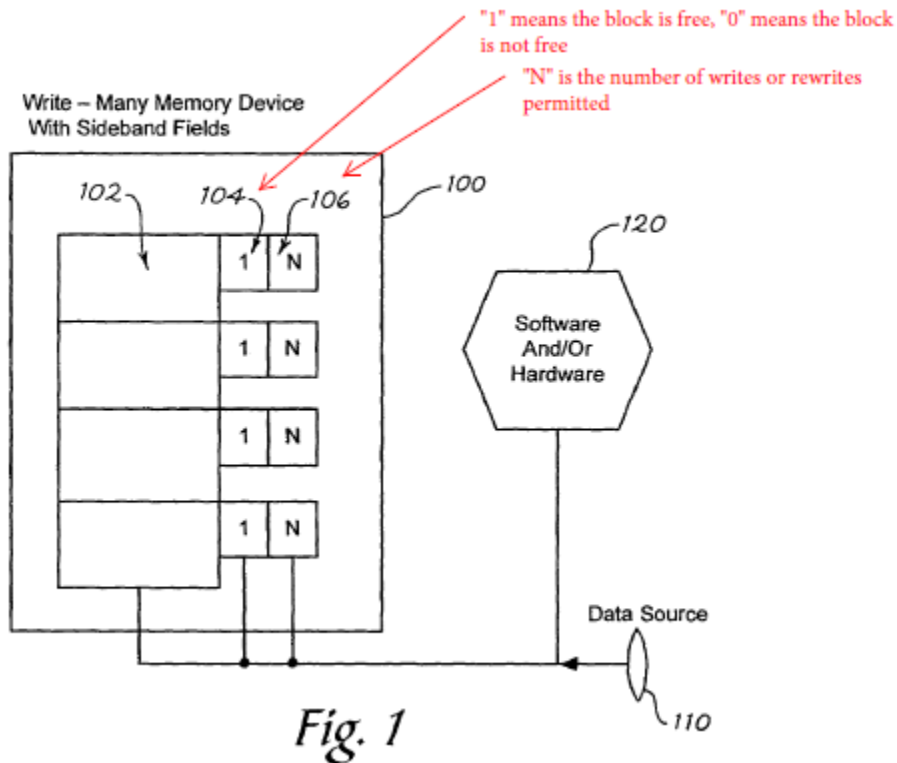
B. The '063 Patent

The '063 patent is titled “Write-Many Memory Device and Method For Limiting A Number Of Writes to The Write-Many Memory Device” and filed October 5, 2001, and issued February 14, 2006. Ex. 1001, at [22] and [45]. The '063 patent generally relates to

a write-many memory device and method for limiting a number of writes to the write-many memory device. In one preferred embodiment, a write-many memory device is provided comprising a plurality of blocks of memory, each block being limited to N number of writes. *Data can be stored in a block of memory only if there has been fewer than N number of writes to the block.*

Ex. 1001, Abstract (emphasis added).

Figure 1 of the '063 patent, including our annotations, is reproduced below.



Ex. 1001, Fig. 1. Figure 1 depicts write-many device 100 in communication with data source 110 and software and/or hardware components 120 that are operative to store data supplied by data source 110 in write-many memory device 100. *Id.* at col. 2, ll. 45–48. Each block 102 of write-many memory device 100

is associated with 16 bytes of “reserved” memory that is not user accessible. At least some of the 16 bytes are used for the first and second sideband fields 104, 106. The 512-byte block and its associated 16-byte reserved memory is referred to as a “page.”

The first and second sideband fields 104, 106 are used in a method for limiting a number of writes to the write-many memory device 100. The first sideband field 104 stores data indicating whether its associated block 102 is free. A block is free if the block does not contain data that should not be overwritten or erased. In one preferred embodiment, the first sideband field 104 stores a “1” if the block 102 is free and stores a “0” if the block 102 is not free. The second sideband field 106 stores data indicating how many times the block 102 has been written into. For example, the second sideband field 106 can store a count of how many times the block 102 has been written into, and each time the block 102 is written into, the count is increased. *Alternatively, the second side-band field 106 can store a count representing the remaining number of times that the block 102 can be written into, and this count is decremented each time the block 102 is written into.* In either alternative, the count can represent the number of re-writes instead of the number of writes.

Id. at col. 3, ll. 27–50 (emphasis added).

Second sideband fields 106 may be set to limit the number of writes to a certain number N, and the number N may be set to as few as one. *Id.* at col. 3, ll. 51–58; *see id.* at col. 6, ll. 5–12 (describing embodiments in which N=5 and N=10). In particular, when N=1, write-many memory block 102

may operate as a Write Once, Read Many (“WORM”). *Id.* at col. 3, ll. 56–59; *see id.* at Figs. 4A–4D (depicting embodiments in which $N=1$).

The value for the number N may be preset by the manufacturer. *Id.* at col. 3, ll. 56–57; *see id.* at col. 3, ll. 61–67 (defining “manufacturer”).

Moreover, referring to Figure 2, the Specification of the ’063 patent teaches that write-many memory device 100 may be a removable device that couples with host device 200, containing data source 110 and software and/or hardware components 120. *Id.* at col. 2, ll. 60–64; *see id.* at col. 2, ll. 64–67 (defining “coupled with”).

C. Illustrative Claim

Claim 42 is the challenged, independent claim of the ’063 patent. Each of claims 43 and 44 depends directly from claim 42. Claim 42 is illustrative and is reproduced below.

42. A method for creating a write-once memory device from a write-many memory device, the method comprising:

- (a) providing a memory device comprising a memory array comprising a plurality of write-many memory cell; and
- (b) *rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to said at least some of the write-many memory cells.*

Id. at col. 10, ll. 23–32 (disputed limitation emphasized).

D. Applied References, Document, and Declaration

Petitioner relies on the following references, document, and declaration in support of its asserted grounds of unpatentability:

Exhibit	References, Document, and Declaration
1002	File History '063 patent
1003	Declaration of Dr. R. Jacob Baker
1005	Patent No. US 6,662,262 B1 to Kasa <i>et al.</i> (“Kasa”), filed Oct. 19, 1999; issued Dec. 9, 2003
1006	B. Dipert and M. Levy, <i>Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards</i> (Annabooks 1994) (“Dipert”)
1007	Patent No. US 5,999,447 to Naura <i>et al.</i> (“Naura”), filed (FR) Nov. 28, 1997; filed (US) Nov. 25, 1998; issued Dec. 7, 1999

Pet. iv.

The '063 patent issued from U.S. Patent Application No. 09/972,787, filed October 5, 2001. Ex. 1001 at [21] and [22]. Petitioner asserts and Patent Owner does not here dispute that each of the applied references has an effective date prior to October 5, 2001. See Pet. 3–5.

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Reference(s)	Basis	Challenged Claim(s)
Kasa	35 U.S.C. § 102(e)	42 and 44
Kasa and Dipert	35 U.S.C. § 103(a)	43
Naura	35 U.S.C. § 102(b)	42
Naura	35 U.S.C. § 103(a)	44
Naura and Dipert	35 U.S.C. § 103(a)	43

Pet. 3–5.

II. ANALYSIS

A. Claim Interpretation

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs.*,

LLC v. Lee, No. 15-446, slip op. 12–20 (U.S. June 20, 2015). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

1. “write-many memory device”/write-many memory cell” (Claims 42–44)

Petitioner argues that the terms “write-many memory device” and “write-many memory cell” mean “an electronic storage device/cell to which data can be written more than once.” Pet. 10–11 (citing Ex. 1003 ¶¶ 52–55); see Ex. 1001, col. 2, ll. 18–23, col. 3, ll. 56–61, col. 5, ll. 43–57. Patent Owner agrees with Petitioner’s proposed constructions for these terms. Prelim. Resp. 6. On this record and for purposes of this Decision, we are persuaded that Petitioner’s proposed constructions for these terms are their broadest reasonable interpretations in the context of the claims and consistent with the Specification of the ’063 patent.

2. “write-once memory cells” (Claims 42–44)

Patent Owner contends that the term “write-once memory cells” means “memory cells to which data can be written *only* once.” Prelim. Resp. 7 (emphasis added). Petitioner does not propose a construction for this term. See Pet. 9–12.

Within independent claim 42, *some* of the “write-many memory cells” of the memory array are “rendered” into “write-once memory cells.” Ex. 1001, col. 10, ll. 28–31. Patent Owner contends that

[t]he ‘063 patent also provides “[t]he memory device 100 can be preset by the manufacturer so that it writes *as few as one time* (resulting in the write-many memory device operating as a WORM).” MICRON-1001.007, ‘063 patent, col. 3, lines 56-61. One of ordinary skill in the art would readily appreciate that a “WORM” is a “**Write Once, Read Many**” device, i.e., a device to which data can be written only once.

Prelim. Resp. 7 (emphasis added); *see* Ex. 1001, col. 6, ll. 5–12 (describing write-once memory device and various write-many memory devices), Figs. 1, 4A–4D. Further, the Specification of the ‘063 patent describes that “[t]here is a need, therefore, for a write-many memory . . . method *for limiting a number of writes to the write-many memory device.*” Ex. 1001, col. 1, ll. 38–40 (emphasis added).

On this record and for purposes of this Decision, we are persuaded that the broadest reasonable interpretation of the term “write-once memory cells,” as that term is used in the context of claim 42 and consistent with the Specification of the ‘063 patent, is “memory cells to which data can be written only once.”

3. Other Claim Terms

For purposes of this Decision, no other claim terms require express interpretation. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (explaining that “claim terms need only be construed ‘to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Anticipation by Kasa

1. Overview

Petitioner argues that claims 42 and 44 are unpatentable under 35 U.S.C. § 102(e) as anticipated by Kasa. *See supra* Section I.E. “A claim

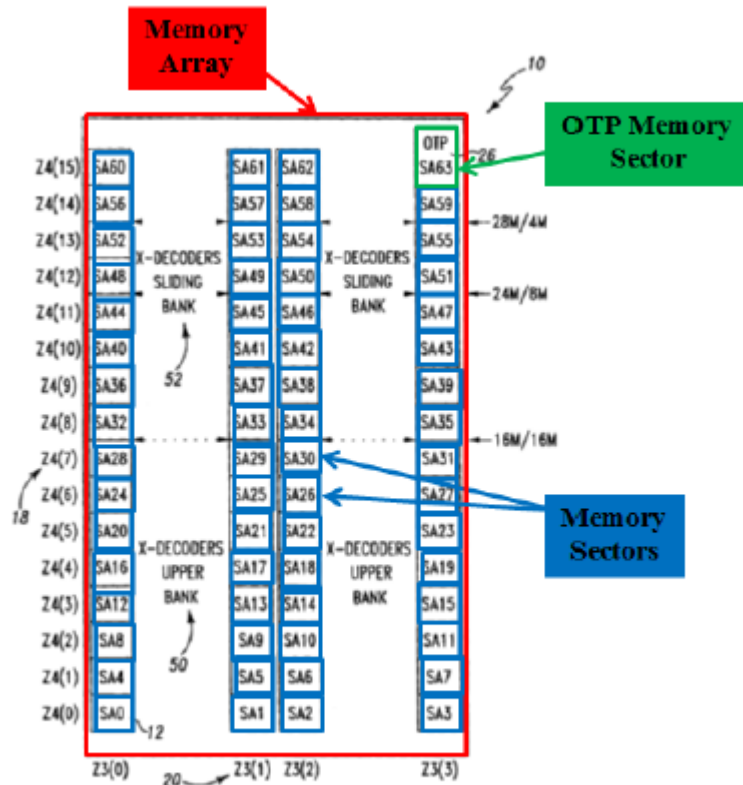
is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test. *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). “[U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed, and thus, cannot anticipate under 35 U.S.C. § 102.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008); *accord Application of Arkley*, 455 F.2d 586 (CCPA 1972). Moreover, “it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826 (CCPA 1968). On this record and for the reasons set forth below, we are not persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in this challenge to claims 42 and 44 of the ’063 patent.

2. *Kasa* (Ex. 1005)

Kasa is titled “OTP Sector Double Protection for a Simultaneous Operation Flash Memory” and relates generally to flash memory devices, including an array of storage sectors having memory cells, in which portions of the memory can be write-protected using a double-lock mechanism. Ex. 1005 at [54], Abstract; *see id.* at col. 3, ll. 41–43, col. 4, ll. 50–62, Fig. 4 (depicting “OTP Sector Write Protect CAM” and “OTP Sector Lock CAM”). *Kasa* refers to these portions of memory as one-time programmable

(“OTP”) sectors. *Id.* at col. 1, ll. 14–18, col. 3, ll. 31–40. As described in more detail below, the OTP sector of Kasa functions by converting write-many memory cells to read-only memory cells.

Kasa’s Figure 1, with Petitioner’s annotations, is reproduced below.



MICRON-1005, Kasa at Figure 1 (with annotations).

Pet. 14. Figure 1 depicts flash memory 10 including an array of storage sectors 12 (SA0–SA63) that include memory cells, each “preferentially arranged to store 512 kilobits of data.” Ex. 1005, col. 5, ll. 3–5, 35–59. One of storage sectors 12 may be OTP sector 26. *Id.* at col. 6, ll. 46–48; see *id.* at col. 3, l. 61–col. 4, l. 4.

[T]he OTP sector 26 is used to store data that cannot be erased in the simultaneous operation flash memory 10. In the preferred embodiment, the OTP sector 26 is programmed and tested during

fabrication, *then locked in a read-only state* after it is determined that the OTP sector 26 has been properly programmed.

Id. at col. 6, ll. 49–54 (emphasis added); *see id.* at col. 3, ll. 19–44, col. 3, l. 61–col. 4, l. 4, col. 4, ll. 33–62. In a preferred embodiment, OTP sector 26 has dual write protection, using two content addressable memories (“CAM”) that can be used to store data. *Id.* at col. 4, ll. 8–10, 18–22. “The two CAMs are the OTP sector write-protect CAM, which is used to write-protect data that has been written into the OTP sector, and the OTP sector lock CAM, which is used to lock the OTP sector write-protect CAM.” Prelim. Resp. 11 (citing Ex. 1005, col. 4, ll. 50–62). As noted above, when OTP sector write-protect CAM is programmed, the memory cells in OTP sector 26 are read only. Ex. 1005, col. 4, ll. 11–13. The OTP sector lock CAM, which is electrically connected to the OTP sector write-protect CAM, provides an additional level of security, and the OTP sector is protected from being altered. *Id.* at col. 4, ll. 18–32, 44–49.

3. *Analysis of Challenges*

a. *Claim 42*

As noted above, Petitioner argues that Kasa discloses each and every element of independent claim 42 of the ’063 patent. *See* Pet. 18–24; Ex. 1003, A1–23. In particular, Petitioner argues that Kasa discloses “[a] method for creating a write-once memory device from a write-many memory device” (Pet. 18–19; Ex. 1003, A1–7), including the step of “providing a memory device comprising a memory array comprising a plurality of write-many memory cell” (Pet. 20–21; Ex. 1003, A7–15). Petitioner and its Declarant, Dr. Baker, provide a detailed mapping of these elements onto Kasa’s disclosure, and Patent Owner does not expressly

dispute this mapping. See Prelim. Resp. 15–17. Consequently, we agree with Petitioner that Kasa discloses the elements of the preamble and the “providing” step of claim 42 of the ’063 patent.

Petitioner also argues that Kasa discloses “rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to at least some of the write-many memory cells.” Pet. 21; see Ex. 1003, A15–23. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the term “write-many memory cell” in the context of the ’063 patent to mean a “memory cell to which data can be written more than once.” See *supra* Section II.A.1. Petitioner further argues that

Kasa explains that it is necessary to write protect portions of the flash memory (i.e., the “write-many memory device”) to protect, for example, program code that is used to execute various operations that the flash memory is capable of performing. [Ex. 1005, col. 3, ll. 18–30.] Accordingly, it is necessary to include an OTP sector in the memory device, which cannot be erased or reprogrammed. [*Id.* at col. 3, ll. 31–37.]

Pet. 22. In particular, Petitioner argues that, *after the OTP sector has been programmed with content necessary for the functionality of the device containing the memory* (see Ex. 1005, col. 1, ll. 21–34, col. 3, ll. 36–38), “the OTP sector is protected by programming an OTP write-protect CAM and an OTP sector lock CAM.” Pet. 22 (citing Ex. 1005, col. 4, ll. 7–32).

Patent Owner contends that Kasa does not disclose the “rendering” step of claim 42. Prelim. Resp. 15–17. In particular, Patent Owner contends that Kasa does not disclose causing a write-many memory cell to become a write-once memory cell. *Id.* at 15–16. Instead, Patent Owner contends that “Kasa merely discloses causing a write-many memory cell to become a read-

only memory cell, i.e., a memory cell to which data can no longer be written,” after the data to be protected has been written to the write-many OTP sector. *Id.*; see Ex. 1005, col. 11, ll. 27–30 (“As set forth above, when the OTP sector write-protect CAM 34 is in the programmed state, the OTP sector 26 can only be used *as a read-only sector.*” (emphasis added)).

Patent Owner provides a diagram, reproduced below, comparing the method recited in claim 42 of the ’063 patent to the method disclosed in Kasa.

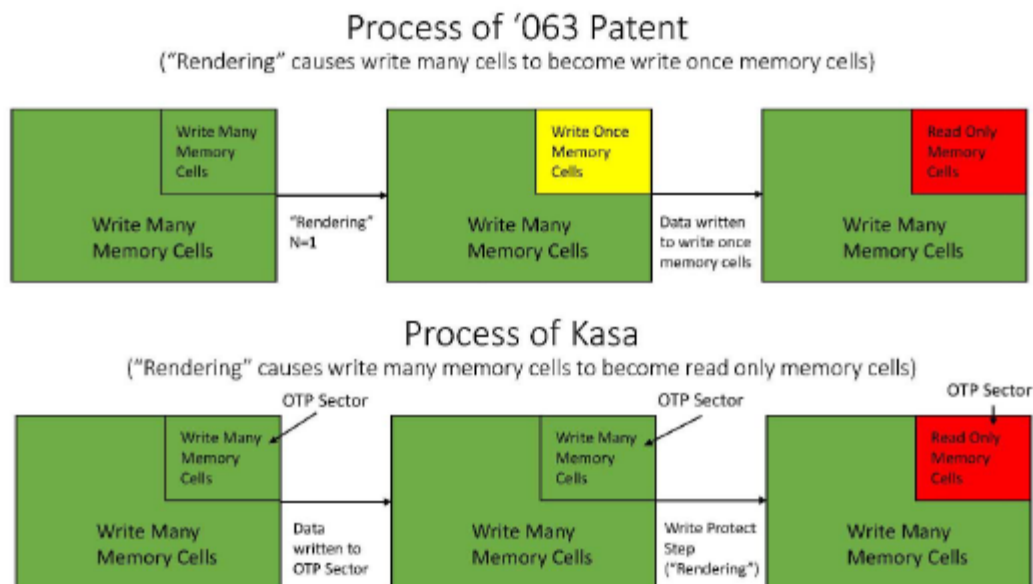


Figure 1

Id. at 17 (Patent Owner’s Figure 1). As shown by Patent Owner’s Figure 1, both the method recited in claim 42 of the ’063 patent and the method disclosed in Kasa begin with the memory array comprising write-many memory cells, but the method recited in claim 42 of the ’063 patent “renders” some of the write-many memory cells as write-once memory cells, e.g., by assigning number N a value of one. See *id.* at 16–17; *cf.* Ex. 1001, col. 10, ll. 40–43 (reciting embodiment of Figures 4A–4D in unchallenged,

dependent claim 45 that depends from independent claim 42); *see also Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) (Other claims of the patent can assist in the understanding of the meaning of a term of a challenged claim.). In Kasa, however, data is stored in the write-many memory cells of the OTP sector, and the CAM protections then are applied to convert the write-many memory cells of the OTP sector to read-only memory cells. *Id.* at 16; *see* Ex. 1005, col. 4, ll. 5–17. As Petitioner’s declarant, Dr. Baker, testifies,

[i]f the OTP sector write-protect CAM is programmed, the OTP sector is read only. However, if the OTP sector write-protect CAM is not programmed, then the OTP sector is not write protected and may be erased or reprogrammed. *In other words, the OTP sector is just like any other sector in the flash memory (i.e., it can be erased or reprogrammed) except for the fact that it can be write protected through a write protect CAM.*

Ex. 1003 ¶ 63 (emphasis added). Therefore, although Patent Owner acknowledges that the result of the method recited in claim 42 of the ’063 patent and the method disclosed in Kasa are substantially the same, namely, a combination of write-many memory cells and read-only memory cells, the recited and disclosed methods are different. To show anticipation, however, Petitioner must demonstrate that Kasa discloses each and every element, as set forth in claim 42. *See Verdegaal Bros.*, 814 F.2d at 631. We agree with Patent Owner that Petitioner fails to demonstrate that Kasa discloses the “rendering” step, as recited in claim 42. Prelim. Resp. 17.

Accordingly, on this record, Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing that Kasa anticipates claim 42 of the ’063 patent.

b. Claim 44

Claim 44 depends directly from independent claim 42 and recites the method of claim 42 “wherein said at least some of the write-many memory cells in the memory array are rendered as write-once memory cells by a manufacturer of the memory device.” Ex. 1001, col. 10, ll. 36–39.

Petitioner argues that Kasa also anticipates claim 44 of the ’063 patent. Pet. 24–25; *see* Ex. 1003, A24–28. However, Petitioner relies solely on the teachings of Kasa to supply the elements of independent claim 42. Pet. 24. Patent Owner contends that, because Kasa fails to disclose each and every element of claim 42, Kasa also fails to disclose each and every element of dependent claim 44. *See* Prelim. Resp. 17–18. In view of our analysis of the arguments with respect to claim 42 (*see supra* Section II.B.3.a.), we agree with Patent Owner. Consequently, on this record, we are persuaded that Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing that Kasa anticipates claim 44 of the ’063 patent.

c. Summary

Accordingly, on this record, we are persuaded that Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing that Kasa anticipates claims 42 and 44 of the ’063 patent.

C. Obviousness over Kasa and Dipert

1. Overview

Petitioner argues that claim 43 is unpatentable under 35 U.S.C. § 103(a) as obvious over Kasa and Dipert. *See supra* Section I.E. A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are “such that the subject matter[,] as a whole[,] would have been obvious at the time the invention

was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including the following: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art;¹ and (4) objective evidence of nonobviousness, i.e., secondary considerations.² *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). On this record and for the reasons set forth below, we are not persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in this challenge to claim 43 of the ’063 patent.

2. *Dipert (Ex. 1006)*

Dipert is a textbook, titled *Designing with Flash Memory, The definitive guide to designing flash memory hardware and software for components and PCMCIA cards* and allegedly published in April of 1994, which describes the basic features of flash memories and how flash memories are used with other electronic devices. Pet. 17; Prelim. Resp. 14. In particular, Dipert teaches that “[f]lash memory cards used for solid-state drives provide consumers with a removable mass storage device.” Ex. 1006, 37.

¹ Petitioner proposes an assessment of a person of ordinary skill in the art. Pet. 12; see Ex. 1003 ¶ 19. At this time, Patent Owner does not contest this assessment expressly or present an alternative assessment. For purposes of this Decision and to the extent necessary, we adopt Petitioner’s assessment.

² Patent Owner does not contend in its Preliminary Response that secondary considerations are present, which would render the challenged claims patentable over the applied references.

3. Analysis of Challenge to Claim 43

Claim 43 depends directly from independent claim 42 and recites the method of claim 42 “wherein the memory device comprises a modular memory device that is removabl[y] couplable [with] a host device.” Ex. 1001, col. 10, ll. 33–35; *see id.*, Certificate of Correction. Petitioner argues that Dipert teaches the additional limitations of claim 43 and that a person of ordinary skill in the art would have reason to combine the teachings of Kasa with those of Dipert to achieve the method recited in claim 43. Pet. 25–28. However, Petitioner relies solely on the teachings of Kasa to supply the limitations of independent claim 42. *Id.* at 27. Patent Owner contends that, because Kasa fails to disclose each and every element of claim 42, Kasa also fails to teach or suggest the limitations of dependent claim 44. *See* Prelim. Resp. 18. In view of our analysis of the arguments with respect to claim 42 (*see supra* Section II.B.3.a.), we agree with Patent Owner. Consequently, on this record, we are persuaded that Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing that Kasa and Dipert render claim 43 of the ’063 patent obvious.

D. Anticipation by Naura

1. Overview

Petitioner argues that claim 42 is unpatentable under 35 U.S.C. § 102(b) as anticipated by Naura. *See supra* Section I.E. On this record and for the reasons set forth below, we are not persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in this challenge to claim 42 of the ’063 patent. *See supra* Section II.B.1.

2. *Naura (Ex. 1007)*

Naura is titled “Non-Volatile Electrically Erasable and Programmable Memory” and relates generally to a write-many memory device, specifically “[e]lectrically erasable and programmable non-volatile memory devices.” Ex. 1007 at [54], col. 1, ll. 11–13. The memory devices may “comprise[] a memory array having a plurality of memory cells each for storing an information bit.” *Id.* at col. 2, ll. 51–52. The “cells of the memory array” may be subjected to “repeated write and erase cycles.” *Id.* at col. 3, ll. 1–3. The memory device, however, may include a row of memory cells in the memory array that can be programmed only once, i.e., a one-time programmable (“OTP”) row. *Id.* at col. 1, ll. 15–16, 25–27, col. 5, ll. 19–28. For example, the OTP row may store manufacturing references registered by the manufacturer, such as the date of manufacture. *Id.* at col. 1, ll. 11–21.

In addition, Naura teaches an OTP bit or state bit that indicates whether the OTP row of the memory has been programmed. *Id.* at col. 1, ll. 31–35. The OTP bit is programmed once data has been written into the OTP row. *Id.* at col. 1, ll. 34–37. The OTP bit has one value if the OTP portion has been programmed and the complimentary value if it has not been programmed. *Id.* at col. 1, ll. 31–35. If the OTP bit is programmed, the memory will not allow another write operation to the OTP row. *Id.* at col. 1, ll. 32–50. The OTP bit can be a special bit within the OTP row of the memory array or, alternatively, can be stored in a supplementary cell outside the memory array. *Id.* at col. 1, ll. 35–50, col. 2, l. 66–col. 3, l. 3, col. 5, ll. 19–23, 34–43; *see id.* at Fig. 1 (depicting “OTPCELLS”).

Because the “cells of the memory array” may be subjected to “repeated write and erase cycles” (*id.* at col. 3, ll. 1–3), Naura teaches

transferring the OTP bit from the memory array, where it was susceptible to deterioration due to high voltages used to program and erase the cells of the memory array, to a separate supplementary cell. *Id.* at col. 1, ll. 41–45, col. 2, ll. 66–67. Because of the importance of the data stored in the OTP row, the OTP bit must maintain its value, so that the OTP row is not erased by a new write operation. *Id.* at col. 5, ll. 40–43.

Although Kasa teaches write-protecting OTP sectors using dual CAMs, Naura teaches write-protecting an OTP row using an OTP bit and, optionally, storing the OTP bit in a supplementary cell that is not part of the memory array. Prelim. Resp. 12–13. Patent Owner contends, however, that both references teach that write-many memory cells of a memory array are rendered as read-only memory cells. *Id.* at 13.

3. Analysis of Challenge to Claim 42

As noted above, Petitioner argues that Naura discloses each and every element of independent claim 42 of the '063 patent. *See* Pet. 29–33; Ex. 1003, A37–54. In particular, Petitioner argues that Naura discloses “[a] method for creating a write-once memory device from a write-many memory device” (Pet. 29; Ex. 1003, A37–42), including the step of “providing a memory device comprising a memory array comprising a plurality of write-many memory cell[s]” (Pet. 29–31; Ex. 1003, A42–47). Petitioner and its Declarant, Dr. Baker, provide a detailed mapping of these elements onto Naura’s disclosure, and Patent Owner does not expressly dispute this mapping. *See* Prelim. Resp. 18–21. Consequently, we agree with Petitioner that Naura discloses the elements of the preamble and the “providing” step of claim 42 of the '063 patent.

Petitioner also argues that Naura discloses “rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to at least some of the write-many memory cells.” Pet. 31–33; see Ex. 1003, A47–54. Under the broadest reasonable interpretation standard, a person of ordinary skill in the art would have understood the term “write-many memory cell” in the context of the ’063 patent to mean a “memory cell to which data can be written more than once.” See *supra* Section II.A.1. Petitioner further argues that

Naura explains that it is necessary to make a portion of the write-many memory device one-time programmable to contain, for example, manufacturing data. These one-time programmable cells in the memory device can be a row of the memory array known as the “OTP row.” These memory cells in the OTP row are protected by a state bit called the OTP bit. The OTP bit can be in the OTP row in the memory array or alternatively in a supplementary cell outside the memory array. The OTP bit indicates whether the OTP row has been programmed or not. Whether the memory permits writing to the OTP row depends on the value of the OTP bit. *Thus, Naura discloses preventing more than one write to memory cells in the OTP row of the memory device by setting the value of the OTP bit (i.e., creating “write-once memory cells” from the “write-many memory cells”).*

Pet. 31–32 (emphasis added, citations omitted).

Patent Owner contends that Naura does not disclose the “rendering” step of claim 42. Prelim. Resp. 18–21. In particular, Patent Owner contends that

Naura never writes data to a write-once memory cell. The memory cells in Naura are either write-many, before the OTP row has been locked, or read-only, after the OTP row has been locked. All writing in Naura is to write-many memory cells. Thus, the “rendering” disclosed in Naura (locking the OTP row) never causes at least some of the write-many memory cells to

become *write-once* memory cells, but rather, causes them to become *read-only* memory cells.

Id. at 20. Patent Owner provides a diagram, reproduced below, comparing the method recited in claim 42 of the '063 patent to the method disclosed in Naura.

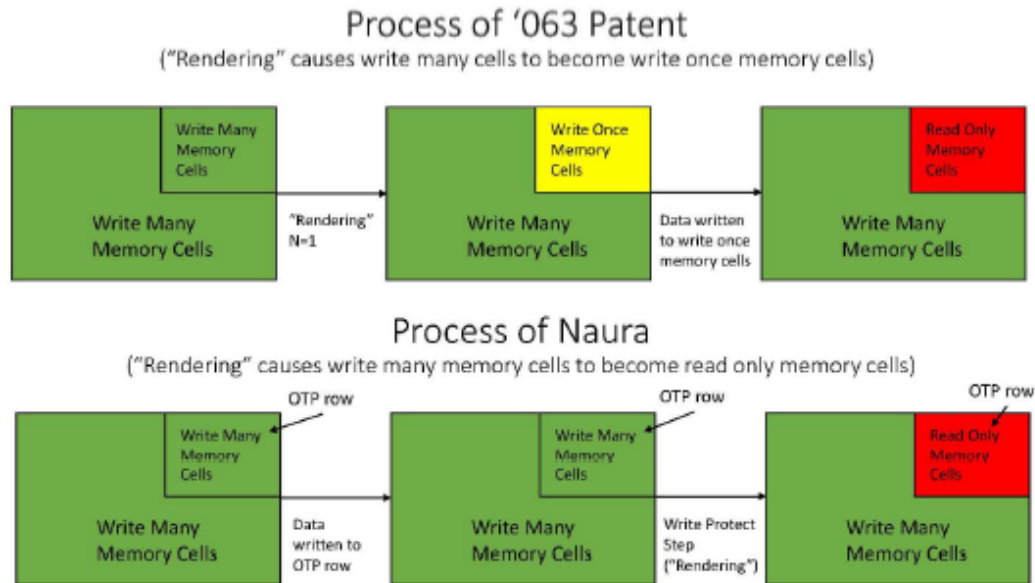


Figure 2

Id. at 21 (Patent Owner’s Figure 2). As shown by Patent Owner’s Figure 2, both the method recited in claim 42 of the '063 patent and the method disclosed in Naura begin with the memory array comprising write-many memory cells, but the method recited in claim 42 of the '063 patent “renders” some of the write-many memory cells as write-once memory cells, e.g., by assigning number N a value of one. *See id.* at 20–21; *cf.* Ex. 1001, col. 10, ll. 40–43 (reciting embodiment of Figures 4A–4D in unchallenged, dependent claim 45 that depends from independent claim 42). In Naura, however, data is stored in the write-many memory cells of the OTP row and then the OTP bit is selected to prevent further writing to the write-many

memory cells of the OTP row, thus, rendering those write-many memory cells as read-only memory cells. *Id.* at 20; *see* Ex. 1007, col. 1, ll. 36–39. As Petitioner’s Declarant, Dr. Baker, testifies, “[t]he OTP cells are just like the other memory cells in the memory array and thus can be accessed by an appropriate address.” Ex. 1003 ¶ 72 (citing Ex. 1007, col. 1, ll. 28–31). Therefore, although Patent Owner acknowledges that the result of the method recited in claim 42 of the ’063 patent and the method disclosed in Naura are substantially the same, namely, a combination of write-many memory cells and read-only memory cells, the recited and disclosed methods are different. To show anticipation, however, Petitioner must demonstrate that Naura discloses each and every element, as set forth in claim 42. *See Verdegaal Bros.*, 814 F.2d at 631. We agree with Patent Owner that Petitioner fails to demonstrate that Naura discloses the “rendering” step, as recited in claim 42. Prelim. Resp. 21.

Accordingly, on this record, Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing that Naura anticipates claim 42 of the ’063 patent.

E. Obviousness Over Naura

As noted above, claim 44 depends directly from independent claim 42 and recites the method of claim 42 “wherein said at least some of the write-many memory cells in the memory array are rendered as write-once memory cells by a manufacturer of the memory device.” Ex. 1001, col. 10, ll. 36–39. Petitioner argues that Naura alone renders claim 44 of the ’063 patent obvious. Pet. 36–39; *see* Ex. 1003, A66–69. However, Petitioner relies solely on the teachings of Naura to supply the elements of independent claim 42. Pet. 37. Patent Owner contends that, because Naura fails to disclose

each and every element of claim 42, Naura also fails to teach or suggest all of the limitations of dependent claim 44. *See* Prelim. Resp. 22. In view of our analysis of the arguments with respect to claim 42 (*see supra* Section II.B.3.a.), we agree with Patent Owner. Consequently, on this record, we are persuaded that Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing that Naura renders claim 44 of the '063 patent obvious. *See supra* Section II.B.3.b.

F. Obviousness Over Naura and Dipert

As noted above, claim 43 depends directly from independent claim 42 and recites the method of claim 42 “wherein the memory device comprises a modular memory device that is removabl[y] couplable [with] a host device.” Ex. 1001, col. 10, ll. 33–35; *see id.*, Certificate of Correction. Petitioner argues that Dipert teaches the additional limitations of claim 43 and that a person of ordinary skill in the art would have reason to combine the teachings of Naura with those of Dipert to achieve the method recited in claim 43. Pet. 33–36. However, Petitioner relies solely on the teachings of Naura to supply the limitations of independent claim 42. *Id.* at 35. Patent Owner contends that, because Naura fails to disclose each and every element of claim 42, Naura also fails to teach or suggest the limitations of dependent claim 44. *See* Prelim. Resp. 21–22. In view of our analysis of the arguments with respect to claim 42 (*see supra* Section II.B.3.a.), we agree with Patent Owner. Consequently, on this record, we are persuaded that Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing that Naura and Dipert render claim 43 of the '063 patent obvious. *See supra* Section II.C.3.

III. CONCLUSION

For the foregoing reasons, we are not persuaded that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that any of claims 42–44 of the '063 patent are unpatentable over the applied references. *See supra* Section I.E.

IV. ORDER

Accordingly, it is:

ORDERED that the Petition is *denied*, and no *inter partes* review is instituted as to any of claims 42–44 of the '063 patent.

FOR PETITIONER:

Douglas W. McClellan
Jeremy Jason Lang
WEIL, GOTSHAL & MANGES, LLP
doug.mcclellan@weil.com
jason.lang@weil.com

FOR PATENT OWNER:

Robert W. Morris
Philip E. Levy
ECKERT SEAMANS CHERIN & MELLOTT, LLC
rwmorris@eckertseamans.com
plevy@eckertseamans.com