

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

INNOVATIVE MEMORY SYSTEMS, INC.,
Patent Owner.

Case IPR2016-00330
Patent 6,901,498 B2

Before KARL D. EASTHOM, JAMES B. ARPIN, and
KEVIN W. CHERRY, *Administrative Patent Judges*.

CHERRY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a); 37 C.F.R. § 42.73

I. INTRODUCTION

A. *Background*

Micron Technology, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting institution of *inter partes* review of claims 1, 2, 5, 6, 11, 12, 15, 16, 21, 22, 27, 32, 33, 38, 43, 44, 47, and 48 of U.S. Patent No. 6,901,498 B2 (Ex. 1001, “the ’498 patent”). Innovative Memory Systems, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 8, “Prelim. Resp.”). Pursuant to 35 U.S.C. § 314, we instituted this trial (“Decision to Institute”) as to each of the challenged claims of the ’498 patent. Paper 10 (“Dec.”).

After the Decision to Institute, Patent Owner filed a Patent Owner Response (Paper 22, “PO Resp.”) and Petitioner filed a Reply to the Patent Owner Response (Paper 26, “Pet. Reply”). An oral hearing was held March 23, 2017, in this matter. A transcript of the oral hearing has been entered into the record. Paper 39 (“Tr.”).

Petitioner relies on the testimony of Dr. Vivek Subramanian (Ex. 1003 (“Subramanian Declaration”) & Ex. 1014 (“Subramanian Reply Declaration”)) in support of its contentions. Patent Owner relies on the testimony of Dr. Scott M. Nettles (Ex. 2002 (“Nettles Declaration”)) in support of its contentions.

Patent Owner filed a Motion to Exclude certain evidence. Paper 31 (“Mot. Exclude”). Petitioner filed an opposition. Paper 35 (“Opp.”). Patent Owner filed a reply. Paper 36 (“PO Reply”).

Patent Owner also filed a Motion for Observations on Cross Examination of Dr. Subramanian. Paper 32 (“Obs.”). Petitioner filed a response. Paper 34 (“Obs. Resp.”). Pursuant to our authorization by email,

Patent Owner also filed an Unopposed Motion for Observation of Patent Owner's Own Witness. Paper 33 ("Nettles Obs."). We have reviewed and considered Patent Owner's observations and Petitioner's response in arriving at our Final Written Decision in this case.

We have jurisdiction under 35 U.S.C. § 6(b). This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. We determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1, 2, 5, 6, 11, 12, 15, 16, 21, 22, 27, 32, 33, 38, 43, 44, 47, and 48 of the '498 patent are unpatentable.

B. Related Proceedings

According to the parties, the '498 patent is involved in, at least, the following lawsuit: *Innovative Memory Sys., Inc. v. Micron Tech., Inc.*, 14-cv-1480 (D. Del.). Pet. 2.

Petitioner filed a number of other petitions challenging the patentability of certain subsets of claims in the following patents owned by Patent Owner: (1) U.S. Patent No. 6,169,503 B1 (Case IPR2016-00320); (2) U.S. Patent No. 7,045,849 B2 (Case IPR2016-00322); (3) U.S. Patent No. 7,495,953 B2 (Case IPR2016-00323); (4) U.S. Patent No. 7,886,212 B2 (Case IPR2016-00324) (Institution Denied); (5) U.S. Patent No. 7,000,063 B2 (Case IPR2016-00325) (Institution Denied); (6) U.S. Patent No. 6,324,537 B1 (Case IPR2016-00326) (Terminated, Adverse Judgment Requested by Patent Owner); and (6) U.S. Patent No. 7,085,159 B2 (Case IPR2016-00327) (Terminated, Adverse Judgment Requested by Patent Owner). See Pet. 2.

C. The References

Petitioner relies upon the following references:

Tanaka	EP 0 896 280 A2	Feb. 10, 1999	Ex. 1005
Estakhri	US 6,034,897	Mar. 7, 2000	Ex. 1006
Mukaida	US 7,020,739 B2	Mar. 28, 2006	Ex. 1007
Hazen	US 6,088,264	July 11, 2000	Ex. 1008
Garvin	US 6,260,156 B1	July 10, 2001	Ex. 1009

D. The Asserted Grounds of Unpatentability

We instituted this proceeding based on the following grounds of unpatentability:

References	Basis	Challenged Claims
Tanaka and Estakhri	§ 103(a)	1, 2, 11, 12, 21, 27, 32, 38, 43, and 44
Tanaka, Estakhri, and Mukaida	§ 103(a)	5, 6, 15, 16, 47, and 48
Tanaka, Estakhri, and Hazen	§ 103(a)	5, 6, 15, 16, 47, and 48
Tanaka, Estakhri, and Garvin	§ 103(a)	22 and 23

E. The '498 Patent

The '498 patent is entitled “Zone Boundary Adjustment for Defects in Non-Volatile Memories,” and issued May 31, 2005. Ex. 1001, [54], [45]. The '498 patent generally relates to non-volatile semiconductor memories, such as electrically erasable programmable read-only memories (“EEPROM”), their architectures, and their methods of operation. *Id.* at 1:5–10. The '498 patent describes a non-volatile memory device capable of adjusting the boundaries of logical zones within the memory to accommodate defects in the memory. *Id.*, Abstract. According to the '498 patent, such a device improves memory card yields and extends the useable lifetime of the memory card. *Id.*

The '498 patent explains that flash EEPROM devices are composed of one or more arrays of transistor cells, with each cell capable of non-volatile storage of one or more bits of data. *Id.* at 1:18–20. The '498 patent explains that flash memory does not require power to retain the bits of data, but once it is programmed, a cell must be erased before it can be reprogrammed with a new value. *Id.* at 1:21–23. To provide for the efficient implementation of read, program, and erase functions, the arrays of cells in the flash memory are partitioned into groups. *Id.* at 1:23–26. The '498 patent states that a typical flash memory architecture for mass storages arranges large groups of cells into erasable blocks, wherein a block contains the smallest number of cells that are erasable at one time (i.e., the unit of erase). *Id.* at 1:26–30.

Flash memory systems use a controller that performs high-level host and memory control functions. *Id.* at 3:14–15. One of the functions performed by the controller includes the translation between logical addresses received by the memory sub-system from a host and physical addresses within the memory cell array. *Id.* at 1:49–55. The '498 patent describes that a memory often will have defective portions, either from the manufacturing process or that arise during the operation of the device. *Id.* at 5:65–67. One method of dealing with these defects is to test the device before being shipped to find a defective portion of the memory that needs to be eliminated and storing the location of the defective portions, so that the controller can substitute a good portion of the memory for the defective portion. *Id.* at 6:5–13. In such a solution, the controller will need to refer to a pointer structure in the controller for the re-mapping of the memory. *Id.* at 6:13–15. The '498 patent explains that, although memories often are designed with a number of redundant blocks to replace defective blocks, the

blocks generally are not distributed between the logical structure areas of the memory. *Id.* at 6:16–19. The '498 patent states that, if the number of bad blocks is too large or too unevenly distributed, this results in yield losses or downgrades the capacity of the memory card. *Id.* at 6:19–21.

The '498 patent purports to solve these shortcomings. The '498 patent describes that the non-volatile memory is divided into logical zones by the card controller in order to reduce the size of the data structures used for address translation. *Id.* at 6:24–28. The '498 patent provides a method to adjust the zone boundaries to accommodate defects found in testing and to adjust boundaries in the field to extend the usable life of the memory card. *Id.* at 6:28–32.

The '498 patent describes performing this method at two times. First, at the time of card production, an operation is performed that sets zone boundaries. *Id.* at 6:33–34. During this process, the firmware scans for the presence of defective blocks on the memory card. *Id.* at 6:34–36. Once the locations of all the blocks are known, the firmware calculates the zone boundaries in such a way that good blocks are equally distributed among the zones. *Id.* at 6:36–38. Second, the '498 patent explains that the controller can perform dynamic boundary adjustments. *Id.* at 6:41–42. When defects occur, the controller performs the analysis again and, if the number of good blocks becomes unbalanced, redistributes the zone boundaries, moving any user data. *Id.* at 6:42–45.

F. Illustrative Claim

Of the challenged claims, claims 1, 11, 21, 32, and 43 are independent. Claims 2, 5, and 6 depend, directly or indirectly, from claim 1; claims 12, 15, and 16 depend, directly or indirectly, from claim 11;

claims 22 and 27 depend from claim 21; claims 33 and 38 depend from claim 32; and claims 44, 47, and 48 depend, directly or indirectly, from claim 43.

Illustrative claim 1 follows:

1. A memory system circuit, comprising:
a memory comprising a plurality of blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable, and
a controller that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time, wherein the memory is organized into logical zones each comprised of one or more blocks for address translation, and wherein the correspondence of blocks to zones is adjustable by controller.

Ex. 1001, 12:56–68.

II. CLAIM CONSTRUCTION

In an *inter partes* review, the Board gives claim terms in an unexpired patent their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable interpretation standard, and absent any special definition, claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). “Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history.” *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016).

As a first step in our analysis, we determine the meaning of the claims. Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

In the Decision to Institute, we preliminarily adopted the agreed constructions for three terms found in each of the challenged claims. The claim terms and our preliminary constructions are reproduced in the table below:

Claim Term	Claim Construction in the Decision to Institute
Logical zone	“a logical subdivision of the total capacity of the non-volatile memory die” (Dec. 7)
Multi-state storage units	“storage elements that store two or more bits of data per storage element” (<i>Id.</i>)
Plane	“physical subdivision of the memory on a single die” (<i>Id.</i>)

Neither party contests these constructions. See Paper 12, 3 (“**The patent owner is cautioned that any arguments for patentability not raised in the response will be deemed waived.**”). Having considered all of the evidence of record in this trial, we maintain these constructions. In the Decision to Institute, we also construed the claim limitation “wherein the correspondence of blocks to zones is adjustable by controller.” Dec. 7–10. We discuss this term in detail below.

- A. “wherein the correspondence of blocks to zones is adjustable by controller” (Claim 1) and Related Limitations (Claims 11, 21, 32, and 43)

Claim 1 recites the limitation “wherein the correspondence of blocks to zones is adjustable by controller.” Ex. 1001, 12:66–67. Challenged

independent claims 11, 21, 32, and 43 include similar limitations.¹ *See id.* at 13:37–38, 14:11–13, 14:65–68, 16:6–9. In our Decision to Institute, we declined to limit the claims to the situation in which the blocks, whose logical relationship are adjusted, are those already assigned to logical zones. Dec. 10. In its Response, Patent Owner argues that this construction is incorrect. *See* PO Resp. 28–36. Instead, Patent Owner argues that the phrase means “adjusting zone boundaries such that blocks from one logical zone are shifted to another logical zone.” *Id.* at 28. Patent Owner raises similar arguments with respect to the similar claim language in independent claims 11, 21, 32, and 43. *See id.* at 44–45, 46–47, 47. In particular, Patent Owner argues that this claim limitation is not satisfied by a remapping scheme, such as that taught by Tanaka, wherein a redundant block, which Patent Owner contends is not assigned to or associated with any logical zone, is used to replace a defective block within a logical zone. *Id.* at 28. In other words, Patent Owner asserts that the claim language requires that the blocks whose correspondence to the zones is being adjusted must be blocks that already were assigned to a zone before the adjustment.

¹ Claim 11 includes a requirement that the adjustment occurs “dynamically,” and claims 21, 32, and 43 include requirements that the adjustment occurs in response to defects. Those variations in the claim language are dealt with in those respective claims. With respect to claim 43, that claim recites adjustment of the correspondence of physical blocks to logical address sections. Patent Owner contends that the broadest reasonable interpretation of this limitation has the same requirement contended here with respect to claim 1, namely, that the blocks whose correspondence is adjusted must be blocks already assigned to logical address sections. *See* PO Resp. 45. Because Patent Owner’s reasoning is largely the same for claim 1 and for the contested limitation of claim 43, we consider them together, as well.

Patent Owner begins by pointing to the structure of the claims to support this argument. In claim 1, the limitation immediately before this disputed limitation requires that the “memory is organized into logical zones each comprised of one or more blocks.” *Id.* at 28 (emphasis omitted). Patent Owner contends that “it is only those ‘one or more blocks’ whose correspondence to zones can be adjusted by the controller.” *Id.* at 29. Patent Owner argues that the other references to blocks, including the “addressed blocks” and “plurality of blocks,” are not tied to the limitations relating to dividing the memory into logical zones and adjusting the correspondence of blocks to zones. *Id.* at 29–30.

Patent Owner also points to the Specification of the ’498 patent as supporting its understanding of the claims. *Id.* at 30–31. In particular, Patent Owner submits that the Specification of the ’498 patent “describes ‘the present invention’ or ‘principal aspect of the present invention’” as “adjusting zone boundaries, that results in blocks already assigned to one logical zone being shifted into another logical zone.” *Id.* at 30 (citing Ex. 1001, 6:28–32, 6:40–44, 7:48–51, 8:20–34). Patent Owner and its declarant, Dr. Nettles, contend that “zone boundary adjustment is the ‘heart of the invention.’” *Id.* (citing Ex. 2002 ¶ 100). Patent Owner argues that “[n]ot a single embodiment of the invention of the ’498 Patent describes an in-place physical address repair mechanism, such as that disclosed by Tanaka, that moves blocks from outside of any logical zone into a logical zone in order replace defective blocks within that zone.” *Id.* at 30–31.

We are not persuaded that the claims are limited in the manner that Patent Owner proposes. To begin with, we are not persuaded that the claims are as clear as Patent Owner suggests. Claim 1 refers to several different

groups of blocks—the “plurality of blocks” that comprise the memory, the “addressed blocks,” and the “one or more blocks” organized into the logical zones. The disputed claim language does not specify explicitly to which one of these different groups of blocks it is referring. Patent Owner would have us assume that it must be the “one or more blocks” organized into the logical zones, but the lack of antecedent basis referring explicitly back to that group suggests that there are other possible interpretations. PO Resp. 29–30. Given that we must apply the *broadest reasonable interpretation*, this ambiguity counsels against a narrow interpretation.

As for the Specification, Patent Owner does not point us to a definition, but does point us to the Specification’s characterization of certain aspects of the description as “the present invention” and certain criticisms of the prior art found in the Specification. See PO Resp. 29–31. Although the use of the “present invention” can, in certain circumstances, result in a disavowal of claim scope, see, e.g., *Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021, 1024–25 (Fed. Cir. 2015), we are not persuaded that the statements identified disclaim all other methods of replacing blocks other than adjusting zone boundaries. Importantly, the identified passages of the Specification discuss adjusting zone boundaries, but the claims do not use the term “boundaries.” See Ex. 1001, 12:66–67 (claim 1), 13:37–38 (claim 11), 14:11–13 (claim 21), 14:65–67 (claim 32), 16:7–9. Instead, the claims are cast in the broader concept of adjusting the “correspondence of blocks to zones.” The plain and ordinary meaning of the term “correspondence” is “connection” or “relation.” See Ex. 3001; Ex. 3002. This meaning is broad enough to encompass both the situation where blocks are assigned to zones and the situation where the blocks are not yet assigned

to a zone. *See* Pet. Reply 3 (“Patent Owner’s argument also misses the point because ‘the correspondence’ of the blocks found in the zones is adjusted any time that a block within a zone is replaced by a new block outside the zone, regardless of whether the new block originated from a zone.”).

Moreover, Patent Owner’s efforts to cast its construction as the “heart of the invention” is not a basis for limiting the claims. *See Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1322 (Fed. Cir. 2007) (“This court . . . has rejected a claim construction process based on the ‘essence’ of an invention.”); *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1345 (Fed. Cir. 2002) (“It is well settled that there is no legally recognizable or protected essential element, gist or heart of the invention in a combination patent.” (internal quotation marks omitted)).

Contrary to Patent Owner position, the intrinsic evidence of the Specification suggests that the patentee knew how to restrict its claim coverage to only the situation of adjusting zone boundaries. The patentee could have used the word “boundaries,” but instead chose a different term that implies a broader scope. *See Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 807 (Fed. Cir. 2007) (noting patentee’s choice to use broader term suggests broader scope). Moreover, the criticism of alternative approaches in the Specification is limited to the situation, in which each logical zone only has a fixed number of pre-assigned spare or redundant blocks. *See* Ex. 1001, 8:4–12 (“the spare blocks are typically distributed uniformly across the sub-units . . . the defective blocks may be clustered in a given sub-unit . . . [so] the number of spare blocks may be spread too thin in one zone while another zone maintains its original excess number of spare blocks”). There does not appear to be any criticism of approaches of providing spare

blocks in a different logical division of the memory. Thus, we decline to limit the claims to the situation, in which the blocks, whose logical relationships are adjusted, are those already assigned to logical zones or that involve the adjustment of boundaries between zones.

III. ANALYSIS

A. *Obviousness of Claims 1, 2, 11, 12, 21, 27, 32, 38, 43, and 44 over Tanaka and Estakhri*

Petitioner asserts that a combination of the teachings of Tanaka and Estakhri renders obvious claims 1, 2, 11, 12, 21, 27, 32, 38, 43, and 44. *See* Pet. 21–49. The Petition includes discussion identifying where Tanaka and Estakhri allegedly teach or suggest the limitations of each challenged claim. *Id.*

1. *Tanaka (Ex. 1005)*

Tanaka is entitled “Method for Controlling Nonvolatile Semiconductor Memory System,” and generally relates to methods for controlling a non-volatile semiconductor memory system, such as a non-volatile semiconductor memory card. Ex. 1005, [54], ¶ 1. As part of its control methods, Tanaka discloses a procedure for ensuring sufficient storage in each logical division of the memory. *Id.* ¶ 176. In order to ensure this, “the flash memory must have a writable and erasable effective block as a block replaced when the defective block is produced.” *Id.* In Tanaka, the memory “is provided with a plurality of redundant blocks,” and the defective blocks are replaced with the redundant blocks “by means of a redundant circuit as a hardware when the flash memory is shipped.” *Id.* ¶ 177. Tanaka explains that, “[w]hen the redundant circuit is used, the redundant blocks are allocated to addresses of defective blocks.” *Id.* Tanaka also explains that

the replacement can be performed sequentially, with the defective blocks with smaller addresses being replaced first, or the blocks can be replaced with redundant blocks, so that all the zone have the required number of effective blocks. *Id.* ¶¶ 178, 181–183. Figure 48 of Tanaka is reproduced below.

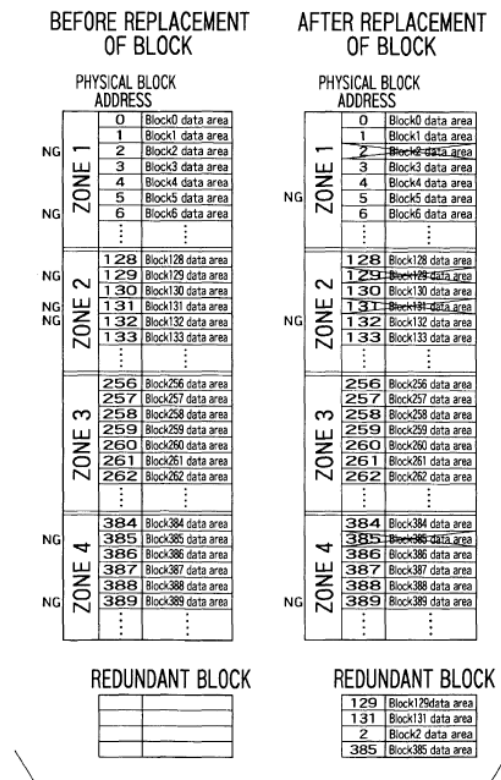


FIG. 48

Figure 48 depicts “the state of a physical block when defective blocks existing in each zone are replaced with redundant blocks so that the number of defective blocks [does not] exceed[] the number permitted in each zone. *Id.* ¶ 184. Tanaka explains that, given the distribution of defective blocks in the zones, using the conventional method of simply replacing memory blocks sequentially, from the lowest address to the highest, would result in a product that could not be shipped. *Id.* In order to reduce losses, Tanaka

discloses an algorithm that replaces blocks, such that the number of defective blocks does not exceed the number of defective blocks permitted in each zone. *Id.*

2. *Estakhri (Ex. 1006)*

Estakhri is entitled “Space Management for Managing High Capacity Nonvolatile Memory.” Ex. 1006, [54]. Estakhri generally relates to the use of flash memory as mass storage and discloses a controller device for use in a digital system having a host and a nonvolatile memory device. *Id.* at 1:7–9, 3:17–22. The controller device includes a space manager circuit responsive to address information from the host and operative to read, write, or erase information in a nonvolatile memory unit based upon the host address information. *Id.*, Abstract. The information stored in the nonvolatile memory is organized in blocks, and each block is uniquely addressable by the controller. *Id.* at 2:20–23. The controller device erases the digital information stored in the blocks of the nonvolatile memory devices in-parallel form. *Id.* at 3:25–27. Estakhri explains that the space manager assigns a predetermined number of blocks, in sequential order, to each of the nonvolatile memory devices; forms “super” blocks, each “super” block having blocks arranged in parallel; and identifies a particular “super” block having at least two blocks, a first block being located in a first nonvolatile memory device and a second block being located in a second nonvolatile memory device, for erasure of the particular “super” block. *Id.* at 3:31–40.

3. *Level of Ordinary Skill in the Art*

Dr. Subramanian testifies about the level of ordinary skill in the art as follows:

In my opinion, a person of ordinary skill in the art at the time of the claimed inventions would have had a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least 2–3 years of experience in the development and use of NAND flash memory controllers and interfaces. An individual with an advanced degree in a relevant field, such as computer or electrical engineering with appropriate experience, would require less experience in the development and use of flash memory controllers and interfaces.

Ex. 1003 ¶ 17. Patent Owner does not contest Petitioner's assessment of the level of ordinary skill in the art as of the date of the invention. Accordingly, for the purposes of this Decision, we adopt Dr. Subramanian's proposed assessment of the level of ordinary skill in the art.

4. *Analysis*

a. Claims 1, 11, and 43

With respect to the preamble of independent claims 1, 11, and 43 (“[a] memory system circuit, comprising”), we find that Tanaka discloses a memory system circuit. Ex. 1005, Abstract, Figs. 24, 49, ¶¶ 67, 190, 197; Ex. 1003, A1–A4. We further find that Tanaka discloses of “non-volatile semiconductor memory system” using “NAND flash” with blocks of flash cells that are simultaneously erasable as disclosing “a memory comprising a plurality of blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable,” as recited in claims 1, 11, and 43. Ex. 1005 ¶¶ 4, 8, 17, 206, Fig. 44; Ex. 1003, A4–A5. Patent Owner does not dispute that Tanaka accounts for these limitations.

Claims 1, 11, and 43 also recite “a controller that controls programming of data into addressed blocks, reading data from addressed

blocks and erasing data from one or more of addressed blocks at a time.”

Ex. 1001, 12:61–64, 13:32–35, 16:1–4. Petitioner contends that the combination of the teachings of Tanaka and Estakhri accounts for this limitation. Pet. 23–25, 32, 46. In particular, Petitioner contends that Tanaka discloses a flash memory controller (“controller 103” on “PC card adapter 102”) that controls the flash memory, including programming (i.e., writing), reading, and erasing data from addressed blocks. *Id.* at 23 (citing Ex. 1005 ¶¶ 17, 55, 76, 82, 126, 136, 190, 196, 197, Figs. 22, 35, 36).

Petitioner further argues that Tanaka discloses that the blocks are “addressed blocks” because they are addressed via logical block addresses, physical block addresses, and translation table to translating from one to another. *Id.* at 23–24. Petitioner further submits that, to the extent that Tanaka does not expressly disclose that the controller can perform these functions, it would have been obvious in view of Estakhri. *Id.* at 24. In particular, Petitioner contends that Estakhri discloses a single non-volatile memory “controller device” (“controller 14”) that controls not only programming, reading, and erasing of blocks, but also the addressing of blocks and formation of zones and logical address translation. *Id.* at 24–25 (citing Ex. 1006, Abstract, 2:20–22, 1:64–66, 2:38–50, 3:25–27, 3:45–56, 5:34–36, 9:65–66, 14:39–45, Fig. 1).

Petitioner argues that it would have been obvious to combine the teaching of the block management scheme of Tanaka with the teachings of the controller of Estakhri for several reasons. *Id.* at 16–18. First, Petitioner submits it would have been obvious to combine these teachings because the references are in the same field and address the common issues of controlling flash memory devices, managing defects, and creating logical

groups of blocks. *Id.* at 16. Second, Petitioner argues that Estakhri, by disclosing that its controller is “for use in a digital system having a host and nonvolatile memory,” which is the type of system Tanaka discloses, provides a reason to combine the teachings of these references. *Id.* at 17. Third, Petitioner submits that using the controller taught by Estakhri in systems taught by Tanaka would be a simple substitution that would have been understood to yield predictable results. *Id.* Fourth, Petitioner argues that applying Estakhri’s teachings to Tanaka would have involved the use of a known technique to improve a similar device in a similar way. *Id.* 17–18 (citing Ex. 1003 ¶ 81). Finally, Petitioner asserts that using the controller and planes taught by Estakhri in the systems taught by Tanaka would have been obvious to try as a well-known design choice. *Id.* at 18 (citing Ex. 1003 ¶ 82).

Patent Owner does not dispute that the combined teachings account for this limitation, but rather, as discussed below, Patent Owner argues that the combination does not account for a controller that has both this functionality and the additional functionality of “wherein the correspondence of blocks to zones is dynamically adjustable by controller.” *See* PO Resp. 36–44.

We agree with Petitioner that the combined teachings of Tanaka and Estakhri account for this limitation. We find that Tanaka discloses a flash memory controller (“controller 103”) that controls the flash memory, including programming (i.e., writing), reading, and erasing data from addressed blocks. Ex. 1005 ¶¶ 17, 55, 76, 82, 126, 136, 190, 196, 197, Figs. 22, 35, 36. We further find that Estakhri discloses a single non-volatile memory “controller device” that controls not only programming, reading,

and erasing of blocks, but also the addressing of blocks and formation of zones and logical address translation. Ex. 1006, Abstract, 2:20–22, 1:64–66, 2:38–50, 3:25–27, 3:45–56, 5:34–36, 9:65–66, 14:39–45, Fig. 1. We also find that it would have been obvious to combine the functionality taught in Tanaka with that of Estakhri’s controller device, such that a single controller would control “programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time,” as recited in claims 1, 11, and 43. Moreover, we agree with Dr. Subramanian that a person of ordinary skill would have had reason to combine the teachings of Tanaka and Estakhri based at least on the suggestion in Estakhri that its controller was meant to be used in a digital system having a host and a nonvolatile memory such as Tanaka. Ex. 1003 ¶ 79. As Dr. Subramanian explains, both references are directed to the controller’s management of defects, and one of ordinary skill would have been motivated to consider the teachings of Estakhri to further improve the management of defects using other known solutions. *Id.* (citing Ex. 1005 ¶ 52; Ex. 1006, 2:38–45; Ex. 1010, 112–113; Ex. 1011, 134–138); see *In re Ethicon*, 844 F.3d 1344, 1351 (Fed. Cir. 2017) (“The normal desire of artisans to improve upon what is already generally known can provide the motivation to optimize variables . . . for use in a known device.”). We further agree with Dr. Subramanian that such a combination would merely be the use of a known technique to improve a similar device. *Id.* ¶ 81. As Dr. Subramanian explains, the use of a flash controller to divide a memory into planes to allow parallel operations was known in the art, and applying these known techniques from Estakhri would improve systems taught by Tanaka in the same way, namely by facilitating parallel operations and

augmenting the logic to physical address translation. *Id.* Thus, we conclude that the combined teachings of Tanaka and Estakhri would account for this limitation of claims 1, 11, and 43.

Petitioner also relies on Tanaka as disclosing “wherein the memory is organized into logical zones comprised of one or more blocks for address translation,” as recited in independent claim 1, and the similar limitation recited in claims 11. *See* Pet. 25–27, 33. We find that Tanaka discloses that blocks can be organized into logical zones, which Tanaka refers to as “logical zones,” “zones,” “logical areas,” and “physical block areas.” Ex. 1005 ¶¶ 158, 160, 187. We further find that Tanaka discloses using the zones for address translation, i.e., generating tables on a zone-by-zone basis thereby enabling smaller translation tables because the RAM need only load the table for a specific zone. Ex. 1005 ¶¶ 162–165, 187, 204, Figs. 44–46, 48; Ex. 1003 ¶¶ 59, 60, A-12–A-17. We find, as Dr. Subramanian testifies, that by disclosing logical zones comprised of multiple blocks in a logical grouping for purposes of address translation, Tanaka accounts for this limitation. Ex. 1003, A-17.

Claim 43 has a similar limitation and recites “wherein the non-volatile is organized into logical address sections as seen by the controller.” Ex. 1001, 16:4–5. Petitioner submits that the combined teachings of Tanaka and Estakhri account for this limitation. Petitioner submits that Tanaka’s zones are “logical address sections.” Pet. 46–47 (citing Ex. 1005 ¶¶ 44, 45, 160, 204, Figs. 34, 44, 45). Petitioner further submits that the controller taught by Tanaka and Estakhri accounts for a nonvolatile memory organized into logical address sections as seen by the same controller that also controls the programming, reading, and erasing of data in addressed blocks. *Id.*

We agree with Petitioner that the combined teachings of Tanaka and Estakhri account for the limitation of claim 43 of “wherein the non-volatile is organized into logical address sections as seen by the controller.” As we have found above, the combined teachings of Tanaka and Estakhri account for a controller that can control programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time. We further agree with Petitioner that Tanaka teaches dividing the memory into “zones,” which, as Dr. Subramanian testifies, are “logical address sections.” Ex. 1003, A-67–A-69; Ex. 1005 ¶¶ 44, 45, 160, 204, Figs. 34, 44, 45. These zones would be “seen” by controller in the combination of Tanaka and Estakhri. Ex. 1003, A-69.

Finally, independent claims 1, 11, and 43 have requirements regarding the adjustment of the correspondence of blocks to zones (or logical address sections) by the controller. With respect to claim 1, Petitioner relies on the combined teachings of Tanaka and Estakhri for disclosing the limitation of claim 1 requiring that the “correspondence of blocks to zones is adjustable by controller.” Pet. 27. Petitioner submits that Tanaka discloses adjusting the correspondence of blocks to zones by replacing defective blocks in the zones. *Id.* Petitioner argues that Tanaka discloses “monitoring for defects and using the specific algorithm in paragraph 184 to reassign blocks to zones.” *Id.* Specifically, Petitioner asserts that Tanaka discloses a “zone division control” management scheme in which the flash memory controller monitors the number of defective blocks within each zone and replaces defective blocks to keep the number of defective blocks in each zone below a predetermined number (e.g., a maximum of 1 defective block per zone). *Id.* (citing Ex. 1005 ¶¶ 52, 55, 177, 178, 180–185, 187, 208, Figs. 46–48).

Petitioner further contends that the controller taught by Tanaka “would have been understood to control this adjustment.” *Id.* at 29 (citing Ex. 1003 ¶ 57). However, Petitioner argues that, to the extent that we find that Tanaka does not expressly disclose that the controller is performing the remapping, it would have been obvious from the combined teachings of Tanaka and Estakhri that the same “controller device 14” in Estakhri that controls the programming, reading, and erasing of data could also perform the zone adjustments. *Id.* at 29. Petitioner asserts that Estakhri discloses a single nonvolatile memory “controller device” that controls each of the following functions: (a) the programming (i.e., writing), reading, and erasing of data from the addressed blocks, (b) the formation and management of zones (e.g., “super blocks”), (c) logical block address translations, and (d) identifying and tracking defective blocks. *Id.* at 29–30. Petitioner further argues that it would be obvious to combine functionality taught by Tanaka with controller taught by Estakhri, as discussed above with respect to the controller limitation.

Patent Owner raises several arguments alleging why the combined teachings of Tanaka and Estakhri does not render claim 1 obvious. PO Resp. 22–44. First, Patent Owner argues, based on its claim construction discussed above, that the claims exclude the remapping scheme that is taught by Tanaka, wherein a redundant block, that is not assigned or associated with any logical zone, is used to replace a defective block within a logical zone. *See id.* at 28–36. However, as discussed above, we have determined that the claims do not exclude such a remapping scheme. *See supra*, at 8–12. Instead, based on our construction, we find that Tanaka, by assigning redundant blocks in place of defective blocks, “adjusts” the correspondence

of blocks to zones within the meaning of the claims. Ex. 1005 ¶¶ 52, 55, 177, 178, 180–185, 187, 208, Figs. 46–48; Ex. 1003 ¶ 57, A-17–A-26.

Moreover, even if we adopted Patent Owner’s construction, we agree with Petitioner that the combined teachings of Tanaka and Estakhri would still teach this limitation. *See* Pet. Reply 15–17. Under the construction of “zone” we have adopted, we agree with Petitioner that the redundant block area is itself a zone—even though it is not given the name “zone” in Tanaka. *Id.* As Dr. Subramanian testified, the redundant blocks are part of the overall memory system. Ex. 1014 ¶ 25; Ex. 2006, 58:8–59:13. As Dr. Subramanian explains, the control algorithm of Tanaka (*see* Ex. 1005 ¶ 184) that replaces defective blocks with redundant blocks must know where the redundant blocks are located. *Id.* We find this testimony to well-supported and persuasive. In contrast, Patent Owner’s expert relies on an overly narrow definition of “zone” to rebut Dr. Subramanian’s contention. *See* Ex. 2002 ¶ 105. In Dr. Nettles’s declaration, he adds the additional requirement that to be part of a logical zone a block must (1) have a logical address assigned to it and (2) be part of the logical address map. *See id.* Neither Patent Owner nor Dr. Nettles, however, offers adequate support for why these requirements are necessary. Our claim construction, which Patent Owner does not contest, only requires that a “logical zone” is “a logical subdivision of the total capacity of the non-volatile memory die.” There is no requirement that the blocks have a logical address assigned or be part of a logical address map. Without any explanation or support for these additional limitations, we decline to give Dr. Nettles’s testimony substantial weight. Thus, by shifting the blocks from the redundant block, which is itself a logical zone, as we have construed the term, to one of Tanaka’s

zones, we agree with Petitioner and Dr. Subramanian that Patent Owner's claim construction would be satisfied. *Id.* ¶ 23.

Second, Patent Owner argues that Tanaka and Estakhri do not, alone or in combination, teach or suggest a memory controller having a single controller that is able to perform both adjusting correspondence of blocks to zones, *and* programming, reading, and erasing of data. PO Resp. 36–44. With respect to Tanaka, Patent Owner argues that the controller of Tanaka is not part of the flash memory card and that the controller does not perform the remapping of Tanaka where in the redundant blocks are used to replace defective blocks. *Id.* at 37–44. Rather, Patent Owner asserts that the remapping scheme of Tanaka is performed by means of a “redundant circuit” only at the time of manufacture (i.e., prior to shipment), so it cannot be part of Tanaka's controller. *Id.*

We find that Petitioner has shown sufficiently that the combination of Tanaka and Estakhri teaches a controller that performs both functions. We begin by addressing Patent Owner's characterization of our Decision to Institute. *See* Tr. 39:15–41:9. As we explained, in our Decision to Institute, Petitioner proposed two alternatives for why the combined teachings of Tanaka and Estakhri accounted for the requirement that the controller perform all of the various functions recited in the independent claims:

[a]s for the remaining requirement of claims 1 and 11 that the controller both performs the logical assignment of the blocks to the logical zones and performs the reading, writing, and erasing, Petitioner further contends that the controller in Tanaka “would have been understood to control this adjustment.” [Pet.] 29 (citing Ex. 1003 ¶ 57). However, Petitioner argues that to the extent that we find that Tanaka does not expressly disclose that the controller is performing the remapping, it would have been obvious to combine the functionality in view of Estakhri. *Id.* at

29. In particular, Petitioner contends that Estakhri discloses a single nonvolatile memory “controller device” that controls not only programming, reading, and erasing of blocks, but also the addressing of blocks and formation of zones and logical address translation. *Id.* at 29–30 (citing Ex. 1006, Abstract, 2:20–22, 1:64–66, 2:38–50, 5:34–36, Fig. 1).

Dec. 15.

Our description is clear that Petitioner offered two alternative theories for why the combined teachings of Tanaka and Estakhri taught or suggested this limitation—if we concluded that Tanaka did not disclose expressly the functionality as part of the controller, then the combined teachings would teach or suggest this feature. *Id.* In its Response, Patent Owner emphasizes that we found that Estakhri does not teach adjusting the correspondence of blocks to zones (PO Resp. 37), but Petitioner has never contended that Estakhri had that functionality (*see* Pet. 27–32). As we explained in our Decision to Institute, “the combination relies on Tanaka, not Estakhri, for that functionality.” Dec. 17. Although we acknowledged that “Petitioner’s Declarant concedes that Tanaka does not disclose expressly where the redundant circuit and its functionality are located” (*id.* (citing Ex. 1003, A-24)), we concluded that “[n]evertheless, Petitioner has offered testimony from its Declarant that this functionality is found in the controller” (*id.* at 18 (citing Ex. 1003, A-24)). We noted that “Patent Owner has not offered any evidence at this preliminary stage to rebut this testimony.” *Id.* From this posture of the case, we determined that “[g]iven [Dr. Subramanian’s] testimony and our construction of the ‘correspondence of blocks to zones’ limitation, we agree, on this record, that Petitioner has shown sufficiently that the combination of the functionality of Tanaka’s controller with Estakhri’s controller accounts for this limitation.” *Id.* Thus, our Decision to

Institute makes clear, our Decision only addressed the first of Petitioner's two alternative theories. The reason we only addressed this first theory is because we concluded that Petitioner had established sufficiently for institution purposes the evidentiary basis for the first theory—that Tanaka's redundant circuit was located in the controller. Given this determination, there was sufficient reason to institute trial, and there was no need to address Petitioner's alternative theory. As we repeatedly emphasized in our Decision to Institute, our determination to institute trial was only preliminary and not our final determination. *See, e.g.*, Dec. 18. Thus, we do not agree that our Decision to Institute, in any way, foreclosed Petitioner from relying on its obviousness theory for how the combination accounted for this limitation.

In addition, we note that, besides a footnote in its motion to exclude, Patent Owner never sought further clarification from us whether Patent Owner's interpretation that we had limited Petitioner's obviousness arguments was correct. In its Reply, Petitioner again raised the argument that, regardless of where the redundant circuit of Tanaka was located, it would have been obvious to a person of ordinary skill in the art to include this functionality in the controller taught by the combination of Tanaka and Estakhri. *See* Pet. Reply 12–15. Patent Owner never sought a sur-reply or moved to strike. As the U.S. Court of Appeals for the Federal Circuit recently noted, when the arguments are in the Petition, the Board may properly rely on them. *See EMC Corp. v. Clouding Corp.*, 2017 WL 1541226, at * (Fed. Cir. May 1, 2017) (unpublished) (“Because EMC had already made these arguments in its Petition and Clouding did not dispute them, we disagree with the Board that EMC was required to explicitly argue

in its Reply to the Board that it was relying on Allen to teach or suggest [the disputed limitation]. Even so, EMC *did* provide support in its Reply for its reliance on Allen, in combination with Barnett, as teaching or suggesting this limitation.”). Thus, we disagree with Patent Owner that one of Petitioner’s obviousness theories is no longer present in this case, and we now consider Patent Owner’s arguments on the merits as to whether the combination accounts for this limitation.

In its Response, Patent Owner argues that Tanaka fails to teach or suggest, or at the very least it is ambiguous, that its redundant circuit that performs its remapping algorithm is located in Tanaka’s controller. PO Resp. 37–44. Petitioner responds with its own analysis of why Tanaka does teach or suggest its redundant circuit is included in the controller. Pet. Reply 7–12. However, we do not need to resolve where precisely Tanaka’s redundant circuit is disclosed, because we agree with Petitioner that it would have been obvious to include the functionality of the redundant circuit in the controller taught by the combination of Tanaka and Estakhri. *See* Pet. 29–31; Pet. Reply 12–15.

We agree with Petitioner and Dr. Subramanian that combining the teachings of Tanaka’s functionality with that of the controller of Estakhri would have been consistent with purpose of Tanaka, which was providing the “function of selectively replacing a defective physical block[] including defective cells with redundant physical blocks.” Ex. 1005 ¶¶ 33, 52; Ex. 1003, A-24. As Dr. Subramanian testifies, in the combination, the same nonvolatile memory “controller device 14” in Estakhri that controls the programming (i.e., writing), reading and erasing of data from the addressed blocks would also have been used to perform the control functions described

in Tanaka related to assigning and adjusting the correspondence of blocks to zones. Ex. 1003, A-24. As Dr. Subramanian explains and we agree, Estakhri already discloses that its controller is a single nonvolatile memory “controller device” that controls each of the following functions: (a) the programming (i.e., writing), reading, and erasing of data from the addressed blocks, (b) the formation and management of zones (e.g., “super blocks”), (c) logical block address translations, and (d) identifying and tracking defective blocks. *Id.* at A-24–A26 (citing Ex. 1006, Abstract, 2:20–22, 1:64–66, 2:38–50, 5:34–36). Furthermore, as we discussed above, a person of ordinary skill would have been motivated to combine the teachings of Tanaka and Estakhri. *See supra*, at 17–19; Ex. 1003 ¶¶ 77–82. In particular, we agree with Dr. Subramanian that give the existing functionality of Estakhri that the incorporation of Tanaka’s redundant circuit functionality would merely be the use of known techniques to improve a similar device in the same way. Ex. 1003 ¶ 81; *see also Unwired Planet, LLC v. Google, Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (“For the technique’s use to be obvious, the skill artisan need only be able to recognize, based on her background knowledge, its potential to improve the device and be able to apply the technique.”).

Patent Owner provides no other arguments as to why the combined teachings of Tanaka and Estakhri, as described in the Petition, would not meet this limitation. Moreover, Patent Owner provides no argument or evidence that the combined teachings of Tanaka and Estakhri would not have been obvious at the time of the invention. Instead, Patent Owner’s arguments are merely directed at Tanaka alone. However, “[t]he test for obviousness is what the combined teachings of the references would have

suggested to those having ordinary skill in the art.” *In re Mouttet*, 686 F.3d 1322, 1333 (Fed. Cir. 2012). “[O]ne cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references.” *In re Keller*, 642 F.2d 413, 426 (CCPA 1981). Accordingly, we find that Petitioner has shown that the combined teachings of Tanaka and Estakhri account for this element.

Thus, we determine that Petitioner has shown by preponderance of the evidence that claim 1 of the ’498 patent is unpatentable as obvious over Tanaka and Estakhri.

Claim 11 has an additional limitation requiring that the adjustment of the correspondence of blocks to zones by the controller occur “dynamically.” Petitioner relies on Tanaka’s disclosure of “dynamically” adjusting the correspondence of blocks to zones “by replacing ‘acquired defective block[s]’ (*i.e.*, blocks that become defective due to use of the flash memory) with spare blocks (also called ‘effective blocks’).” *Id.* at 33 (citing Ex. 1005 ¶¶ 176, 177, 184). Petitioner argues that Tanaka discloses “detecting and monitoring the number of defective blocks in each zone and replacing the defective blocks with ‘redundant blocks’ anytime that the number of defective blocks per zone becomes too high to ensure that all the zones ‘meet the number of effective blocks.’” *Id.* at 33–34 (citing Ex. 1005 ¶¶ 177, 183, 184, 187, 208). Petitioner contends that “by disclosing replacing redundant blocks after they develop defects in the normal course of use (‘acquired defective blocks’) and by disclosing monitoring the number of defective blocks and maintaining an adequate number of non-defective blocks by ongoing replacements,” Tanaka accounts for this “dynamically” limitation. *Id.* at 34.

With respect to claim 11, in addition to the arguments considered above with respect to claim 1, Patent Owner argues that Petitioner has failed to show that Tanaka discloses its remapping scheme is performed “dynamically,” i.e., during operation in the field, as recited in claim 11. PO Resp. 45. With respect to this limitation, Patent Owner only argues that “Tanaka only discloses the controller that is part of the conventional PC card adapter” and “[i]f the functionality of Tanaka’s redundant circuit cannot be show[n] to reside in that controller, it necessarily follows that Tanaka fails to meet this claim limitation.” *Id.* At the oral hearing, however, Patent Owner conceded that, if the functionality of the redundant circuit were located on the controller, it would meet this limitation. Tr. 38:15–39:6, 42:12–17. We have found above that including the redundant circuit, regardless of where it is located in Tanaka, in the controller of the combined teachings of Tanaka and Estakhri would have been obvious to a person of ordinary skill in the art. Thus, because the redundant circuit and its functionality are included in the controller taught by Tanaka and Estakhri, we find that the combined teachings of Tanaka and Estakhri would account for additional requirement of claim 11 that the allocation be performed “dynamically.” Moreover, as discussed above, we find that Petitioner has shown that it would have been obvious to combine the teachings Tanaka and Estakhri in the manner suggested by Petitioner. *See supra*, at 19–20, 24–29. Thus, we determine that Petitioner has shown by a preponderance of the evidence that claim 11 would have been obvious over the combination of Tanaka and Estakhri.

The final limitation of claim 43 recites “wherein the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory.” As discussed above, we

find that Tanaka's zones satisfy the "logical address sections" of claim 43. *See supra*, at 20–21. We further find that the combined teachings of Tanaka and Estakhri account for this limitation. Ex. 1005 ¶¶ 7, 96, 148, 149, 176, 177, 180–185, 187, 208, Figs. 33, 43; Ex. 1003, A-63, A-64, A-69–A-71. As discussed above, we have found that Petitioner has shown that a person of ordinary skill would have been motivated to combine the teachings of Tanaka and Estakhri in the manner suggested by Petitioner. *See supra*, at 26–28. Patent Owner's arguments regarding claim 43 are substantially similar to those addressed with respect to claims 1 and 11 above. *See* PO Resp. 45–47. Our reasoning regarding why Tanaka satisfies the limitations of claims 1 and 11 also applies here to claim 43, even though claim 43 recites "logical address sections," instead of "zones"; because, as discussed above, Tanaka's zones and redundant block are logical address sections within the meaning of claim 43.

Accordingly, Petitioner has shown by a preponderance of the evidence that independent claims 1, 11, and 43 are unpatentable as obvious over Tanaka and Estakhri.

b. Claims 21 and 32

Claims 21 and 32 are method claims. The preambles of claims 21 and 32 are the same and contain nearly identical limitations to a number of the limitations of claim 1. The claims' preambles recite the following:

A method of operating a non-volatile memory system comprising a plurality of blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable, and a memory controller circuit that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time wherein the nonvolatile storage

elements are organized by the controller into logical zones each comprised of one or more blocks for address translation, the method comprising:

As we found above with respect to claim 1, the combined teachings of Tanaka and Estakhri account for these limitations. *See supra*, at 16–29; *see also* Ex. 1003, A-37–A-39, A-60 (Dr. Subramanian’s testimony on this limitation). Claim 21 next recites “identifying one or more of said blocks as defective.” We find that Tanaka accounts for this limitation. Ex. 1005 ¶¶ 7, 96, 148, 149, 180–185, 187, 208, Figs. 33, 43; Ex. 1003, A-39–A-43. Finally, claim 21 recites “assigning a first correspondence of blocks to zones by the controller based on distribution of the identified defective blocks.” We find that the combined teachings of Tanaka and Estakhri account for this limitation. Ex. 1003, A-44–A-51; Ex. 1005 ¶¶ 52, 55, 177, 178, 180–185, 187, 197. Claim 32, on the other hand, recites “assigning an initial correspondence of blocks to zones.” We also find that Tanaka accounts for this limitation. *See* Ex. 1005 ¶¶ 177, 178, 180, 181; Ex. 1003, A-62–A-63. Claim 32, as with claim 21, next recites “subsequently identifying one or more of said blocks as defective.” We find that Tanaka accounts for this limitation. Ex. 1005 ¶¶ 7, 96, 148, 149, 180–185, 187, 208, Figs. 33, 43; Ex. 1003, A-63. Finally, claim 32 recites “assigning a first correspondence of blocks to zones by the controller based on distribution of the identified defective blocks.” We find that the combined teachings of Tanaka and Estakhri account for this limitation. Ex. 1005 ¶¶ 176, 177; Ex. 1003, A-63–A-64.

As discussed above, we have found that Petitioner has shown that a person of ordinary skill would have had reason to combine the teachings of Tanaka and Estakhri in the manner suggested by Petitioner. *See supra* at

26–28. Patent Owner does not raise any separate arguments for claims 21 and 32 besides those addressed with respect to claims 1, 11, and 43 above. *See* PO Resp. 47. Upon consideration of the arguments and evidence presented by the parties, we are persuaded that Petitioner has shown by a preponderance of the evidence that the combined teachings of Tanaka and Estakhri would have rendered obvious claims 21 and 32.

c. Dependent Claims 2, 12, 27, 38, and 44

Claim 2 depends from claim 1, claim 12 depends from claim 11, and claim 44 depends from claim 43, and each additionally recites “wherein said storage elements are multi-state storage units.” Ex. 1001, 13:1–2, 13:39–40, 16:10–11. We find that Petitioner has shown sufficiently that Tanaka accounts for this limitation. Ex. 1005 ¶¶ 30, 36, 189, 190, Fig. 18; Ex. 1003, A-27–A-29. As discussed above, we have found that Petitioner has shown sufficiently that the combined teachings of Tanaka and Estakhri account for the remaining limitations of claims 1, 11, and 43, and Petitioner has shown that a person of ordinary skill would have had reason to combine the teachings of Tanaka and Estakhri in the manner suggested by Petitioner. Patent Owner does not raise any separate arguments, aside from those considered above with respect to the independent claims. Thus, we find that Petitioner has shown by a preponderance of the evidence that Tanaka and Estakhri would have rendered obvious claims 2, 12, and 44.

Claim 27 depends from claim 21 and claim 38 depends from claim 32, and both additionally recite “wherein said assigning a first correspondence comprises distributing blocks to zones based on minimizing the variation in the number of non-defective blocks in said zones.” Ex. 1001, 14:28–31, 15:15–18. We find that Petitioner has shown sufficiently that Tanaka

accounts for this limitation. Ex. 1005 ¶¶ 52, 158, 171, 173, 180–185; Ex. 1003, A-52–A-59. In particular, we find Dr. Subramanian’s testimony to be detailed, well-supported, and entitled to substantial weight. Ex. 1003, A-52–A-59. As discussed above, we have found that Petitioner has shown sufficiently that Tanaka and Estakhri account for the remaining limitations of claims 21 and 38, and Petitioner has shown that a person of ordinary skill would have been motivated to combine Tanaka and Estakhri in the manner suggested by Petitioner. Patent Owner does not raise any separate arguments, aside from those considered above with respect to the independent claims. Upon consideration of the arguments and evidence presented by the parties, we are persuaded that Petitioner has shown by a preponderance of the evidence that the combined teachings of Tanaka and Estakhri would have rendered obvious claims 27 and 38.

B. Obviousness of Claims 5, 6, 15, 16, 47, and 48 Over Tanaka, Estakhri, and Mukaida

Petitioner contends that claims 5, 6, 15, 16, 47, and 48 are unpatentable under 35 U.S.C. § 103(a) as obvious over Tanaka, Estakhri, and Mukaida. Pet. 49–53. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Subramanian Declaration (Ex. 1003) to support its positions.

1. *Mukaida (Ex. 1007)*

Mukaida is entitled “Memory Controller, Flash Memory System Having Memory Controller and Method for Controlling Flash Memory Device.” Ex. 1007, [54]. Mukaida is directed generally at a memory controller that can perform a series of data write operations so as to complete the data writing at a high speed. *Id.*, Abstract. In particular, Mukaida classifies a plurality of physical blocks in the memory into groups using virtual addressing. *Id.* at 6:11–20. Mukaida further teaches virtually combining the groups of physical blocks, so that these physical blocks are treated as a single virtual block. *Id.* at 6:21–25. In one embodiment, Mukaida teaches that the groups are divided according to memory chips. *Id.* at 6:30–31. By combining the groups into a single virtual block, a plurality of host addresses associated with the same physical block can be assigned to different physical blocks from one another. *Id.* at 6:25–28. Therefore, according to Mukaida, sets of operations can be performed at high speed. *Id.* at 6:28–29.

2. *Analysis*

Claims 5, 15, and 47 depend from independent claims 1, 11, and 43, respectively, and each recites the additional limitation of “wherein the memory is comprised of a plurality of planes and wherein one or more of said zones are comprised of blocks from a plurality of planes.” Ex. 1001, 13:8–12, 13:47–50, 16:19–22. Claims 6, 16, and 48 depend from claims 5, 15, and 47, respectively, and each recites the additional limitation of “wherein said plurality of planes are from more than one chip.” Ex. 1001, 13:13–14, 13:51–52, 16:23–24.

Petitioner argues that the combined teachings of Tanaka, Estakhri, and Mukaida account for these limitation. Pet. 49–53. Petitioner also relies on its analysis for independent claims 1, 11, and 43 to account for the remaining limitations. *Id.* at 49, 52, 53. Patent Owner does not raise any separate arguments for these claims, apart from those considered above with respect to the independent claims. PO Resp. 47–48.

We find that Mukaida discloses “virtual blocks,” i.e., logical zones, which represent a plurality of physical blocks from a plurality of “groups” or “banks,” i.e., planes, located on a single memory chip. Ex. 1007, Abstract, 6:21–33, 26:32–35; Ex. 1003, A-73–A-84. We further find that Mukaida discloses that a logical zone (i.e., virtual block) can simultaneously include (a) multiple blocks located in different planes (i.e., banks) on the same flash memory chip, and (b) additional blocks located in planes (i.e., banks) on a second flash memory chip. Ex. 1007, 31:19–22, 3:6–11, 37:19–24, Figs. 16, 23; Ex. 1003, A-73–A-84. As for claims 6, 16, and 48, we find that Mukaida’s disclosure of the “banks” found within a “virtual block” can be from more than one chip as accounting for the limitation that a “plurality of planes are from more than one chip.” Ex. 1007, 37:19–24; Ex. 1003, A-79–A-80.

We agree with Petitioner and Dr. Subramanian that a person of ordinary skill would have had reason to combine the teachings of Tanaka, Estakhri, and Mukaida to achieve the systems recited in these claims. Pet. 18; Ex. 1003 ¶¶ 83–87. As Dr. Subramanian explains, Tanaka, Estakhri, and Mukaida are in the same field of endeavor and address common issues—controlling flash memory devices, creating logical groups of blocks (zones), and managing defects. Ex. 1003 ¶ 84 (citing Ex. 1007,

Abstract, 11:38–42, 11:47–56; Ex. 1005, [54], ¶¶ 52, 208). Furthermore, both Estakhri and Mukaida disclose controllers that divide the physical addresses into planes on different chips and create zones of blocks to facilitate parallel operations. *Id.* ¶ 85 (citing Ex. 1006, Abstract, 3:48–56, 7:55–62, 9:52–61, Fig. 2; Ex. 1007, 2:56–59, 3:5–16, 6:21–33, 26:32–35, 37:19–24, Figs. 16, 23). We agree with Dr. Subramanian’s explanation that applying Mukaida’s teachings to those of Tanaka and Estakhri would have been obvious because (1) a person of ordinary skill in the art would have had reason to combine such similar teachings to use parallel operations to increase speed and performance, and (2) it would involve the use of a known technique to improve a similar device. Ex. 1003 ¶¶ 86, 87.

We determine that Petitioner has shown by a preponderance of the evidence that claims 5, 6, 15, 16, 47, and 48 are unpatentable as obvious over the combined teachings of Tanaka, Estakhri, and Mukaida.

C. Obviousness of Claims 5, 6, 15, 16, 47, and 48 Over Tanaka, Estakhri, and Hazen

Petitioner contends that claims 5, 6, 15, 16, 47, and 48 are unpatentable under 35 U.S.C. § 103(a) as obvious over Tanaka, Estakhri, and Hazen. Pet. 53–58. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Subramanian Declaration (Ex. 1003) to support its positions.

1. Hazen (Ex. 1008)

Hazen is entitled “Flash Memory Partitioning for Read-While-Write Operation.” Ex. 1008, [54]. Hazen relates generally to partitioning a flash memory to allow “each partition [to be] able to be read, written, or erased

simultaneously with the other partitions.” *Id.*, Abstract. Hazen further discloses that each of the partitions is implemented on a different physical plane. *Id.* at 2:24–29.

2. *Analysis*

Claims 5, 15, and 47 depend from independent claims 1, 11, and 43, respectively, and each recites the additional limitation of “wherein the memory is comprised of a plurality of planes and wherein one or more of said zones are comprised of blocks from a plurality of planes.” Ex. 1001, 13:8–12, 13:47–50, 16:19–22. Claims 6, 16, and 48 depend from claims 5, 15, and 47, respectively, and each recites the additional limitation of “wherein said plurality of planes are from more than one chip.” *Id.* at 13:13–14, 13:51–52, 16:23–24.

Petitioner argues that the combined teachings of Tanaka, Estakhri, and Hazen render these limitations obvious. Pet. 53–58. Petitioner also relies on its analysis for independent claims 1, 11, and 43 to account for the remaining limitations. *Id.* at 53–54, 57, 58. Patent Owner does not raise any separate arguments for these claims, apart from those considered above with respect to the independent claims. PO Resp. 47–48.

We find that that Estakhri discloses logical zones (i.e., “super blocks”) that are each made up of a plurality of physical blocks from “block rows” (i.e., planes) located on different flash memory devices, which also are known as chips or dies. Ex. 1006, 7:55–62, Fig. 2; Ex. 1003, A-85–A-97. We further find that, regardless of whether a “plane” requires that each “plane” contain more than one block on a single die, Hazen satisfies this limitation through its disclosure of “partitions” including one or more blocks, where the partitions are physical subdivisions of memory on a single

die. Ex. 1008, 2:28–29, Figs. 2, 3; Ex. 1003, A-85–A-97. We further find that Hazen’s teaching of a “plane” containing multiple blocks on the same die accounts for the limitations of claims 6, 16, and 48. *See id.*

We agree with Petitioner and Dr. Subramanian that a person of ordinary skill at the time of the invention would have had reason to combine the teachings of Tanaka, Estakhri, and Hazen to achieve the systems recited in these claims. Ex. 1003 ¶¶ 88–91. Hazen teaches erasing multiple blocks at one time, which is one of the specific aims of Estakhri in forming a logical zone. Ex. 1008, Abstract, 5:11–12; Ex. 1006, 7:55–62, 9:52–61. Each of Estakhri and Hazen discloses controllers that divide the physical addresses into partitions (planes) to facilitate parallel operations. Ex. 1006, 3:48–56, 7:55–62, 9:52–61, Fig. 2; Ex. 1008, Abstract, Fig. 3, 1:60–64, 2:27–30, 2:17–21, 5:11–12. As Dr. Subramanian explains, and we agree, applying Hazen’s teachings to those of Tanaka and Estakhri would have been obvious because it would solve common issues addressed in each reference, such as space management and parallel operations, including the simultaneous erasure of blocks; and it would involve the use of a known technique to improve a similar device. Ex. 1003 ¶¶ 90, 91.

Thus, we find that Petitioner has shown by a preponderance of the evidence that claims 5, 6, 15, 16, 47, and 48 are unpatentable as obvious over the combined teachings of Tanaka, Estakhri, and Hazen.

D. Obviousness of Claims 22 and 33 Over Tanaka, Estakhri, and Garvin

Petitioner contends that claims 22 and 33 are unpatentable under 35 U.S.C. § 103(a) as obvious over Tanaka, Estakhri, and Garvin. Pet. 58–60. To support its contentions, Petitioner provides explanations as to how

the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Subramanian Declaration (Ex. 1003) to support its positions.

1. *Garvin (Ex. 1009)*

Garvin is entitled “Method and System for Managing Bad Areas in Flash Memory.” Ex. 1009, at [54]. Garvin describes a method and system for managing bad areas in flash memory called Bad Block Management where bad areas of flash memory are remapped to good areas without corrupting or losing any information stored in the flash memory. *Id.* at 4:3–7. As part of Garvin’s bad block management method, the process determines if the free block can pass a stress test, which is described as well-known in the art. *Id.* at 8:60–64. If a block fails the stress test, the block then is marked as bad. *Id.* at 9:26–31.

2. *Analysis*

Claim 22 depends from claim 21, and claim 33 depends from claim 32. Each claim recites the additional limitation of “wherein said identifying comprises: testing said memory blocks; and determining said defective blocks based on said testing.” Ex. 1001, 14:13–16, 15:1–4. Petitioner argues that the combined teachings of Tanaka and Garvin account for this limitation. Pet. 58–60. Petitioner relies on its analysis for independent claims 21 and 32 to account for the remaining limitations. *Id.* at 58, 60. Patent Owner does not raise separate arguments for these claims, apart from those considered above with respect to the independent claims. PO Resp. 47–48.

We find that Tanaka discloses identifying defective blocks before shipping and after use of the flash memory. Ex. 1005 ¶¶ 7, 102, 136, 184,

Figs. 33, 43; Ex. 1003, A-98–A-103. We further find that Garvin discloses a “stress test” for identifying defective blocks. Ex. 1009, 8:60–67, 9:22–30, 9:59–10:2, 17:17–26, Fig. 10; Ex. 1003 ¶ 76, A-98–A-103.

We agree with Petitioner and Dr. Subramanian that a person of ordinary skill would have had reason to combine the teachings of Tanaka, Estakhri, and Garvin to achieve the methods recited in these claims. Ex. 1003 ¶¶ 92–96. We find that Tanaka addresses methods to improve yield and increase the life of the flash device. Ex. 1005 ¶¶ 177, 184, 208. We find that Petitioner’s reasoning that Garvin’s teachings of a stress test would supplement Tanaka’s teaching regarding the detection of defects to assist in managing defects is articulated and supported by rational underpinnings. *Id.* (citing Ex. 1009, 8:55–9:15, 9:27–30, 17:17–26). We also find that applying Garvin’s teachings to those of Tanaka and Estakhri would have been obvious because it would have involved the use of a known technique to improve a similar device. Ex. 1003 ¶ 95.

Thus, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 22 and 33 are unpatentable as obvious over the combined teachings of Tanaka, Estakhri, and Garvin.

E. Patent Owner’s Motion to Exclude

We have reviewed Patent Owner’s Motion to Exclude (Paper 31), Petitioner’s Opposition to the Motion (Paper 35), and Patent Owner’s Reply in Support of the Motion (Paper 36). Patent Owner moves to exclude certain paragraphs of the reply testimony of Dr. Subramanian (Ex. 1014 ¶¶ 24, 38) and Exhibit 1015. Paper 31. We did not rely on the testimony to which Patent Owner objects or the exhibit identified in Patent Owner’s Motion to

Exclude. Accordingly, for these reasons, we *dismiss* Patent Owner's Motion to Exclude as *moot*.

IV. CONCLUSION

We determine that Petitioner has demonstrated, by a preponderance of the evidence, that

- A. Claims 1, 2, 11, 12, 21, 27, 32, 38, 43, and 44 of the '498 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Tanaka and Estakhri;
- B. Claims 5, 6, 15, 16, 47, and 48 of the '498 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Tanaka, Estakhri, and Mukaida;
- C. Claims 5, 6, 15, 16, 47, and 48 of the of the '498 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Tanaka, Estakhri, and Hazen; and
- D. Claims 22 and 23 of the '498 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Tanaka, Estakhri, and Garvin.

V. ORDER

Accordingly, it is

ORDERED that, based on a preponderance of the evidence, claims 1, 2, 5, 6, 11, 12, 15, 16, 21, 22, 27, 32, 33, 38, 43, 44, 47, and 48 of the '498 patent have been shown unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude is *dismissed as moot*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2016-00330
Patent 6,901,498 B2

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