

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

INNOVATIVE MEMORY SYSTEMS, INC.,
Patent Owner.

IPR2016-00330
Patent 6,901,498 B2

Before KARL D. EASTHOM, JAMES B. ARPIN, and
KEVIN W. CHERRY, *Administrative Patent Judges*.

CHERRY, *Administrative Patent Judge*.

JUDGMENT

Final Written Decision on Remand
Determining Some Claims Unpatentable
35 U.S.C. §§ 144, 318

I. INTRODUCTION

A. BACKGROUND

1. *Original Proceedings Before the Board*

Micron Technology, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting institution of *inter partes* review of claims 1, 2, 5, 6, 11,

12, 15, 16, 21, 22, 27, 32, 33, 38, 43, 44, 47, and 48 (“the challenged claims”) of U.S. Patent No. 6,901,498 B2 (Ex. 1001, “the ’498 patent”). Innovative Memory Systems, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 8, “Prelim. Resp.”).

The Petition challenges the patentability of claims 1, 2, 5, 6, 11, 12, 15, 16, 21, 22, 27, 32, 33, 38, 43, 44, 47, and 48 of the ’498 patent under the following grounds:

References	35 U.S.C. §	Claims Challenged
Tanaka ¹ , Estakhri ²	103(a) ³	1, 2, 11, 12, 21, 27, 32, 38, 43, 44
Tanaka, Estakhri, Mukaida ⁴	103(a)	5, 6, 15, 16, 47, 48
Tanaka, Estakhri, Hazen ⁵	103(a)	5, 6, 15, 16, 47, 48
Tanaka, Estakhri, Garvin ⁶	103(a)	22, 33

Pursuant to 35 U.S.C. § 314, we instituted this trial (“Decision to Institute”) as to each of the challenged claims of the ’498 patent. Paper 10 (“Dec.”).

¹ European Patent Application No. 0 896 280 A2, published Feb. 10, 1999 (Ex. 1005).

² U.S. Patent No. 6,034,897, issued Mar. 7, 2000 (Ex. 1006).

³ Because the claims at issue have an effective filing date prior to March 16, 2013, the effective date of the applicable provisions of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), we apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103 in this Decision.

⁴ U.S. Patent No. 7,020,739 B2, issued Mar. 28, 2006 (Ex. 1007).

⁵ U.S. Patent No. 6,088,264, issued July 11, 2000 (Ex. 1008).

⁶ U.S. Patent No. 6,260,156 B1, issued July 10, 2001 (Ex. 1009).

After the Decision to Institute, Patent Owner filed a Patent Owner Response (Paper 22, “PO Resp.”) and Petitioner filed a Reply to the Patent Owner Response (Paper 26, “Pet. Reply”). An oral hearing was held March 23, 2017. A transcript of the oral hearing has been entered into the record. Paper 39 (“Tr.”).

Petitioner relies on the testimony of Dr. Vivek Subramanian (Ex. 1003 & Ex. 1014 (“Reply Declaration”)) in support of its contentions. Patent Owner relies on the testimony of Dr. Scott M. Nettles (Ex. 2002) in support of its contentions.

Patent Owner filed a Motion to Exclude certain evidence. Paper 31 (“Mot. Exclude”). Petitioner filed an opposition. Paper 35 (“Opp.”). Patent Owner filed a reply. Paper 36 (“PO Reply”).

Patent Owner also filed a Motion for Observations on Cross Examination of Dr. Subramanian. Paper 32. Petitioner filed a response. Paper 34. Pursuant to our authorization by email, Patent Owner also filed an Unopposed Motion for Observation of Patent Owner’s Own Witness. Paper 33. We considered Patent Owner’s observations and Petitioner’s response in arriving at our Final Written Decision in this case.

On June 22, 2017, we issued a Final Written Decision finding all of the challenged claims unpatentable. *See* Paper 40 (“Final Written Decision” or “Final Dec.”). We found Petitioner had carried its burden on all of the grounds raised in the Petition. *See id.* at 42. Patent Owner appealed our Final Written Decision to the U.S. Court of Appeals for the Federal Circuit. *See* Paper 41 (Notice of Appeal).

2. *Federal Circuit Decision*

On August 27, 2019, the Federal Circuit issued a decision affirming-in-part, reversing-in-part, vacating-in-part, and remanding our Final Written Decision. *Innovative Memory Systems, Inc. v. Micron Technology, Inc.*, 781 F. App’x 1013 (Fed. Cir. 2019) (also in the record as Ex. 3001). The Federal Circuit agreed with Patent Owner that we erred in construing the claim term “wherein the correspondence of blocks to zones is adjustable by controller” found in claims 1 and 11 and the corresponding term “wherein the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects the in memory” from claim 43. *Id.* at 1016. Finding our construction incorrect, the Federal Circuit adopted Patent Owner’s proposed construction and held that “[t]he term requires that the controller can adjust zone boundaries such that blocks from one logical zone are shifted to another logical zone.” *Id.* at 1017.

The Federal Circuit then reviewed our analysis of the prior art. *Id.* at 1017–18. In our Final Written Decision, we had addressed Patent Owner’s construction and found that Tanaka still taught or suggested a controller meeting the limitation under Patent Owner’s construction. Final Dec. 23–24. Referring to claim 1 as representative, the Federal Circuit held, however, that our analysis “ignored the requirements of the claim,” and we “cut the analysis short.” *See Innovative Memory*, 781 F. App’x 1017–18. The court explained that “[t]he claim does not simply require that the memory is organized into ‘logical zones’ of any nature.” *Id.* at 1018 (footnote omitted). Instead, the full claim limitation expressly requires that the memory is “organized” into “logical zones each comprised of one or more blocks for address translation.” *Id.* (quoting Ex. 1001, 12:64–66). The

court reasoned that the claim requires that “the zones contain blocks that are already assigned for address translation.” *Id.* Patent Owner argued that the Federal Circuit should reverse because “there is no evidence to show that the ‘redundant block area’ in Tanaka is a zone in which memory is already organized or mapped to an address.” *Id.* The Federal Circuit noted that Dr. Nettles testified that these redundant blocks do not have logical addresses until they are used to replace a defective block, *id.* (citing Ex. 2002 ¶¶ 105, 106), and that Dr. Subramanian “appeared not to dispute this point,” *id.* (citing Ex. 2006 (Subramanian Deposition), 27:2–16). Rather than reverse on this issue, the Federal Circuit decided that “the better course is to remand to the Board for determination of the factual issue under the proper construction.” *Id.* Consequently, the court vacated our “conclusion about this limitation and remanded for further proceedings regarding whether the prior art teaches this limitation in independent claims 1, 11, and 43 and their respective dependent claims (2, 5, 6, 12, 15, 16, 44, 47, and 48).” *Id.*

Patent Owner also challenged our finding that the combination of Tanaka and Estakhri teaches or suggests “a single controller” in independent claims 1, 11, 21, 32, and 43. *Id.* at 1018. The Federal Circuit disagreed with Patent Owner’s arguments. *Id.* at 1018–19. Because the “single controller” was Patent Owner’s only challenge to our decision with respect to claims 21, 22, 27, 32, 33, and 38, the Federal Circuit affirmed our finding that claims 21, 22, 27, 32, 33, and 38 are unpatentable as obvious.⁷ *Id.* at 1019.

⁷ Claim 33 depends from claim 32 and adds a limitation identical to the limitation added to claim 21 by claim 22. Thus, although the Federal Circuit did not include claim 33 in its list of affirmed claims, it also did not include claim 33 in the list of remanded claims, and based on the court’s affirmance

3. *Remand Proceedings*

On November 12, 2019, we authorized additional briefing on the narrow issue of whether one or more blocks in Tanaka’s redundant block area are “for address translation,” as recited in claims 1 and 11, and why the redundant block area is a “logical address section,” as recited in claim 43. Paper 43, 5. Petitioner filed an opening Brief on Remand (Paper 44, “Pet. Br.”), Patent Owner filed an Opposition Brief on Remand (Paper 46, “PO Br.”), Petitioner filed a Reply Brief on Remand (Paper 47, “Remand Reply”), and Patent Owner filed a Sur-Reply Brief on Remand (Paper 48, “PO Sur-Reply”).

We have jurisdiction under 35 U.S.C. §§ 6(b) and 144(b). This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. We determine that Petitioner has not shown that claims 1, 2, 5, 6, 11, 12, 15, 43, 44, 47, and 48 are unpatentable. As to claims 21, 22, 27, 32, 33, and 38, we observe that the Federal Circuit affirmed that these claims are unpatentable as obvious. *See* 781 F. App’x at 1018–20.

B. RELATED PROCEEDINGS

According to the parties, the ’498 patent is involved in, at least, the following lawsuit: *Innovative Memory Sys., Inc. v. Micron Tech., Inc.*, 14-cv-1480 (D. Del.). Pet. 2.

of claims 21, 22, and 32, we understand the omission of claim 33 from the list of affirmed claims to have been an oversight. *See Innovative Memory*, 781 F. App’x at 1019 (listing disposition of various claims). Neither party discusses claim 33 in their remand briefing. Accordingly, we include claim 33 in the group of affirmed claims.

C. THE '498 PATENT

The '498 patent is entitled “Zone Boundary Adjustment for Defects in Non-Volatile Memories,” and issued May 31, 2005. Ex. 1001, codes (54), (45). The '498 patent generally relates to non-volatile semiconductor memories, such as electrically erasable programmable read-only memories (“EEPROM”), their architectures, and their methods of operation. *Id.* at 1:5–10. The '498 patent describes a non-volatile memory device capable of adjusting the boundaries of logical zones within the memory to accommodate defects in the memory. *Id.*, Abstract. According to the '498 patent, such a device improves memory card yields and extends the useable lifetime of the memory card. *Id.*

The '498 patent explains that flash EEPROM devices are composed of one or more arrays of transistor cells, with each cell capable of non-volatile storage of one or more bits of data. *Id.* at 1:18–20. The '498 patent explains that flash memory does not require power to retain the bits of data, but once it is programmed, a cell must be erased before it can be reprogrammed with new data. *Id.* at 1:21–23. To provide for the efficient implementation of read, program, and erase functions, the arrays of cells in the flash memory are partitioned into groups. *Id.* at 1:23–26. The '498 patent states that a typical flash memory architecture for mass storages arranges large groups of cells into erasable blocks, wherein a block contains the smallest number of cells that are erasable at one time (i.e., the unit of erase). *Id.* at 1:26–30.

Flash memory systems use a controller that performs high-level host and memory control functions. *Id.* at 3:14–15. One of the functions performed by the controller includes the translation between logical addresses received by the memory sub-system from a host and physical

addresses within the memory cell array. *Id.* at 1:49–55. The '498 patent describes that a memory often will have defective portions, either from the manufacturing process or that arise during the operation of the device. *Id.* at 5:65–67. One method of dealing with these defects is to test the device before being shipped to find a defective portion of the memory that needs to be eliminated and storing the location of the defective portions, so that the controller can substitute a good portion of the memory for the defective portion. *Id.* at 6:5–13. In such a solution, the controller will need to refer to a pointer structure in the controller for the re-mapping of the memory. *Id.* at 6:13–15. The '498 patent explains that, although memories often are designed with a number of redundant blocks to replace defective blocks, the blocks generally are not distributed between the logical structure areas of the memory. *Id.* at 6:16–19. The '498 patent states that if the number of bad blocks is too large or too unevenly distributed, this results in yield losses or downgrades the capacity of the memory card. *Id.* at 6:19–21.

The '498 patent purports to solve these shortcomings. The '498 patent describes that the non-volatile memory is divided into logical zones by the card controller in order to reduce the size of the data structures used for address translation. *Id.* at 6:24–28. The '498 patent provides a method to adjust the zone boundaries to accommodate defects found in testing and to adjust boundaries in the field to extend the usable life of the memory card. *Id.* at 6:28–32.

The '498 patent describes performing this method at two times. First, at the time of card production, an operation is performed that sets zone boundaries. *Id.* at 6:33–34. During this process, the firmware scans for the presence of defective blocks on the memory card. *Id.* at 6:34–36. Once the

locations of all the blocks are known, the firmware calculates the zone boundaries in such a way that good blocks are distributed equally among the zones. *Id.* at 6:36–38. Second, the '498 patent explains that the controller can perform dynamic boundary adjustments. *Id.* at 6:41–42. When defects occur, the controller performs the analysis again and, if the number of good blocks becomes unbalanced, redistributes the zone boundaries, moving any user data. *Id.* at 6:42–45.

Of the challenged claims, claims 1, 11, 21, 32, and 43 are independent. Claims 2, 5, and 6 depend, directly or indirectly, from claim 1; claims 12, 15, and 16 depend, directly or indirectly, from claim 11; claims 22 and 27 depend from claim 21; claims 33 and 38 depend from claim 32; and claims 44, 47, and 48 depend, directly or indirectly, from claim 43.

Claim 1, 11, and 43 are illustrative and are reproduced below. The limitations remaining in dispute are emphasized.

1. A memory system circuit, comprising:

- a memory comprising a plurality of blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable, and
- a controller that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time, *wherein the memory is organized into logical zones each comprised of one or more blocks for address translation, and wherein the correspondence of blocks to zones is adjustable by controller.*

11. A memory system circuit, comprising:

- a memory comprising a plurality of blocks of non-volatile storage elements wherein the storage elements within

individual ones of the blocks are simultaneously erasable,
and

- a controller that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time, *wherein the memory is organized into logical zones each comprised of one or more blocks for address translation, and wherein the correspondence of blocks to zones is dynamically adjustable by controller.*

43. A memory system circuit, comprising:

- a memory comprising a plurality-of blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable,
- a controller that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time, *wherein the non-volatile is organized into logical address sections as seen by the controller, wherein the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory.*

II. ANALYSIS

A. TANAKA

Tanaka is entitled “Method for Controlling Nonvolatile Semiconductor Memory System,” and generally relates to methods for controlling a non-volatile semiconductor memory system, such as a non-volatile semiconductor memory card. Ex. 1005, code (54), ¶ 1. As part of its control methods, Tanaka discloses a procedure for ensuring sufficient storage in each logical division of the memory. *Id.* ¶ 176. In order to ensure this, “the flash memory must have a writable and erasable effective block as a block replaced when the defective block is produced.” *Id.* In Tanaka, the

memory “is provided with a plurality of redundant blocks,” and the defective blocks are replaced with the redundant blocks “by means of a redundant circuit as a hardware when the flash memory is shipped.” *Id.* ¶ 177. Tanaka explains that, “[w]hen the redundant circuit is used, the redundant blocks are allocated to addresses of defective blocks.” *Id.* Tanaka also explains that the replacement can be performed sequentially, with the defective blocks with smaller addresses being replaced first, or the blocks can be replaced with redundant blocks, so that each of the zones has the permitted number of effective blocks. *Id.* ¶¶ 178, 181–183. Figure 48 of Tanaka is reproduced below.

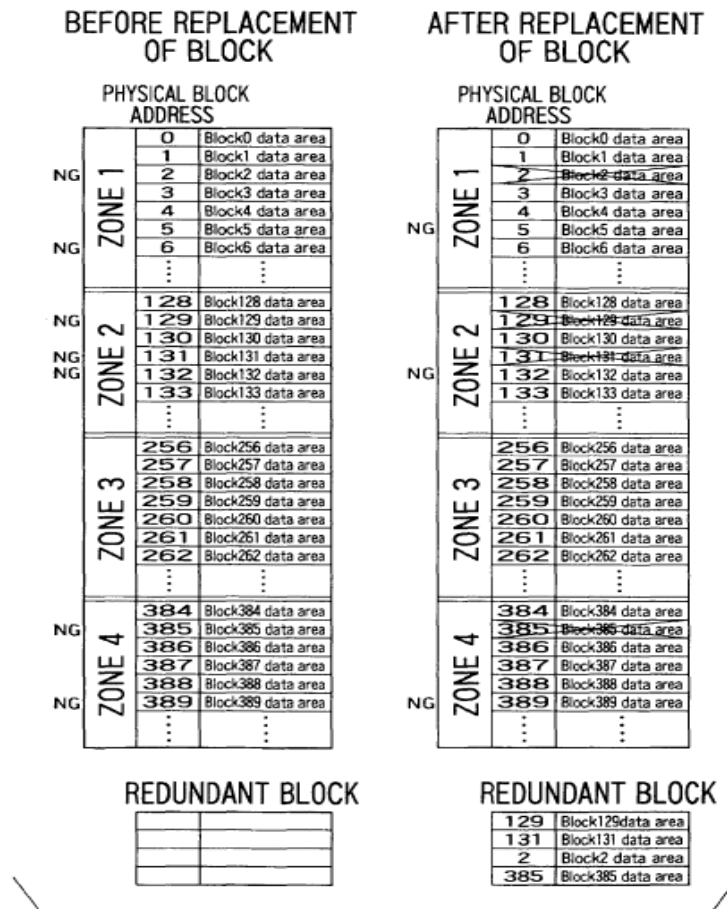


FIG. 48

Figure 48, reproduced above, depicts “the state of a physical block when defective blocks existing in each zone are replaced with redundant blocks so that the number of defective blocks [does not] exceed[] the number permitted in each zone. *Id.* ¶ 184.

Tanaka explains that, given the distribution of defective blocks in the zones, using the conventional method of simply replacing memory blocks sequentially, from the lowest address to the highest, would result in a product that could not be shipped. *Id.* In order to reduce losses, Tanaka discloses an algorithm that replaces blocks, such that the number of defective blocks does not exceed the number of defective blocks permitted in each zone. *Id.*

B. CLAIMS 1, 2, 5, 6, 11, 12, 15, 23, 32, 43, 44, 47, AND 48

As discussed above, the Federal Circuit remanded on the limited issue of whether Tanaka teaches or suggests the limitations “wherein the memory is organized into logical zones each comprised of one or more blocks for address translation, and wherein the correspondence of blocks to zones is adjustable by controller” in claims 1 and 11 and “wherein the non-volatile is organized into logical address sections as seen by the controller, wherein the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory” in claim 43. Petitioner raises several arguments why it contends that Tanaka teaches or suggests these limitations under the Federal Circuit’s construction. We consider them below.

1. Whether the Blocks in Tanaka’s Redundant Block Area Are “For Address Translation”

The parties agree that Tanaka’s redundant blocks are not assigned logical addresses until they replace defective blocks. *See* Ex. 2002 ¶ 105,

106; Ex. 2006, 27:2–16; Pet. Br. 6 (“Namely, redundant blocks are not assigned logical addresses or included in address-translation tables until they replace defective blocks.”); PO Br. 4. Yet, in its remand briefing, Petitioner argues that there are two reasons that Tanaka’s redundant blocks satisfy the requirement that the blocks be organized in logical zones “for address translation.” Pet. Br. 1–8. First, Petitioner argues that the blocks in Tanaka’s redundant block area teach or suggest this limitation because “they are earmarked for address translation.” *Id.* at 1, 2–5. Second, Petitioner argues that “by not being included in address-translation tables before they replace defective blocks, the redundant blocks accomplish the ’498 patent’s goal of reducing the size of data structures used for address translation.” *Id.* at 1, 5–8. Neither of these arguments is persuasive.

Petitioner’s first argument ignores the analysis of the Federal Circuit. The Federal Circuit rejected our prior analysis because “[t]he claim does not simply require that the memory is organized into ‘logical zones’ of any nature.” *Innovative Memory*, 781 F. App’x at 1018. Instead, the Federal Circuit explained as follows:

Thus, the zones contain blocks that are already assigned for address translation. As discussed above, the properly construed remaining language in the claim then requires a controller that can adjust boundaries between zones of assigned blocks “such that blocks from one logical zone are shifted to another logical zone.”

Id. Given this analysis and the Federal Circuit’s construction, we agree with Patent Owner that “adjusting blocks that are not yet assigned to logical zones to replace defective blocks that are already assigned to logical zones is not enough to satisfy the claim limitations.” PO Br. 2. Indeed, Federal Circuit noted that our original analysis found that “Tanaka discloses taking

spare blocks unassociated with an address and assigning them to a zone” and that the redundant block area “could be considered a logical zone, though none of the blocks within it are assigned to an address.” *Id.* at 8. We have difficulty seeing, and Petitioner does not explain, how its argument that “being earmarked for address translation” is in any meaningful way different from our prior analysis that the Federal Circuit rejected.

Moreover, it cannot be disputed that the blocks in the redundant block area are “available” or “earmarked” for address translation. Yet, the Federal Circuit focused on whether the blocks had been “assigned” for address translation, directing us to the testimony of the experts on whether Tanaka’s blocks had been assigned logical addresses. *See Innovative Memory*, 781 F. App’x at 1018. Thus, we are not persuaded by Petitioner’s argument that merely being available for address translation is sufficient to satisfy the claim limitation.

As for Petitioner’s other argument that Tanaka’s redundant blocks are assigned “for address translation” because they “further the ’498 patent’s goal of ‘reduc[ing] the size of the data structures . . . use[d] for address translation,” we do not find it persuasive. Pet. Br. 5–6. The fact that Tanaka’s redundant blocks may similarly accomplish one of the goals of the invention of the ’498 patent does not persuade us that Tanaka teaches or suggests the disputed limitation. There can be many ways to accomplish a similar goal, but our focus is on what is claimed. The claims of the ’498 patent recite a particular way of allegedly accomplishing the goals set forth in the Specification. Thus, the fact that both Tanaka and the ’498 patent share similar goals does not necessarily mean that Tanaka teaches or suggests the specific limitations recited in the claims. The Federal Circuit

made clear that a block's presence in any logical zone was insufficient. *Innovative Memory*, 781 F. App'x at 1018. Instead, the Federal Circuit required that the blocks be actually "assigned for address translation." *Id.*

As for Petitioner's contention that the lack of a logical address is not dispositive, we disagree. Pet. Br. 7–8. In *Tanaka*, a block sits unused until the system assigns it a logical address so it then can be used for address translation and storage of data. *See* Ex. 2009, 20:5–21:24. Although the Federal Circuit did not say the assignment of logical addresses was dispositive, we agree with Patent Owner that this is the logical conclusion resulting from the court's analysis. PO Br. 6–7. Here, there is no dispute that *Tanaka*'s redundant blocks are not assigned logical addresses until they replace defective blocks. Thus, we agree with Patent Owner that Petitioner has failed to show that *Tanaka*'s system adjusts blocks in the redundant zone between logical zones "for address translation," as required by claims 1 and 11.

2. *Whether Tanaka's Spare Blocks Are "For Address Translation"*

In its original Reply Brief, Petitioner offered a new theory as to why *Tanaka* accounted for the "adjustable by controller" limitation. Pet. Reply 17–19. Petitioner notes that it is not disputed that in each of Zones 1 to 4 in Figure 48 of *Tanaka*, there are "spare blocks" that can be used to replace defective blocks that occur in Zone 1 to 4. *Id.* at 18 (citing Ex. 2002 ¶ 75). Petitioner contends that each set of "spare blocks" within Zones 1 to 4 itself constitutes a "zone" under the construction of "zone" in the '498 patent. *Id.* (citing Ex. 1014 ¶ 24). In addition, Petitioner argues that each "active data block" area that contains the collection of good blocks

(i.e., where valid user data is stored) in Zones 1 to 4 also constitutes a “zone” as defined in the ’498 patent. *Id.* Based on these contentions, Petitioner asserts the logical address remapping in Tanaka satisfies Patent Owner’s construction. *Id.*

Initially, this theory that Zones 1–4 actually each constitute two zones (the active data blocks and the spare blocks) was not presented in the Petition. Thus, there is some force to Patent Owner’s contentions that this is an improper new argument and can be disregarded for that reason alone. *See Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). However, we elect to reach the merits of the argument here regardless of whether it reasonably can be said to be ‘new,’ in the interest of completeness. We reject the argument as meritless. Indeed, this theory suffers not only from the same problem as Petitioner’s theory for the blocks in the redundant block area—there is no evidence that the spare blocks in each of Tanaka’s zones are assigned a logical address “for address translation”—this theory suffers from other problems as well.

The first, and most significant hurdle facing this theory, is that this type of arrangement—spare blocks within a logical zone—is discussed and distinguished in the ’498 patent. *See* Ex. 1001, 7:66–8:12. As the Federal Circuit explained, the claim requires more than the memory being organized into “logical zones” of any nature. *Innovative Memory*, 781 F. App’x at 1018. Thus, the fact that “active block area” and “spare block area” can be characterized as logical zones is irrelevant. Given the ’498 patent distinguishes spare blocks within an existing logical zone from being within the scope of claimed invention, we fail to see, and neither Petitioner nor Dr. Subramanian explains, how remapping the spare blocks to logical

addresses meets the construction of “the correspondence of blocks to zones is adjustable by the controller” where those blocks must be assigned “for address translation,” as explained by the Federal Circuit.

Even if the ’498 patent did not expressly distinguish this configuration, Petitioner’s contentions suffer from a second problem. Just as with its original contentions regarding the redundant block area, there is no evidence that the “spare blocks” are “for address translation,” as required by the claim. Indeed, Tanaka explains that fewer logical addresses are assigned to zones than the number of physical blocks. *See* Ex. 1005 ¶¶ 171, 173 (describing embodiment where 128 physical blocks are allocated to zone but only 125 logical addresses), 179 (describing embodiment where 512 physical blocks are allocated, but only 500 logical addresses).⁸ The evidence suggests that the “spare” physical blocks sit unused until a logical address is assigned. Petitioner provides no evidence that the spare blocks are assigned for address translation as the Federal Circuit has held that the claims require. Thus, Petitioner’s alternative theory is also unpersuasive.

⁸ In its Reply Brief on remand, Petitioner cites to alleged “admissions” that the spare blocks are included in the address-translation tables. *See* Remand Reply 5. These alleged admissions are in the form of questions that Patent Owner’s counsel asked Dr. Subramanian at his deposition. Reading these questions, we are not persuaded that Patent Owner’s counsel made any such admissions. *See* Ex. 2009, 20:5–21:2, 17:10–23. Moreover, and more importantly in our view, Dr. Subramanian admitted that the “spare blocks” do not have logical addresses written into them until they replace defective blocks within the table. *See id.* at 20:24–21:2. Thus, the spare blocks remain unused and unassigned “for address translation” until they replace defective blocks and have logical addresses written into them. *See id.* at 20:5–21:2.

3. *Claims 43, 44, 47, and 48*

Claim 43 recites, in relevant part, “the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory.” Petitioner argues that we should reach a different result for independent claim 43 (and claims 44, 47, and 48, which depend from claim 43) because claim 43 does not include the “for address translation” limitation discussed above with respect to independent claims 1 and 11. Pet. Br. 8–10. Instead, claim 43 recites adjusting the relationship between “blocks” and “logical address sections.” *Id.* Petitioner argues that our Final Written Decision equated a “logical address section” with a logical zone, and found that Tanaka’s redundant block area was a “logical address section” because it was a logical zone. *Id.* at 9. Petitioner asserts that this is consistent with how Patent Owner treated this limitation, and that Patent Owner cannot now argue for a different construction of “logical address section.” *Id.* at 9–10 (citing PO Resp. 45–47; Ex. 2002 ¶ 130). Petitioner contends that because the Federal Circuit did not disturb our finding that Tanaka’s redundant block area is a logical zone, we again should find claim 43 (and the claims that depend from it) unpatentable. *Id.* at 10. We disagree.

Petitioner’s argument rests on two incorrect premises. First, we do not agree that Patent Owner equated “logical address section” with all types of “logical zone.” Instead, Dr. Nettles makes clear that the same arguments considered for claims 1 and 11 apply to “Tanaka’s teaching of moving redundant blocks that are not part of any logical zone into a logical zone in response to defects detected in the memory does not result in a change in the correspondence of a physical block from one logical address section to

another, and is thus insufficient to meet this claim limitation.” Ex. 2002

¶ 130. Integral to that argument was the requirement that blocks be assigned to logical zones for address translation, i.e., that the blocks be already assigned logical addresses. *See id.* ¶¶ 103–110. Thus, rather than concede that “logical address section” does not impose the same “for address translation” requirement of claims 1 and 11, we find that Patent Owner argued that the requirement that the blocks are assigned logical addresses “for address translation” was present in claim 43.

Second, Petitioner suggests that the Federal Circuit did not already decide this issue. However, the Federal Circuit explicitly included claim 43 in its analysis saying that the same analysis for claims 1 and 11 “holds true” for claim 43. *Innovative Memory*, 781 F. App’x at 1016. Moreover, in its analysis of the prior art, the Federal Circuit noted that our “reasoning was not meaningfully different [from our analysis of claim 1] for claims 11 or 43.” *Id.* at 1018. The Federal Circuit then went on to treat claim 1 as representative. *Id.* Petitioner does not appear to have objected to this treatment or sought rehearing. Thus, we are unpersuaded by Petitioner’s arguments that claim 43 does not include the same requirement that the blocks be assigned logical addresses before they are move from zone to zone.

Because the same analysis applies to each of claims 1, 11, and 43, we determine that Petitioner has failed, for the reasons discussed above, to show by a preponderance of the evidence that Tanaka accounts for “the correspondence between physical blocks and logical address sections [being] adaptable by the controller in response to defects in the memory,” as recited in claim 43.

4. *Summary*

We conclude that Petitioner has not shown by a preponderance of the evidence that Tanaka teaches or suggests “wherein the memory is organized into logical zones each comprised of one or more blocks for address translation, and wherein the correspondence of blocks to zones is adjustable by controller” of claims 1 and 11 and “wherein the non-volatile is organized into logical address sections as seen by the controller, wherein the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory” of claim 43. Claims 2, 5, 6, 12, 15, 16, 44, 47, and 48 depend from claims 1, 11, or 43. Petitioner does not allege that any other reference accounts for these limitations. Accordingly, we find that Petitioner has not shown that claims 1, 2, 5, 6, 11, 12, 15, 16, 43, 44, 47, and 48 are unpatentable as obvious.

C. CLAIMS 21, 22, 27, 32, 33, AND 38

The Federal Circuit affirmed our Final Written Decision with respect to claims 21, 22, 27, 32, 33, and 38. For completeness, we note that we previously found Petitioner has shown that claims 21, 22, 27, 32, 33, and 38 are unpatentable. *See* Final Dec. 31–34, 39–41.

D. PATENT OWNER’S MOTION TO EXCLUDE

In our Final Written Decision, we dismissed Patent Owner’s Motion to Exclude (Paper 31) as moot. However, on remand, we now have considered the specific testimony Patent Owner sought to exclude, so we address Patent Owner’s Motion to Exclude anew with respect to Paragraph 24 of Dr. Subramanian’s Reply Declaration. *See* Mot. Exclude 1.

Patent Owner argues that Petitioner's arguments in its Reply and the supporting testimony of Dr. Subramanian in his Reply Declaration as involving its new "spare" blocks theory. Mot. Exclude 1–7. Petitioner responds that Patent Owner's Motion to Exclude amounts to an unauthorized sur-reply or motion to strike. Pet. Opp. Mot. Exclude 1–7. We agree with Petitioner. As the Board has explained:

A motion to exclude must explain why the evidence is not admissible (e.g., relevance or hearsay), but may not be used to challenge the sufficiency of the evidence to prove a particular fact. Office Patent Trial Practice Guide, 77 Fed. Reg. 48,765, 48,767 (Aug. 14, 2012). While a motion to exclude may raise issues related to admissibility of evidence, it is not an opportunity to file a sur-reply, and also is not a mechanism to argue that a reply contains new arguments or relies on evidence necessary to make out a prima facie case.

Liberty Mut. Ins. Co. v. Progressive Cas. Ins. Co., CBM2013–00004, Paper 53, at 62 (PTAB Mar. 13, 2014) (Final Written Decision). Patent Owner's Motion to Exclude contains such improper arguments, and is in the nature of a sur-reply. Moreover, for the reasons discussed above (see *supra* Section II.B.2), we find Petitioner's arguments involving "spare" blocks unpersuasive.

For these reasons, Patent Owner's Motion to Exclude Paragraph 24 of Dr. Subramanian's Reply Declaration as presenting new arguments is *denied*.

III. CONCLUSION

For the reasons expressed above, we determine that Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 5, 6, 11, 12, 15,

23, 43, 44, 47, and 48 are unpatentable. As we previously determined, claims 21, 22, 27, 32, 33, and 38 had been shown to be unpatentable, and the Federal Circuit affirmed that determination. These findings are summarized in the table below.

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 11, 12, 21, 27, 32, 38, 43, 44	103(a)	Tanaka, Estakhri	21, 27, 32, 38	1, 2, 11, 12, 43, 44
5, 6, 15, 16, 47, 48	103(a)	Tanaka, Estakhri, Mukaida		5, 6, 15, 16, 47, 48
5, 6, 15, 16, 47, 48	103(a)	Tanaka, Estakhri, Hazen		5, 6, 15, 16, 47, 48
22, 23	103(a)	Tanaka, Estakhri, Garvin	22, 33	

We further deny Patent Owner's Motion to Exclude.

IV. ORDER

Accordingly, it is:

ORDERED that claims 21, 22, 27, 32, 33, and 38 of U.S. Patent No. 6,901,498 B2 have been shown to be unpatentable;

FURTHER ORDERED that claims 1, 2, 5, 6, 11, 12, 15, 23, 43, 44, 47, and 48 of U.S. Patent No. 6,901,498 B2 have not been shown to be unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude (Paper 31) is *denied*; and

FURTHER ORDERED that parties to the proceeding seeking judicial review of this Final Written Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2016-00330
Patent 6,901,498 B2

PETITIONER:

Jeremy Lang
PTABDocketJJL2@orrick.com

Jared Bobrow
doug.mcclellan@weil.com

PATENT OWNER:

Robert Morris
rwmorris@eckertseamans.com

Philip Levy
plevy@eckertseamans.com