

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00389
Patent 8,035,233 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and
FRANCES L. IPPOLITO, *Administrative Patent Judges*.

IPPOLITO, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively “Petitioner”) filed a Petition on December 28, 2015, requesting an *inter partes* review of claims 22, 31, 33, and 34 of U.S. Patent No. 8,035,233 B2 (Ex. 1001, “the ’233 patent”). (Paper 4, “Pet.”). On April 2, 2016, Patent Owner, Elm 3DS Innovations, LLC statutorily disclaimed claims 22 and 31 (Ex. 2138), thus, we did not consider Petitioner’s unpatentability challenges of claims 22 and 31. *See* 37 C.F.R. § 107(e). Subsequently, Patent Owner filed a Preliminary Response to the Petition on April 4, 2016 (Paper 11, “Prelim. Resp.”).

Based on these submissions, we instituted an *inter partes* review of claims 33 and 34 of the ’233 patent on the following grounds:

Reference(s)	Basis	Claim(s) Challenged
Leedy ’695 ¹ and Hitachi ²	§ 103	33 and 34
Matsumoto ³ , Bower ⁴ , and Leedy ’695	§ 103	33 and 34

Paper 14 (“Dec. on Inst.”).

¹ US Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, “Leedy ’695”).

² JP Patent Application Publication No. H8-125120, published May 17, 1996 (Ex. 1015, “Hitachi”). Petitioner has provided a certified English translation. Ex. 1015, 17.

³ T. Matsumoto, *Three-Dimensional Integration Technology Based on Wafer Bonding Technique Using Micro-Bumps*, in International Conference on Solid State Devices and Materials 1073–1074 (1995) (Ex. 1013, “Matsumoto”).

⁴ US Patent No. 5,503,704, issued Apr. 2, 1996 (Ex. 1014, “Bower”).

After institution, Patent Owner filed its Patent Owner Response on October 14, 2016 (Paper 53, “PO Resp.”) and Petitioner filed a Reply (Paper 59, “Reply”). A consolidated oral hearing was held on April 6, 2017, and a transcript of the oral hearing is of record. Paper 65 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 33 and 34 of the ’233 patent are unpatentable.

A. Related Proceedings

Petitioner indicates that the ’233 patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

Additionally, patents related to the ’233 patent are the subject of petitions filed in IPR2016-00386 (US Patent No. 8,653,672); IPR2016-00387 (US Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (US Patent No. 7,193,239); IPR2016-00390 (US Patent No. 8,629,542); IPR2016-00391 (US Patent No. 8,796,862); IPR2016-00394 (US Patent No. 8,410,617); IPR2016-00395 (US Patent No. 7,504,732); IPR2016-00687 (US Patent No. 8,928,119); IPR2016-00691 (US Patent No. 7,474,004); IPR 2016-00708 (US Patent No. 8,907,499); IPR 2016-00786 (US Patent No. 8,933,570); and IPR 2016-00770 (US Patent No. 8,907,499). Dec. on Inst. 3.

We also note that Petitioner filed two additional petitions requesting *inter partes* review of U.S. Patent No. 8,791,581 (IPR2016-00703 and IPR2016-00706) for which we did not institute a review.

B. Time Bar under 35 U.S.C. § 315(b)

In our Decision to Institute, we did not agree with Patent Owner that the Petition was barred under 35 U.S.C. § 315(b) because, according to Patent Owner, the Office lacked authority to treat certain days, on which the Office experienced an emergency situation such that many of its online and information technology systems were shut down, as federal holidays. Dec. on Inst. 3–5. Patent Owner has not raised this issue subsequent to institution in this proceeding.

C. The '233 Patent

The '233 patent is directed generally to a “[t]hree-[d]imensional [s]tructure (3DS)” for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

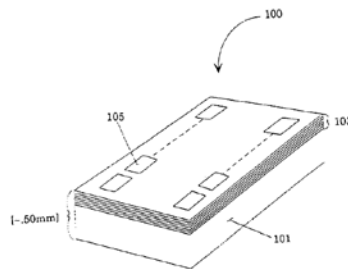


Figure 1a

Figure 1a shows 3DS memory device 100 having a stack of integrated circuit layers with a “fine-grain inter-layer vertical interconnect” between all

circuit layers. *Id.* at 4:13–17. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:33–35. The '233 patent discloses that “each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness.” *Id.* at 4:38–40. The '233 patent further discloses that the “thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm²) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication.” *Id.* at 8:61–66.

Figure 1b is reproduced below.

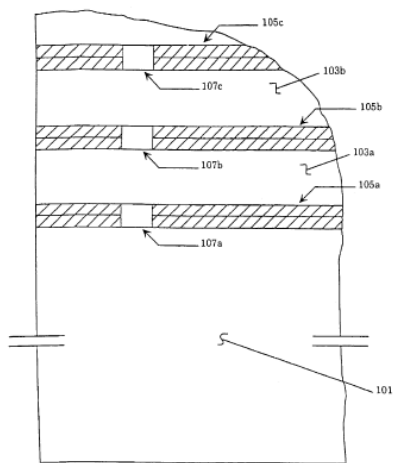


Figure 1b

Referring to Figure 1b, the '233 patent shows a cross-section of a 3DS DRAM integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:53–56. Bond and interconnect layers 105a, 105b, etc. are shown between circuit layers 103a and 103b. *Id.* at Fig. 1b. The '233 patent discloses that pattern 107a, 107b, etc. in the bond and interconnect layers 105a, 105b, etc. defines the vertical interconnect contacts between the

integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4: 27–31. Additionally, the '233 patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:31–32.

Further, the '233 patent teaches that the “term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 μm .” *Id.* at 4:16–21. The fine-grained inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:21–23.

D. Illustrative Claim

Dependent claims 33 and 34 are the challenged claims in this proceeding. Claims 33 and 34 depend from disclaimed independent claim 22, and, as such, include the limitations recited in claim 22. Thus, claims 22 and 33 are reproduced below to illustrate the subject matter of the '233 patent:

22. An integrated circuit structure comprising:

first, second, and third substrates each having integrated circuits formed thereon;

at least one of metal and non-polymeric first bonding layers on the first and second substrates, wherein the first bonding layers comprise bond-forming material on a majority of first surfaces of the first and second substrates that bonds the first and second substrates to each other; and

at least one of metal and non-polymeric second bonding layers on the second and third substrates, wherein the second bonding layers comprise bond-forming material on a majority of a second surface of the second substrate and a first surface of the third substrate that bonds the second and third substrates to each other.

33. The apparatus of claim 22, wherein the circuitry are formed with a low stress dielectric.

II. ANALYSIS

A. Claim Construction

Following institution, the parties submitted briefing regarding the claim construction standard applicable in this proceeding. Papers 21, 24, 26. Patent Owner further filed a Notice of Patent Expiration, representing that the '233 patent will not expire prior to the deadline for issuing a final written decision in this matter. Paper 22, 2.

In our Decision regarding claim construction, we determined that the broadest reasonable construction standard continues to apply to the claims at issue in the unexpired '233 patent. Paper 29, 6. Accordingly, here, we interpret claims of an unexpired patent using the “broadest reasonable construction in light of the specification of the patent in which [the claims] appear[.]” 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144 (2016) (concluding the broadest reasonable construction “regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office”).

Under this standard, we note that the Board may not “construe claims during IPR so broadly that its constructions are *unreasonable* under general claim construction principles. . . . ‘[T]he protocol of giving claims their broadest reasonable interpretation . . . does not include giving claims a legally incorrect interpretation.’” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2016). “Rather, ‘claims should always be read in light of the specification and teachings in the underlying patent’” and “[e]ven under the broadest reasonable interpretation, the Board’s

construction ‘cannot be divorced from the specification and the record evidence.’” *Id.* (citations omitted).

1. “*low stress dielectric*” (claims 33 and 34)

In the Decision on Institution, we construed “low stress dielectric” to mean a dielectric having a stress of less than 8×10^8 dynes/cm². The parties have not challenged this construction. Further, based on the complete record before us, we discern no reason to deviate from our previous determination here. For example, we note that the disclosure in the Specification of the ’233 patent is consistent with our construction, and teaches that dielectrics in low stress include those that have a stress of less than 5×10^8 dynes/cm² and “low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695.” Ex. 1001, 8:60–9:2. Looking to the disclosure of Leedy ’695, U.S. Patent No. 5,354,695, the reference teaches “[l]ow stress is defined relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being *less than 8×10^8 dynes/cm² (preferably 1×10^7 dynes/cm²) in tension.*” Ex. 1006, 11:33–37 (emphasis added).

2. “*substrate*” (claims 33 and 34)

Patent Owner asserts that the plain and ordinary meaning of the term “substrate” is “the underlying material upon which a device, circuit, or epitaxial layer is fabricated.” PO Resp. 44. According to Patent Owner, this proposed construction is consistent with the ’233 patent because the claim language recites “first, second and third substrates each having integrated circuits formed thereon.” *Id.* (citing Ex. 1001, claim 22).

In its Reply, Petitioner responds that the term “substrate” includes “all forms of structural support for integrated circuits” and should not be limited to an “underlying” structure because the embodiments disclosed in the ’233

patent include circuits formed vertically through a substrate. Reply 4–6 (citing Ex. 1001, Fig. 4, 10:11–14). Additionally, Petitioner refers to Patent Owner’s Exhibit 2146 as describing circuit components embedded within or buried under the epitaxial substrate, not just on its surface. *Id.* at 6 (citing Ex. 2146, 414, 632, 636–37, 640). Further, Petitioner asserts that Patent Owner conceded during prosecution that the term “substrate” includes the circuit membranes disclosed in Leedy ’695 (e.g., circuit membrane 160a, 160b, 160c). Reply 6. We understand Petitioner’s argument to be that Patent Owner’s statements or actions during prosecution constitute an admission that the meaning of “substrate” includes the circuit membrane described in Leedy ’695.

Based on the complete record, we adopt Patent Owner’s construction with the modification that the term “substrate” is not restricted to *underlying* structures. At the Oral Hearing, Patent Owner clarified that its proposed construction included fabricating below, above, or through a “substrate.” Tr. 65, 53:22–54:7. Patent Owner’s clarification is consistent with the disclosure in the ’233 patent, which teaches forming vertical components of circuits through substrates. Ex. 1001, 11–15.

Accordingly, under the broadest reasonable interpretation, we construe the term “substrate” to mean the “material on or in which a device, circuit, or epitaxial layer is fabricated.”

B. Grounds Under 35 U.S.C. § 103

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a

person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). 35 U.S.C. § 103. The ultimate determination of obviousness under § 103 is a question of law based on underlying factual findings. *In re Baxter Int’l, Inc.*, 678 F.3d 1357, 1362 (Fed. Cir. 2012) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966)). These underlying factual considerations consist of: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) “secondary considerations” of non-obviousness such as “commercial success, long-felt but unsolved needs, failure of others, etc.” *KSR*, 550 U.S. at 406 (quoting *Graham*, 383 U.S. at 17–18).

We analyze the asserted grounds based on obviousness with the principles identified above in mind.

2. *Level of Skill in the Art*

Petitioner’s declarant, Dr. Paul D. Franzon, testifies that a person of ordinary skill in the art at the time of the invention would have had at least a bachelor’s degree in electrical engineering, material science, or equivalent thereof, and at least 3–5 years of experience in the relevant field, e.g., semiconductor processing. Ex. 1002 ¶¶ 53–54; Pet. 12. Patent Owner does not dispute Petitioner’s assessment. See Tr. 161:21–25, 112:5–14. We adopt Petitioner’s proposed level of skill in the art, which is consistent with the ’233 patent and the asserted prior art. For example, the ’233 patent is directed to stacked integrated circuits and Leedy ’695 is directed to methods for fabricating integrated circuits from membranes formed of low stress dielectric materials. Ex. 1001, 1:23–24; Ex. 1006, Abstract.

3. Claims 33 and 34 – Obvious over Matsumoto, Bower, and Leedy '695

i. Summary of Leedy '695 (Ex. 1006)

Leedy '695 relates to the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In the Abstract, Leedy '695 indicates that the disclosed integrated circuits are fabricated from flexible membranes “formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers.” *Id.* at Abstract. Leedy '695 also discloses forming a “tensile low stress dielectric membrane” on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy '695 further defines “[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8×10^8 dynes/cm² (preferably 1×10^7 dynes/cm²) in tension.” *Id.* at 11:33–37. Additionally, Leedy '695 discloses two chemical vapor deposition (CVD) process recipes for manufacturing “structurally enhanced low stress dielectric circuit membranes.” *Id.* at 11:51–65. Referring to Figure 8, Leedy '695 discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.

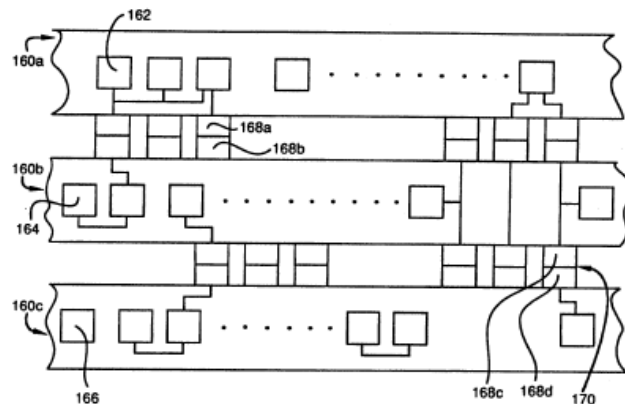


Fig_8

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 μm and 25 μm in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

ii. Summary of Matsumoto (Ex. 1013)

Matsumoto relates to three-dimensional LSI (Large Scale Integration) technology based on a wafer bonding technique using micro-bumps. Ex. 1013, 3. Figure 2 is reproduced below.

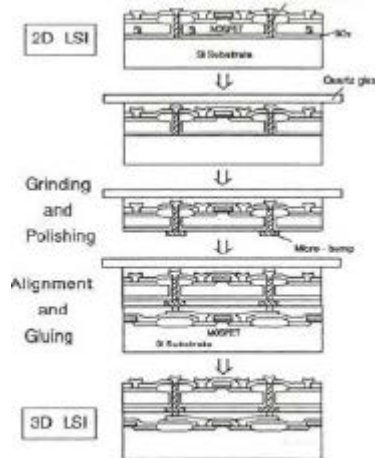


Fig.2 Fabrication sequence of 3D LSI.

Figure 2 illustrates the fabrication process sequence for fabrication of a three dimensional image processing LSI. Ex. 1013, 3. As shown in Figure 2, a 2D LSI wafer with buried interconnections is used as a starting wafer for the 3D LSI. *Id.* The buried interconnections are formed by depositing n+ poly-

Si into trenches. *Id.* The 2D LSI wafer is then glued to a quartz glass and thinned by grinding and polishing. *Id.* The thinned wafer is bonded to a thick wafer through micro-bumps and a UV hardening adhesive layer is inserted between the two wafers to enhance bonding. According to Matsumoto, “3D LSI can be fabricated by repeating such sequence.” *Id.*

iii. Summary of Bower (Ex. 1014)

Bower describes a process for direct bonding similar or dissimilar materials at low temperatures in which a material surface is rendered hydrophilic and reactive by creating nitrogen based radicals on the surface, the surface is direct bonded to a second surface. Ex. 1014, Abstract. Bower discloses bonding two surfaces by “combining a nitrogen based constituent with an activator to render a surface both hydrophilic and reactive at low temperatures.” Ex. 1014, 2:12–15. In one example, Bower discloses that “pure silicon or titanium can be rendered hydrophilic and reactive by subjecting the material to a plasma of NH_3 Once the materials are rendered hydrophilic and reactive in this manner, the materials can be brought into physical contact at room temperature to form an initial bond, and thereafter annealed at a temperature below approximately 500° C” *Id.* at 2:15–26. Bower further teaches that the described process “can be applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers.” *Id.* at 3:11–12. Bower also teaches that “organic glues and indium bumps have been used” previously, but that both have “limitations” compared to low temperature nitride bonding. *Id.* at 3:17–20.

iv. Analysis

Petitioner argues that claims 33 and 34 are obvious over the combination of Matsumoto, Bower, and Leedy ’695. *See* Pet. 3. For this

challenge, Petitioner argues that Matsumoto discloses first, second, and third substrates each having integrated circuits formed thereon. Pet. 43.

Referring to Figure 1 of Matsumoto, Petitioner argues Matsumoto discloses stacking four integrated circuit wafers to form a 3D integrated circuit structure. *Id.* (citing Ex. 1013, 1073; Ex. 1002 ¶ 124). Petitioner argues that each “2D wafer” is a substrate having integrated circuits formed thereon. *Id.*

Petitioner further argues that one of ordinary skill in the art would have been motivated to apply the direct bonding method disclosed in *Bower* to the three-dimensional image sensor device disclosed by *Matsumoto* by modifying Matsumoto’s stack “such that titanium-nitride (“TiN”) bond pads are used to form the vertical interconnection (in place of micro-bumps), and silicon nitride bonds are used to bond the remaining surfaces (in place of an adhesive layer).” Pet. 47; see *id.* at 40–41 (citing Ex. 1014, 3:11–13; 3:17–20; Ex. 1002 ¶ 109). Petitioner further notes that *Bower* discloses the “benefits of applying its direct bonding technique—the formation of a strong bond at low temperature—to the integration of electronic circuitry.” Pet. 41 (citing Ex. 1014, 1:64–67).

Additionally, Petitioner argues that the combination of Matsumoto, *Bower*, and Leedy ’695 discloses that “the circuitry are formed with a low stress dielectric” limitation recited in claim 33, and “the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have a stress of about 5×10^8 dynes/cm² or less” limitation recited in claim 34 (which depends from claim 33). Pet. 52–57. With respect to these limitations, Petitioner acknowledges that neither Matsumoto nor *Bower* discloses a low stress dielectric. Pet. 56. However, Petitioner argues

Matsumoto discloses the use of a dielectric layer in forming its

integrated circuit. *See* Ex. 1013 at 1073 (“The buried interconnections are formed by depositing n+ poly-Si into trenches which are formed through the field oxide.”); Fig. 2; Ex. 1002 at ¶127. This is one of two types of “low stress dielectric” described in the ’233 Patent. *See* Ex. 1001 at 8:61-9:2 (describing silicon dioxide). Similarly, Bower also discloses the use of a silicon nitride dielectric layer overlying at least the first substrate. *See* Ex. 1014 at 3:21-28; Ex. 1002 at ¶127. This is the second of the two types of “low stress dielectric” described in the ’233 Patent. *See* Ex. 1001 at 8:61-9:2 (silicon nitride).

Id. Further, Petitioner argues that there are several reasons one of ordinary skill in the art would have combined the references with a reasonable expectation of success of achieving the claimed inventions recited in claims 33 and 34. *Id.* at 52–57.

For the reasons that follow, we determine that Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have had a reason to combine the references in the manner proposed by Petitioner to arrive at the claimed invention, or would have had a reasonable expectation of success.

1. Reason to Substitute

To start, Petitioner contends that the Office has previously found that Leedy ’695 discloses the subject matter of claims 33 and 34, and that Patent Owner (Applicant at the time) did not dispute the Examiner’s findings. Pet. 56–57 (citing Ex. 1017, 690, 709–712, 728, 739–760, 782–784, 979–980). Petitioner, however, does not acknowledge, much less address adequately, the significant difference in the record before the Office, which lacked the testimonial evidence of the Petitioner’s expert, Paul D. Franzon, Ph.D. (Ex. 1002 (declaration); Ex. 2164 (deposition transcript)) and testimonial evidence of Patent Owner’s expert, Alexander D. Glew, Ph.D. (Ex. 2166

(declaration)). Thus, we are not persuaded that the relied upon sections of the prosecution history are controlling in this instance.

Next, Petitioner refers to many general benefits and advantages of Leedy '695's disclosed dielectric, but does not explain how these advantages apply to the specific dielectric materials of Matsumoto or Bower. For example, Petitioner asserts that

having a low tensile stress dielectric layer in a stacked integrated circuit device allows the layer “to withstand a wide range of IC processing techniques and processing temperatures ... without noticeable deficiency in performance.” Ex. 1006 at 2:37-40. *Leedy* '695 explains the alleged importance of having low tensile stress as follows: “If the membrane is not in tensile stress, but in compressive stress, surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane.” *Id.* at 5:63-6:5; Ex. 1002 at ¶95. Thus, in light of the potential benefits disclosed by *Leedy* '695—including improved surface flatness, improved ability to cope with subsequent high-temperature processing steps, lower dielectric film stress, and improved structural integrity—a person of ordinary skill in the art would have been motivated to apply the low-stress dielectric deposition techniques disclosed in *Leedy* '695 to manufacture the stacked integrated circuit structures disclosed in *Matsumoto* and *Bower*. See Ex. 1002 at ¶95.

Pet. 53.

We first observe that Petitioner incorrectly attributes benefits of the entire Membrane Dielectric Isolation (MDI) process to the single low stress dielectric component. Pet. 53 (citing Ex. 1006, 2:37–40, 5:63–6:5). Column 2, lines 37 through 40 of *Leedy* '695, which is cited on page 53 of Petition, provides the “[flexible thin film free standing dielectric] *membrane* is able to withstand a wide range of IC processing techniques and processing

temperatures (of at least 400° C.) without noticeable deficiency in performance.” Emphasis added. Further, column 5, line 63 through column 6, line 5 states that

[t]here are many established methods for forming thin semiconductor substrates or membranes. The MDI process requires that the semiconductor membrane forming process (thinning process) produce a highly uniform membrane typically less than 2 μm thick and that the surface tension of the semiconductor membrane be in low tensile stress. If the *membrane* is not in tensile stress, but in compressive stress, surface flatness and *membrane* structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing *membrane*.

Emphasis Added. Here, Leedy '695 indicates explicitly that the ability to withstand high temperature processes is attributed to the *membrane* and not solely to the dielectric that is a component of the membrane. Ex. 1006, 2:37–40. Similarly, Leedy '695 advises that if the *membrane* is in compressive stress, surface flatness and *membrane* structural integrity will be inadequate. Thus, the probative value of Petitioner's argument is diminished because these cited sections of Leedy '695 do not support Petitioner's position that the low stress dielectric imparts the advantages attributed to the membrane structure or membrane isolation techniques.

We further observe that paragraph 95 of Dr. Franzon's testimony largely mirrors the Petition, but adds the following:

It is worth noting that Matsumoto shows that the ID-VD characteristics of MOS transistor were slightly different after stacking compared with before stacking. *See id.* at Fig. 8. Although the authors do not discuss why, one possible reason is the changed transistor channel strain caused by the stress being different after bonding as compared with before. One possible solution might have been to implement the low-stress dielectric

deposition technique disclosed by Leedy '695 to the stacked integrated circuit structures disclosed in Matsumoto.

Ex. 1002 ¶ 95. Here, Dr. Franzon's testimony does not cite to Matsumoto or any other source that supports this opinion. Even in referring to Figure 8 in Matsumoto, Dr. Franzon acknowledges that Matsumoto does not disclose why the ID-VD characteristics of MOS transistors were shown to be slightly different, or that this is a problem. Dr. Franzon speculates that the difference could be attributed to strain that possibly could be resolved by a low stress dielectric, but does not explain how strain contributes to the ID-VD difference, and, more importantly, why and how one of ordinary skill in the art would have viewed the low stress dielectric deposition technique in Leedy '695 as a solution to this potential problem. Thus, in this regard, we determine Dr. Franzon's testimony is entitled little weight. *See In re Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); *see also* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

Further, even assuming that Dr. Franzon is correct in his assessment, we note that Petitioner did not present these arguments in its Petition, and we decline to adopt these arguments on behalf of the Petitioner. *In re Magnum Oil*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (indicating that the Board is not free "to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR. Instead, the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.").

Additionally, Petitioner's reliance on express reasons that low tensile stress is important for Leedy '695's process for constructing Leedy '695's low tensile stress dielectric membranes (e.g., surface flatness) has minimal probative value in supporting Petitioner's proposed substitution with Matsumoto, which is fabricated in a different process relying on a conventional, rigid substrate. *See* Ex. 1013, Figure 2. This is because Petitioner does not explain sufficiently why or how the importance of low tensile stress for Leedy '695's process for constructing low tensile stress dielectric membranes bears on why one of ordinary skill in the art would have substituted Leedy '695's dielectric material for the purported dielectric layer in Matsumoto. For example, Petitioner does not argue that Matsumoto's dielectric layer experiences surface flatness or other structural problems that would be improved by the use of a low stress dielectric, or how this substitution would be accomplished in light of the fabrication processes disclosed in Leedy '695. *See* Pet. 53–57.

Petitioner also does not explain why or how the importance of low tensile stress in Leedy '695's process bears on why one of ordinary skill in the art would have substituted a low stress dielectric for the bonding material in Bower. *See* Pet. 55 (“Bower also discloses the use of a silicon nitride dielectric layer overlying at least the first substrate. *See* Ex. 1014 at 3:21-28; Ex. 1002 at ¶127.”). Indeed, other than relying on the '233 patent's mention of a silicon nitride dielectric, (Pet. 55), Petitioner does not explain how the Bower bonding layer performs as a dielectric material. According to Petitioner:

Bower discloses methods of directly bonding two wafers by “combining a nitrogen based constituent with an activator to render a surface both hydrophilic and reactive at low

temperatures.” Ex. 1014 at 2:12-15. Under this approach, a non-polymeric bond-forming material would cover the entire surface of an integrated circuit chip or wafer. *See id.*; Ex. 1002 at ¶¶102, 124. Specifically, *Bower* discloses that its direct bonding method that “can be applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers” to replace conventional bonding through “organic glues and indium bumps” to produce a “clean, low temperature” bond that is superior to the bond formed by conventional processes. *See* Ex. 1014 at 3:11-20; Ex. 1002 at ¶109.

Pet. 49.

Nonetheless, turning to column 3, lines 21 through 28, we observe that *Bower* teaches that TiN complements Si₃N₄ to provide both insulating and conducting surfaces which can be bonded at low temperatures. Even assuming the silicon nitride disclosed has insulating or dielectric properties, Petitioner has failed to explain why one of ordinary skill in the art would have replaced the silicon nitride insulating bonding material described in *Bower* with Leedy ’695’s low stress dielectric. For example, Petitioner does not point to any evidence in the record that demonstrates Leedy ’695’s low stress dielectric material performs any bonding, or that *Bower*’s bonding layer exhibits structural problems that would be improved by the use of a low stress dielectric such as one fabricated by the MDI processes disclosed in Leedy ’695.

Petitioner further argues that replacement of one dielectric for another is a matter of simple substitution because the deposition processes disclosed in *Bower* and Leedy ’695 are compatible with each other. Pet. 54 (citing Ex. 1002 ¶ 98). Petitioner additionally asserts that

each of *Matsumoto*, *Bower*, and *Leedy* ’695 discloses a stacked integrated circuit device. *See* Ex. 1013 at 1073; Ex. 1014 at 3:11-20; Ex. 1006 at 45:49-53; Ex. 1002 at ¶97. Thus, a person of ordinary skill in the art would have found it obvious to

combine *Leedy '695* with *Matsumoto* and *Bower* because they are in the same field of technology and attempt to address the same problem of vertically integrating integrated circuit devices. See Ex. 1002 at ¶97.

Pet. 54. Dr. Franzon adds that a person of skill in the art would have been motivated to combine *Leedy '695* and *Bower* because *Leedy '695* uses anodic bonding to form a 3D structure and *Bower* discloses bonding of Nitride at a lower temperature. Ex. 1002 ¶ 98.

On this point, Petitioner essentially argues that *Matsumoto*, *Bower*, and *Leedy '695* were directed generally to similar structures and problems in the semiconductor fabrication arts, and a skilled artisan could have looked at both references to improve upon fabrication processes that are *compatible*. In this regard, we find that Petitioner's "reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they *could* be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention." *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017). While the references need not explicitly provide a reason for the asserted substitution, Petitioner, nevertheless, must explain why a person of ordinary skill in the art would have substituted *Leedy '695*'s low stress dielectric for the specific dielectrics in *Matsumoto* and *Bower*. "[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015).

We recognize that “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill” (*KSR*, 550 U.S. at 417). Here, however, Petitioner’s testimony is conclusory without explaining what types of problems or improvements in “vertically integrating integrated circuit devices” would have motivated one of ordinary skill in the art to make Petitioner’s proposed substitution of Leedy ’695’s dielectric in Matsumoto or Bower’s devices. *In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) (“The factual inquiry whether to combine references must be thorough and searching.”)). Further, Petitioner does not explain in the Petition what aspects of Leedy ’695’s process and Bower’s process lends support to the conclusion that these processes are compatible, and how that alleged compatibility would have motivated a substitution of Leedy ’695 low stress dielectric for the bonding material in Bower.

Moreover, here, too, the probative value of Petitioner’s argument is diminished by Petitioner’s reliance on Dr. Franzon’s testimony in paragraphs 97 and 98 of his declaration. Petitioner cites to paragraph 97 of Dr. Franzon’s declaration testimony without further discussing or explaining the relevance of the testimony. Pet. 54 (citing Ex. 1002 ¶ 97). In paragraph 97, Dr. Franzon asserts that

Leedy ’695, Matsumoto, and Bower each discloses a stacked integrated circuit structure, and are all in the same technology field of three-dimensional integration and address similar challenges relating to the stacking of integrated circuit devices.

Accordingly, applying the process methods disclosed by Leedy '695 to Matsumoto and Bower merely involves the substitution of the Leedy '695 low-stress dielectric film for the dielectric films disclosed by Matsumoto and Bower, which would have yielded predictable results.

Ex. 1002 ¶ 97. Although “any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed” (*KSR*, 550 U.S. at 420), Dr. Franzon’s two sentence conclusory assertions lack specifics as to what those similar challenges are, and fail to provide any citations to the references themselves or explanation and analysis as to how these references support his assertions. Thus, we weigh Dr. Franzon’s testimony accordingly. *See In re Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) (“[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.”); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Further, in paragraph 68, Dr. Franzon testifies that “[g]iven that Bower discloses bonding of Nitride at lower temperatures than Leedy '695 and that Leedy '695 discloses a low-stress Silicon Nitride recipe, a person of skill in the art would have been motivated to combine their teachings.” Ex. 1002 ¶ 98. Here, essentially Dr. Franzon asserts that Bower’s nitride layer to nitride layer bonding process occurs at a lower temperature than Leedy '695’s silicon nitride deposition process. *Id.* Even assuming that to be the case, we do not see where in this cited testimony that Dr. Franzon explains why one of skill in the art would have substituted Leedy '695’s low stress silicon nitride dielectric for the bonding material in Bower. Rather, Dr.

Franzon argues, as Petitioner does, that Leedy '695 discloses a “recipe” that could be used in Bower to form a nitride layer in Bower. *Id.* Again, testimony that one of ordinary skill in the art *could have used* the techniques is not sufficient to support Petitioner’s contention that one of ordinary skill in the art would have had a reason to combine the references as proposed by Petitioner in the manner of the claimed invention. *In re Giannelli*, 739 F.3d 1375, 1380 (Fed. Cir. 2014) (indicating that the Board should have determined whether it would have been obvious to modify the prior art apparatus to arrive at the claimed invention and finding the mere capability to do so insufficient).

In Reply, Petitioner contends, without support of expert or citation to law, that “the lack of disclosure of ‘tensile’ dielectrics or how to make a [low tensile stress dielectric, aside from incorporating a § 102(b) reference, indicates that it was trivial to substitute Leedy '695’s [low tensile stress dielectrics] in place of other dielectrics. Reply 2. We disagree with Petitioner—one does not necessarily follow from the other.

Similarly, we disagree that the record supports Petitioner’s assertions in its Reply that the specific benefits of (1) enhancing structural integrity and surface flatness of stacked circuit structures (Pet. 53; Ex. 1002 ¶¶ 95, 121⁵; (2) reducing likelihood of heat damage (Pet. 53; Ex. 1002 ¶¶ 95–96); and (3) providing a dielectric that can withstand heat from subsequent processing (Pet. 53; Ex. 1002 ¶¶ 95–96) would have motivated the proposed substitution. As discussed above, Petitioner relies on benefits that Leedy '695 attributes to the entire *membrane* or membrane fabrication process, not

⁵ Paragraph 121 of Dr. Franzon is directed to the combination of Leedy '695 and Hitachi.

to the dielectric alone. *See* Ex. 1002 ¶ 95; *see also* Ex. 1006, 2:9–31, 2:37–40 (“This *membrane* is able to withstand a wide range of IC processing techniques and processing temperatures (of at least 400° C.) without noticeable deficiency in performance.”), 3:56–4:13 ((Listing benefits to fabricating an IC with the MDI process), 5:63–6:5 (“If the *membrane* is not in tensile stress, but in compressive stress, surface flatness and *membrane* structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane.”), 6:48–58 (“The ability to form large durable temperature tolerant low tensile stress films of both semiconductor and dielectric materials as components or layers of a substrate for the fabrication of integrated circuits and interconnect structures is unique to the *MDI process*. The large free standing semiconductor and dielectric *membrane* substrates of the *MDI process* provide unique structural advantages to lower the cost and complexity of circuit fabrication and enhance the performance of circuit operation.”). Accordingly, we determine Petitioner’s conclusory assertions in its Reply are insufficient to overcome Patent Owner’s well-reasoned and supported arguments.

2. *Expected Success*

In addition, it is Petitioner’s burden to demonstrate both “that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *Intelligent Bio-Systems, Inc. v. Illumina Cambridge LTD.*, 821 F.3d 1359, 1368–1369 (Fed. Cir. 2016) (citing *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.* 688 F.3d 1342, 1360 (Fed. Cir. 2012)).

In considering the record before us, we take into account the complexity of integrated circuit fabrication. Without question, fabrication of integrated circuits is complex technology. No less than four prior art text books, ranging from 600 pages to nearly 850 pages and describing the fabrication of integrated circuits, have been provided as background references, principally in support of the declaration testimony of Alexander D. Glew, Ph.D., Patent Owner's expert. Ex. 1040 (Wolf et al., *Processing for the VLSI Era, Volume 1–Process Technology* (1986)); Ex. 2146 (Wolf, *Silicon Processing for the VLSI Era, Volume 2 – Process Integration* (1990)); Ex. 2159 (W. R. Runyan & K. E. Bean, *Semiconductor Integrated Circuit Processing Technology* (1990)); Ex. 2162 (Multi-Chip Module Technologies and Alternatives: The Basics (Daryl Ann Doane & Paul D. Franzon eds., 1993)). Also of record are two other background references of around 100 pages and 650 pages. Ex. 2169 (*Handbook of Semiconductor Manufacturing Technology* (Robert Doering & Yoshio Nishi eds., 2nd ed. 2008)); Ex. 2158 (Peter van Zant, *Microchip Fabrication* (4th ed., 2000)).

Patent Owner, with liberal citations to those references, other prior art references, and declaration testimony of its expert explaining the same, explains how integrated circuits are fabricated to illustrate the complexity of the process and the detailed planning and decisions required for fabrication. PO Resp. 2–29. According to Dr. Glew, integrated circuit fabrication is a “complex manufacturing process . . . that can be generally divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer

fabrication; and (4) packaging. Ex. 2166 ¶ 23 (citing Ex. 2158, 13^{6,7}); *see also* PO Resp. 5 (citing Ex. 2166 ¶ 23; Ex. 2158, 13). In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and then sliced into thin disks called “wafers.” PO Resp. 4 (citing Ex. 2166 ¶ 25; Ex. 2158, 13–14). Most helpful is the explanation of different techniques for producing and layering dielectrics (PO Resp. 15–29), including growing dielectrics using thermal oxidation (PO Resp. 17–18), depositing dielectrics (PO Resp. 18–19), and a comparison of thermal chemical vapor deposition (PO Resp. 19) with plasma-enhanced chemical vapor deposition (PO Resp. 20–21).

We understand from the testimony of Dr. Glew and reference citations that a typical fabrication of a semiconductor integrated circuit may include thousands of process steps (Ex. 2166 ¶¶ 29–30 (citing Ex. 2158, 14, 29–31, 71)). Explaining different techniques for producing and layering dielectrics, Dr. Glew explains that “different dielectric materials are layered throughout the fabrication process, with each dielectric layer having a different location, each being created at a different stage, and each serving a different specific

⁶ We follow Patent Owner’s practice of citing to page numbers of the text, rather than the pagination of Exhibit 2158.

⁷ We recognize that the text cited by Dr. Glew (Ex. 2158) is the fourth edition and has publication dates of 1984, 1997, and 2000. Dr. Glew relies on this text as supporting his testimony and recognizes the earliest effective filing date claimed by the challenged patent of April 4, 1997. Ex. 2166 ¶ 104. Petitioner does not contend that Dr. Glew’s reliance on this text is in error or that Dr. Glew’s summary of integrated circuit fabrication is faulty. Nor does Petitioner contend that the general explanation of integrated circuit fabrication found in the text, and used by Dr. Glew to support his testimony, changed between the 1997 edition of the text and the later editions.

purpose.” Ex. 2166 ¶ 61 (citing Ex. 2158, 72–73, 79, 81–82); *see generally* PO Resp. 15–29 (discussing different techniques for producing and layering dielectrics). Dr. Glew continues:

These dielectrics can be produced and layered using a large number of techniques, and the particular technique used will greatly impact the properties of the resulting dielectric (and, therefore, its usefulness for any particular dielectric layer and purpose). For example, dielectric silicon dioxide layers can be produced and applied in hundreds of different ways, each resulting in a silicon dioxide with different properties (and potential uses). (Ex. 2158 at 154; Ex. 2146 at 225, 306; Ex. 2159 at 55).

Ex. 2166 ¶ 62. Thus, selecting a dielectric material involves choosing particular fabrication techniques that are part of an overall fabrication process for a particular integrated circuit.

Turning again to the Petition, Petitioner asserts that

Leedy ’695 discloses fabrication techniques for low-stress dielectric films that are compatible with “most of the established integrated processing methods for the fabrication of circuit devices and interconnect metallization.” Ex. 1006 at 1:50-52. *Leedy* ’695 provides two process recipes for depositing low stress silicon dioxide and silicon nitride films using Novellus deposition equipment, a common tool in the semiconductor fabrication industry around the priority date of the ’233 patent. *See id.* at 11:51-65; Ex. 1002 at ¶96. Thus, a person of ordinary skill in the art would have reasonably expected success from applying the known deposition recipes disclosed in *Leedy* ’695 to manufacture the stacked integrated circuit structure disclosed in *Matsumoto* and *Bower*. *See id.*

Pet. 54.

Based on the complete record, we determine that Petitioner’s arguments and conclusion are insufficiently supported. The fact that *Leedy* ’695 discloses fabrication for low stress dielectric films using Novellus

deposition equipment does not sufficiently support Petitioner’s conclusion in view of the complexities of integrated circuit fabrication. Furthermore, Petitioner’s assertion that a person of ordinary skill in the art “would have reasonably expected success from applying the known deposition recipes disclosed in *Leedy* ’695 to manufacture the stacked integrated circuit structure disclosed in Matsumoto and Bower” is not supported by the record. Petitioner’s citations to *Leedy* ’695 (Ex. 1006, 1:50–52, 11:51–65) do not on their face, without explanation, support Petitioner’s position.

Petitioner’s citation to column 1 indicates: “[t]hese membranes permit the application (continued use) of most of the established integrated processing methods for the fabrication of circuit devices and interconnect metallization.” Ex. 1006, 1:50–52. In the preceding sentence, *Leedy* ’695 refers to “these membranes,” discussed in lines 50 through 52, as “large area free standing membranes . . . [fabricated] from low stress dielectric and/or semiconductor films.” *Id.* at 1:44–49. As such, *Leedy* ’695’s statements apply to the *free standing membrane*, not solely to the dielectric layer within the *membrane*. At a minimum, Petitioner’s reliance on this cited passage requires additional explanation on how this teaching demonstrates one of ordinary skill in the art would have reasonably expected success from the substitution of only the dielectric material from *Leedy* ’695’s membrane in Matsumoto’s and Bower’s structures (e.g., nitride bonding layer).

Petitioner’s citation to column 11 similarly requires further explanation regarding how it supports Petitioner’s position. Column 11, lines 51 through 65 teach “recipes” for silicon dioxide and silicon nitride. In doing so, *Leedy* ’695 cautions that “[s]mall variations in the parameters of the recipes can produce changes in the material structure, etch rate,

refractive index, surface stress, or other characteristics of the deposited dielectric material.”). Ex. 1006, 11:46–50. Thus, while Leedy ’695 provides recipes for dielectric material for use in its MDI process, Leedy ’695 acknowledges that even small changes to these recipes will change the character of the resulting dielectric. *Id.* This teaching is consistent with the testimony provided by both experts, which weighs against Petitioner’s conclusion that replacing dielectrics in integrated circuit fabrication is a matter of simple substitution.

Specifically, both Dr. Franzon and Dr. Glew agree that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties. *See, e.g.*, Ex. 2164 (Dr. Franzon deposition transcript), 69:17–19 (Q. Do the different methods result in different properties of the dielectrics? A. Yes.”); Ex. 2166 (Dr. Glew’s declaration) ¶ 139 (Identifying eighteen properties⁸ of dielectrics; testifying that one of ordinary skill in the art would consider many of those factors when choosing a dielectric); *see also* PO Resp. 60–63 (discussing Dr. Franzon’s and Dr. Glew’s testimony); *see also* Ex. 2146 (Wolf Volume 2), 195 (Table 4.4 listing eighteen desired properties of interlevel dielectrics); PO Resp. 28 (citing Ex. 2146, 195); Tr. 125:12–17

⁸ Dr. Glew identifies the following properties of dielectrics: dielectric constant, breakdown of field strength, leakage, surface conductance, moisture absorption or permeability to moisture, stress, adhesion to aluminum, adhesion to other dielectric layers, stability, etch rate, permeability to hydrogen, amount of incorporated electrical charge or dipoles, amount of impurities, quality of step coverage, thickness and uniformity of the film, ability to provide good doped uniformity across a wafer, defect density, and amount of residual constituents that “outgas” during later processing. Ex. 2166 ¶ 139.

(Patent Owner's counsel referencing Ex. 2146, 195 (table of eighteen properties). Dr. Franzon acknowledges dielectric properties should be considered when selecting a dielectric. Ex. 2164 (Dr. Franzon deposition transcript), 59:25–60:2, 61:10–13, 79:25–80:3, 91:8–12); Ex. 2164, 78:23–79:1 (Dr. Franzon testifies that “[t]here is likely quite a long list of factors that go into choosing between them [dielectrics], and an engineer would weigh those using his knowledge and skills.”). This weighs against a finding that one of ordinary skill in the art would have had expected success substituting Leedy '695's low tensile stress dielectric material for Matsumoto's or Bower's dielectric materials.

In reviewing Dr. Franzon's testimony, we are mindful of the sentiment that “[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton.” *KSR*, 550 U.S. at 421. However, in his deposition, Dr. Franzon responded to many questions about dielectrics by indicating research would be needed to answer the particular question and he did not consider how the different processes would affect dielectric properties, which weighs against a finding that one of ordinary skill would have a reasonable expectation of success in substituting Leedy '695's dielectric. See Ex. 2164, 133:5–135:5. For example, an excerpt of Dr. Franzon's testimony is provided below:

Q. What are some of the differences in the properties of a silicon dioxide grown through plasma-enhanced CVD as opposed to grown through oxidation?

A. I haven't researched a detailed answer to that question. There is many variations on the formulas for these CVDs.

Q. But you understand that there is a difference. Right?

THE WITNESS: There may be differences, depending on the details of the formulations and the processing parameters and so forth.

Q. What are some of the details of the formulation parameters that you would need to know in order to answer that question?

A. I haven't researched the answer to that question in general, so I would need a variety of references that I can't anticipate in order to properly answer that question.

Ex. 2164, 133:8–134:3; *see, e.g.*, Ex. 2164, 71:9–73:17 (“Q. Do you consider oxidation to be a growth or a deposition? A. I haven't researched that answer to the question. Thermal oxidation [requires] oxygen atoms in contact with the surface, at least, in order to grow the thermal oxide. But there's a lot of variance on thermal oxide techniques that I haven't researched. Q. And can you give me an example of some variants in thermal oxide techniques? A. One example that comes to mind is a wet oxide deposition versus a dryer one. Q: And does a wet oxide deposition versus a drier one cause different arrangements of the bonds in silicon dioxide? A: I haven't researched the answer to that question. . . . Q: Do you know if wet oxide versus dry oxide would affect the dielectric constant of silicon dioxide? A. I haven't researched the answer to that question. Q. Do you know if PDCVD [sic] would result in a different dielectric constant than thermal oxide? A. I haven't researched the answer to that question.”).

We are not suggesting that a reasonable expectation of success in the complex field of integrated circuit fabrication would preclude one of ordinary skill in the art from researching aspects of making the combination. Rather, we find the number of Dr. Franzon's responses that research is required weighs against Petitioner's conclusory assertions in this regard,

which were discussed previously. *See, e.g.*, Ex. 2164, 71:9–73:17, 73:18–74:4, 24:6–22, 65:10–14, 129:7–9, 130:17–25, 134:20–25; Pet. 52–55.

Thus, considering the complex field of integrated circuit fabrication and taking into account the level of ordinary skill in that art as set forth by Petitioner, there is insufficient evidence of record to conclude that ordinary creativity would support a conclusion that one of ordinary skill in the art would have reasonably expected success in substituting Leedy '695's dielectric material for Matsumoto's or Bower's purported dielectrics.

3. Expert Testimony

In general, we weigh Dr. Glew's testimony concerning the reasons why one of ordinary skill in the art would not have had reason to combine these references in the manner proposed by Petitioner more heavily than Dr. Franzon's declaration testimony that one of ordinary skill in the art would have done so and would have had an expectation of success.

Dr. Franzon's testimony, in large measure, is that Leedy '695 identifies advantages of "the disclosed dielectric deposition techniques (Ex. 1002 ¶ 95); that Leedy '695 discloses dielectric deposition processes that are compatible with conventional integrated circuit fabrication methods (*id.* at ¶¶ 96, 98); and all three references are in the same technological field and "address similar challenges relating to the stacking of integrated circuit devices" (*id.* at ¶ 97). Pet. 52–55. Dr. Franzon's testimony, however, does not adequately address why one of ordinary skill in the art would have specifically used Leedy '695's fabrication process to make Matsumoto or Bower's structures with Leedy '695's low tensile stress dielectric as a dielectric layer or bonding nitride layer, which is the combination on which

Petitioner relies for the recited dielectric material characterized by the particular tensile stress claimed. *See id.*

Notably, too, Dr. Franzon does not specify or otherwise explain the “similar challenges relating to the stacking of integrated circuit devices” he refers to in his testimony. Ex. 1002 ¶ 97. We, however, recognize that “any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *KSR*, 550 U.S. at 420. Noting, however, that references are in the same general field and address similar unnamed challenges in the circumstances of this case—involving complex technology of integrated circuit fabrication, we conclude that Dr. Franzon’s testimony about the benefits of Leedy ’695’s general process is insufficient to support Petitioner’s position regarding dielectric substitution of particular structures in Matsumoto and Bower. *See In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) (“The factual inquiry whether to combine references must be thorough and searching.”)); *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014) (“While an analysis of any teaching, suggestion, or motivation to combine elements from different prior art references is useful in an obviousness analysis, the overall inquiry must be expansive and flexible.”).

In contrast, Patent Owner relies on Dr. Glew’s testimony, which is specific as to reasons why one of ordinary skill in the art would not have combined Leedy ’695’s fabrication process to modify Matsumoto’s or Bower’s structures. Specifically, for example, Patent Owner relies on

Dr. Glew’s testimony that Matsumoto’s silicon dioxide field oxide is grown directly on the Si Substrate at high temperatures using thermal oxidation and could not be produced using plasma-enhanced chemical vapor deposition used by Leedy ’695. PO Resp. 49–52; Ex. 2166 ¶¶ 127–128. Dr. Glew further testified that one of ordinary skill in the art would understand that Matsumoto’s silicon dioxide dielectric could not be deposited using plasma-enhanced chemical vapor deposition described by Leedy ’695 “because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining . . . steps^[9] without changing its form.” Ex. 2166 ¶ 130 (citing Ex. 2169, 29–30). Notably, Dr. Glew testifies that plasma-enhanced chemical vapor deposition (a known technique used by Leedy ’695) cannot be used with Matsumoto’s techniques because “positive ions present in the plasma can strike and damage the wafer and the exposed active components in and on its surface.” Ex. 2166 ¶ 140 (citing Ex. 2159, 139).

We also note the absence of further declaration testimony by Dr. Franzon opposing Dr. Glew’s position or otherwise supporting Petitioner’s Reply to Patent Owner’s Response. For the reasons noted previously, because of the complexity of integrated circuit fabrication, expert testimony is critical to explaining why a reason one of ordinary skill

⁹ Petitioner and Patent Owner dispute what is meant by front-end and back-end processing steps, we are not persuaded that resolving this issue is necessary to determine whether a skilled artisan would have had reason to combine the asserted references in the manner proposed by Petitioner to arrive at the claimed invention, and whether one of ordinary skill in the art would have had a reasonable expectation of success of doing so.

in the art would have had a reason to combine the references as the claims require. *Kinetic Concepts*, 688 F.3d at 1369. This is particularly true in view of Dr. Glew’s well-reasoned and supported testimony. Petitioner’s attorney-argument in its Reply consists of conclusory statements with insufficiently explained citations to Leedy ’695 and other references and is insufficient to establish that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner. *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (a petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements”).

For example, in Reply to Dr. Glew’s testimony supporting Patent Owner Response, Petitioner’s attorneys assert that plasma-enhanced chemical vapor deposition dielectrics are compatible with silicon substrates and high temperature processes. Reply 18–23 (citing Ex. 1082, 1006, 1088)). We recognize that sometimes expert testimony is not always necessary. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1369 (Fed. Cir. 2012) (indicating expert technology is not always required) (citing *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1240 n.5 (Fed. Cir. 2010) (“However, as we [have] noted . . . ‘expert testimony regarding matters beyond the comprehension of layperson is sometimes essential,’ particularly in cases involving complex technology. In such cases, expert testimony may be critical, for example, to establish . . . the existence (or lack thereof) of a motivation to combine references.” (internal citations omitted)) (alteration in original)). Accordingly, because of the complexity of integrated circuit fabrication discussed above, however, attorney-argument addressing Dr. Glew’s well-reasoned and supported testimony does not

persuade us that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner or would have had a reasonable expectation of success.

4. Conclusion

As described above, Petitioner in its Petition made arguments as to why one of ordinary skill in the art would be motivated to combine Matsumoto, Bower, with Leedy '695 to achieve the purported claimed invention and would have had a reasonable expectation of success. Patent Owner provided well-reasoned argument based on testimonial evidence, background references, and prior art references identifying shortcomings in Petitioner's position. There is evidence from both sides regarding the presence or absence of a reason to combine Matsumoto, Bower, and Leedy '695 in the manner proposed by Petitioner to arrive at the claimed invention and regarding whether one of ordinary skill in the art would have had a reasonable expectation of success.

Here, Petitioner has the burden to show, by a preponderance of the evidence, a reason why one of ordinary skill in the art would have combined the prior art references to arrive at the invention and why one of ordinary skill in the art would have reasonable expectation of success of combining the references to meet the limitations of the claimed invention. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) ("The reasonable expectation of success requirement refers to the likelihood of success in combining the references to meet the limitations of the claimed invention. . . . [O]ne must have a motivation to combine [the references] accompanied by a reasonable expectation of achieving what is claimed in the

patent-at-issue.”). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)).

It is well-settled that identifying a reason to combine references is not confined to a “rigid or mandatory formula[.]” *KSR*, 550 U.S. at 419; see *In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016). Moreover, “[w]hile an analysis of any teaching, suggestion, or motivation to combine elements from different prior art references is useful in an obviousness analysis, the overall inquiry must be expansive and flexible.” *InTouch Techns., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014). Furthermore, the inquiry cannot be met by conclusory statements but rather must be “thorough and searching.” See *In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) (“The factual inquiry whether to combine references must be thorough and searching.”)). Additionally, we must be careful not to allow hindsight reconstruction of references to reach the claimed invention without adequate explanation as to how or why the references would be combined to produce the claimed invention. See, e.g., *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368 (Fed. Cir. 2012) (quoting *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 n.3 (“We must still be careful not to allow hindsight reconstruction of the references to reach the claimed

invention without any explanation as to how or why the references would be combined to produce the claimed invention.”)).

We find Petitioner’s arguments regarding its proposed combination to be incomplete. In the context of these cases, it is insufficient to propose incorporating “the material” of Leedy ’695 without providing sufficient detail as to the combined process to produce the claimed combination. We recognize that it is axiomatic that bodily incorporation is not required. *See, e.g., In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (“It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of the elements.”). To be clear, we are not suggesting that Petitioner must explain how Leedy ’695’s entire membrane dielectric isolation process would or could be included with Matsumoto’s or Bower’s integrated circuit fabrication process. Rather, we find Petitioner’s explanation to be incomplete because it does not adequately explain how Matsumoto’s (or Bower’s) fabrication process would be changed to use Leedy ’695’s dielectric material, which is formed in a different manner than Leedy ’695’s MDI (membrane dielectric isolation) process. This is necessary, at least, to support a conclusion that one of ordinary skill in the art would have had a reasonable expectation of success of using Leedy ’695’s dielectric material in place of purported dielectric material in Matsumoto or Bower.

For these reasons above, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the challenged claims 33 and 34 are unpatentable over the combination of Matsumoto, Bower, and Leedy ’695.

4. Claims 33 and 34 – Obvious over Leedy '695 and Hitachi

i. Summary of Hitachi (Ex. 1015)

Hitachi “pertains to a semiconductor device suitable to achieve a highly reliable three-dimensional LSI having extremely high integration density.” Ex. 1007 ¶ 1. As an example of a “LSI,” Hitachi refers to Figure 5 (reproduced below) as showing three-dimensional LSI 21 with eight layers of thin film 19 laminated via connection surface terminals 20. *Id.* ¶ 35.

[FIG. 5]

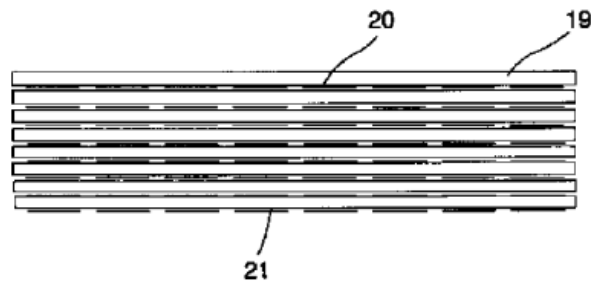
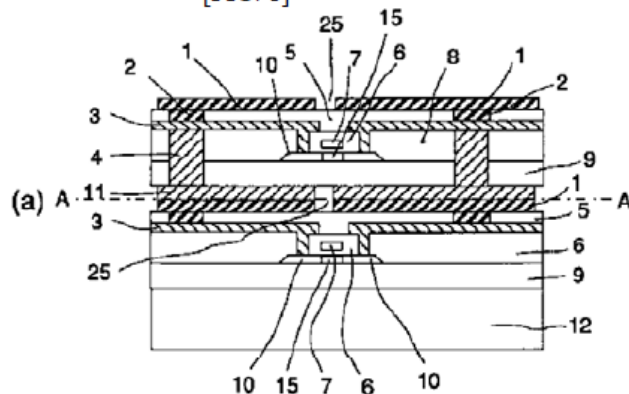


Figure 1 (reproduced below) is a cross sectional view showing an example of embodiment in which two layers of LSIs were laminated.

[FIG. 1]



In Figure 1, front connection surface terminal 1, consisting of a gold (Au) film formed on the upper surface, of the first transistor arranged below was connected to back connection surface terminal 11, consisting of a gold film formed on the back surface, of the second transistor arranged above. Front

connection surface terminal 1 and back connection surface terminal 11 were all planar; both connection became a surface connection, so the contact area was very large. *Id.* ¶ 14. Wirings 3 of the first and the second LSI were connected to front connection surface terminal 1 via a conductive film filled in surface through-hole 2 formed in surface insulating film 5, and wiring 3 of the second LSI arranged on the upper part was connected to back connection surface terminal 11 via a conductive film that further fills the inside of the back surface through-hole 4. *Id.* ¶ 17. Hitachi further discloses that “a highly reliable connection will be achieved as long as the front connection surface terminal 1 and the back connection surface terminal 11 are arranged as densely as possible and the gap between the adjoining connection surface terminals is made small.” *Id.* ¶ 20.

ii. Analysis

Petitioner argues that claims 33 and 34 are obvious over the combination of Leedy '695 and Hitachi. *See* Pet. 3. Although Patent Owner has statutorily disclaimed claims 22 and 31 (Ex. 2138), claims 33 and 34 depend from claim 22 and require all the limitations recited in disclaimed claim 22. Thus, we will include the limitations recited in claim 22 in our discussion of claims 33 and 34 below.

Claim 33 is directed to an integrated circuit structure that includes “first, second, and third substrates each having integrated circuits formed thereon” recited in independent claim 22. For this limitation, Petitioner argues that Leedy '695's Figure 8 teaches first (160a), second (160b), and third (160c) substrates. Pet. 27 (citing Ex. 1006 at 16:38–40; Fig. 8; Abstract). Petitioner further asserts that Leedy '695 teaches that each substrate includes active circuit devices (e.g., “SDs 162, 164, 166”) formed

thereon. *Id.* (citing Ex. 1006 at 16:40–43, 26:3, Ex. 1002 ¶ 119).

Additionally, Petitioner argues that Hitachi also discloses stacking up to eight integrated circuit substrates to form a 3D integrated circuit structure. Pet. 27–28 (citing Ex. 1015 ¶ 35, Fig. 5).

Patent Owner argues that Leedy '695's Figure 8 depicts the vertical bonding of circuit membranes, which Patent Owner argues are not "substrates." PO Resp. 45–46. Patent Owner further asserts that Leedy '233 teaches "fabricating the IC devices on a standard silicon substrate, which is then, in turn, processed, trenched and thinned until all that is left are the discrete, individual transistor-sized islands." *Id.* at 46 (citing Ex. 1006, 3:23–33, 24:20–32, 7:1–28, 9:65–10:40).

In its Reply, Petitioner responds, among other things, that even under Patent Owner's construction, Leedy '695's discloses "substrates." Reply 8. Petitioner first refers to Leedy '695's "Method #2" for fabricating semiconductor devices 24, 26, 28 on a substrate membrane 20. *Id.* (citing Ex. 10:14–30; Figs. 3a–b). Petitioner asserts that substrate membrane 20 remains in the final structure and may be oxidized into a dielectric through an optional isolation process. Reply 8 (citing 8:40–58; 10:4–5, 10:26–30; Figs. 3a–b). Petitioner argues that Figure 3b "is an inverted figure with substrate 20 on top and dielectric layer 36 on the bottom." Reply 9 n.6.

Based on the complete record, we agree with Petitioner that Leedy '695 teaches that a substrate may remain in the integrated circuit, and further may include a dielectric layer. In particular, Leedy '695 describes a Membrane Dielectric Isolation (MDI) process "as two methods, depending on which method of forming the semiconductor substrate thin film is selected." Ex. 1006, 6:59–61.

With respect to “Method #2” of MDI, Leedy ’695 generally describes the steps as:

1. Form a free standing low stress semiconductor substrate membrane.
2. Optionally grow the desired epitaxial device layers.
3. Complete all desired top side IC processing steps including deposition of a low stress dielectric membrane.
4. Optionally trench isolate the semiconductor device areas from the back side.
5. Complete IC processing steps on the back side of substrate and remaining top side of substrate.

IC processing steps used on the top side and backside of the semiconductor membrane substrate are well known and not unique in application to the semiconductor substrate membrane; nearly any semiconductor process technique can be applied.

Ex. 1006, 9:64–10:13. Leedy ’695 adds that a thin low stress semiconductor substrate membrane 20, such as the one shown in Figure 2, is fabricated prior to deposition of the low stress dielectric membrane and fabrication of semiconductor devices. Ex. 1006, 10:14–17. Leedy ’695 further teaches that “[a]fter the semiconductor substrate membrane 20 is fabricated (*see* FIG. 3a), semiconductor devices 24, 26, 28, . . . , 30 are fabricated and interconnected on the substrate 20 with the use of low stress dielectric material.” Ex. 1006, 10: 26–30. Additionally, we note that Figure 3b shows an enlarged view of the portion of Figure 3a, which includes the presence of “substrate membrane 20,” semiconductors 24, 26, 28, and a dielectric layer 36 covering the semiconductor devices. Ex. 1006, 9:27–28, Fig. 3b.

In the case of a vertical three dimensional circuit structure, as shown in Figure 8 of Leedy ’695, we understand Petitioner to argue that each circuit membrane (e.g., circuit membranes 160a, 160b, 160c) is a substrate

structure that may include substrate membrane 20 and dielectric layer 36 formed from a MDI method (e.g., Method #2). *See* Pet. 27 (annotated Fig. 8 from Leedy '695) (citing Ex. 1006, 16:40–43, 26:3; Ex. 1002 ¶ 119).

In this regard, applying our construction of “substrate,” we determine that each of Leedy '695's circuit membranes serves as a “material on or in which a device, circuit, or epitaxial layer is fabricated” because the three dimensional vertical circuit, described in Figure 8 of Leedy '695, is formed by interconnecting the circuit membranes through compression bonding of surface electrodes 168a, 168b, 168c, 168d (bond pads) on the circuit membranes. Ex. 1006, 16:38–49; *see also id.* at 1:8–10 (“[t]his invention relates to methods for fabricating integrated circuits on and in flexible membranes, and to structures fabricated using such methods.”). Leedy '695, teaches that the vertically bonded circuit membrane structure disclosed in Figure 8 is an example of “MDI Circuit Membrane Advantages” in which “[t]he fabrication of circuit membranes provides the capability to fabricate and use integrated circuits in novel ways.” Ex. 1006, 15:61–64. To fabricate the three dimensional integrated circuit structure, the circuit membranes are bonded via surface electrodes 168a–d. Our reading of Leedy '695 is consistent with Leedy '695's additional teaching of a method for forming a MOSFET transistor. *See* Ex. 1006, Fig. 10a–d. In this regard, Leedy '695 teaches the use of a “starting *substrate* structure” that is “a combination of silicon and dielectric 204 film forming a membrane 202.” Ex. 1006, 16:1–3. Leedy '695 further teaches that “membrane 202 is formed by one of the methods disclosed above,” *id.* at 16:3–4, which we understand to include “Method #2.” Thus, Leedy '695 itself refers to described membranes as substrates.

Furthermore, our determination that Leedy '695's "circuit membrane" is a "substrate" is consistent with the '233 patent use of the term "substrate," which does not exclude the material used for a "substrate." Specifically, the '233 patent teaches

The two 3DS memory fabrication methods, however, have a common objective which is the thermal diffusion metal bonding (also referred to as thermal compression bonding) of a number of circuit substrates onto a rigid supporting or common substrate which itself may optionally also be a circuit component layer.

The supporting or common substrate can be a standard semiconductor wafer, a quartz wafer or *a substrate of any material composition that is compatible with the processing steps of the 3DS circuit, the operation of the circuit and the processing equipment used.*

Ex. 1001, 7:35–45 (emphasis added).

In sum, having considered Leedy '695's disclosure, the parties' arguments and evidence, and our construction of the term "substrate," we determine that Petitioner has demonstrated sufficiently how Leedy '695's circuit membranes 160a, 160b, 160c teach substrates, i.e., material in or on which the three dimensional circuit is fabricated/formed through the interconnection and bonding of the bond pads on the surface of the circuit membranes.

We note that we need not determine whether the statements and actions by Patent Owner in the prosecution of the '233 patent constitute admissions, acquiesce, or disclaimers. We have adopted Patent Owner's proposed claim construction of "substrate," and even under this construction, we have determined that Petitioner has presented persuasive arguments and evidence supporting its position that Leedy '695 discloses first, second, and

third substrates as recited in claim 22 and required in claim 33 (and claim 34). See Reply 9–10 (“The ’233 Patent is not limited to semiconductor substrates, but describes using ‘a substrate of *any material composition*,’ including a dielectric ‘quartz wafer.’ Ex. 1001, 7:41–45.”).

Claim 33 further requires through its dependence from disclaimed 22:

at least one of metal and non-polymeric first bonding layers on the first and second substrates, wherein the first bonding layers comprise bond-forming material on a majority of first surfaces of the first and second substrates that bonds the first and second substrates to each other; and

at least one of metal and non-polymeric second bonding layers on the second and third substrates, wherein the second bonding layers comprise bond-forming material on a majority of a second surface of the second substrate and a first surface of the third substrate that bonds the second and third substrates to each other.

For these limitations, Petitioner argues that Leedy ’695 performs “compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads).” Pet. 28 (citing Ex. 1006, 16:40–43). For example, Petitioner provides annotated Figure 8 (reproduced below) to show bond pads between circuit membranes 160a, 160b, 160c.

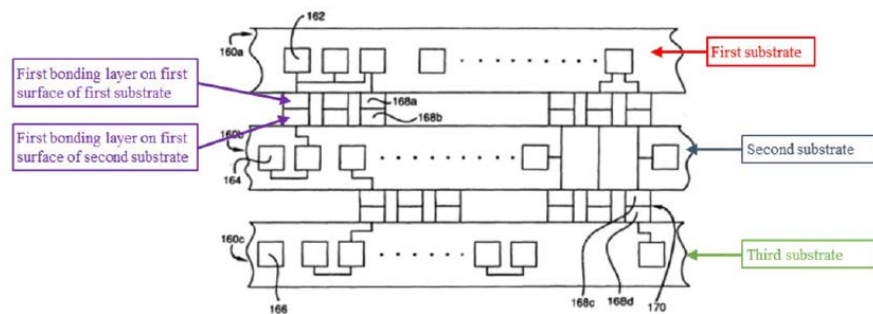


Fig_8

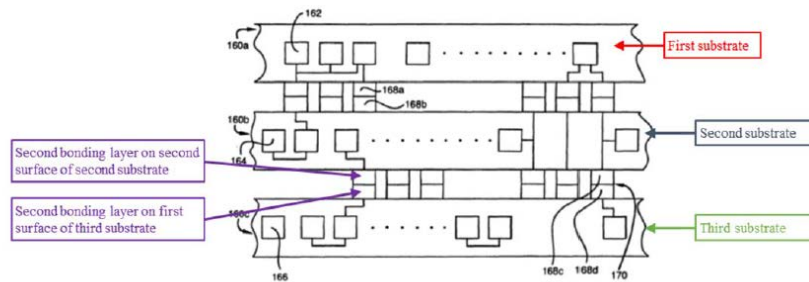


Fig_8

Id. at 28, 33–34. According to Petitioner, Leedy ’695 teaches “[b]onding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 μ m and 25 μ m in diameter) on the surface of two MDI circuit membranes 160b, 160c and using a mechanical or gas pressure source to press the bond pads 168c, 168d together.” Pet. 28 (citing Ex. 1006, 16:43–49).

Petitioner adds that Leedy ’695 teaches bonding multiple substrates by welding metal solder pads or through thermal compression bonding. Pet. 28 (citing Ex. 1006, 16:51–56). According to Petitioner, “bonding layers 168a and 168b are metal first bonding layers on the first and second substrates (160a and 160b), wherein the first bonding layers comprise bond-forming material that bonds the first and second substrates to each other.” Pet. 29 (citing Ex. 1006, Fig. 8; Ex. 1002 ¶ 119). Petitioner further argues that “bonding layers 168c and 168d are metal second bonding layers on the second (160b) and third (160c) substrates.” Pet. 32.

Petitioner acknowledges that Leedy ’695 does not teach bond-forming material on the *majority* of the first surfaces. Pet. 29. However, Petitioner argues that Hitachi discloses that bond pads 1 and 11 (i.e. “connection surface terminals”) form “very large contact areas” and are arranged “as densely as possible” to minimize the gaps between the bonding surfaces.

Pet. 29 (citing Ex. 1015 ¶ 14). Petitioner further relies on the testimony of Dr. Franzon, for the proposition that “[b]y arranging the bond pads ‘as densely as possible’ with small gaps between, the bond-forming materials would cover more than half of the surface area of the chip.” Pet. 30 (citing Ex. 1002 ¶¶ 84–85).

Additionally, Petitioner argues that “a person of ordinary skill in the art would have found it obvious to enlarge the bond pads in the *Leedy* ’695 structure based on the motivation provided by *Hitachi*.” Pet. 31–32 (citing Ex. 1002 ¶¶ 86–88). Petitioner argues that Hitachi teaches maximizing the size of bond pads improves reliability and performance by decreasing thermal and electrical resistance. *Id.* (citing Ex. 1015 ¶¶ 7, 13; Ex. 1002 ¶ 87). Petitioner further asserts that “[i]n light of these benefits, a person of ordinary skill in the art would have been motivated to modify the bond pad design of *Leedy* ’695 such that the bond-forming material cover a majority of first surfaces of the first and second substrates, and would have reasonably expected success from making this change.” *Id.*

Based on the entire record, we determine that Petitioner has explained persuasively how and why a person of ordinary skill in the art would have modified *Leedy* ’695’s disclosure of “compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads),” (Pet. 28 (citing Ex. 1006, 16:40–43)) with the enlarged pads shown in *Hitachi* (Pet. 30–32). Specifically, we determine that *Leedy* ’695 teaches metal bond pads 168a, 168b, 168c, 168d between surfaces of circuit membranes 160a, 160b, 160c (i.e., surfaces of substrates). Ex. 1006, 16:40–43. Additionally, we determine that *Hitachi* teaches the benefits of enlarged bond pads, which include improving the electrical and thermal conductivity of the

interconnections in a stacked circuit structure. Ex. 1015 ¶ 14. For example, in Hitachi's Figure 1(a) (reproduced below), Hitachi discloses vertically bonding two substrates through two pads – “back connection surface terminal 11” and “front connection surface terminal 1.” Ex. 1015 ¶ 14; Fig. 1(a). Hitachi indicates that the contact area between front connection surface terminal 1 and back connection surface terminal 11 “was very large,” and that “a highly reliable connection will be achieved as long as the front connection surface terminal 1 and the back connection surface terminal 11 are arranged as densely as possible and the gap between the adjoining connection surface terminals is made small.” *Id.* at ¶¶ 14, 20.

With respect to this disclosure, we further credit the testimony of Dr. Franzon, who testifies that

Hitachi explains that its enlarged bond pad design provides multiple benefits, such as improving the electrical and thermal conductivity of the interconnections. Ex. 1015 at [0007], [0013]. In view of the benefits taught by *Hitachi*—such as minimizing contact resistance and improving thermal resistance—a person of ordinary skill in the art would have been motivated to enlarge the bond pad design of *Leedy* '695 such that they occupy a majority of the bonding surface, as illustrated in Figure 1(b) of *Hitachi*. *See id.*

Ex. 1002 ¶ 87. In this regard, Dr. Franzon's testimony is persuasive because it comports with and is supported by citations to Hitachi's disclosure of arranging the connection surface terminals “as densely as possible” and to minimize the “gap between the adjoining connection surface terminals.” *See Id.* For example, Dr. Franzon cites to paragraph 7 of Hitachi, which teaches the prior art structure disclosed in Figure 2 employs a small connection area between connecting pin 14 and pad 13. Ex. 1015 ¶ 7. With regard to Figure 2, Hitachi teaches that the prior art structures utilized a high bump 14 with a

large gap between adjoining pins 14. *Id.* at ¶ 6. As Dr. Franzon notes, Hitachi explains that an enlarged pad design provides benefits over the prior art (e.g., Figure 2) because “there have been many problems many problems such as increased contact resistance due to a small contact area, causing an unstable operation, increased thermal resistance due to the presence of a gap, and raising temperature, causing difficult high integration.” *See* Ex. 1002 ¶ 87; Ex. 1015 ¶ 7. Further, in paragraph 13, also cited by Dr. Franzon, Hitachi teaches that its improved structure has a larger connection area “not only cracks hardly occur due to the generation of local stress in thermal cycles after connection formation, but the contact resistance is also small, eliminating the possibility of unstable contact resistance. The gap between connecting pins does not exist.” We further note that the Petition cites to paragraph 20 of Hitachi, which is consistent with the disclosure discussed above and Dr. Franzon’s testimony. Pet. 30. Paragraph 20 provides that “a highly reliable connection will be achieved as long as the front connection surface terminal 1 and the back connection surface terminal 11 [(see Ex. 1015, Figs. 1a–1b)] are arranged as densely as possible and the gap between the adjoining connection surface terminals is made small”.

In weighing Dr. Franzon’s testimony, we observe, that in this particular instance and for this specific asserted combination of references, Dr. Franzon has provided and explained the underlying basis for his opinions as well as provided citations to the references to support his testimony. *See* Ex. 1002 ¶ 87. Based on the complete record, this aspect of Dr. Franzon’s testimony is consistent with the arguments provided by Petitioner and the citations to the references. Further, while we are cognizant that it is ultimately Petitioner’s burden to demonstrate by a

preponderance of the evidence that the challenged claims are unpatentable over this asserted combination, we also recognize that in considering the weight to give to Dr. Franzon's expert testimony, we review the arguments provided by both of the parties, the evidence cited, and the teachings in the references relied upon by Hitachi. We have not been made aware of any reason to doubt Dr. Franzon's testimony with respect to these bonding layer(s) limitations, nor have we determined otherwise that these particular portions of Dr. Franzon's opinion, directed to these limitations, are suspect. Thus, we weigh Dr. Franzon's testimony accordingly and credit his testimony in this regard.

Moreover, we note that while the IC fabrication process is a complex one, it does not follow that the complexity with respect to another obviousness challenge (i.e., obviousness challenge based on the combination of Matsumoto, Bower, and Leedy '695) binds the separate and distinct challenge based on Leedy '695 and Hitachi. For example, unlike Petitioner's other challenge, Petitioner does not assert that a dielectric substitution must be made, with its attendant complexities of fabrication that must be accounted for, into Matsumoto or Bower. Rather, here, in this particular challenge, Petitioner relies on Leedy '695 for its primary integrated circuit structure (e.g., Ex. 1006, Fig. 8) and cites Hitachi for a design change, i.e., enlargement of Leedy '695's existing metal bond pads, that Petitioner argues would have been obvious based on the benefits of enlarged bond pads described in Hitachi. Pet. 22–26. Given the difference in the challenges presented, we do not ascribe the arguments made by either party in one obviousness challenge to another completely separate challenge when the record does not indicate the parties' intentions of doing so. *See In*

re Magnum Oil, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (indicating that the Board is not free “to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR. Instead, the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.”).

Additionally, as discussed above, Petitioner relies on Figure 8 of Leedy '695 to show a stacked circuit structure with bond pads between circuit substrate membranes 160a, 160b, 160c. *See* Pet. 29. With regard to Figure 8, Leedy '695 teaches that after the circuit substrate membranes have been formed (e.g., through Method #2), the vertical bonding of two or more circuit membranes form a three dimensional circuit structure. *See* Ex. 1006, 38–40. In other words, the bonding of the circuit membranes is subsequent fabrication processing (i.e., interconnection) that occurs after the circuit membranes have been formed by the MDI fabrication process. *Id.* at 15:63–65 (“The fabrication of circuit membranes provide the capability to fabricate and use integrated circuits in novel ways.”). With respect to interconnection, such as that shown between bond pads in Figure 8 of Leedy '695, Leedy '695 further teaches that “[t]hese [circuit] membranes permit the application (continued use) of most of the established integrated processing methods for the fabrication of circuit devices and *interconnect metallization*. Ex. 1006, 1:49:52 (emphasis added). Thus, Leedy '695 indicates that established interconnection metallization processes may be used with the circuit membranes after the circuit membranes are made from MDI fabrication process. *Id.*

Based on the complete record, we determine that Petitioner has demonstrated by a preponderance of the evidence how the asserted

combination of Leedy '695 and Hitachi teach or suggest the “bonding layer” limitations recited in claim 33 (and claim 34).

Claim 33 further recites “the circuitry are formed with a low stress dielectric.” Petitioner argues that Leedy '695 discloses “‘methods for fabricating integrated circuits ... formed of very thin low stress dielectric materials,’ and applying such methods to ‘3D IC fabrication.’” Pet. 37 (citing Ex. 1006, Abstract). Petitioner further asserts Leedy '695 discloses forming a “tensile low stress dielectric membrane” on a semiconductor substrate and that low stress dielectric may include “silicon dioxide” or “silicon nitride” formed by deposition. *Id.* at 37–38 (citing Ex. 1006, 1:53–58, 11:33–36; Ex. 1002 ¶¶ 75–77).

Based on the complete record, Petitioner’s position is persuasive and consistent with the disclosure in Leedy '695, which we determine discloses *low stress* silicon dioxide and silicon nitride deposition recipes for the MDI process. Ex. 1006, 11:25–64 (emphasis added). Accordingly, based on the complete record, we determine that Petitioner has demonstrated by a preponderance of the evidence that the combination of Leedy '695 and Hitachi would have conveyed to one of ordinary skill in the art the invention recited claim 33.

With respect to claim 34, claim 34 depends from claim 33 and further recites “the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have a stress of about 5×10^8 dynes/cm² or less.” Petitioner argues that Leedy '695 discloses forming a “silicon dioxide” dielectric film that is caused to have a stress of preferably 1×10^7 dynes/cm². Pet. 38 (citing Ex. 1006, 11:33–37).

Based on the complete record, we determine that Petitioner’s

arguments are persuasive and consistent with Leedy '695's disclosure. *See* Ex. 1006, 11:33–37. As discussed above, our construction of a “low stress dielectric” as “a dielectric having a stress of less than 8×10^8 dynes/cm²” takes into account the teaching in the Specification of the '233 patent that dielectrics in low stress include those that have a stress of less than 5×10^8 dynes/cm² and “low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695.” Ex. 1001, 8:60–9:2. Thus, we determine that Leedy '695 discloses low stress dielectrics with a stress of 1×10^7 dynes/cm², and teaches that “[l]ow stress is defined relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8×10^8 dynes/cm² (preferably 1×10^7 dynes/cm²) in tension.” Ex. 1006, 11:33–37.

Accordingly, based on a review of the complete record, we determine that Petitioner has demonstrated by a preponderance of the evidence claims 33 and 34 of the '233 patent are unpatentable over the combination of Leedy '695 and Hitachi.

III. CONCLUSION

Having considered the parties' arguments and evidence, we conclude that Petitioner has satisfied its burden of demonstrating, by a preponderance of the evidence, that the subject matter of claims 33 and 34 of the '233 patent would have been obvious over the combination of Leedy '695 and Hitachi. Separately, we determine that Petitioner has not met its burden of demonstrating, by a preponderance of the evidence, that the combination of Matsumoto, Bower, and Leedy '695 would have conveyed to one of skill in the art the claimed inventions recited in claims 33 and 24.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 33 and 34 of the '233 patent have been shown by a preponderance of the evidence to be unpatentable; and

FURTHER ORDERED that this is a Final Written Decision under 35 U.S.C. § 318(a), and that parties to the proceeding seeking judicial review of the decision under 35 U.S.C. § 319 must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2016-00389
Patent 8,035,233 B2

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