

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD;
MICRON TECHNOLOGY, INC., and
SK HYNIX, INC.

Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00395
Patent 7,504,732 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and
FRANCES L. IPPOLITO, *Administrative Patent Judges*.

PERRY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a); 37 C.F.R. § 42.73

I. INTRODUCTION

A. Procedural History

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively “Petitioner”) filed a Petition (Paper 4, “Pet.”) on December 28, 2015, requesting an *inter partes* review of claims 1, 10, 11, 13, and 14 of U.S. Patent No. 7,504,732 B2 (Ex. 1001, “the ’732 patent”). Subsequently, Patent Owner filed a Preliminary Response to the Petition on April 6, 2016 (Paper 8, “Prelim. PO Resp.”).

Based on these submissions, we instituted an *inter partes* review of claims 1, 10, 11, 13, and 14 of the ’732 patent on the following grounds:

References	Basis	Claims Challenged
Yu ¹ and Leedy ’695 ²	§ 103(a)	1, 10, 11, 13, and 14
Finnila ³ , Yu, and Leedy ’695	§ 103(a)	1, 10, 11, 13, and 14

Paper 11 (“Dec. on Inst.”). In our Decision to Institute, we did not agree with Patent Owner that the Petition was barred under 35 U.S.C. § 315(b) because, according to Patent Owner, the Office lacked authority to treat certain days, on which the Office experienced an emergency situation such

¹ Yu, et al., *Real-Time Microvision System with Three-Dimensional Integration Structure*, Proc. of the 1996 IEEE/SICE/RSJ Int’l Conf. on Multisensor Fusion and Integration for Intelligent Systems, 1996 (Ex. 1009, “Yu”).

² US Patent No. 5,354,695, issued October 11, 1994 (Ex. 1006, “Leedy ’695”).

³ US Patent No. 5,426,072, issued June 20, 1995 (Ex. 1011, “Finnila”).

that many of its online and information technology systems were shut down, as federal holidays. Dec. 4–5. Patent Owner has not raised this issue subsequent to institution in this proceeding.

After institution, Patent Owner filed its Patent Owner Response on October 14, 2016 (Paper 49, “PO Resp.”) and Petitioner filed a Reply (Paper 55, “Pet. Reply,”).

This *inter partes* review pertains to one member of the “Elm 3DS family” of patents that share a common core of written description but have different claims (continuations and divisional applications of a common parent). Some of the patents being considered in *inter partes* reviews of patents in the Elm 3DS family have expired and others have not (*e.g.* the ’732 patent). On April 5, 2017, we held a consolidated hearing in which we heard argument on fourteen *inter partes* reviews (including this one and all having the same panel of Administrative Patent Judges) of Elm 3DS family patents. Although there are differences among these related *inter partes* reviews (different claims and different combinations of prior art references applied) there is a significant overlap of evidentiary records among the reviews. Each decision regarding an Elm 3DS family patent is based on its own evidentiary record. A transcript of the oral hearing is included in the record of each proceeding, including this one. Paper 61 (“Tr.”). This Decision relies in part on analysis set forth in the combined Final Written Decision in IPR2016-00386, IPR2016-00387, and IPR2016-00388, particularly with regard to claim construction.

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. For the reasons discussed herein, Petitioner has not

demonstrated by a preponderance of the evidence that claims 1, 10, 11, 13, and 14 of the '732 patent are unpatentable.

B. Related Proceedings

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 1–2; *see also* Paper 6 (Patent Owner's Mandatory Notices).

Petitioner indicates that the '732 patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK Hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

The challenged patent and related family member patents (collectively "Elm 3DS patents" or "Elm 3DS family") are the subject of petitions filed in IPR2016-00386 (US Patent No. 8,653,672); IPR2016-00387 (US Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (US Patent No. 7,193,239); IPR2016-00389 (US Patent No. 8,035,233); IPR2016-00390 (US Patent No. 8,629,542); IPR2016-00391 (US Patent No. 8,796,862); IPR2016-00393 (US Patent 7,193,239); IPR2016-00394 (US Patent No. 8,410,617); IPR2016-00395 (US Patent No. 7,504,732) (this case); IPR2016-00687 (US Patent No. 8,928,119); IPR2016-00691 (US Patent No. 7,474,004); IPR2016-00703 (US Patent No. 8,791,581) (not instituted); IPR2016-00706 (US Patent No. 8,791,581) (not instituted); IPR2016-00786 (US Patent No. 8,933,570); IPR2016-00708 (US Patent No. 8,907,499); and IPR2016-00770 (US Patent No. 8,907,499).

C. The '732 Patent (the Challenged Patent)

The '732 patent and the other patents of the Elm 3DS family have in common written description of a “three-dimensional structure (3DS)” for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

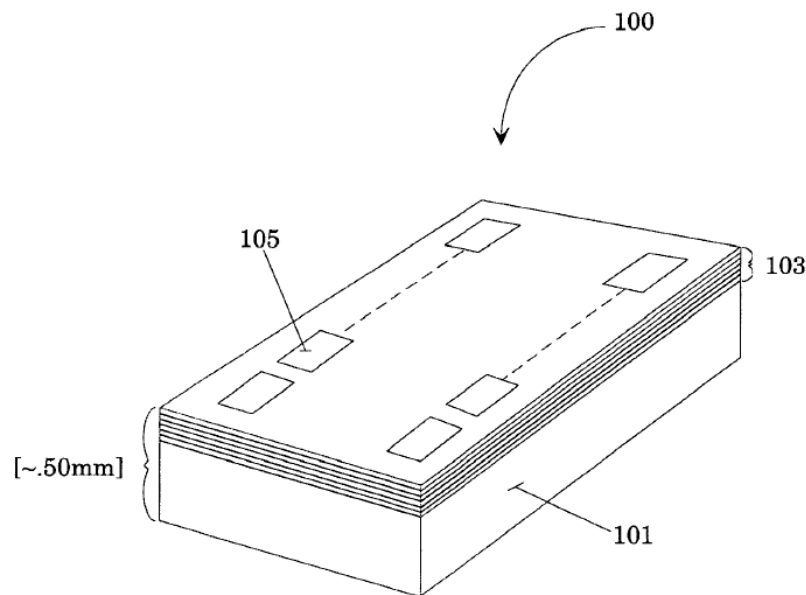


Figure 1a is a pictorial view of a 3DS DRAM IC manufactured with Method A or Method B and demonstrating the same physical appearance of I/O bond pads as a conventional IC die. Ex. 1001, 3:44–47.

Figure 1a of the '732 patent shows 3DS memory device 100 having a stack of integrated circuit layers with a “fine-grain inter-layer vertical interconnect” between all circuit layers. *Id.* at 4:8–12. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:30–32. The '732 patent discloses that “each memory array circuit layer

is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness.” *Id.* at 4:28–31. The written description states that the “thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm²) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication.” *Id.* at 8:58–63.

Figure 1b is reproduced below.

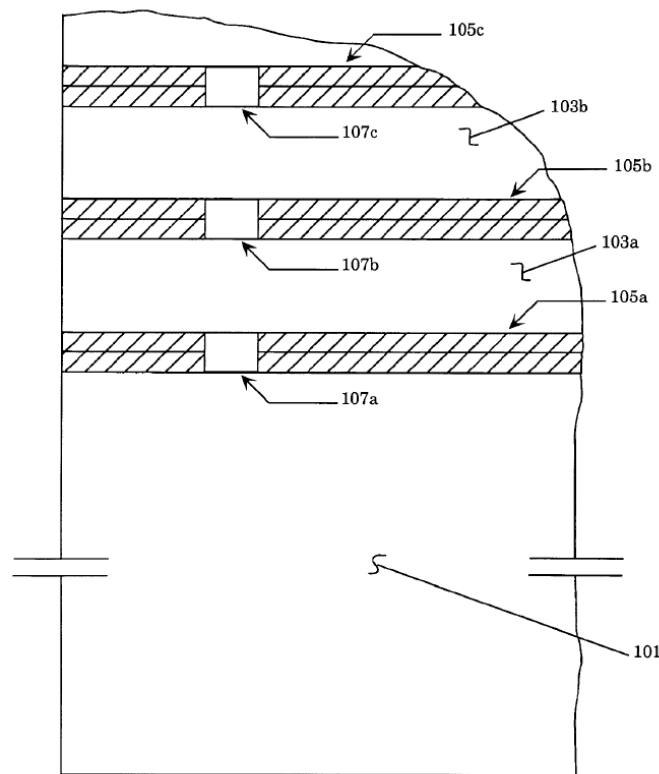


Figure 1b is a cross-sectional view of a 3DS memory IC showing the metal bonding interconnect between several thinned circuit layers. Ex. 1001, 3:48–50.

Referring to Figure 1b, the '732 patent shows a cross-section of a 3DS DRAM integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:48–50. Bond and interconnect layers 105a, 105b, etc. are shown between circuit layers 103a and 103b. *Id.* at Fig. 1b. The '732 patent discloses that pattern 107a, 107b, etc. in the bond and interconnect layers 105a, 105b, etc. defines the vertical interconnect contacts between the integrated circuit layers and serves to electrically isolate these contacts from each and the remaining bond material. *Id.* at 4: 22–24. Additionally, the '732 patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:24–27.

Further, the '732 patent teaches that the “term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 μm . *Id.* at 4:11–14. The fine-grain inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:16–21.

D. Illustrative Claim

Claim 1, reproduced below, is independent and illustrative of the challenged claims. The other challenged claims depend either directly or indirectly from claim 1.

1. A stacked integrated circuit comprising:
 - a first thinned substantially flexible integrated circuit layer having a bottom-side surface;
 - a second thinned *substantially flexible* integrated circuit layer having a top-side surface, wherein the first integrated circuit layer overlies the second integrated circuit layer such that the bottom-side surface overlies at least part of the top-side

surface, and wherein at least one of the first and second thinned substantially flexible integrated circuit layers comprises a *low stress dielectric layer*; and

an inter-layer stacked between the bottom-side surface of the first integrated circuit layer and the top-side surface of the second integrated circuit layer, wherein the inter-layer includes at least a first inter-layer portion and a second inter-layer portion that is electrically isolated from at least the first inter-layer portion, wherein each one of the first and second inter-layer portions forms a bond between the bottom-side surface of the first integrated circuit layer and the top-side surface of the second integrated circuit layer, and wherein only one of the first and second inter-layer portions forms at least one interconnection electrically coupling the first integrated circuit layer to the second integrated circuit layer for the transfer of information, wherein the at least one interconnection between the first and second integrated circuit layers is formed only on the bottom-side and top-side surfaces. (emphasis added)

II. ANALYSIS

A. Principles of Claim Construction

Members of the Elm 3DS family share a common core of written description but have different claims (continuations and divisional applications of a common parent). Some of the patents being considered have expired and others have not.

The '732 patent has not yet expired. Thus, the broadest reasonable construction standard applies to the claims at issue. Accordingly, here, we interpret claims of an unexpired patent using the “broadest reasonable construction in light of the specification of the patent in which [the claims] appear[.]” 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144 (2016) (concluding the broadest reasonable construction

“regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office”).

Under this standard, the Board may not “construe claims during IPR so broadly that its constructions are unreasonable under general claim construction principles. . . . ‘[T]he protocol of giving claims their broadest reasonable interpretation . . . does not include giving claims a legally incorrect interpretation.’” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2016). “Rather, ‘claims should always be read in light of the specification and teachings in the underlying patent’” and “[e]ven under the broadest reasonable interpretation, the Board’s construction ‘cannot be divorced from the specification and the record evidence.’” *Id.* (citations omitted).

B. Principles of Law Concerning Demonstrating Unpatentability

To prevail in challenging Patent Owner’s claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes*

review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

Petitioner asserts that certain claims of the challenged patents are unpatentable under 35 U.S.C. § 103(a) as obvious over various combinations of references. A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Consideration of the *Graham* factors helps inform the ultimate obviousness determination.” *Apple v. Samsung Elecs. Co.*, 839 F.3d 1034, 1048 (Fed. Cir. 2016) (en banc).

C. Level of Ordinary Skill

In determining whether an invention would have been obvious at the time it was made, 35 U.S.C. § 103 requires us to resolve the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. “The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991). The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC*,

Inc., 57 F.3d 1573, 1579 (Fed. Cir. 1995). Factors that may be considered in determining the level of ordinary skill in the art include, but are not limited to, the types of problems encountered in the art, the sophistication of the technology, and educational level of active workers in the field. *GPAC*, 57 F.3d at 1579. In a given case, one or more factors may predominate. *Id.* Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *Innovation Toys, LLC v. MGA Entm't, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) (“A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.”).

Petitioner, with support of its declarant Paul D. Franzon, Ph.D., contends that one of ordinary skill in the art at the time of the inventions of the challenge patents “would have had at least a B.S. degree in electrical engineering, material science, or equivalent thereof, and at least 3–5 years of experience in the relevant field, e.g., semiconductor processing.” Pet. 5 (citing Ex. 1002 ¶¶ 52–53). According to Dr. Franzon, his testimony as to the level of ordinary skill is based on considering “the types of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field.” Ex. 1002 ¶ 53. Patent Owner did not propose expressly a particular level of ordinary skill. *See, e.g., generally* PO Resp. At the oral hearing, however, Petitioner indicated that there did not seem to be any dispute as to the correct level of ordinary skill. Tr. 112:11–14 (“I don’t think there was any dispute about whether [Dr. Franzon’s proposed level of ordinary skill] was the correct level of skill, although Patent Owner can correct me.”).

Having reviewed the prior art asserted in these proceedings (*see, e.g.*, Exs. 1004–07, 1009, 2160), we determine that the level of ordinary skill proposed by Petitioner’s declarant is consistent with the challenged patent and the referenced prior art, and we adopt Petitioner’s proposed definition of the level of ordinary skill in the art for the purposes of the analysis below.

*D. Construction of “Substantially Flexible”*⁴

For reasons stated in our final written decision for IPR2016-00386 we construe “substantially flexible” in the context of the related patents to as “largely able to bend without breaking.” The ’732 patent, at issue here, has not yet expired; thus, the applicable construction is broadest reasonable interpretation. At Oral Hearing, Petitioner’s counsel asserted that the claim construction of “substantially flexible” would be the same under both claim construction standards. Tr. 12:2–4 (Petitioner’s counsel indicating that the “we don’t see there as being a difference, whether BRI or Phillips is applied.”); *see generally* Tr. 11:21–13:16. Similarly, Patent Owner’s counsel at Oral Hearing indicated that the same construction would apply under broadest reasonable construction standard or the standard under *Phillips*. Tr. 50:10–14 (Q: “[I]n terms of the different claim construction standards, I understood that your position is that the same construction

⁴ The term “substantially flexible” is at issue in thirteen of the Elm 3DS *inter partes* reviews: IPR2016-00386 (’672 patent), IPR2016-00387 (’778 patent), IPR2016-00388 (’239 patent), IPR2016-00390 (’542 patent), IPR2016-00391 (’862 patent), IPR2016-00393 (’239 patent), IPR2016-00394 (’617 patent), IPR2016-00395 (’732 patent), IPR2016-00687 (’119 patent), IPR2016-00691 (’004 patent), IPR2016-00708 (’499 patent), IPR2016-00770 (’499 patent), and IPR2016-00786 (’570 patent).

would apply under BRI or in District Court for substantially flexible.” A: “That’s correct.”).

In the context of the Elm 3DS family, we find that the broadest reasonable interpretation of “substantially flexible” is the same as our construction under the *Philips* standard. Under the broadest reasonable construction standard, we presume a claim term carries its ordinary and customary meaning, which “is the meaning that the term would have to a person of ordinary skill in the art in question” at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). As discussed in detail in the Final Written Decisions in IPR2016–00386, IPR2016-00387, and IPR2016–388, the ordinary and customary meaning of “substantially flexible” is “largely able to bend without breaking.” Also as discussed extensively in those Final Written Decisions, the inventor did not give the term “substantially flexible” a particular meaning in the specification with “reasonable clarity, deliberateness, and precision.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

All of the challenged claims of the ’732 patent, use the term “substantially flexible” as a modifier of “integrated circuit layer.” We construe the term “thinned substantially flexible integrated circuit” as having two separate and distinct requirements: 1) “thinned”, and 2) “substantially flexible.” We do not read the term “substantially flexible” out of the claims. Both requirements must be met.

E. Summary of Prior Art Disclosures

1. Yu

Yu is a paper published in the proceedings of a technical conference sponsored by IEEE Industrial Electronics Society, the IEEE Robotics and Automation Society, the Society of Instrument and Control Engineers, and the Robotics Society of Japan. Ex. 1009, 4. Yu describes a three-dimensional integrated circuit structure for implementing a real-time microvision system. Ex. 1009, 831–32. “The system consists of a number of 2D LSIs vertically stacked using 3D LSI technology. . . .” *Id.* at 832. Yu’s Figure 1 is reproduced below.

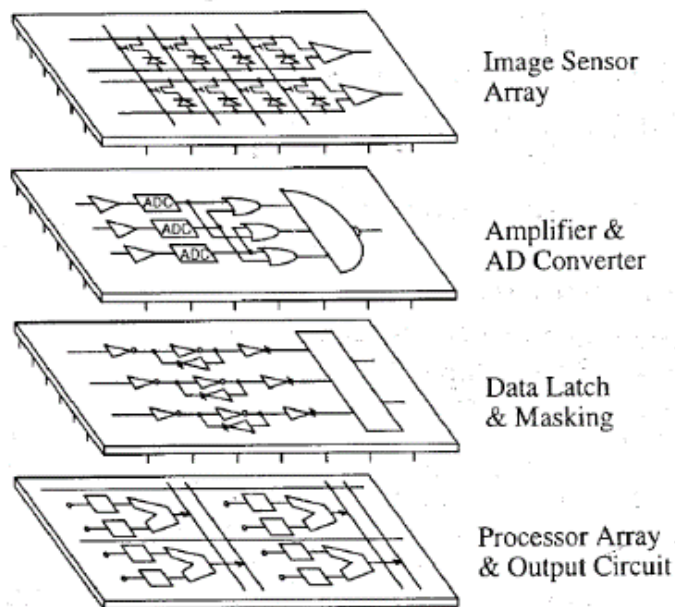


Figure 1: Basic concept of real-time microvision system with 3D integration structure

Figure 1 shows a basic concept of a real-time microvision system with a 3D integration structure.

In Yu's microvision system, substrates are ground and polished to thin the substrates to about 30 microns. *Id.* at 831–32 (“The Si substrate of the 2D-LSI which has the basic circuits is ground and polished to make thin wafer.”); *id.* at Abstract (“In fabrication, grinding and chemical-mechanical polishing techniques are used to thin the wafer to 30 μm .”). Wafers then are bonded together using a combination of conductive microbumps and a UV-hardening adhesive. *Id.* at 834–35 (“The thinned wafer is bonded to a thick wafer using In/Au micro-bumps with the minimum size of 5 μm x 5 μm and UV hardening adhesive layer with thickness of 1 μm by forcing the z direction pressure after careful wafer alignment.”). The microbumps connect to buried interconnect structures that form vertical interconnects between vertically stacked circuitry. *Id.* at Fig. 8.

2. Leedy '695

Leedy '695 is a United States Patent naming Glenn J. Leedy as sole inventor. The patent relates to the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In its Abstract, Leedy '695 indicates that the disclosed integrated circuits are fabricated from flexible membranes “formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers.” *Id.* at Abstract. Leedy '695 also discloses forming a “tensile low stress dielectric membrane” on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy '695 defines “[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8×10^8 dynes/cm² (preferably 1×10^7

dynes/cm²) in tension.” *Id.* at 11:33–37. Additionally, Leedy ’695 discloses two chemical vapor deposition (CVD) process recipes for manufacturing “structurally enhanced low stress dielectric circuit membranes.” *Id.* at 11:51–65.

Referring to Figure 8, Leedy ’695 discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.

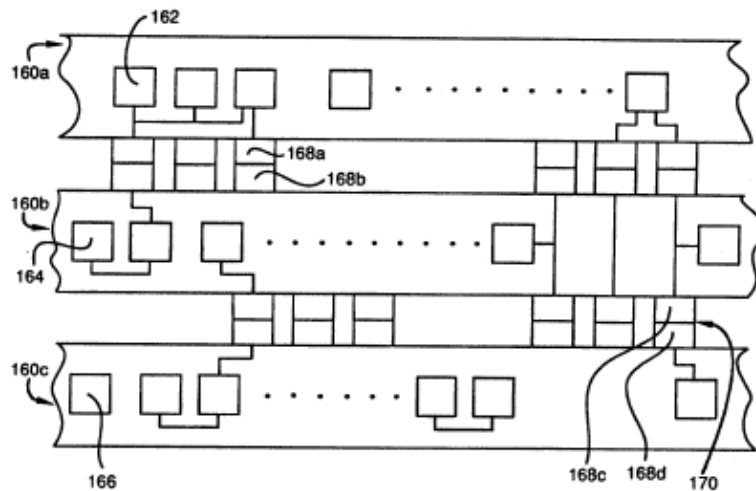


Fig_8

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40.

Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 μ m and 25 μ m in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

3. Finnila

Finnila Figure 8 is reproduced below.

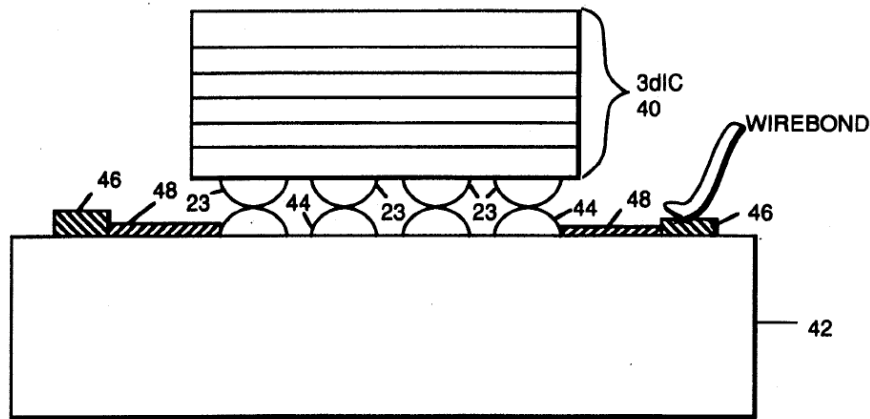


Fig. 8

Figure 8, not to scale, illustrates an embodiment of a 3D integrated circuit assembly that is connected to a larger diameter carrier wafer. Ex. 1011 at 2:62–64.

Finnila describes a “[p]rocess of manufacturing a three dimensional integrated circuit from stacked SOI wafers.” Ex. 1011 at Title. Fabrication begins with “SOI wafer 1 that includes [] a silicon film 12 separated from a bulk silicon wafer 10 by an SiO₂ layer 11.” *Id.* at 3:4–6, Fig. 1. A silicon film of 0.2 micrometers to 10 micrometers is formed “by bonding two silicon wafers together with a fused oxide layer, and then thinning one of the wafers to form the thin film Si layer 12.” *Id.* at 3:8–21; *see also* Ex. 1002 ¶¶ 80–90. The Si film can be characterized as being either a “thick” film, having a thickness greater than approximately one micron, or a “thin” film having a thickness less than approximately one micron. In the thick film case, trenches are formed to provide vertical feedthroughs.” Ex. 1011 at 3:35–40. “[I]soplanar oxide 13” is deposited to insulate active areas of the

substrate from one another. *Id.* at 3:45–50, Fig. 2. Vertical trenches are created “by an anisotropic plasma etch process.” *Id.* at 3:50–55. “[T]he structure formed thus far is processed to form an integrated circuit. A CMOS process is described, but any other process, such as bipolar or bipolar/CMOS, may also be employed.” *Id.* at 4:18–21.

An “SiO₂ layer 17 is formed to serve as the gate oxide” of the transistors in the integrated circuitry. *Id.* at 4:26–28, Fig. 5. “A layer 20 of SiO₂ is then deposited over the” active area. *Id.* at 4:35–36. “Openings are defined and etched within the SiO₂ layer 20, and metallization 21 is deposited so as to contact the conductive feedthroughs 16.” *Id.* at 4:36–38, Fig. 5. An “insulating overglass layer 22” is deposited to passivate the integrated circuitry. *Id.* at 4:45–46. “Finally, openings are defined and etched into the overglass layer 22, and ‘topside’ indium bumps 23 are formed to contact the metalization 21 within the openings.” *Id.* at 4:46–49. The indium bumps are formed to be part of the “eventual interconnection to another wafer.” *Id.* at 4:50–52.

The completed wafer is temporarily bonded to the “temporary substrate” using a material that can be “readily removed” like wax, for example. *Id.* at 4:58–5:9, Fig. 6. The bottom of the wafer is etched or lapped to remove a portion of the bottom substrate—stopping at the silicon dioxide layer 11. *See id.* at 5:10–17. The result is a thin silicon film 12 sitting on the silicon dioxide layer 11.

“Conventional processing steps” are used “to define and etch contact openings and form bonding pads 28. *Id.* at 5:31–35.

“A multiplicity of structures or wafers after stacking and interconnection [] form a 3d integrated circuit assembly 40.” *Id.* at Fig. 7,

6:27–29. A rigid Structure 1 is placed at the bottom of the stack to provide mechanical support. *Id.* at 6:29–33. Structures 2 and 3 are identical to the thinned SOI wafers disclosed above. *Id.* at 6:36–39. Structure 4 is the disclosed wafer modified such that “aluminum bonding pads 32 that have been fabricated on the topside surface instead of the indium bumps 23.” *Id.* at 6:39–43. The structures are aligned so that bottomside and topside bumps of respective structures are “brought into contact and fused together” using a “conventional cold welding process.” *Id.* at 6:44–52.

Gaps between the structures are then filled with “suitable material 34, such as an epoxy adhesive, to provide mechanical support.” *Id.* at 6:53–58.

F. Asserted Ground of Obviousness over Yu and Leedy ’695

1. Petitioner’s Contentions

Petitioner, with support of its declarant, Dr. Franzon, provides analysis purporting to explain how the combination of Yu and Leedy ’695 would have conveyed to one of ordinary skill in the art the limitations recited in claims 1, 10, 11, 13, and 14. Pet. 20–38.

According to Petitioner, “Yu teaches or suggests all but a few of the features recited in the Challenged Claims.” Pet. 20. Petitioner acknowledges that Yu does not explicitly disclose that its dielectric is “low stress” characterized by a tensile stress of about 5×10^8 dynes/cm² and argues that it would have been obvious to substitute the Leedy ’695 dielectric conforming to the stress limitation (5×10^8 dynes/cm²) required by claim 10 (claim 1 refers to “low stress”) in place of the Yu dielectric. *Id.*

Petitioner argues that one of ordinary skill would have been motivated to modify the teachings of Yu to implement the silicon oxide nitride

deposition processes disclosed by Leedy '695—which result in the deposition of dielectric material having tensile stress of preferably 1×10^7 dynes/cm²—for several reasons. Pet. 20–21 (citing Ex. 1002 ¶¶ 70–72).

First, both references seek to achieve advantageous IC performance by constructing 3D ICs from 2D ICs. Pet. 21 (citing Ex. 1009, 831; Ex. 1006, Abstract, 2:9–14, 45:49–59, 47:31–33). Second, Leedy '695 provides express motivations for modifying Yu's processes and device to incorporate Leedy '695's low tensile stress dielectric material, in that Leedy '695 explains that low tensile stress is important because otherwise “surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane.” Pet. 21 (citing Ex. 1006 at 5:63–6:5). Leedy '695 explains that the described low tensile stress dielectrics can advantageously be used to insulate circuit devices and interconnect metallization, while at the same time increasing structural integrity and durability. Pet. 21–22 (citing Ex. 1006 at Abstract, 1:53–62, 2:9–31, 2:66–3:3, 3:56–4:13, 30:36–42, 45:49–46:26, 46:52–47:33, Figs. 32a–32d). Leedy '695 also explains that such dielectrics advantageously have lower stress. *Id.* (citing Ex. 1006 at 6:30–33; Ex. 1002 ¶¶ 92–103). Finally, Leedy '695 also discloses use of plasma-enhanced chemical vapor deposition (“PECVD”) to deposit the low tensile stress dielectrics. Pet. 22 (citing Ex. 1006 at 11:28–63; Ex. 1039 at 2). Petitioner argues that PECVD was a well-known and widely used deposition technique that provided conformal deposition at lower substrate temperatures and at faster rates compared to other depositions techniques. *Id.* (citing Ex. 1040, 171).

2. Patent Owner's Contentions

Patent Owner argues that “substantially flexible” cannot be read out of the claims; “thinned” does not mean “flexible.” PO Resp. 1. According to Patent Owner, Petitioner does not establish the claimed “substantial flexibility” of an integrated circuit layer. PO Resp. 46.

Based on our preliminary claim construction, Patent Owner argues that based on the ordinary meaning of “flexible,” Yu does not disclose or even suggest a “substantially flexible integrated circuit layer,” and Petitioner does not argue or attempt to show otherwise. Rather, according to Patent Owner, Petitioner argued only that Yu discloses a substrate that has been thinned, without any regard for whether the substrate or the resulting circuit is in fact flexible. *Id.*

Patent Owner also argues that dielectrics are not fungible; and that one of ordinary skill would not have substituted the Leedy '695 dielectric for the Bertin '754 dielectric. *Id.*

In support of its argument against dielectric substitution, Patent Owner presents a tutorial explaining the complexity of semiconductor fabrication, with numerous citations to the prior art references and declaration testimony of its expert, Alexander D. Glew, Ph.D. (Ex. 2166).

The tutorial stresses the detailed planning and decisions required to establish a fabrication process for a semiconductor integrated circuit. PO Resp. 3–30. It explains four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. PO Resp. 5 (citing Ex. 2166 ¶ 23; Ex. 2158, 13). In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and then sliced into thin disks called “wafers.” PO

Resp. 6 (citing Ex. 2166 ¶ 25; Ex. 2158, 13–14). The tutorial explains different techniques for producing and layering dielectrics (PO Resp. 16 – 30), including growing dielectrics using thermal oxidation (PO Resp. 18 – 19), depositing dielectrics (PO Resp. 19) and a comparison of thermal CVD (PO Resp. 20) with Plasma Enhanced CVD (PO Resp. 21); different kinds and uses of dielectrics (PO Resp. 22–29) including field oxide dielectrics, gate oxide dielectrics, pre-metal dielectrics, intermetal dielectrics, and passivation dielectrics.

3. “Substantially Flexible” Integrated Circuit Layer

We are not persuaded by Petitioner’s argument that the “substantially flexible” limitation of claims 1, 10, 11, 13, and 14 is met by Yu or Leedy ’695 (or their combined teachings). Both of these references describe thinned and polished/smoothed substrates, but neither describes flexibility or bendability. Specifically, Yu describes a thinned substrate of less than 30µm, but does not discuss its flexibility.

As discussed previously, we agree with Patent Owner’s proposed construction for “substantially flexible” as being “largely able to bend without breaking.” Petitioner does not contend that Yu discloses the recited “substantially flexible” integrated circuit layer as construed by Patent Owner. A preponderance of the evidence establishes that, in the context of the common specification and the ’732 patent claims, mere thinning is not the same as flexibility—being able to bend without breaking.

Per our claim construction of “substantially flexible,” we view “thinned” and “substantially flexible” as separate requirements distinct from each other. Petitioner relies on Yu and Leedy ’695 as teaching “thinned”

substrates. See e.g. Pet. 24. There is no evidence of record that Yu’s “thinned” substrate is “flexible.”

The Examiner, during prosecution of the now-abandoned ’652 application, stated that flexibility is not the equivalent of mere thinning. Ex. 2168, 4.

Petitioner’s expert, Dr. Franzon, testified that the flexibility of a semiconductor substrate depends on many factors, only one of which is the physical dimensions of the substrate—width and thickness. Ex. 1002 ¶ 71. Specifically, Dr. Franzon stated:

In the context of semiconductor processing, the flexibility of a semiconductor substrate depends on a number of factors, including, for example, the type of semiconductor substrate (e.g., while silicon and gallium arsenide are both semiconductors, they have different elastic moduli), the crystal orientation of the material (e.g., {100} and {111} silicon wafers have different elastic moduli), and the physical dimensions of the substrate (e.g., width and thickness).

Ex. 1002 ¶ 71; *see also* Tr. 33:8–24 (Patent Owner’s counsel at oral hearing discussing Dr. Franzon’s testimony about the factors on which flexibility of a semiconductor substrate depends); Tr. 64:16–65:11 (Petitioner’s counsel responding to Patent Owner’s argument about Dr. Franzon’s testimony regarding the various factors that would be considered to determine whether something is flexible).

Petitioner’s counsel asserted at the oral hearing that the prior art shows bendability in addition to thinning because the asserted “prior [art] mirrors the prior [preferred] embodiment.” Tr. 175:21–176:2. Petitioner, however, does not point to sufficient evidence to support its position that prior art mirrors the preferred embodiment in the challenged patent. *See*

generally Tr. 175:13–180:16. For example, Petitioner contends that Dr. Franzon’s testimony that the limitations are met by the prior art supports its position. Tr. 178:20–22 (Asking “is there any evidence of record that any of the combinations that you propose would be the same as the preferred embodiment”?); Tr. 180:8–10 (Ppetitioner’s counsel responding that “[i]t’s Dr. Franzon’s testimony that those limitations are met by the prior art, and it’s the prior art itself, lining up with the claims,”). Dr. Franzon, however, testifies that he was given Petitioner’s proposed construction of “a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed” and he “applied Petitioner’s construction in [his] analysis.” Ex. 1002 ¶ 72.

Per our construction of “substantially flexible,” we do not equate “thinned” with “substantially flexible.” Common sense also supports a conclusion that thickness is not the only factor that determines whether a material is flexible. After all, a thicker piece of rubber is more flexible than a thinner potato chip. Without comparing and considering materials, conditions and fabrication steps, relying upon thinness alone does not satisfy the claim requirement of “substantially flexible.”

Because the challenged claims all require a “thinned substantially flexible integrated circuit layer,” Petitioner has not established that the challenged claims are unpatentable. This reason alone sufficiently supports our conclusion. However, we also conclude, as set forth below that for a second, independent reason, Petitioner has not established that the challenged claims are unpatentable.

4. Low Tensile Stress Dielectric Substitution

Petitioner contends that one of ordinary skill in the art would have reason “to modify the processes and device in Yu such that the dielectrics used therein would be characterized by the [required] tensile stress based on the disclosure of Leedy ’695.” Pet. 20–23.

As an initial matter, we note that much of Dr. Franzon’s testimony on which Petitioner relates to both Bertin ’754 and Yu. *See, e.g.*, Ex. 1002 ¶ 99 (“It was also well known that [plasma-enhanced chemical vapor deposition] is a conformal deposition process capable of coating TSV sidewalls, like those disclosed in Bertin and Yu, to provide TSV insulation.”); ¶ 100 (“Thus, a person of ordinary skill in the art would have been motivated by these advantages to implement the low-stress dielectric deposition techniques disclosed by Leedy to the stacked integrated circuit structures disclosed in each of Bertin (alone or in combination with Poole) and Yu.”); ¶ 101 (“One of ordinary skill in the art would have reasonably expected success combining the teachings of Leedy ’695 with the teachings of each of Bertin (alone or in combination with Poole) and Yu. . . . Leedy ’695 discloses using [plasma-enhanced chemical vapor deposition], which was a commonly available deposition technique that could have been used in place of the techniques for growing or depositing dielectrics described in Bertin and Yu to obtain the predictable result of stacked integrated circuits having low tensile stress dielectrics.”); ¶ 102 (“A person of ordinary skill in the art would have been encouraged to combine Leedy ’695 with each of Bertin (alone or in combination with Poole) and Yu to obtain the predictable result of stacked integration circuits having low

tensile stress dielectrics.”). We see no arguments or evidence from Petitioner that would demand a different result with regard to Yu.

Petitioner provides three purported reasons for combining the references. First, similar to its arguments concerning combining Leedy ’695 with Bertin ’754, Petitioner argues that an ordinarily skilled artisan would have combined Leedy ’695 with Yu is because Leedy ’695 uses “a conformal chemical vapor deposition (CVD) process”; would reduce “the probably of cracking and warpage due to elevated stress in the vias”; and Leedy ’695’s low tensile stress dielectric “would be able to withstand a wide range of processing techniques and processing temperatures.” Pet. 22 (citing Ex. 1002 ¶¶ 99–100).

Dr. Franzon’s testimony in paragraphs 99 and 100 does not support sufficiently a conclusion that one of ordinary skill in the art would have combined the references in the manner proposed by Petitioner. First, Dr. Franzon’s conclusion is too general in that it addresses only: “the stacked integrated circuit structures disclosed in . . . Yu.” Ex. 1002 ¶ 100. Dr. Franzon’s testimony in paragraph 99 is that the chemical vapor deposition processes of Leedy ’695 were well-known and advantages of the technique were well known. Ex. 1002 ¶ 99. As discussed above, this reasoning is insufficient, in view of the complex technology of integrated circuit fabrication and the well-reasoned and well-supported opposing testimony of Patent Owner’s expert, Dr. Glew.

Second, Petitioner contends that one of ordinary skill in the art would have reasonably expected success in combining the references in the manner proposed by Petitioner. Specifically, Petitioner contends:

Modifying the dielectric layer of Yu such that it constitutes a low tensile stress layer as disclosed by Leedy '695 would have been recognized by those of skill in the art as involving nothing more than the use of a known technique to improve similar devices in the same way to manufacture improved 3D integrated circuits. One of ordinary skill in the art could have combined the features by known methods, with each feature retaining its advantageous function, yielding the predictable result of a 3D multichip package.

Pet. 23 (citing Ex. 1002 ¶¶ 92–103).

We do not agree that such broad statements are sufficient to support a conclusion of reasonable expectation of success in view of the complexity of integrated circuit fabrication and the well-reasoned and well-supported opposing testimony of Patent Owner's expert, Dr. Glew. We also note that Dr. Franzon's testimony in paragraph 103 (which Petitioner cites as support for its argument) does not address whether one of ordinary skill in the art would have had a reasonable expectation of success. *See* Ex. 1002 ¶ 103.

Given the well-reasoned and well-supported opposing testimony of Patent Owner's expert, we conclude that Dr. Franzon's testimony to be insufficient to support Petitioner's position regarding dielectric substitution in Yu. *Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation).

The proposed substitution is not simply the substitution of one known element for another. The record does not support Petitioner's statement that the substitution of one dielectric for another, without more information about the substitution, is not a substitution yielding predictable results with known benefits. As discussed previously, both experts agree that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties.

For these reasons, we determine that Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art (i) would have a reason to combine Yu and Leedy '695 in the manner proposed by Petitioner to arrive at the claimed invention and (ii) would have had a reasonable expectation of success of doing so.

For reasons stated above, and separate and distinct from the insufficiency of proof regarding “substantial flexibility” discussed in the section above, we determine that Petitioner does not established sufficiently that one of ordinary skill would have utilized the Leedy '695 dielectric in Bertin '754, as proposed, thereby failing to meet the low stress dielectric limitation required by claims 1, 10, 11, 13, and 14.

G. Asserted Ground of Obviousness over Finnila, Yu, and Leedy '695

1. Petitioner's Contentions

Petitioner, with support of its declarant, Dr. Franzon, provides analysis purporting to explain how the combination of Finnila, Yu, and Leedy '695 would have conveyed to one of ordinary skill in the art the limitations recited in claims 1, 10, 11, 13, and 14. Pet. 38–58.

According to Petitioner, “Finnila teaches or suggests all but a few of the features recited in claims 1, 10, 11, 13, and 14, as construed by Petitioner, ... but does not explicitly disclose (i) that its thinned semiconductor substrate is subsequently polished or smoothed and (ii) that its dielectric are ‘low stress’ characterized by a tensile stress of about 5×10^8 dynes/cm² or less.” *Id.* at 38. Petitioner further contends, however, that it would have been obvious to one of ordinary skill in the art at the time of the alleged invention to modify the processes and device in Finnila such that its thinned semiconductor substrate is subsequently polished or smoothed and

the dielectrics used in Finnila would be characterized by a tensile stress of about 5×10^8 dynes/cm² or less, based on the disclosure of Yu and Leedy '695. *Id.* at 38–39 (citing Ex. 1002 ¶ 111(element 1a)).

Petitioner suggests that it would have been understood to replace the thinning process disclosed in Finnila with another thinning process that involves a subsequent polishing step that was well-known in the art to obtain the same result, which is a thin semiconductor substrate with a planar and smooth surface. *Id.* at 39.

Petitioner notes that both Finnila and Yu address a need for a semiconductor substrate thinned from the backside to produce a planar surface. *Id.* at 40. Further, they both describe thinning that stops on a silicon dioxide layer. *Id.* at 40–41.

Based on these similarities, Petitioner argues that one of ordinary skill would have been motivated to combine the teachings of Finnila and Yu. *Id.* at 42. Further, Petitioner alleges “express” motivations for modifying Yu’s process to incorporate Leedy '695’s low tensile stress dielectric material. *Id.* at 43. The reasons given are essentially the same as discussed above with respect to the combination of Yu and Leedy '695.

2. Patent Owner’s Contentions

According to Patent Owner, Finnila does not disclose or suggest a substantially flexible substrate or circuit. PO Resp. 46. Patent Owner points out that Petitioner does not argue or attempt to show otherwise. *Id.*

3. “Substantially Flexible”

We agree with Patent Owner that Petitioner does not argue flexibility, other than by arguing thinning, as detailed above with respect to the combination of Yu and Leedy '695. Thus, on the issue of meeting the claim

limitations requiring “substantial flexibility,” Petitioner has not shown including Finnila in the combination adds anything.

We therefore conclude that Petitioner has not established sufficiently that the combination of Finnila, Yu, and Leedy '695 renders claims 1, 10, 11, 13, and 14 unpatentable, for the same reasons set forth above in the analysis of Yu and Leedy.

4. Substitution of Low Tensile Dielectric

Also, for the same reasons discussed above, with respect to the obviousness analysis based on the combination of Yu and Leedy '695, Petitioner has not established that one of ordinary skill would have substituted the Leedy '695 dielectric for those of either Finnila or Yu. No new arguments for the substitution were made with respect to Finnila.

For the separate and distinct reason that Petitioner has not established that one of ordinary skill would have made the dielectric substitution, we conclude that Petitioner has not established that the combination of Finnila, Yu, and Leedy '695 renders claims 1, 10, 11, 13, and 14 unpatentable.

III. SUMMARY OF CONCLUSIONS

We now summarize our determinations and conclusions.

“Substantially flexible” is construed to mean “largely able to bend without breaking.” A “thinned substantially flexible integrated circuit layer” requires that at least one integrated circuit layer be both “thinned” and “substantially flexible.”

Petitioner has not demonstrated sufficiently that any of the references, singly or taken in combinations as proposed would meet the “substantially flexible” requirement of the claims.

Petitioner has not demonstrated sufficiently that one of ordinary skill would have substituted the dielectric of Leedy '695 into Yu or Finilla.

We conclude, based on a preponderance of the evidence, that Petitioner has not established that claims 1, 10, 11, 13, and 14 of the '732 patent are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1, 10, 11, 13, and 14 of U.S. Patent No. 7,504,732 have not been shown to be unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to the proceedings seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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