

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00691
Patent 7,474,004 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and FRANCES L.
IPPOLITO, *Administrative Patent Judges*.

IPPOLITO, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Samsung Electronics Co., Ltd.; Micron Technology, Inc. and SK Hynix Inc. (collectively “Petitioner”) filed a Petition on February 29, 2016, requesting an *inter partes* review of claims 1 and 20–23 of U.S. Patent No. 7,474,004 B2 (Ex. 1001, “the 004 patent”). (Paper 1, “Pet.”). Patent Owner, Elm 3DS Innovations, LLC, filed a Preliminary Response to the Petition on June 6, 2016 (Paper 10, “Prelim. Resp.”).

Based on these submissions, we instituted an *inter partes* review of claims 1 and 20–23 of the ’004 patent on the following grounds:

References	Basis	Claim(s) Challenged
Finnila ¹ , Yu ² , and Leedy ’695 ³	§ 103	1 and 20–23
Finnila, Blonder, ⁴ Yu, and Leedy ’695	§ 103	1 and 20–23
Yu, Blonder, and Leedy ’695	§ 103	1 and 20–23
Finnila and Leedy ’695	§ 103	1 and 20–23
Finnila, Blonder, and Leedy ’695	§ 103	1 and 20–23

Paper 13 (“Dec. on Inst.”).

After institution, Patent Owner filed its Patent Owner Response on November 30, 2016 (Paper 35, “PO Resp.”) and Petitioner filed a Reply (Paper 38, “Reply,”).

¹ US Patent No. 5,426,072, issued June 20, 1995 (Ex. 1011, “Finnila”).

² Yu, et al., Real-Time Microvision System with Three-Dimensional Integration Structure, Proc. of the 1996 IEEE/SICE/RSJ Int’l Conf. on Multisensor Fusion and Integration for Intelligent Systems, 1996 (Ex. 1009, “Yu”).

³ US Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, “Leedy ’695”).

⁴ US Patent No. 4,937,653, issued June 26, 1990 (Ex. 1068, “Blonder”).

This *inter partes* review pertains to one member of the “Elm 3DS family” of patents that share a common core of written description but have different claims (continuations and divisional applications of a common parent). Some of the patents being considered in *inter partes* reviews of patents in the Elm 3DS family have expired and others have not (*e.g.* the ’004 patent). On April 5, 2017, we held a consolidated hearing in which we heard argument on fourteen *inter partes* reviews (including this one and all having the same panel of Administrative Patent Judges) of Elm 3DS family patents. Final written decisions have been issued in some of the proceedings. *See, e.g.*, IPR2016-00386–IPR2016-00391, IPR2016-00393–IPR2016-00395.

Although there are differences among these related *inter partes* reviews (different claims and different combinations of prior art references, different reasons to combine, and different arguments regarding reasonable expectation of success), there is a significant overlap of evidentiary records among the reviews. Each *inter partes* review has been decided on its own evidentiary record. A transcript of the oral hearing is included in the record of each proceeding, including this one. Paper 41 (“Tr.”). This Decision relies in part on analysis set forth in the combined Final Written Decision in IPR2016-00386 (Paper 68), IPR2016-00387 (Paper 63), and IPR2016-00388 (Paper 60), particularly with regard to claim construction. In addition, we analyze, where appropriate, different prior art combinations including reasons to combine and reasonable expectation of success.

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. For the reasons that follow, we determine Petitioner has not shown by a preponderance of the evidence that claims 1 and 20–23 of

IPR2016-00691

Patent 7,474,004 B2

the '004 patent are unpatentable.

A. Related Proceedings

Petitioner indicates that the '004 patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK hynix Inc.*, No. 1:14-cv-01432 (D. Del.). Pet. 1.

Additionally, patents related to the '004 patent are also the subjects of petitions filed in IPR2016-00386 (US Patent No. 8,653,672); IPR2016-00387 (US Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (US Patent No. 7,193,239); IPR2016-00389 (US Patent No. 8,035,233); IPR2016-00390 (US Patent 8,629,542); IPR2016-00391 (US Patent No. 8,796,862); IPR2016-00394 (US Patent No. 8,410,617); IPR2016-00395 (US Patent No. 7,504,732); IPR2016-00687 (US Patent No. 8,928,119); IPR2016-00786 (US Patent No. 8,933,570); IPR2016-00708 (US Patent No. 8,907,499); and IPR2016-00770 (US Patent No. 8,907,499). Pet. 1–2.

We also note that Petitioner filed two additional petitions requesting *inter partes* review of U.S. Patent No. 8,791,581 (IPR2016-00703 and IPR2016-00706) for which we did not institute a review.

B. The '004 Patent

The '004 patent is directed generally to a “[t]hree-[d]imensional [s]tructure (3DS)” for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

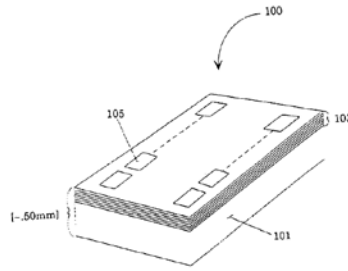


Figure 1a

Figure 1a shows 3DS memory device 100 having a stack of integrated circuit layers with a “fine-grain inter-layer vertical interconnect” between all circuit layers. *Id.* at 4:13–16. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:33–35. The ’004 patent discloses that “each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness.” *Id.* at 4:38–40. The ’004 patent further discloses that the

thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm²) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication.

Id. at 8:62–67.

Figure 1b is reproduced below.

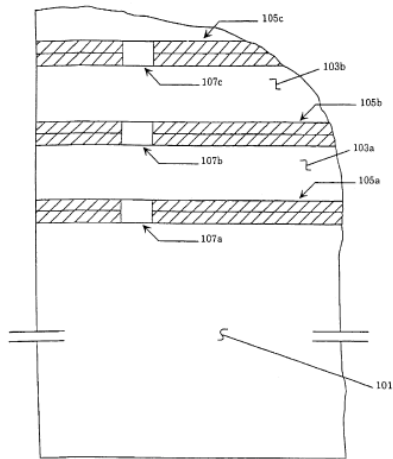


Figure 1b

Referring to Figure 1b, the '004 patent shows a cross-section of a 3DS DRAM integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:53–56. Bond and interconnect layers 105a, 105b, etc. are shown between circuit layers 103a and 103b. *Id.* at Fig. 1b. The '004 patent discloses that pattern 107a, 107b, etc. in the bond and interconnect layers 105a, 105b, etc. defines the vertical interconnect contacts between the integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4: 27–31. Additionally, the '004 patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:31–32.

Further, the '004 patent teaches that the “term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 μm .” *Id.* at 4:16–19. The fine-grain inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:21–23.

C. Illustrative Claim

Of the challenged claims, claim 1 is independent. Claim 1 is illustrative of the subject matter of the '004 patent:

1. A stacked integrated circuit comprising:

an integrated circuit;

a plurality of thinned substantially flexible integrated circuits, wherein at least one of the plurality of thinned substantially flexible integrated circuits comprises a low stress dielectric layer, further comprising:

a first substantially flexible integrated circuit having a first surface, wherein a plurality of first interconnections are located on the first surface;

a second substantially flexible integrated circuit having a second surface, wherein a plurality of second interconnections are located on the second surface, said first and second surfaces face each other, said plurality of first interconnection and said plurality of second interconnections are substantially aligned with each other, and said plurality of first interconnections and said plurality of second interconnections are electrically coupled together to form a plurality of vertical interconnections, including redundant vertical interconnections; and

a third interconnection electrically coupling the integrated circuit and at least one of the plurality of thinned substantially flexible integrated circuits, wherein the integrated circuit and the plurality of thinned substantially flexible integrated circuits are positioned in a stacked relation to one another, and wherein at least one of the substantially flexible integrated circuits comprises a substrate formed of a single crystal semiconductor.

II. ANALYSIS

A. Claim Construction

We interpret claims of an unexpired patent using the “broadest reasonable construction in light of the specification of the patent in which [the claims] appear[.]” 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131 (2016) (concluding the broadest reasonable

construction “regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office.”). The Board, however, may not “construe claims during IPR so broadly that its constructions are unreasonable under general claim construction principles . . . ‘[T]he protocol of giving claims their broadest reasonable interpretation . . . does not include giving claims a legally incorrect interpretation.’”

Microsoft Corp. v. Proxyconn, Inc., 789 F.3d 1292, 1298 (Fed. Cir. 2015).

“Rather, ‘claims should always be read in light of the specification and teaching in the underlying patent’” and “[e]ven under the broadest reasonable interpretation, the Board’s construction ‘cannot be divorced from the specification and the record evidence.’” *Id.* (citations omitted). We construe the challenged claims according to these principles.

“substantially flexible integrated circuits” (claim 1)

Based on the preliminary record, we did not construe expressly any term in the ’004 patent. Dec. on Inst. 7. At this juncture, based on the complete record, we construe “substantially flexible integrated circuit” as discussed below.

In reviewing the complete record for the instant proceeding, we note that the parties’ proposed constructions, arguments, and supporting evidence are very similar to those submitted in IPR2016-00386, IPR2016-00387, and IPR2016-00388. IPR2016-00386, -00387, and -00388 all involve related patents that share the same specification as the ’004 patent. In those cases, the construction of “substantially flexible semiconductor substrate” is at issue. See IPR2016-00386, Paper 68. Nonetheless, we note that the term “substantially flexible” is used to modify “substrate,” “circuit substrate,” and “integrated circuit” in several related patents that share the same specification. See IPR2016-00687, Paper 42 (Final Written

Decision construing “substantially flexible monocrystalline semiconductor substrate” and “substantially flexible integrated circuit.”).

Additionally, we observe that at the consolidated Oral Hearing, the parties presented arguments directed to the construction of “substantially flexible,” generally, without any indication of there being any difference in construction for any one of the consolidated cases (e.g., IPR2016-00386, -00387, -00388, and -00390). *See* Tr. 63, 5:7–19:15, 24:1–52:20, 56:20–66:9. Further, Petitioner’s counsel asserted that the claim construction of “substantially flexible” would be the same under both claim construction standards. Tr. 12:2–4 (Petitioner’s counsel indicating that the “we don’t see there as being a difference, whether BRI or Phillips is applied.”); *see generally* Tr. 11:21–13:16. Similarly, Patent Owner’s counsel at Oral Hearing indicated that the same construction would apply under broadest reasonable construction standard or the standard under *Phillips*. Tr. 50:10–14 (Q: “[I]n terms of the different claim construction standards, I understood that your position is that the same construction would apply under BRI or in District Court for substantially flexible.” A: “That’s correct.”).

Consistent with related proceedings (*see* IPR2016-00687), Petitioner construes the term “substantially flexible integrated circuit” to mean an “integrated circuit[s] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm² tensile or less.” Pet. 9. In response, Patent Owner proposes that “substantially flexible” should be construed to mean “largely able to bend without breaking.” PO Resp. 53–54 (citing Ex. 2165).

Our construction of “substantially flexible” and the basis for this construction are discussed in extensive detail in the Final Written Decisions issued in IPR2016-00386, IPR2016-00387, and IPR2016-00388. In those Final Written Decisions, having considered the intrinsic evidence (including the claim language, written description, and prosecution history of related patent applications) and extrinsic evidence, we determine that one of ordinary skill in the art in the context of the challenged patent would understand “substantially flexible” to mean, within the context of the subject matter of the patent, “largely able to bend without breaking.” *See* IPR2016-00386, Paper 68, 23–39. Given the shared specification of the patents and identical constructions and arguments presented by the parties, our analysis in IPR2016-00386, -00387, and -00388 applies with equal force here. Indeed, much of the relied upon evidence of record in those cases are also of record in this case. *See* Pet. 9; PO Resp. 53–54 (citing Ex. 2165).

Further, in the challenged claims here, even though the term “substantially flexible” modifies “integrated circuit,” (Ex. 1001, claim 1), we find that our construction of “substantially flexible” does not depart from the ordinary and customary meaning of “largely able to bend without breaking” in this context. As such, we construe “substantially flexible integrated circuit” to mean “an integrated circuit that is largely able to bend without breaking.”

Petitioner asserts that Patent Owner (then, Applicant) defined “substantially flexible integrated circuit” during examination of related patent applications. Pet. 10–16. Specifically, Petitioner cites to responses provided by Patent Owner during examination of U.S. Patent Application

No. 12/497,652 (“the ’652 application”).⁵ *Id.* Petitioner argues exclusively from the examination of the ’652 application—not the prosecution history of the ’542 patent at issue here.⁶ Even so, “[t]he prosecution history of a related patent can be relevant if, for example, it addresses a limitation in common with the patent” at issue. *Advanced Cardiovascular Sys., Inc. v. Medtronic, Inc.*, 265 F.3d 1294, 1305 (Fed. Cir. 2001).

In this regard, Petitioner contends that during examination of the ’652 application, the Applicant defined “substantially flexible” integrated circuit to require a sufficiently thin semiconductor material (e.g., 50 microns or less) and a low stress dielectric material of 5×10^8 dynes/cm² or less. Pet. 10 (citing Ex. 1023, 28). Petitioner further asserts that the Applicant confirmed this definition in a later September 26, 2013 response. *Id.* at 10 (citing Ex. 1021, 2–3).

Looking to the prosecution of the ’652 application, we are not persuaded that these statements from the Applicant amount to a clear and unmistakable definition or disavowal of claim scope. In the April 5, 2013 response, Applicant stated that

both Bertin and Kato fail to teach or suggest that at least one of the first and second *circuit layers* is substantially flexible, and the substrate thereof is a substantially flexible semiconductor substrate. Two features are required to achieve substantial flexibility. One is that the semiconductor material must be sufficiently thin, e.g., 50 microns or less. Bertin and Kato are believed to satisfy this requirement. The other is that the dielectric material used in processing the semiconductor

⁵ Petitioner refers to the prosecution history of U.S. Patent Application No. 12/497,653. However, Exhibits 1021 and 1023 are both responses from the examination of the ’652 application.

⁶ The ’652 application was ultimately expressly abandoned by the Applicant, and did not issue.

material must be sufficiently low stress. Otherwise, substantial flexibility is defeated. As set forth in the present specification, stress of 5×10^8 dynes/cm² or less has been demonstrated to satisfy this requirement.

Ex. 1023, 28 (emphasis added). In a subsequent response on September 26, 2013, Applicant stated

The *circuit layer* may be fabricated in a manner that undoes or defeats flexibility of the semiconductor substrate. More particularly, a circuit layer requires one or more dielectric layers. Dielectric material has an associated level of stress. For a circuit layer to be substantially flexible, Applicant has found that the dielectric material must have low tensile stress, for example, 5×10^8 dynes/cm² tensile.

Ex. 1021, 2–3 (emphasis added).

Initially, we note that Applicant's statements are directed to a "circuit layer," which is not the language at issue in this proceeding (i.e., "integrated circuit"). For this reason, we are not persuaded that Applicant's statements regarding "circuit layer" is controlling, or even informative, on whether Applicant defined or disavowed claim scope for different limitations "substantially flexible" integrated circuit. We note that Footnote 5 in the Petition cites to Ex. 1001, 1:23–24, 1:45–49, 3:16–17, and 4:13–15 for the proposition that the term "circuit layers" means integrated circuits stacked in layers. Pet. 9–10. These cited passages discuss integrated circuits generally, but do not define "circuit layer," or indicate otherwise that Applicant intended to define or disavow claim scope for "substantially flexible integrated circuit."

Further, even considering Petitioner's arguments and Applicant's statements, we determine that these statements do not define or disavow claim scope for these specific limitations at issue. Having reviewed these responses and the prosecution history of the '652 application, we understand

Applicant to have taken the position that the thinness of the *semiconductor material* and the stress level of dielectric material used in processing the *semiconductor material* are factors for substantial flexibility. The Applicant did not, however, define a “substantially flexible” integrated circuit in terms of the thinness of a semiconductor substrate, as Petitioner proposes. Rather, the Applicant’s statements refer to a *semiconductor material*, not a semiconductor substrate, and do not discuss polishing or smoothing. This is further confirmed in the September 2013 response in which the Applicant states that the flexibility of the semiconductor substrate does not control the flexibility of the circuit layer because the “circuit layer may be fabricated in a manner that undoes or defeats flexibility of the semiconductor substrate.” Ex. 1021, 2–3.

Additionally, we are not persuaded that the Applicant defined “substantially flexible” integrated circuit to include a stress range. Instead, Applicant states “[a]s set forth in the present specification, stress of 5×10^8 dynes/cm² or less has been demonstrated to satisfy this requirement.” Ex. 1023, 28. We view this statement as providing an example of low stress dielectrics that may allow for “substantially flexibility.” Our reading of Applicant’s statements is consistent with the Specification, which teaches that “[t]he thinned substantially flexible substrate circuit layers are *preferably* made with dielectrics in low stress (less than 5×10^8 dynes/cm²),” (Ex. 1001, 8:58–63) (emphasis added), and the 3DS memory stacks are “typically organized” with a “thinned and substantially flexible circuit with net low stress,” (*id.* at 4:30, 35–36)(emphasis added). Thus, we are not persuaded that Applicant’s statements constitute a clear and unmistakable definition or disavowal of claim scope sufficient for us to depart from the ordinary and customary meaning of “substantially flexible,” which is

“largely able to bend without breaking” as discussed above, and in further detail in the Final Written Decisions of IPR2016-00386, -00387, and -00389.

Further, Petitioner notes that during the prosecution of related U.S. Patent No. 8,907,499 (“the ’499 patent”), the Examiner objected that the term “substantially” rendered the pending claims unclear, resulting in claims that “do not clearly set for[th] the metes and bounds of the patent protection desired.” Pet. 12 (citing Ex. 1018, 4). Petitioner argues that the Applicant overcame the objection by arguing that “substantially flexible” is unambiguous because it is “clearly explained in the [S]pecification.” Pet. 12-13 (citing Ex. 1019, 9; Ex. 1020, 18:1–3).

Petitioner relies on the following language of the Applicant as defining substantially flexible:

With respect to the language “substantially flexible,” the meaning of this phrase as used in the claims is clearly explained in the specification including, **for example**, at page 18, lines 1-3.^[13] As described in this passage, a semiconductor substrate is caused to be substantially flexible by thinning it to 50 microns or less and polishing or smoothing the thinned semiconductor substrate to relieve stress. The phrase “substantially flexible” is used in the claims **consistent** with this description, which is unambiguous.

Pet. 13 (quoting Ex. 1019, 9) (emphasis added).

The statement itself indicates that the described grinding and polishing is an example of one way to achieve a substantially flexible substrate. As such, the cited statement does not evidence a clear and unmistakable intent to limit the scope of the term “substantially flexible **integrated circuit**,” as Petitioner contends. *See Aventis*, 675 F.3d at 1330 (requiring “a clear and unmistakable disavowal of claim scope” in the prosecution history to narrow the customary and ordinary meaning of a claim term).

Accordingly, based on the complete record, we determine that a “substantially flexible” integrated circuit means “an integrated circuit that is largely able to bend without breaking.”

B. Grounds Under 35 U.S.C. § 103

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). 35 U.S.C. § 103. The ultimate determination of obviousness under § 103 is a question of law based on underlying factual findings. *In re Baxter Int’l, Inc.*, 678 F.3d 1357, 1362 (Fed. Cir. 2012) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966)). These underlying factual considerations consist of: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) “secondary considerations” of non-obviousness such as “commercial success, long-felt but unsolved needs, failure of others, etc.” *KSR*, 550 U.S. at 406 (quoting *Graham*, 383 U.S. at 17–18).

We analyze the asserted grounds based on obviousness with the principles identified above in mind.

2. Level of Skill in the Art

Petitioner’s declarant, Dr. Paul D. Franzon, testifies that a person of ordinary skill in the art at the time of the invention would have had at least a bachelor’s degree in electrical engineering, material science, or equivalent thereof, and at least 3–5 years of experience in the relevant field, e.g., semiconductor processing. Ex. 1002 ¶¶ 52–53; Pet. 4–5. Patent Owner does

not dispute Petitioner's assessment. *See* Tr. 161:21–25, 112:5–14. We adopt Petitioner's proposed level of skill in the art, which is consistent with the '004 patent and the asserted prior art. For example, the '004 patent is directed to stacked integrated circuits and Leedy '695'695 is directed to methods for fabricating integrated circuits from membranes formed of low stress dielectric materials. Ex. 1001, 1:23–24; Ex. 1006, Abstract.

3. *Claims 1 and 20–23— Obvious over Finnila, Yu, and Leedy '695*

i. *Summary of Finnila (Ex. 1011)*

Finnila's Figure 8 is reproduced below.

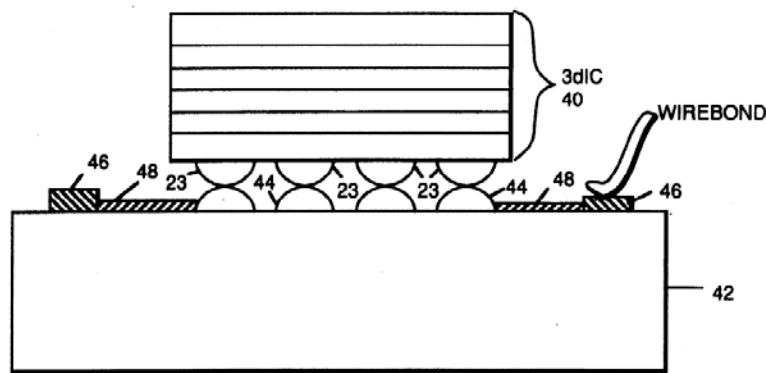


Fig. 8

Figure 8, not to scale, illustrates an embodiment of a 3D integrated circuit assembly that is connected to a larger diameter carrier wafer. Ex. 1011, 2:62–64. Finnila describes a “[p]rocess of manufacturing a three dimensional integrated circuit from stacked SOI wafers.” Ex. 1011, Title. Fabrication begins with “SOI wafer 1 that includes [] a silicon film 12 separated from a bulk silicon wafer 10 by an SiO₂ layer 11.” *Id.* at 3:4–6, Fig. 1. A silicon film of 0.2 micrometers to 10 micrometers is formed “by bonding two silicon wafers together with a fused oxide layer, and then thinning one of the wafers to form the thin film Si layer 12.” *Id.* at 3:8–21;

see also Ex. 1002 ¶¶ 80–90. The Si film can be characterized as being either a “thick” film, having a thickness greater than approximately one micron, or a “thin” film having a thickness less than approximately one micron. “In the thick film case, trenches are formed to provide vertical feedthroughs.” Ex. 1011, 3:35–40. “[I]soplanar oxide 13” is deposited to insulate active areas of the substrate from one another. *Id.* at 3:45–50, Fig. 2. Vertical trenches are created “by an anisotropic plasma etch process.” *Id.* at 3:50–55. “[T]he structure formed thus far is processed to form an integrated circuit. A CMOS process is described, but any other process, such as bipolar or bipolar/CMOS, may also be employed.” *Id.* at 4:17–20.

A “SiO₂ layer 17 is formed to serve as the gate oxide” of the transistors in the integrated circuitry. *Id.* at 4:26–28, Fig. 5. “A layer 20 of SiO₂ is then deposited over the” active area. *Id.* at 4:35–36. “Openings are defined and etched within the SiO₂ layer 20, and metallization 21 is deposited so as to contact the conductive feedthroughs 16.” *Id.* at 4:36–38, Fig. 5. An “insulating overglass layer 22” is deposited to passivate the integrated circuitry. *Id.* at 4:45–46. “Finally, openings are defined and etched into the overglass layer 22, and ‘topside’ indium bumps 23 are formed to contact the metalization 21 within the openings.” *Id.* at 4:46–49. The indium bumps are formed to be part of the “eventual interconnection to another wafer.” *Id.* at 4:50–52.

The completed wafer is temporarily bonded to the “temporary substrate” using a material that can be “readily removed” like wax, for example. *Id.* at 4:58–5:9, Fig. 6. The bottom of the wafer is etched or lapped to remove a portion of the bottom substrate—stopping at the silicon dioxide layer 11. *See id.* at 5:10–17. The result is a thin silicon film 12 sitting on the silicon dioxide layer 11.

“[C]onventional processing steps” are used “to define and etch contact openings and form bonding pads 28. *Id.* at 5:31–35. “[A] multiplicity of structures or wafers after stacking and interconnection [] form a 3d integrated circuit assembly 40.” *Id.* at Fig. 7, 6:27–29. A rigid Structure 1 is placed at the bottom of the stack to provide mechanical support. *Id.* at 6:29–33. Structures 2 and 3 are identical to the thinned SOI wafers disclosed above. *Id.* at 6:36–39. Structure 4 is the disclosed wafer modified such that “aluminum bonding pads 32 that have been fabricated on the topside surface instead of the indium bumps 23.” *Id.* at 6:39–43. The structures are aligned so that bottomside and topside bumps of respective structures are “brought into contact and fused together” using a “conventional cold welding process.” *Id.* at 6:44–52.

Gaps between the structures are then filled with “suitable material 34, such as an epoxy adhesive, to provide mechanical support.” *Id.* at 6:53–58.

ii. Summary of Yu (Ex. 1009)

Yu describes a three-dimensional integrated circuit structure for implementing a real-time microvision system. Ex. 1009, 831–32. “The system consists of a number of 2D LSIs vertically stacked using 3D LSI technology” *Id.* at 832. Yu’s Figure 1 is reproduced below.

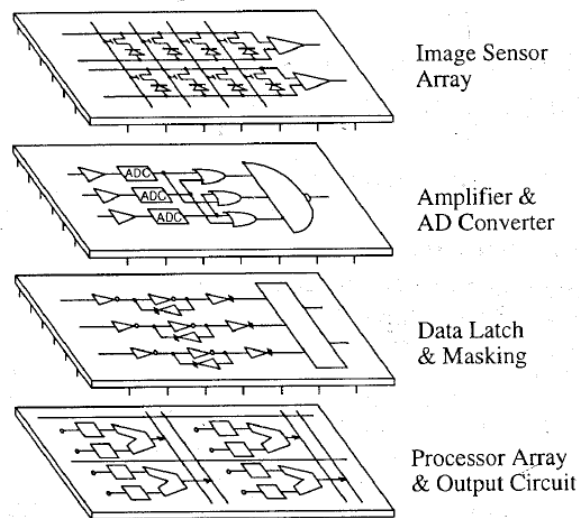


Figure 1: Basic concept of real-time microvision system with 3D integration structure

Figure 1 shows a basic concept of a real-time microvision system with a 3D integration structure.

In Yu's microvision system, substrates are ground and polished to thin the substrates to about 30 microns. *Id.* at 831–32 (“The Si substrate of the 2D-LSI which has the basic circuits is ground and polished to make thin wafer.”); *id.* at Abstract (“In fabrication, the grinding and chemical-mechanical polishing techniques are used to thin the wafer to 30 μm .”). Wafers then are bonded together using a combination of conductive micro-bumps and a UV-hardening adhesive. *Id.* at 834–35. (“The thinned wafer is bonded to a thick wafer using In/Au micro-bumps with the minimum size of 5 μm x 5 μm and UV hardening adhesive layer with thickness of 1 μm by forcing the z direction pressure after careful wafer alignment.”). The micro-bumps connect to buried interconnect structures that form vertical interconnects between vertically stacked circuitry. *Id.* at Fig. 8.

iii. *Summary of Leedy '695 (Ex. 1006)*

Leedy '695 relates to the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In the Abstract, Leedy '695 indicates that the disclosed integrated circuits are fabricated from flexible membranes “formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers.” *Id.* at Abstract. Leedy '695 also discloses forming a “tensile low stress dielectric membrane” on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy '695 further defines “[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8×10^8 dynes/cm² (preferably 1×10^7 dynes/cm²) in tension.” *Id.* at 11:33–37. Additionally, Leedy '695 discloses two chemical vapor deposition (CVD) process recipes for manufacturing “[s]tructurally [e]nhanced [l]ow [s]tress [d]ielectric [c]ircuit [m]embranes.” *Id.* at 11:51–65.

Referring to Figure 8, Leedy '695 discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.

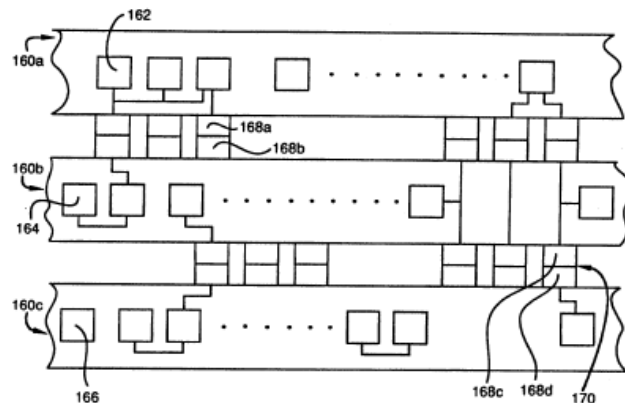


Fig_8

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 μm and 25 μm in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

iv. Analysis

Petitioner argues that claims 1 and 20–23 would have been obvious over the combination of Finnila, Yu, and Leedy '695. *See* Pet. 3. Below we discuss independent claim 1, which is illustrative of the subject matter of claims 20–23.

a) “substantially flexible integrated circuits”

Claim 1 is directed to a stacked integrated circuit that includes “a plurality of thinned substantially flexible integrated circuits, wherein at least one of the plurality of thinned substantially flexible integrated circuits comprises a low stress dielectric layer . . . [,] a first substantially flexible integrated circuit . . . [,] [and] a second substantially flexible integrated circuit.”

For these limitations, Petitioner argues that Finnila discloses a stacked structure with first and second substantially flexible integrated circuits, shown in Figure 7 of Finnila annotated by Petitioner (reproduced below). Pet. 27–41.

Based on the complete record, we do not find that Petitioner has adequately demonstrated that Finnila, modified by the thinning process described in Yu, teaches or suggests a “substantially flexible integrated circuit” as required in claim 1 (and dependent claims 20–23). Rather, Petitioner relies on its proposed construction of “substantially flexible integrated circuit” that requires a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed. Pet. 23, 28–29. Nonetheless, we have not adopted Petitioner’s construction, and have construed “substantially flexible integrated circuit” to mean “an integrated circuit that is largely able to bend without breaking.” Petitioner has not explained persuasively how the asserted prior art references (e.g., Finnila and Yu) teach or suggest that the disclosed integrated circuits, such as those shown in Figure 7 of Finnila, are largely able to bend without breaking.

Even assuming that a skilled artisan would have had reason to modify Finnila with the grinding and thinning process described in Yu, as proposed by Petitioner (*see* Pet. 22 (citing Ex. 1009, Abstract, 831–32, 834, Fig. 9; Ex. 1011, Abstract, 5:10–24; Ex. 1002 ¶ 109), Petitioner fails to establish that the disclosure of substrate thinness is sufficient to teach flexibility. A preponderance of the evidence establishes, however, that, in the context of semiconductor substrates and integrated circuits, mere thinning is not the same as flexibility—being able to bend without breaking. The Examiner, during the prosecution history of the now-abandoned ’652 application, agreed that flexibility is not the equivalent of mere thinning. Ex. 2168, 4 (The Examiner indicating that another reference “Bertin” failed to specifically teach wherein at least one of the first and second circuit layers is substantially flexible.). Neither party disputes this characterization of the

Examiner's statement. PO Resp. 34–36 (Patent Owner indicating that the “Examiner agreed that flexibility is not the equivalent of mere thinning.” (quoting Ex. 2168, 4)); Tr. 24:23–25:1 (Petitioner's counsel agreeing with Patent Owner's characterization that flexibility is not the equivalent of mere thinning).

Moreover, Petitioner's expert, Dr. Franzon, also testifies that the flexibility of an integrated circuit depend on a number of factors, only one of which is the physical dimensions of the substrate—width and thickness.

Ex. 1002 ¶ 71. Specifically, Dr. Franzon stated:

In the context of semiconductor processing, the flexibility of a semiconductor substrate depends on a number of factors, including, for example, the type of semiconductor substrate (e.g., while silicon and gallium arsenide are both semiconductors, they have different elastic moduli), the crystal orientation of the material (e.g., {100} and {111} silicon wafers have different elastic moduli), and the physical dimensions of the substrate (e.g., width and thickness). ***The flexibility of a more complex structure, such as an integrated circuit, that comprises multiple different layers of different materials (e.g., semiconductors, dielectrics, conductors), must take into account additional factors, including the type and dimensions of all the materials in that structure.***

Ex. 1002 ¶ 71 (emphasis added); see also Tr. 33:8–24 (Patent Owner's counsel at oral hearing discussing Dr. Franzon's testimony about the factors on which flexibility of a semiconductor substrate depends); Tr. 64:16–65:11 (Petitioner's counsel responding to Patent Owner's argument about Dr. Franzon's testimony regarding the various factors that would be considered to determine whether something is flexible). Common sense also supports a conclusion that thickness is not the only factor that determines whether a material is flexible. After all, a thicker piece of rubber is more flexible than a thinner potato chip.

Furthermore, even assuming that Leedy '695's low stress dielectric may be used in Finnila, which Petitioner has not adequately established as discussed in the next section, Petitioner has not demonstrated by a preponderance of the evidence that the combination of the substrate thinness and a low stress dielectric provides substantial flexibility for an integrated circuit. As Dr. Franzon stated, the "*flexibility of a more complex structure, such as an integrated circuit, that comprises multiple different layers of different materials (e.g., semiconductors, dielectrics, conductors), must take into account additional factors, including the type and dimensions of all the materials in that structure.*" Ex. 1002 ¶ 71 (emphasis). Given the complex nature of an integrated circuit, we are not persuaded that Petitioner's reliance solely on thinness of a substrate and stress of the dielectric is sufficient, on this record, to demonstrate by a preponderance of the evidence that the proposed modification of Finnila's various integrated circuits would render them "substantially flexible," or largely able to bend without breaking.

In addition, Petitioner's counsel argued at the Oral Hearing that the asserted art shows bendability in addition to thinning because the asserted "prior [art] mirrors the prior [preferred] embodiment" described in the '004 patent. Tr. 175:21–176:2. Petitioner's counsel did not identify with particularity any portion of the asserted prior art that "mirrors" the preferred embodiment in the challenged patent, nor even identify what preferred embodiments Petitioner's counsel had in mind as being mirrored by the prior art. Furthermore, Petitioner does not otherwise point to sufficient evidence to support its position that the prior art mirrors these embodiments in the challenged patent. *See generally* Tr. 175:13–180:16. For example, Petitioner contends that Dr. Franzon's testimony that the limitations are met by the prior art supports its position. Tr. 178:20–22 (Asking "is there any

evidence of record that any of the combinations that you propose would be the same as the preferred embodiment”?); Tr. 180:8–10 (Petitioner’s counsel responding that “[i]t’s Dr. Franzon’s testimony that those limitations are met by the prior art, and it’s the prior art itself, lining up with the claims.”).

Dr. Franzon’s testimony is also unhelpful in this regard. Dr. Franzon states that he simply applied the Petitioner’s proposed constructions in his analysis.⁷ Ex. 1002 ¶¶ 73–74. However, none of the applied constructions provided by Petitioner takes into account the ordinary and customary meaning of “substantially flexible integrated circuit,” which we have adopted.

We are mindful that Petitioner has the burden “to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)). Accordingly, we are not persuaded that Petitioner has demonstrated by a preponderance of the evidence that the prior art embodiments mirror the preferred embodiment in the challenged patent and, therefore, the prior art shows bendability. Furthermore, Petitioner’s counsel

⁷ Petitioner provided Dr. Franzon with three alternative proposed constructions of “substantially flexible integrated circuit/circuit substrate.” These being: (1) “an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm² tensile or less”; (2) “an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm , and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm² tensile or less”; and (3) “an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of 150 μm or less.” Ex. 1002 ¶¶ 76–77.

at the Oral Hearing confirmed that Petitioner's Reply to Patent Owner's claim construction position is that "first and foremost their claim construction is improper because it is indefinite, so in drafting the reply, . . . we couldn't figure out how to apply their construction to the prior art, so the claim construction portion of the reply explains why their construction is incorrect." Tr. 176:7–12.

For these reasons, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the combination of Finnila, Yu, and Leedy '695 would have conveyed to one of ordinary skill in the art the "substantially flexible integrated circuit," as recited in independent claim 1 and required in claims 20–23, which depend from claim 1.

b) Low Tensile Stress Dielectric Substitution

Additionally, for all of the challenged claims, Petitioner asserts that Finnila discloses thinned substantially flexible integrated circuits with a silicon dioxide (SiO₂) dielectric layer. Pet. 30 (Ex. 1011, 4:35–37, Figs. 5–6; Ex. 1002 ¶ 109). Petitioner acknowledges that Finnila does not explicitly teach that its dielectric layer has a low stress or a stress of 5×10^8 dynes/cm² tensile or less. Pet. 30. However, Petitioner argues that a skilled artisan would have been motivated to incorporate, into Finnila, one of the low stress dielectric deposition processes described in Leedy '695 because of the benefits realized by these processes, including improved surface flatness, improved ability to cope with later higher temperature processing steps, lower dielectric film stress, and improved structural integrity. *Id.* (citing Ex. 1002 ¶ 109⁸).

⁸ Notably, Petitioner merely cites Dr. Franzon's twenty-four page claim chart for element, without otherwise discussing or summarizing it. Board rules prohibit incorporating by reference arguments from one document into

For the reasons that follow, we determine that Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have had a reason to combine the references in the manner proposed by Petitioner to arrive at the claimed invention and would have had a reasonable expectation of success.

1. Reason to Substitute

Petitioner refers to many general benefits and advantages of Leedy '695's disclosed dielectric, but does not explain how these advantages apply to the specific dielectric material in Finnila. For example, Petitioner asserts that

Leedy '695 provides express motivations for modifying Finnila to incorporate Leedy '695's low tensile stress dielectric material. *See KSR*, 550 U.S. at 415-21. Leedy '695 explains that low tensile stress is important because otherwise "surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane." *See, e.g.*, Ex. 1006 at 5:63-6:5; Ex. 1002 at ¶¶ 91-103, 109 (claim 1b, p. 73). Accordingly, as discussed above, Leedy '695 describes processes for depositing silicon oxide or silicon nitride dielectrics, preferably having a tensile stress of 1×10^7 dynes/cm². *See, e.g.*, Ex. 1006 at 11:33-37. Leedy '695 explains that the described low tensile stress dielectrics can advantageously be used to insulate circuit devices and interconnect metallization, while at the same time increasing structural integrity and durability. *See, e.g., id.* at Abstract, 1:53-62, 2:9-31, 2:66-3:3, 3:56-4:13, 30:36-42, 45:49-46:26, 46:52-47:33, Figs. 32a-32d. Leedy '695 also explains that such dielectrics advantageously have lower stress. *Id.* at 6:30-33; *see also* Ex. 1002 at ¶ 109 (claim 1b, pp. 72-73).

another document. 37 C.F.R. § 42.6(a)(3); *see Cisco Sys., Inc. v. C-Cation Techs., LLC*, Case IPR2014-00454, slip op. at 7–10 (PTAB August 29, 2014) (Paper 12) (Informative) (not considering arguments in declaration that were not made in the Petition but only incorporated by reference).

We first observe that Petitioner incorrectly attributes benefits of the entire Membrane Dielectric Isolation (MDI) process to the single low stress dielectric component. *See* Pet. 24 (citing Ex. 1006, 1:53–62, 2:9–31, 2:66–3:3, 3:56–4:13, 30:36–42, 45:49–46:26, 46:52–47:33). For example, column 2, lines 9 through 31 of Leedy '695 provides

[t]he primary objectives of the MDI fabrication technology disclosed herein are the cost effective manufacture of high performance, high density integrated circuits and integrated circuit interconnect with the elimination or reduction of detrimental electrical effects on the operation of individual circuit devices (e.g. diodes, transistors, etc.) *by completely isolating with a dielectric material* each such circuit device from the common substrate upon which they are initially fabricated, and therefore, from each other, and to provide a more versatile and efficient physical form factor for the application of integrate circuits. Some of the benefits of the *MDI IC fabrication process* are the elimination or reduction of substrate current leakage, capacitive coupling and parasitic transistor effects between adjoining circuit devices. The *MDI IC fabrication process* benefits extend to several other categories of IC fabrication such as lower IC processing costs due to fewer IC isolation processing steps, greater IC transistor densities through the capability to use established IC processing techniques to fabricate interconnect metallization on both sides of a MDI IC circuit membrane, and greater IC performance through novel transistor structures.

Ex. 1006, 2:9–31 (emphasis added). Here, Leedy '695 indicates that these advantages are due to the MDI fabrication processes (e.g., Method #1 and Method #2), which are multi-step processes that include, but are not limited to, the formation of a low stress dielectric and optional isolation with a dielectric material. Ex. 1006, 7:1–11:24; *see also id.* at 2:66–3:3 (“It is the *combination* of the use of low stress free standing dielectric films with the

appropriate processing qualities and membrane or thin film single crystalline (monocrystalline), polycrystalline or amorphous semiconductor substrate formation that provides much of the advantage of the MDI IC fabrication process.”) (emphasis added); *see, eg., id.* at 3:56–4:13 (Listing benefits to fabricating an IC with the *MDI process*).

Looking to another passage cited by Petitioner, column 30, lines 36 through 42 of Leedy ’695 also refers to the MDI IC process in its entirety for the ability to form a flexible and elastic membrane structure. Ex. 1006, 30:36–42. Thus, rather than supporting Petitioner’s position that the *low stress dielectric* provides flexibility, this cited passage also refers to the MDI process as a whole and does not support Petitioner’s assertion that Leedy ’695’s low stress dielectric alone imparts these benefits.

Additionally, other citations by Petitioner discuss advantages of its low tensile stress dielectric flexible *membrane* or its *membrane dielectric isolation fabrication* techniques. *See, e.g.,* Ex. 1006, Abstract (“In another version, the flexible membrane is used as support and electrical interconnect for conventional integrated circuit die bonded thereto, with the interconnect formed in multiple layers in the membrane.”); 1:53–62 (“In accordance with the invention, an integrated circuit is formed on a tensile low stress dielectric membrane comprised of one layer or a partial layer of semiconductor material in which are formed circuit devices and several layers of dielectric and interconnect metallization. Also, a structure in accordance with the invention is a tensile member of semiconductor material in which are formed circuit devices with multiple layers of tensile low stress dielectric and metallization interconnect on either side of the semiconductor membrane.”); *Id.* at 5:63–6:5 (“There are many established methods for forming thin semiconductor substrates or membranes. The *MDI process* requires that the

semiconductor membrane forming process (thinning process) produce a highly uniform *membrane* typically less than 2 μm thick and that the surface tension of the semiconductor membrane be in low tensile stress. If the *membrane* is not in tensile stress, but in compressive stress, surface flatness and *membrane* structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane.”) (emphasis added); *Id.* at 6:30–33 (“Thermally formed silicon dioxide forms as a strongly compressive film and most deposited dielectrics currently in use form typically with compressive surface stress. High temperature silicon dioxide and silicon nitride dielectric deposited films with tensile surface stress levels 100 times less than their fracture strength have been demonstrated as large area free standing membranes consistent with the requirements of the MDI process.”); *see id.* at 46:52–47:33 (teaching that the dielectric circuit *membranes* are optically transparent and thin, allowing the circuit membranes to be aligned very accurately prior to bonding; and MDI circuit membrane can be cut from the circuit membrane due to the net low stress of the circuit membrane). Thus, the probative value of Petitioner’s argument is diminished because Leedy ’695 does not support Petitioner’s position that the low stress dielectric alone imparts the advantages described in the cited passages directed to the membrane structure, membrane isolation techniques, or membrane fabrication process.

Further, Petitioner’s reliance on express reasons that low tensile stress is important for Leedy ’695’s process for constructing Leedy ’695’s low tensile stress dielectric membranes (e.g., surface flatness) has minimal probative value in supporting Petitioner’s proposed substitution of Finnilla’s dielectric material, which is fabricated in a different process relying on a

conventional, rigid substrate. This is because Petitioner does not explain sufficiently why or how the importance of low tensile stress for Leedy '695's process for constructing low tensile stress dielectric membranes bears on why one of ordinary skill in the art would have substituted Leedy '695's dielectric material for Finnila's dielectric. For example, Petitioner does not explain why a person of ordinary skill in the art would replace the specific SiO₂ material in Finnila with a low stress dielectric where the dielectric material disclosed in Finnila already insulates. Tr. 85:11–12 (“So I think at a fundamental level all dielectric layers perform an insulating function.”). Indeed, Petitioner does not argue that Finnila's dielectric material experiences surface flatness or other structural problems that would be improved by the use of a low stress dielectric, or how this substitution would be accomplished in light of the fabrication processes disclosed in Leedy '695. *See* Pet. 23–26.

Petitioner additionally argues that

Finnila and Leedy '695 both seek advantageous IC performance by constructing 3D ICs from 2D ICs. *See, e.g.*, Ex. 1009 at 831; Ex. 1006 at Abstract, 2:9-14, 45:49-59, 47:31-33. One of ordinary skill would thus have looked to the teachings in Leedy '695 to improve Finnila. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-21 (2007); Ex. 1002 at ¶¶ 91-103, 109 (claim 1b, pp. 73-74).

Pet. 24. We understand Petitioner's position to be that Finnila and Leedy '695 were directed generally to similar general goals and problems in the semiconductor fabrication arts, and a skilled artisan would have looked at both references to improve upon fabrication processes. However, based on the complete record here, Petitioner's “reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not

imply a motivation to pick out those two references and combine them to arrive at the claimed invention.” *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017). While the references need not explicitly provide a reason for the asserted substitution, Petitioner must, nevertheless, explain why a person of ordinary skill in the art would have substituted Leedy ’695’s low stress dielectric for the specific dielectric in Finnila. “[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015).

We recognize that “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill” (*KSR*, 550 U.S. at 417). Here, however, Petitioner’s testimony is conclusory without explaining what types of improvements in 3D integrated circuits would have motivated one of ordinary skill in the art to make Petitioner’s proposed substitution of Leedy ’695’s dielectric in Finnila’s device. *In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) (“The factual inquiry whether to combine references must be thorough and searching.”)).

In addition, Petitioner cites to paragraphs 91 through 101 and paragraph 109 of Dr. Franzon’s declaration testimony without further discussing or explaining the relevance of the testimony. *See* Pet. 23–25. Paragraphs 91 through 98 of Dr. Franzon’s declaration provide a summary of Leedy ’695 teachings including, in paragraph 96, a description of the

“two process recipes for manufacturing ‘structurally enhances low stress dielectric circuit membranes.’” See Ex. 1002 ¶ 91–98. In paragraphs 99 through 100, Dr. Franzon’s statements largely track those presented on page 24 of the Petition in that Dr. Franzon asserts Leedy ’695’s dielectric provides the benefits of “electrical isolation of circuit devices and interconnect metallization, higher temperature tolerance, improved surface flatness, increased structural integrity, and better durability.” Ex. 1002 ¶ 100 (citing Ex. 1006, 2:9–31, 2:37–40, 3:56–4:13, 5:63–6:5, 6:26–33, 6:48–58, 45:49–46:26). However, these cited passages, like those cited on page 24 of the Petition, attribute the benefits of Leedy ’695 invention to the MDI process, isolation technique, and membrane fabrication. For example, column 3, line 56 through column 4, line 13 provides:

The benefits to fabricating an IC with the *MDI process* are significant over prior art methods, some of these benefits being:

1. Complete electrical isolation of semiconductor devices.
2. Vertical semiconductor device structures.
3. Lower processing costs through lower processing complexity or fewer device isolation processing steps.
4. Conformal mask lithography through the membrane substrate.
5. Control of depth of focus during lithography exposure due to control of substrate thickness.
6. Application of interconnect metallization to both sides of the IC.
7. Through-membrane (substrate) interconnect metallization routing.
8. Three dimensional IC structures through the bonding of circuit membrane IC layers.

9. Efficient conductive or radiant cooling of IC components of circuit membrane.

10. Direct optical (laser) based communication between parallel positioned membrane ICs.

11. Higher performance ICs.

12. Vertical semiconductor device structure formation.

13. Novel selective epitaxial device formation.

Ex. 1006, 3:56–4:13 (emphasis added). As such, the probative value of Dr. Franzon’s testimony, in this regard, is diminished by the incomplete explanation of how the benefits Leedy ’695 describes arising from its described multi-step MDI process can be attributed solely or directly to the low stress dielectric.

Additionally, in paragraph 101 of Dr. Franzon’s declaration, he asserts that it would have been advantageous to replace thermal silicon oxide of Yu (or Finnila in combination with Yu) used to insulate through-vias with the oxide of Leedy ’695 because “[u]sing the lower stress CVD process of Leedy ’695 to insulate through vias would be advantageous because it would reduce the probability of cracking and warpage due to elevated stress in the vias.” Ex. 1002 ¶ 101. Initially, we note that in the Petition, Petitioner states without explanation that “Leedy ’695 discloses using PECVD, which was a commonly available deposition technique that could have been used in place of the techniques for growing dielectrics described in Yu to obtain the predictable result of stacked integrated circuits having low tensile stress dielectrics.” Pet. 26 (citing Ex. 1002 ¶¶ 91–103). In other words, this appears to be an alternative combination of Finnila, Yu, and Leedy ’695 that involves the modification of Yu’s silicon oxide rather than Finnila’s dielectric as initially proposed on pages 23–25 of the Petition.

Nonetheless, even with this alternative theory, Petitioner does not

explain adequately how one of ordinary skill in the art would have modified the three references to reach the claimed invention. First, Petitioner does not explain how the modification of Yu's silicon oxide has any bearing on the integrated circuits disclosed in Finnila, which are relied upon by Petitioner for the first and second integrated circuits recited the challenged claims. Rather, for this particular challenge, Petitioner argues that Yu is relied upon for its disclosed two-step grinding and thinning process. Pet. 29–30. Thus, Petitioner fails to explain how its proposed combination of Yu's thinning process with Finnila implicates Yu's silicon oxide for replacement with Leedy '695's low stress dielectric. Second, even considering Dr. Franzon's testimony in paragraph 101, which the Petition cites but does not explain on page 26, we find that Dr. Franzon's testimony to be conclusory in that it asserts without supporting citation or explanation that replacing Yu's thermal silicon oxide would reduce the probability of cracking and warpage. In paragraph 101, Dr. Franzon cites to Leedy '695 for the assertion that Leedy '695 discloses a CVD process for a lower stress dielectric. Ex. 1002 ¶ 101. However, Dr. Franzon does not point to any support in the record for the further statement that Yu's silicon oxide in “through-vias” would benefit from the proposed substitution. *Id.*

In addition, Petitioner cites to paragraph 103 of Dr. Franzon's declaration testimony without further discussing or explaining the relevance of the testimony. See Pet. 26 (citing Ex. 1002 ¶¶ 91–103). Dr. Franzon's testimony in paragraph 103 is conclusory. Ex. 1002 ¶ 103 (asserting Finnila, Yu, and Leedy '695 “are in the same technology field of three-dimensional integration and address similar challenges relating to the stacking of integrated circuit devices.”) (citing Ex. 1006, 45:49–53; Ex. 1011, Title, Abstract, 1:8–11, 6:27–43, 7:40–53, Figs. 2–10; Ex. 1009, 831–32, Figs. 8–

9). Although “any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed” (*KSR*, 550 U.S. at 420), Dr. Franzon’s single sentence assertion lacks specifics as to what those similar challenges are, and he only provides a list of citations to various references without further explanation or analysis as to how those citations support his assertion. Thus, we weigh Dr. Franzon’s testimony accordingly. *See In re Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) (“[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.”); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Petitioner further argues that the replacement of one dielectric for another is a matter of simple substitution because Leedy ’695 uses a plasma-enhanced chemical vapor deposition (“PECVD”) to deposit the low tensile stress dielectrics, and “PECVD was a well-known and widely used technique that provided conformal deposition at lower substrate temperatures and at faster rates compared to other depositions techniques.” Pet. 25 (citing Ex. 1002 ¶ 95, Ex. 1006, 11:28–63; Ex. 1039, 2; Ex. 1040, 171). Petitioner adds that “dielectrics can easily be used in place of other dielectrics, including thermal oxide insulators, which Leedy ’695 indicates have high stress.” Pet. 25 (citing Ex. 1006, 6:30–33, 8:59–64; Ex. 1002 ¶¶ 91–103).

Petitioner further relies on other prior art references to support its position that PECVD was compatible with various stages in the fabrication process. *See* Reply 10–15. On this point, Petitioner’s position is that

Finnila's dielectric could have been simply substituted with the PECVD dielectric in Leedy '695. *Id.*; *see also id.* at 3 (Heading: "3D IC Dielectrics Could Have Been Replaced with Leedy '695's PECVD LTSDS").

However, again, Petitioner argues a substitution *could* be made, which is not sufficient to show that a substitution *would* have been made. *In re Giannelli*, 739 F.3d 1375, 1380 (Fed. Cir. 2014) (indicating that the Board should have determined whether it would have been obvious to modify the prior art apparatus to arrive at the claimed invention and finding the mere capability to do so insufficient).

In Reply, Petitioner contends, without support of expert or citation to law, that "the lack of disclosure of 'tensile' dielectrics or how to make a [low tensile stress dielectric, aside from incorporating a § 102(b) reference, indicates that it was trivial to substitute Leedy '695's [low tensile stress dielectrics] in place of other dielectrics. Reply 2. We disagree with Petitioner—one does not necessarily follow from the other.

Similarly, we disagree with Petitioner's conclusory position that the technical obstacles to incorporating Leedy '695's dielectric into prior art integrated circuits are not "real or the challenged claims would not be enabled." Reply 2–3; *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements."). Leedy '695 sets forth sixty-four pages of figures and more than forty-six columns of text to describe his membrane dielectric isolation integrated circuit fabrication techniques and did not also need to explain in detail specific ways to substitute its techniques for those in a conventional integrated circuit fabrication process to obtain the patent. Notably, Petitioner's position is based on attorney argument. Accordingly, we determine Petitioner's

conclusory assertions in its Reply are insufficient to overcome Patent Owner's well-reasoned and supported arguments.

2. *Expected Success*

In addition, it is Petitioner's burden to demonstrate both "that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." *Intelligent Bio-Systems, Inc. v. Illumina Cambridge LTD.*, 821 F.3d 1359, 1368–1369 (Fed. Cir. 2016) (citing *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.* 688 F.3d 1342, 1360 (Fed.Cir.2012)). In considering the record before us, we take into account the complexity of integrated circuit fabrication. Without question, fabrication of integrated circuits is complex technology. No less than four prior art text books, ranging from 600 pages to nearly 850 pages and describing the fabrication of integrated circuits, have been provided as background references, principally in support of the declaration testimony of Alexander D. Glew, Ph.D., Patent Owner's expert. Ex. 1040 (Wolf et al., *Processing for the VLSI Era, Volume 1–Process Technology* (1986)); Ex. 2146 (Wolf, *Silicon Processing for the VLSI Era, Volume 2 – Process Integration* (1990)); Ex. 2159 (W. R. Runyan & K. E. Bean, *Semiconductor Integrated Circuit Processing Technology* (1990)); Ex. 2162 (*Multi-Chip Module Technologies and Alternatives: The Basics* (Daryl Ann Doane & Paul D. Franzon eds., 1993)). Also of record are two other background references of around 100 pages and 650 pages. Ex. 2169 (*Handbook of Semiconductor Manufacturing Technology* (Robert Doering & Yoshio Nishi eds., 2nd ed. 2008)); Ex. 2158 (Peter van Zant, *Microchip Fabrication* (4th ed., 2000)).

Patent Owner, with liberal citations to those references, other prior art references, and declaration testimony of its expert explaining the same, explains how integrated circuits are fabricated to illustrate the complexity of the process and the detailed planning and decisions required for fabrication. PO Resp. 3–30. According to Dr. Glew integrated circuit fabrication is a “complex manufacturing process . . . that can be generally divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. Ex. 2166 ¶ 23 (citing Ex. 2158, 13^{9,10}); *see also* PO Resp. 5 (citing Ex. 2166 ¶ 23; Ex. 2158, 13). In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and then sliced into thin disks called “wafers.” PO Resp. 6 (citing Ex. 2166 ¶ 25; Ex. 2158, 13–14). Most helpful is the explanation of different techniques for producing and layering dielectrics (PO Resp. 16–30), including growing dielectrics using thermal oxidation (PO Resp. 18–19), depositing dielectrics (PO Resp. 19–20), and a comparison of thermal chemical vapor deposition (PO Resp. 20–21) with plasma-enhanced chemical vapor deposition (PO Resp. 21–22).

⁹ We follow Patent Owner’s practice of citing to page numbers of the text, rather than the pagination of Exhibit 2158.

¹⁰ We recognize that the text cited by Dr. Glew (Ex. 2158) is the fourth edition and has publication dates of 1984, 1997, and 2000. Dr. Glew relies on this text as supporting his testimony and recognizes the earliest effective filing date claimed by the challenged patent of April 4, 1997. Ex. 2166 ¶ 104. Petitioner does not contend that Dr. Glew’s reliance on this text is in error or that Dr. Glew’s summary of integrated circuit fabrication is faulty. Nor does Petitioner contend that the general explanation of integrated circuit fabrication found in the text, and used by Dr. Glew to support his testimony, changed between the 1997 edition of the text and the later editions.

We understand from the testimony of Dr. Glew and reference citations that a typical fabrication of a semiconductor integrated circuit may include thousands of process steps (Ex. 2166 ¶¶ 29–30 (citing Ex. 2158, 14, 29–31, 71)). Explaining different techniques for producing and layering dielectrics, Dr. Glew explains that “different dielectric materials are layered throughout the fabrication process, with each dielectric layer having a different location, each being created at a different stage, and each serving a different specific purpose.” Ex. 2166 ¶ 61 (citing Ex. 2158, 72–73, 79, 81–82); *see generally* PO Resp. 16–30 (discussing different techniques for producing and layering dielectrics). Dr. Glew continues:

These dielectrics can be produced and layered using a large number of techniques, and the particular technique used will greatly impact the properties of the resulting dielectric (and, therefore, its usefulness for any particular dielectric layer and purpose). For example, dielectric silicon dioxide layers can be produced and applied in hundreds of different ways, each resulting in a silicon dioxide with different properties (and potential uses). (Ex. 2158 at 154; Ex. 2146 at 225, 306; Ex. 2159 at 55).

Ex. 2166 ¶ 62. Thus, selecting a dielectric material involves choosing particular fabrication techniques that are part of an overall fabrication process for a particular integrated circuit.

Turning again to the Petition, Petitioner asserts that

[g]iven Leedy ’695’s explanation that such dielectrics are versatile, in that they are able “to withstand a wide range of IC processing techniques and processing temperatures (of at least 400 C.) without noticeable deficiency in performance” (Ex. 1006 at 2:37-40; *see also id.* at 1:50-52, 5:32-33), one of ordinary skill in the art would have reasonably expected success combining the teachings of Finnila and Leedy ’695. *See KSR*, 550 U.S. at 415-421. In addition, as mentioned above, Leedy ’695 discloses using PECVD, which was a commonly available

deposition technique that could have been used in place of the techniques for growing dielectrics described in Yu to obtain the predictable result of stacked integrated circuits having low tensile stress dielectrics. Ex. 1002 at ¶¶ 91-103.

Pet. 25–26.

Based on the complete record, we determine that Petitioner’s arguments and conclusion are insufficiently supported. The fact that plasma-enhanced chemical vapor deposition was well-known, commonly available, and has recognized advantages does not sufficiently support Petitioner’s conclusion in view of the complexities of integrated circuit fabrication. Furthermore, Petitioner’s assertion that “dielectrics can be easily used in place of other dielectrics” (Pet. 25) is not supported by the record. Petitioner’s citations to Leedy ’695 (Ex. 1006, 6:30–33, 8:59–64) do not on their face, without explanation, support Petitioner’s position.

Petitioner’s citation to column 6 indicates: “[t]hermally formed silicon dioxide forms as a strongly compressive film and most deposited dielectrics current in use form typically with compressive surface stress.” Ex. 1006, 6:30–33. Petitioner’s citation to column 8 similarly requires further explanation regarding how it supports Petitioner’s assertion that “dielectrics can be easily used in place of other dielectrics” (Pet. 22): “[t]he thermal oxide isolation created by the LOCOS¹¹ method may change the net tensile surface stress of the semiconductor (substrate) membrane layer. The deposition of low stress dielectric films on either side of the semiconductor layer prior to LOCOS processing will offset most compressive effects of the oxide formation.” Ex. 1006, 8:59–64. The fact that Leedy ’695 discloses that the use of a particular method—LOCOS—could be used in either of its two recipes for membrane dielectric isolation fabrication does not, without

¹¹LOCOS (LOCAl Oxidation of Silicon) isolation method.” Ex. 1006, 8:43.

more, suggest that Leedy '695's dielectrics "could be easily" used in place of other dielectrics.

Even setting aside the fact that Petitioner cites but does not discuss its expert's testimony that Petitioner cites in its Petition,¹² Dr. Franzon does not explain how the cited portions of Leedy '695 show "its dielectrics can be easily used." The fact that Leedy '695's deposition processes may be compatible with conventional integrated circuit fabrication methods, (Ex. 1002 ¶ 102) does not in itself indicate that Leedy '695's alternative processes would have been used in place of Finnila's techniques, particularly in view of the complexities of integrated circuit fabrication.

Dr. Franzon further testifies that Leedy '695 explains its *membrane* can be used with "most of the established integrated processing methods for the fabrication of circuit devices and interconnect metallization" or its membrane "is compatible with most higher temperature [integrated circuit] processing techniques." Ex. 1002 ¶ 102. Again, for purposes of addressing Petitioner's arguments, we overlook the fact that Petitioner cites to this testimony without discussing it in its Petition. Dr. Franzon's testimony, while indicating Leedy '695's *membrane* can be used with some conventional methods, does not adequately support Petitioner's contention that "dielectrics can be easily used in place of other dielectrics" (Pet. 25); *see also* Ex. 1006, 2:37–40 ("The ability to make a large area flexible thin film free standing dielectric *membrane*, typically framed or suspended or constrained at its edges by a substrate frame or ring, or bonded frame or ring. This *membrane* is able to withstand a wide range of IC processing techniques and processing temperatures (of at least 400° C.) without

¹² 37 C.F.R. § 42.6(a)(3) (prohibiting incorporation by reference from one document to another).

noticeable deficiency in performance.”). Thus, we conclude that Petitioner’s citation to Dr. Franzon’s testimony is unavailing. Pet. 25 (citing Ex. 1002 ¶¶ 91–103).

Additionally, Dr. Franzon testifies that

it would have been advantageous to replace the thermal silicon oxide of Yu (or Finnila in combination with Yu) used to insulate through vias with the oxide of Leedy ’695 because Leedy ’695 uses a conformal chemical vapor deposition (CVD) process that is inherently lower stress and would be capable of coating the through vias. That Leedy ’695 discloses a CVD process is evident because the disclosed dielectric membranes are produced using a Novellus Systems Concept One apparatus, which is CVD equipment. *See, e.g.*, Ex. 1006 at 11:28-32. Further, the process recipes disclosed in Leedy ’695 specify a temperature of 400° C, a pressure of about 2 Torr, and specify values for high frequency (HF) and low frequency (LF) RF power, all of which are indicative of a CVD process. *See, e.g., id.* at 11:52-62. Using the lower stress CVD process of Leedy ’695 to insulate through vias would be advantageous because it would reduce the probability of cracking and warpage due to elevated stress in the vias.

Ex. 1002 ¶ 101. Again, this testimony is not explained or discussed in the Petition. Nonetheless, even considering Dr. Franzon’s testimony, we find these statements to be conclusory and too general. Dr. Franzon cites to Leedy ’695 for the proposition that Leedy ’695 discloses a CVD process. *Id.* Assuming Dr. Franzon’s reading of the reference to be correct, Dr. Franzon does not explain with citation or support from the record why one of ordinary skill in the art would have understood that Leedy ’695’s CVD process “would reduce the probability of cracking and warpage due to elevated stress in the vias” when applied to Yu. *Id.* Indeed, Dr. Franzon does not explain how “elevated stress” is a concern or a problem in Yu’s or Finnila’s disclosed device, structure, and techniques. *Id.*

Further, we note that Dr. Franzon refers generally to a “thermal silicon oxide of Yu” and “coating the through vias.” Ex. 1002 ¶ 101. However, for this specific challenge, Dr. Franzon does not explain what specific dielectric in Yu’s structure is the proposed target for the asserted combination based on Finnila, Yu, and Leedy ’695. In this regard, the Petition is even more lacking in specificity and clarity. In particular, the Petition states, without any explanation, that “as mentioned above, Leedy ’695 discloses using PECVD, which was a commonly available deposition technique that could have been used in place of the techniques for growing dielectrics described in Yu to obtain the predictable result of stacked integrated circuits having low tensile stress dielectrics.” Pet. 26 (citing Ex. 1002 ¶¶ 91–103). This reasoning is insufficient and too general, in view of the complex technology of integrated circuit fabrication and the well-reasoned and well-supported opposing testimony of Patent Owner’s expert, Dr. Glew.

Moreover, both Dr. Franzon and Dr. Glew agree that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties. *See, e.g.*, Ex. 2164 (Dr. Franzon deposition transcript), 69:17–19 (Q. Do the different methods result in different properties of the dielectrics? A. Yes.”); Ex. 2166 (Dr. Glew’s declaration) ¶ 139 (Identifying eighteen properties¹³ of

¹³ Dr. Glew identifies the following properties of dielectrics: dielectric constant, breakdown of field strength, leakage, surface conductance, moisture absorption or permeability to moisture, stress, adhesion to aluminum, adhesion to other dielectric layers, stability, etch rate, permeability to hydrogen, amount of incorporated electrical charge or dipoles, amount of impurities, quality of step coverage, thickness and uniformity of the film, ability to provide good doped uniformity across a

dielectrics; testifying that one of ordinary skill in the art would consider many of those factors when choosing a dielectric); *see also* PO Resp. 59–60 (discussing Dr. Franzon’s and Dr. Glew’s testimony); *see also* Ex. 2146 (Wolf Volume 2), 195 (Table 4.4 listing eighteen desired properties of interlevel dielectrics); PO Resp. 33 (citing Ex. 2146, 195); Tr. 125:12–17 (Patent Owner’s counsel referencing Ex. 2146, 195 (table of eighteen properties)). Dr. Franzon acknowledges dielectric properties should be considered when selecting a dielectric. Ex. 2164 (Dr. Franzon deposition transcript), 59:25–60:2, 61:10–13, 79:25–80:3, 91:8–12); Ex. 2164, 78:23–79:1 (Dr. Franzon testifies that “[t]here is likely quite a long list of factors that go into choosing between them [dielectrics], and an engineer would weigh those using his knowledge and skills.”). This weighs against a finding that one of ordinary skill in the art would have reasonably expected success in substituting Leedy ’695’s low tensile stress dielectric material for Bertin ’754’s dielectric layer 60 and interconnect insulators.

In reviewing Dr. Franzon’s testimony, we are mindful of the sentiment that “[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton.” *KSR*, 550 U.S. at 421. However, in his deposition, Dr. Franzon responded to many questions about dielectrics by indicating research would be needed to answer the particular question and he did not consider how the different processes would affect dielectric properties, which weighs against a finding that one of ordinary skill would have a reasonable expectation of success in substituting Leedy ’695’s dielectric. *See* Ex. 2164, 133:5–135:5. For example, an excerpt of Dr. Franzon’s testimony is provided below:

wafer, defect density, and amount of residual constituents that “outgas” during later processing. Ex. 2166 ¶ 139.

Q. What are some of the differences in the properties of a silicon dioxide grown through plasma-enhanced CVD as opposed to grown through oxidation?

A. I haven't researched a detailed answer to that question. There is many variations on the formulas for these CVDs.

Q. But you understand that there is a difference. Right?

THE WITNESS: There may be differences, depending on the details of the formulations and the processing parameters and so forth.

Q. What are some of the details of the formulation parameters that you would need to know in order to answer that question?

A. I haven't researched the answer to that question in general, so I would need a variety of references that I can't anticipate in order to properly answer that question.

Ex. 2164, 133:8–134:3; *see, e.g.*, Ex. 2164, 71:9–73:17 (“Q. Do you consider oxidation to be a growth or a deposition?” A. I haven't researched that answer to the question. Thermal oxidation [requires] oxygen atoms in contact with the surface, at least, in order to grow the thermal oxide. But there's a lot of variance on thermal oxide techniques that I haven't researched. Q. And can you give me an example of some variants in thermal oxide techniques? A. One example that comes to mind is a wet oxide deposition versus a dryer one. Q: And does a wet oxide deposition versus a drier one cause different arrangements of the bonds in silicon dioxide? A: I haven't researched the answer to that question. . . . Q: Do you know if wet oxide versus dry oxide would affect the dielectric constant of silicon dioxide? A. I haven't researched the answer to that question. Q. Do you know if PDCVD [sic] would result in a different dielectric constant than thermal oxide? A. I haven't researched the answer to that question.”).

We are not suggesting that a reasonable expectation of success in the complex field of integrated circuit fabrication would preclude one of ordinary skill in the art from researching aspects of making the combination. Rather, we find the number of Dr. Franzon's responses that research is required weighs against Petitioner's conclusory assertions in this regard, which were discussed previously. *See, e.g.*, Ex. 2164, 71:9–73:17, 73:18–74:4, 24:6–22, 65:10–14, 129:7–9, 130:17–25, 134:20–25; Pet. 19–20. Thus, considering the complex field of integrated circuit fabrication and taking into account the level of ordinary skill in that art as set forth by Petitioner, there is insufficient evidence of record to conclude that ordinary creativity would support a conclusion that one of ordinary skill in the art would have had expected success of substituting Leedy '695's dielectric material for Finnilla's or Yu's dielectric material.

3. Expert Testimony

In general, we weigh Dr. Glew's testimony concerning the reasons why one of ordinary skill in the art would not have reason to combine the references in the manner proposed by Petitioner more heavily than Dr. Franzon's declaration testimony that one of ordinary skill in the art would have done so and would have had a reasonable expectation of success.

Dr. Franzon's testimony, in large measure, is that Leedy '695 identifies advantages of "the disclosed dielectric deposition techniques" (Ex. 1002 ¶ 100); the advantages of a chemical vapor deposition process; and the references are in the same technological field and "address similar challenges relating to the stacking of integrated circuit devices." *See* Ex. 1002 ¶¶ 101, 103; Pet. 23–26 (citing Ex. 1002 ¶¶ 91–103, 109). Dr. Franzon's testimony, however does not adequately address why one of ordinary skill in the art would use Leedy '695's fabrication process to make

Finnila's stacked integrated circuit with Leedy '695's low tensile stress dielectric, which is the combination on which Petitioner relies for the recited dielectric material characterized by the particular tensile stress claimed.¹⁴

See id.

Notably, too, Dr. Franzon does not specify or otherwise explain the “similar challenges relating to the stacking of integrated circuit devices” he refers to in his testimony. Ex. 1002 ¶ 103. We, however, recognize that “any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *KSR*, 550 U.S. at 420. Noting, however, that references are in the same general field and address similar unnamed challenges in the circumstances of this case—involving complex technology of integrated circuit fabrication, we conclude that Dr. Franzon's testimony about the benefits of Leedy '695's general process is insufficient to support Petitioner's position regarding dielectric substitution of particular structures in Finnila. *See In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) (“The factual inquiry whether to combine references must be thorough and searching.”)); *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014) (“While an analysis of any teaching, suggestion, or motivation to combine elements from different prior art references is useful in an obviousness analysis, the overall inquiry must be expansive and flexible.”).

¹⁴ We address Petitioner's asserted modification of Yu's dielectric in greater detail in the section regarding Petitioner's combination of Yu, Blonder, and Leedy '695.

In contrast, Patent Owner relies on Dr. Glew’s testimony, which is more specific as to reasons why one of ordinary skill in the art would not have combined Leedy ’695’s fabrication process to make Finnila’s (or Yu’s) stacked integrated circuit having Leedy ’695’s low tensile stress dielectric. For example, Patent Owner relies on Dr. Glew’s testimony that one of ordinary skill would understand that Yu’s or Finnila’s dielectric “are touching circuit components including MOSFET gate, source and drain, they must also have high purity” and using the plasma-enhanced CVD described by Leedy ’695 would be problematic “because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining . . . steps^[15] without changing its form.” Ex. 2166 ¶¶ 151–152 (citing Ex. 2159, 139).

¹⁵ Petitioner and Patent Owner dispute what is meant by front-end and back-end processing steps, we are not persuaded that resolving this issue is necessary to determine whether a skilled artisan would have had reason to combine the asserted references in the manner proposed by Petitioner to arrive at the claimed invention, and whether one of ordinary skill in the art would have had a reasonable expectation of success of doing so. Even assuming that Leedy ’695 dielectrics are used in the front-end of the line and Finnila’s and Yu’s dielectrics could be used in the front-end of the line (as Petitioner contends), this does not explain, as Petitioner must, why one of ordinary skill in the art would have combined the references in the manner proposed by Petitioner to arrive at the claimed invention and would have reasonable expectation of success in doing so. The mere capability of combining Leedy ’695’s plasma-enhanced chemical vapor deposition process to deposit low tensile stress dielectric material in place of Finnila’s or Yu’s process is not our inquiry. Rather our inquiry is whether Petitioner has demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have had a reason to do so. *See, e.g., In re Giannelli*, 739 F.3d 1375, 1380 (Fed. Cir. 2014) (“In the context of the claimed rowing machine, however, the mere capability of pulling the handles is not the

Furthermore, Dr. Glew's testimony is supported by his well-reasoned explanation, citations to background references and asserted prior art. For example, Dr. Glew's declaration testimony cites three pages of the Zant text (Ex. 2158) and a page of the Runyan text (Ex. 2159) to support his statement that "if a silicon dioxide dielectric contacts circuit components, the silicon dioxide must be high-purity to not damage the circuit components." Ex. 2166 ¶ 128 (citing Ex. 2158, 104–106; Ex. 2159, 73). That statement, supported by two reference citations, in turn, supports Dr. Glew's conclusion: "[t]hus, because Finnila describes that layer 20 is deposited over polysilicon gate electrodes 18, and doped source/drain regions 19a and 19b (Ex. 1011 at 4:34–36), a person of ordinary skill would understand that it must have high purity" and is formed using high-temperature thermal CVD). Ex. 2166 ¶¶ 127–128.

We also note the absence of further declaration testimony by Dr. Franzon opposing Dr. Glew's position or otherwise supporting Petitioner's Reply to Patent Owner's Response. For the reasons noted previously, because of the complexity of integrated circuit fabrication, expert testimony is critical to explaining why one of ordinary skill in the art would have had a reason to combine the references as the claims require. *Kinetic Concepts*, 688 F.3d at 1369. This is particularly true in view of Dr. Glew's well-reasoned and supported testimony. Petitioner's attorney-argument in its Reply consists of conclusory statements with insufficiently explained citations to Leedy '695 and other references and is insufficient to establish that one of ordinary skill in the art would have had reason to

inquiry that the Board should have made; it should have determined whether it would have been obvious to modify the prior art apparatus to arrive at the claimed rowing machine.").

combine the references in the manner proposed by Petitioner. *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (a petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements”).

For example, in Reply to Dr. Glew’s testimony supporting Patent Owner Response, Petitioner’s attorneys assert that plasma-enhanced chemical vapor deposition dielectrics are compatible with silicon substrates and high temperature processes. Reply 11–16 (citing Ex. 1082, 1006, 1088)). We recognize that sometimes expert testimony is not always necessary. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1369 (Fed. Cir. 2012) (indicating expert technology is not always required) (citing *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1240 n.5 (Fed. Cir. 2010) (“However, as we [have] noted . . . ‘expert testimony regarding matters beyond the comprehension of layperson is sometimes essential,’ particularly in cases involving complex technology. In such cases, expert testimony may be critical, for example, to establish . . . the existence (or lack thereof) of a motivation to combine references.” (internal citations omitted)) (alteration in original)). Accordingly, because of the complexity of integrated circuit fabrication discussed above, however, attorney-argument addressing Dr. Glew’s well-reasoned and supported testimony does not persuade us that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner or would have had a reasonable expectation of success.

4. Conclusion

As described above, Petitioner in its Petition made arguments as to why one of ordinary skill in the art would have been motivated to combine Finnla, Yu, and Leedy ’695 to achieve the purported claimed invention, and

why a skilled artisan would have had a reasonable expectation of success. Patent Owner provided well-reasoned arguments based on testimonial evidence, background references, and prior art references identifying shortcomings in Petitioner's position. There is evidence from both sides regarding the presence or absence of a reason to combine Finnila and Leedy '695 in the manner proposed by Petitioner to arrive at the claimed invention and regarding whether one of ordinary skill in the art would have had a reasonable expectation of success.

Here, Petitioner has the burden to show, by a preponderance of the evidence, a reason why one of ordinary skill in the art would have combined the prior art references to arrive at the invention and why one of ordinary skill in the art would have had a reasonable expectation of success of combining the references to meet the limitations of the claimed invention. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) ("The reasonable expectation of success requirement refers to the likelihood of success in combining the references to meet the limitations of the claimed invention. . . . [O]ne must have a motivation to combine [the references] accompanied by a reasonable expectation of achieving what is claimed in the patent-at-issue."). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim"))).

It is well-settled that identifying a reason to combine references is not confined to a "rigid or mandatory formula[]." *KSR*, 550 U.S. at 419; *see In*

re Nuvasive, 842 F.3d 1376, 1383 (Fed. Cir. 2016). Moreover, “[w]hile an analysis of any teaching, suggestion, or motivation to combine elements from different prior art references is useful in an obviousness analysis, the overall inquiry must be expansive and flexible.” *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014).

Furthermore, the inquiry cannot be met by conclusory statements but rather must be “thorough and searching.” *See In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) (“The factual inquiry whether to combine references must be thorough and searching.”)). Additionally, we must be careful not to allow hindsight reconstruction of references to reach the claimed invention without adequate explanation as to how or why the references would be combined to produce the claimed invention. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368 (Fed. Cir. 2012) (quoting *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 n.3 (“We must still be careful not to allow hindsight reconstruction of the references to reach the claimed invention without any explanation as to how or why the references would be combined to produce the claimed invention.”)).

We find Petitioner’s arguments regarding its proposed combination to be incomplete. In the context of these cases, it is insufficient to propose incorporating the material of Leedy ’695 without providing sufficient detail as to the combined process to produce the claimed combination. We recognize that it is axiomatic that bodily incorporation is not required. *See, e.g., In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (“It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of the

elements.”). To be clear, we are not suggesting that Petitioner must explain how Leedy ’695’s entire membrane dielectric isolation process would or could be included with Finnila’s fabrication process. Rather, we find Petitioner’s explanation to be incomplete because it does not adequately explain how Finnila’s fabrication process would be changed to use Leedy ’695’s dielectric material. This is necessary, at least, to support a conclusion that one of ordinary skill in the art would have had reasonable expectation of success of using Leedy ’695’s dielectric material in place of Finnila’s dielectric material.

For these reasons above, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 1 and 20–23, would have been unpatentable over the asserted combination of Finnila, Yu, and Leedy ’695.

4. Claims 1 and 20–23 — Obvious over Finnila, Blonder, Yu, and Leedy ’695

i. Summary of Blonder (Ex. 1068)

Blonder is directed to chip-to-chip interconnections for integrated circuits where the interconnections “are made via gold pads on each chip that are bonded to corresponding gold pads on a silicon wafer chip carrier.” Ex. 1068, Abstract. Blonder teaches that the pads on the chips are “characterized by texturing (roughening) with a feature with a feature size of the order of a micrometer or less, so that each of the pads on the chip can be attached to each of the pads on the carrier by compression bonding at room temperature . . .” Ex. 1068, Abstract. Figure 1 is reproduced below.

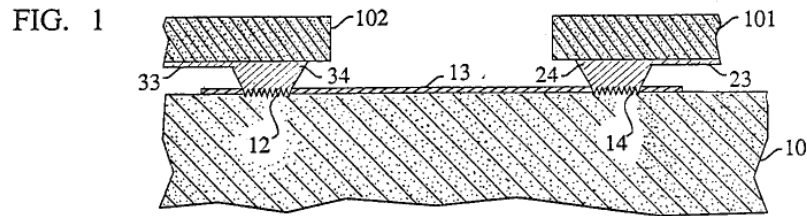


Figure 1 depicts semiconductor integrated circuit chips 101 and 102 mounted circuit-face-down to silicon wafer carrier 10. Ex. 1068, 3:59–61. Each chip 101, 102 is interconnected via chip pads 24, 34 bonded to carrier pads 12, 14, respectively. *Id.* at 3:57-4:1. This allows for “gold-to-gold welding of chip pads to carrier pads.” *Id.* at 4:8–10.

Blonder further discloses that “in view of the relatively large number of pads, either non-electrically-functional (‘dummy’) pads or electrically functional redundant pads can be used for increased strength of attachment, increased electrical reliability, and improved heat-sinking.” Ex. 1068, 6:23–28.

ii. *Analysis*

Petitioner argues that claims 1 and 20–23 would have been obvious over the combination of Finnila, Yu, Blonder, and Leedy. *See* Pet. 3, 39–40. For this challenge, Petitioner argues

[t]o the extent there is any doubt about whether *Finnila* discloses the claim 1d requirement that the plurality of vertical interconnections includes redundant vertical interconnections (see Ex. 1011 at 7:19–24; Ex. 1002 at ¶¶ 114–15), *Blonder* removes that doubt by discussing that “either non-electrically-functional (‘dummy’) pads or electrically functional redundant pads can be used for increased strength of attachment, increased electrical reliability, and improved heat-sinking.” Ex. 1068 at 6:23–28; Ex. 1002 at ¶ 116–17.

Pet. 41. Petitioner argues that given Finnila’s specific disclosure of “redundant circuitry and interconnections,” a person of skill in the art would

have been motivated to include Blonder’s specific notation that the interconnections between stacked chips could be provided redundantly. *Id.* at 39 (citing Ex. 1011, 7:19–24; Ex. 1068, 6:23–28; Ex. 1002 ¶¶ 116–117).

Petitioner relies on the alleged disclosure in Blonder for “redundant vertical interconnections” features recited in independent claim 1. However, Petitioner relies on the asserted combination of Finnila, Yu, and Leedy ’695, as discussed above, for the “substantially flexible integrated circuit” and “low stress dielectric layer” elements recited in independent claim 1 and dependent claims 20–23. Petitioner does not propose or argue that Blonder cures any of the deficiencies discussed above with respect to Petitioner’s combination based on Finnila, Yu, and Leedy ’695. Pet. 39–42.

Accordingly, for the same reasons discussed above, we find that Petitioner has not demonstrated by a preponderance of the evidence that the combination of Finnila, Yu, Blonder, and Leedy ’695 teach or suggest these claimed features.

5. *Claims 1 and 20–23 — Obvious over Yu, Blonder, and Leedy ’695*

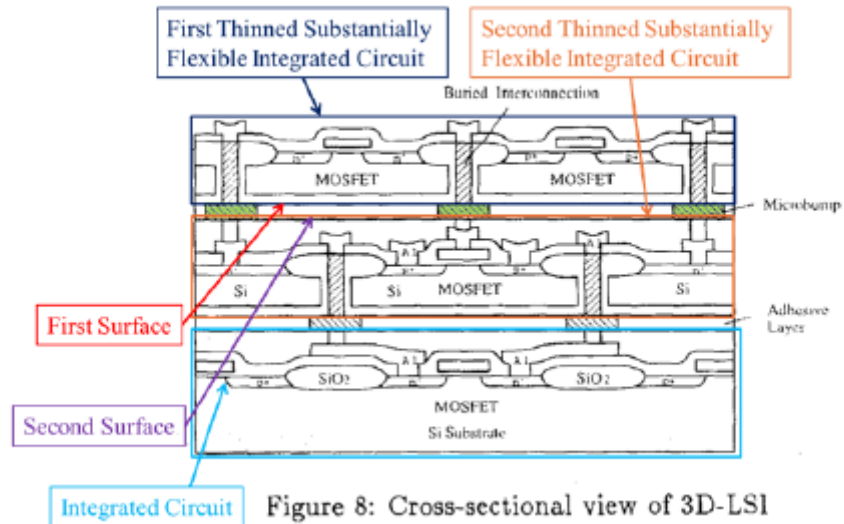
i. *Analysis*

Petitioner argues that claims 1 and 20–23 would have been obvious over the combination of Yu, Blonder, and Leedy ’695. *See* Pet. 3, 42–58. Below we discuss independent claim 1, which is illustrative of the subject matter of claims 20–23.

a) *“substantially flexible integrated circuit”*

Claim 1 is directed to a stacked integrated circuit that includes “a plurality of thinned substantially flexible integrated circuits, wherein at least one of the plurality of thinned substantially flexible integrated circuits comprises a low stress dielectric layer . . . [,] a first substantially flexible integrated circuit . . . [,] [and] a second substantially flexible integrated

For these limitations, Petitioner provides an annotated version of Figure 8 from Yu to show first and second surfaces of substantially flexible integrated circuits with a plurality of interconnections in the form of microbumps.



Pet. 53. Petitioner adds that the “In/Au micro-bumps’ would be understood by those of skill in the art as including an indium layer and a gold layer. Ex. 1002 at ¶ 128.” *Id.* at 53–54. Petitioner further argues Blonder’s disclosure of redundant pads teaches the “redundant vertical interconnections” recited in claim 1. Pet. 54. Petitioner, again, relies on Leedy ’695’s disclosed dielectrics to satisfy the claimed “low stress dielectric layer” recited in claim 1. Pet. 50–51. Petitioner provides several reasons for this proposed combination, including many of those discussed above for the combination of Finnila, Blonder, Yu, and Leedy. See Pet. 42–47.

Similar to Petitioner’s arguments regarding its combination of Finnila, Yu, and Leedy ’695, Petitioner presents arguments that claims 1 and 20–23 would have been obvious over Yu and Leedy ’695 using its proposed narrow

construction of a substantially flexible integrated circuit that includes a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and a dielectric material with a stress of 5×10^8 dynes/cm² tensile or less. *See, e.g.*, Pet. 42, 47–50 (arguments for independent claim 1). Petitioner asserts that Yu’s *thinned* wafer includes a field oxide that one of ordinary skill in the art would have been motivated to modify to incorporate one of the low stress dielectric deposition processes described in Leedy ’695. *Id.* at 48–50.

As discussed previously, we agree with Patent Owner’s proposed construction for “substantially flexible integrated circuit” as “an integrated circuit that is largely able to bend without breaking.” In Reply, Petitioner does not contend that Yu discloses the recited substantially flexible integrated circuit as construed by Patent Owner. As discussed previously with respect to Finnila, a preponderance of the evidence establishes, however, that, in the context of circuit fabrication, mere thinning is not the same as flexibility—being able to bend without breaking. Furthermore, even assuming that a low stress dielectric may be used in Yu, which Petitioner has not established as discussed below, Petitioner has not demonstrated by a preponderance of the evidence that the combination of the substrate thinness and a low stress dielectric provides substantial flexibility for an integrated circuit. As Dr. Franzon stated:

In the context of semiconductor processing, the flexibility of a semiconductor substrate depends on a number of factors, including, for example, the type of semiconductor substrate (e.g., while silicon and gallium arsenide are both semiconductors, they have different elastic moduli), the crystal orientation of the material (e.g., {100} and {111} silicon wafers have different elastic moduli), and the physical dimensions of the substrate (e.g., width and thickness). *The flexibility of a*

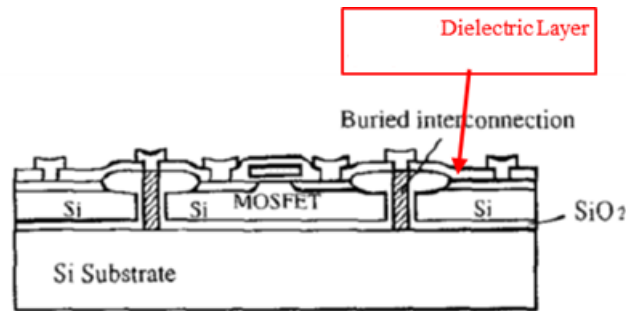
more complex structure, such as an integrated circuit, that comprises multiple different layers of different materials (e.g., semiconductors, dielectrics, conductors), must take into account additional factors, including the type and dimensions of all the materials in that structure.

Ex. 1002 ¶ 71 (emphasis). Given the complex nature of an integrated circuit, we are not persuaded that Petitioner's reliance solely on thinness of a substrate and stress of the dielectric is sufficient, on this record, to demonstrate by a preponderance of the evidence that the proposed modification of Yu's various integrated circuits would render them "substantially flexible," or largely able to bend without breaking.

Accordingly, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the use of Yu's thinned substrate of less than 30 μm , or the use of a thinned substrate with a low stress dielectric, would have conveyed to one of ordinary skill in the art the "substantially flexible integrated circuit," as recited in claim 1.

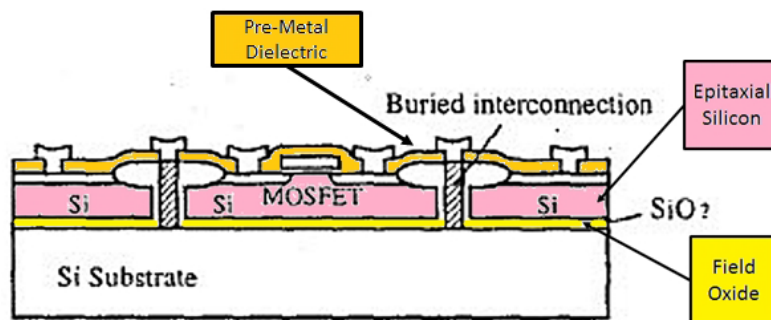
b) *Low Tensile Stress Dielectric Substitution*

Petitioner contends that Yu discloses a dielectric layer as shown in Petitioner's annotated version of Yu's Figure 9 (reproduced below) and that one of ordinary skill in the art would have had several reasons to modify the processes and device in Yu such that the dielectrics used therein would be characterized by the [required] tensile stress based on the disclosure of Leedy '695. Pet. 42–47 (citing Ex. 1002 ¶¶ 91–103). Petitioner's annotated version of Figure 9 from the Petition is shown below:



Pet. 50.

To start, we note that Patent Owner asserts that Yu includes a “field oxide” and “pre-metal dielectric,” both shown in annotated Figure 9 provided in the Patent Owner Response (reproduced below).



PO Resp. 46. With respect to the SiO₂ field oxide, Patent Owner argues that “[o]ne of ordinary skill would understand that, by definition, a silicon dioxide field oxide is grown directly on the ‘Si Substrate’ at high temperatures using thermal oxidation.” PO Resp. 46 (citing Ex. 2166 ¶ 136, Ex. 2158, 102–103). In this regard, Dr. Glew also explains that, because Yu’s field oxide is “touching the silicon substrate, the silicon dioxide ‘field oxide’ must have high purity, which again means a person skilled in the art would understand it was grown at high temperatures using thermal oxidation.” Ex. 2166 ¶ 137. Dr. Glew adds that replacing Yu’s thermally grown field oxide with a plasma-enhanced CVD process would result in a dielectric that is not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high

temperatures of the remaining . . . steps without changing its form.” Ex. 2166 ¶ 139 (citing Ex. 2169, 29–30). Notably, Dr. Glew testifies that plasma-enhanced chemical vapor deposition (a known technique used by Leedy ’695) cannot be used with Yu’s techniques because “positive ions present in the plasma can strike and damage the surface of the silicon substrate.” Ex. 2166 ¶ 139 (citing Ex. 2159, 139).

In response, Petitioner contends that Leedy ’695’s plasma-enhanced CVD process was compatible with various stages in the fabrication process and that 3D IC dielectrics *could* have been replaced with Leedy ’695’s low stress dielectrics. Reply 3–15. On this point, Petitioner’s position is that Yu’s thermally grown oxide dielectric or pre-metal dielectric could have been simply substituted with the PECVD dielectric in Leedy ’695. *Id.*; see also *id.* at 3 (Heading: “3D IC Dielectrics Could Have Been Replaced with Leedy ’695’s PECVD LTSDS”). However, Petitioner argues a substitution *could* be made, which is not sufficient to show that a substitution *would* have been made. Moreover, even assuming that a substitution could be made (e.g., assuming that Leedy ’695’s PECVD process could be used to replace the field oxide in Yu’s device structure), Petitioner fails to provide a sufficient reason for why a skilled artisan *would* have made this combination.

Much of Petitioner’s Petition, Reply, and Dr. Franzon’s testimony focuses on the benefits of Leedy ’695’s *membrane* structure and MDI *process*. Nonetheless, Petitioner does not explain adequately how these benefits apply to the dielectric described in Leedy ’695, and more importantly, why and how one of ordinary skill in the art would have applied Leedy ’695’s teaching to the specific dielectrics, devices, and processes identified in Yu for Petitioner’s asserted combination. In short, the

reasoning in the Petition is incomplete and falls short of providing an adequate showing required under the preponderance of the evidence standard to demonstrate obviousness of the challenged claims.

We note also that much of Dr. Franzon's testimony on which Petitioner relies relates to both Finnila and Yu, which we have addressed above in the context of Finnila. *See, e.g.*, Ex. 1002 ¶ 101 ("In particular, it would have been advantageous to replace the thermal silicon oxide of Yu (or Finnila in combination with Yu) used to insulate through vias with the oxide of Leedy '695 because Leedy '695 uses a conformal chemical vapor deposition (CVD) process that is inherently lower stress and would be capable of coating the through vias. That Leedy '695 discloses a CVD process is evident because the disclosed dielectric membranes are produced using a Novellus Systems Concept One apparatus, which is CVD equipment. *See, e.g.*, Ex. 1006 at 11:28-32. Further, the process recipes disclosed in Leedy '695 specify a temperature of 400° C, a pressure of about 2 Torr, and specify values for high frequency (HF) and low frequency (LF) RF power, all of which are indicative of a CVD process. *See, e.g., id.* at 11:52-62. Using the lower stress CVD process of Leedy '695 to insulate through vias would be advantageous because it would reduce the probability of cracking and warpage due to elevated stress in the vias.").

For substantially similar reasons to those discussed previously, Dr. Franzon's testimony in paragraphs 91 through 103 do not support sufficiently a conclusion that one of ordinary skill in the art would have combined the references in the manner proposed by Petitioner. For example, as discussed above, the fact that Yu (and Finnila) and Leedy '695 are directed to similar technology, or even that one of ordinary skill in the art was aware of the references, does not in itself establish that one of ordinary

skill in the art *would* have replaced Yu's oxide with Leedy '695's low stress dielectric. Further, in the complicated technology field of integrated circuit fabrication, Dr. Franzon's testimony in paragraph 103 is too general in asserting the reason of "they are in the same technological field of three-dimensional integration and address similar challenges relating to the stacking of integrated circuit devices" without discussing, for instance, what particular challenges are addressed. Ex. 1002 ¶ 103. Although Dr. Franzon lists a string of citations, he does not explain or otherwise reference those citations.

Additionally, while we agree that Leedy '695 may disclose advantages of its described MDI fabrication process and low stress dielectric membrane (*see* Ex. 1002 ¶ 100), Petitioner has not explained how these purported benefits apply to Yu's oxide, or, why one of ordinary skill in the art would have been motivated by these advantages to replace that specific dielectric in Yu's structure. In other words, Petitioner does not explain sufficiently why or how the importance of low tensile stress for Leedy '695's process for constructing low tensile stress dielectric membranes bears on why one of ordinary skill in the art would have substituted Leedy '695's dielectric material for Yu's layer 20. Moreover, as discussed in detail previously, Petitioner characterizes Leedy '695's teaching to be about low tensile stress dielectrics. The citations by Petitioner, however, discuss advantages of its low tensile stress dielectric flexible membrane or its membrane dielectric isolation fabrication techniques.

Here, too, the probative value of Petitioner's argument is diminished because Petitioner credits Leedy '695's low tensile stress dielectric material with the benefits disclosed by Leedy '695 for its membrane dielectric isolation process for fabricating integrated circuits. In similar fashion, Dr.

Franzon attributes benefits of Leedy '695's claimed invention to the dielectric and dielectric deposition technique; however, the cited passages of Leedy '695 describe the benefits of the *membrane* structure and the MDI process as a whole. See Ex. 1002 ¶ 100 (citing Ex. 1001, 2:9–31, 2:37–40, 3:56–4:13, 5:63–6:5, 6:48–58, 45:49–46:26).

Further, we weigh accordingly Dr. Franzon's testimony that one of ordinary skill in the art would have replaced the thermal silicon oxide of Yu with Leedy '695's oxide to reduce "the probability of cracking and warpage due to elevated stress in the vias"; and Leedy '695's low tensile stress dielectric would be able to withstand a wide range of processing techniques and processing temperatures." Pet. 42–45 (citing Ex. 1002 ¶ 101). As discussed previously, Dr. Franzon does not provide the underlying basis, through, for example, explanation or citation to the record, for these statements. While Dr. Franzon cites to Leedy '695 for the proposition that Leedy '695 discloses a conformal CVD process and process recipes, Dr. Franzon does not provide the basis for his assertions that (1) these processes are "inherently lower stress and would be capable of coating the through vias"; and (2) "[u]sing the lower stress CVD process of Leedy '695 to insulate through vias would be advantageous because it would reduce the probability of cracking and warpage due to elevated stress in the vias." Ex. 1002 ¶ 101. "Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight." 37 C.F.R. § 42.65(a).

Additionally, we do not find that Petitioner has adequately explained why one of ordinary skill in the art would have replaced the pre-metal dielectric in Yu's device with Leedy '695's low stress dielectric. Here, Petitioner argues that Leedy '695 describes processes for depositing silicon

oxide or silicon nitride dielectric films having tensile stress of preferably 1×10^7 dynes/cm² that are compatible with conventional integrated circuit fabrication methods. Pet. 50–51 (citing Ex. 1002 ¶¶ 94–97). Petitioner adds that

ordinary skill in the art would have been motivated to modify the processes and device disclosed in *Yu* to incorporate one of the low stress dielectric deposition processes described in *Leedy* '695 because of the many benefits realized by these processes, including improved surface flatness, improved ability to cope with later higher temperature processing steps, lower dielectric film stress, and improved structural integrity. Ex. 1002 at ¶ 128 (claim 1b). When so incorporated, the result is that each of the plurality of thinned layers of *Yu* teaches or suggests one of the claimed thinned substantially flexible integrated circuit, and each comprises a low stress dielectric layer, as is required by this claim limitation. *Id.*

Pet. 51. However, as discussed above, we are not persuaded that Dr. Franzon's testimony of capability sufficiently demonstrates by a preponderance of the evidence that a skilled artisan *would* have made the proposed dielectric replacement. *In re Giannelli*, 739 F.3d 1375, 1380 (Fed. Cir. 2014) (indicating that the Board should have determined whether it would have been obvious to modify the prior art apparatus to arrive at the claimed invention and finding the mere capability to do so insufficient). Further, for the reasons discussed above, we are not persuaded that the benefits of the membrane or MDI process described in *Leedy* '695 are attributed to the *dielectric deposition process*. See Pet. 51.

Further, we observe that Dr. Franzon's testimony that different chemical vapor deposition methods result in different dielectric properties weighs against Petitioner's argument that one dielectric deposition process is easily interchangeable with another process. Ex. 2164, 69:3–19. The cited

portion of Dr. Franzon’s testimony (Ex. 1002 ¶¶ 94–97, 128) does not discuss Yu’s use of a deposition process, the implications of Yu’s disclosure on one of ordinary skill in the art’s awareness of using dielectric layers, or a purported motivation to look to other references as Petitioner contends. As discussed previously, in this complex technology area of integrated circuit fabrication, expert testimony is critical. *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1369 (Fed. Cir. 2012) (indicating expert technology is not always required) (citing *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1240 n.5 (Fed. Cir. 2010) (“However, as we [have] noted . . . ‘expert testimony regarding matters beyond the comprehension of layperson is sometimes essential,’ particularly in cases involving complex technology. In such cases, expert testimony may be critical, for example, to establish . . . the existence (or lack thereof) of a motivation to combine references.” (internal citations omitted)) (alteration in original)). Thus, we find Petitioner’s contention to have minimal probative value.

In addition, Petitioner’s reasoning that the similarity of the references constitutes a motivation to look to other references seems inadequate on its face. Even if true, that statement does not provide a reason one would pick out these particular references and combine them to arrive at the claimed invention. *Cf. Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) (concluding “that reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention (citing *Belden Inc. v. Berk–Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to

make the combinations or modifications of prior art to arrive at the claimed invention.”)).

Similarly, in view of the complex technology involved in integrated circuit fabrication and, particularly and the agreement of both experts that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties (as discussed previously), we determine that Petitioner’s contentions and Dr. Franzon’s broad conclusions (Pet. 42–57; Ex. 1002 ¶¶ 91–103, 128) of success to be insufficient to meet its burden, which requires a preponderance of evidence. For example, as discussed previously, we find Petitioner’s contention that “Leedy ’695 thus discloses that its dielectrics *can be easily used* in place of other dielectrics” to be insufficiently supported by the evidence of record.

Accordingly, for these, we determine Petitioner has not demonstrated by a preponderance of the evidence that Yu in combination with Leedy ’695 and Blonder teaches these features. Petitioner does not rely on Blonder to cure the deficiencies identified with respect to Petitioner’s arguments discussed above. Rather, Petitioner relies on Blonder solely for the disclosure of redundant vertical interconnections. Pet. 45–47.

6. *Claims 1 and 20–23 — Obvious over Finnila and Leedy; and
Claims 1 and 20–23 — Obvious over Finnila, Blonder, and Leedy*

Petitioner included these challenges in the event that our construction of the term “substantially flexible integrated circuit” is not construed to require polishing and grinding. Pet. 59. In that circumstance, Petitioner argues that Yu is not needed to show polishing for the challenged. *Id.* However, Petitioner maintains that claims 1 and 20–23 are unpatentable over the combinations of (1) Finnila and Leedy; and (2) Finnila, Blonder, and

Based on the complete record, including our construction of “substantially flexible integrated circuit,” we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 1 and 20–23 are unpatentable over the combination of (1) Finnila and Leedy '695; and (2) Finnila, Blonder, and Leedy '695. As discussed above, independent claim 1 requires a “substantially flexible integrated circuit” and a “low stress dielectric layer.” For these limitations, Petitioner relies on the same arguments based on thinness and substitution of Leedy '695's dielectric material, which we have determined are not sufficient to satisfy Petitioner's burden. For the same reasons discussed above, we determine Petitioner has not demonstrated by a preponderance of the evidence that the challenged claims are unpatentable over the asserted combination of (1) Finnila and Leedy '695; and (2) Finnila, Blonder, and Leedy '695.

III. CONCLUSION

We conclude, based on a preponderance of the evidence, that Petitioner has not established that claims 1 and 20–23 of the '004 patent are unpatentable.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1 and 20–23 of the '004 patent have not been shown by a preponderance of the evidence to be unpatentable; and

FURTHER ORDERED that this is a Final Written Decision under 35 U.S.C. § 318(a), and that parties to the proceeding seeking judicial review of the decision under 35 U.S.C. § 319 must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2016-00691
Patent 7,474,004 B2

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