

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC. and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00703
Patent 8,791,581 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and
FRANCES L. IPPOLITO, *Administrative Patent Judges*.

BENOIT, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

This is a preliminary proceeding to decide whether *inter partes* review of U.S. Patent No. 8,791,581 B2 (Ex. 1001, “the ’581 patent” or “the challenged patent”) should be instituted under 35 U.S.C. §314(a). Micron Technology, Inc. and SK Hynix Inc. (collectively “Petitioner”) filed a Petition (Paper 3, “Pet.”) seeking *inter partes* review of claims 1, 5, 12, 36, 54, 78, 113, 116, 133, and 136 of the ’581 patent. Patent Owner, Elm 3DS Innovations, LLC, filed a Preliminary Response to the Petition (Paper 9, “Prelim. Resp.”). We have jurisdiction under 35 U.S.C. § 314(a), which provides that *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Upon consideration of the Petition and the Preliminary Response, we conclude the information presented does not show there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of the challenged claims of the challenged patent. Accordingly, for the reasons that follow, we deny institution of an *inter partes* review.

A. Related Proceedings

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 1–2; Paper 6 (Patent Owner’s Mandatory Notices). Petitioner indicates that the challenged patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations*,

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LLC v. Micron Tech., Inc., No. 1:14-cv-01431 (D. Del.) and *Elm 3DS Innovations, LLC v. SK Hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

Additionally, the challenged patent is the subject of a petition filed in IPR2016-00706 and patents related to the challenged patent are the subjects of petitions filed in IPR2016-00386 (U.S. Patent No. 8,653,672); IPR2016-00387 (U.S. Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (U.S. Patent No. 7,193,239); IPR2016-00389 (U.S. Patent No. 8,035,233); IPR2016-00390 (U.S. Patent No. 8,629,542); IPR2016-00391 (U.S. Patent No. 8,796,862); IPR2016-00394 (U.S. Patent No. 8,410,617); IPR2016-00395 (U.S. Patent No. 7,504,732); IPR2016-00687 (U.S. Patent No. 8,928,119); IPR2016-00691 (U.S. Patent No. 7,474,004); IPR 2016-00786 (U.S. Patent No. 8,933,570); IPR2016-00708 (U.S. Patent No. 8,907,499); and IPR2016-00770 (U.S. Patent No. 8,907,499).

B. The Challenged Patent

The challenged patent relates generally to a three-dimensional structure (3DS) for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

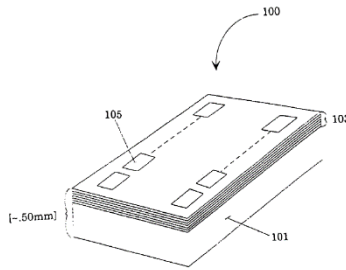


Figure 1a

Figure 1a shows three-dimensional memory device 100 having a stack of integrated circuit layers with a “fine-grain inter-layer vertical interconnect” between all circuit layers. *Id.* at 3:65–4:4. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:19–21. The challenged patent discloses that “each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness.” *Id.* at 4:24–27. The challenged patent further discloses that the “thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm²) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication.” *Id.* at 8:47–52.

Figure 1b is reproduced below.

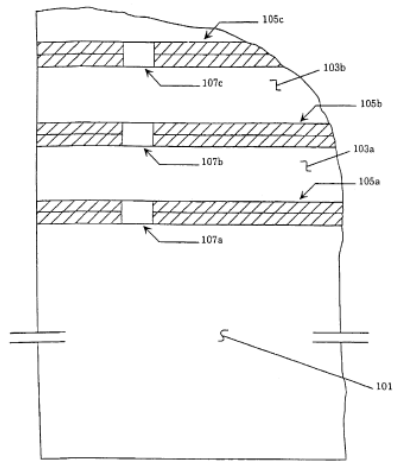


Figure 1b

Figure 1b of the challenged patent shows a cross-section of a three-dimensional integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:39–41. Bond and interconnect layers 105a, 105b, 105c are shown between circuit layers 103a and 103b. *Id.* at Fig. 1b. The challenged patent discloses that pattern 107a, 107b, 107c in the bond and interconnect layers 105a, 105b, 105c defines the vertical interconnect contacts between the integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4:13–17. Additionally, the challenged patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:17–18.

Further, the challenged patent teaches that the “term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 μm” *Id.* at 4:1–4. The fine-

grain inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:8–9.

C. Illustrative Claims

Of the challenged claims, claims 1, 5, 12, 113, and 133 are independent. Claims 1 and 36 are illustrative of the claimed subject matter:

1. A stacked memory integrated circuit comprising:

a plurality of circuit layers comprising at least one control circuit layer and at least one memory circuit layer arranged in a stacked relationship;

wherein the at least one control layer and at least one memory circuit layers of the stacked memory integrated circuit are partitioned into a plurality of vertically interconnected circuit block stacks and configured for a plurality of said vertically interconnected circuit block stacks to independently perform memory operations.

36. The stacked memory integrated circuit of claim 1, further comprising:

at least one thinned, substantially flexible monocrystalline semiconductor substrate of one piece,

wherein the semiconductor substrate is made substantially flexible when it is thinned and polished or smoothed by first grinding away semiconductor wafer material from a backside of the semiconductor substrate to leave an exposed surface thereof, and then polishing or smoothing the exposed surface; and,

a low-stress silicon-based dielectric layer formed above the thinned, substantially flexible monocrystalline semiconductor substrate and having a tensile stress of less than 5×10^8 dynes/cm²,

wherein: the polished or smoothed surface of the thinned, substantially flexible monocrystalline semiconductor substrate is

polished or smoothed to reduce vulnerability to fracture as a result of flexing; and

at least one of the plurality of circuit layers comprises a singulated die having a die area defined by its perimeter;

and the thinned, substantially flexible monocrystalline semiconductor substrate extends in one piece across a substantial portion of the die area.

Ex. 1001, 12:58–67 (claim 1), 18:6–26 (claim 36).

D. The Asserted Grounds of Unpatentability

Petitioner contends that challenged claims are unpatentable under 35 U.S.C. § 103 based on the following specific grounds (Pet. 3–4, 21–60):

References	Claims Challenged
Hsu ¹ and Sakuta ²	1 and 5
Hsu, Sakuta, and Leedy '695 ³	12, 36, 54, 78, and 116
Hsu, Sakuta, and Bertin '333 ⁴	113 and 133
Hsu, Sakuta, Leedy '695, and Bertin '333	136
Hsu, Sakuta, and Kowa ⁵	12, 36, 54, 78, 116, and 136
Hsu, Sakuta, Kowa, and Bertin '333	133

¹ U.S. Patent No. 5,627,106, issued May 6, 1997 (Ex. 1008, “Hsu”).

² U.S. Patent No. 5,208,782, issued May 4, 1993 (Ex. 1067, “Sakuta”).

³ U.S. Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, “Leedy '695”).

⁴ U.S. Patent No. 5,502,333 issued Mar. 26, 1994 (Ex. 1010, “Bertin '333”).

⁵ JP Patent Application Publication No. H3-151637, published June 27, 1991 (Ex. 1007, “Kowa”). Petitioner has provided a certified English translation. Ex. 1007, 13.

II. DISCUSSION

A. Claim Construction

We interpret claims of an unexpired patent using the “broadest reasonable construction in light of the specification of the patent in which [the claims] appear[.]” 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144 (2016) (upholding the use of the broadest reasonable interpretation standard in inter partes reviews). Under that standard, claim terms are presumed to be given their ordinary and customary meaning, which “is the meaning that the term would have to a person of ordinary skill in the art in question” at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). In addition, the Board may not “construe claims during IPR so broadly that its constructions are unreasonable under general claim construction principles.” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015).

We determine that no terms require express construction for this decision.

B. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art;

(2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze the challenge presented in the Petition in accordance with these principles.

C. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. “The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner’s declarant, Paul D. Franzon, Ph.D, opines that one of ordinary skill in the art relevant to the challenged patent “would have had at least a B.S. degree in electrical engineering, material science, or equivalent thereof, and at least 3–5 years of experience in the relevant field, e.g., semiconductor processing.” Ex. 1002 ¶ 58; *see* Pet. 6–7 (relying on Ex. 1002 ¶ 58). Patent Owner does not offer any contrary explanation regarding who would qualify as a person of ordinary skill in the art relevant to the challenged patent. *See generally* Prelim. Resp.

Based on our review of the challenged patent, the types of problems and solutions described in the challenged patent and cited prior art, and the testimony of Petitioner’s Declarant, we adopt and apply Petitioner’s definition of a person of ordinary skill in the art at the time of the claimed

invention. We note that the applied prior art reflects the appropriate level of skill at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

D. Asserted Ground of Obviousness over Hsu and Sakuta,

Petitioner contends that independent claims 1 and 5 of the challenged patent are unpatentable under 35 U.S.C. § 103 as obvious over Hsu and Sakuta. Pet. 3, 21–37. Petitioner supports its contentions with citations to the references and with declaration testimony of Dr. Franzon (Ex. 1002). *Id.* at 21–37. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 6–24.

1. Summary of Hsu

Hsu is a United States Patent that relates generally to a “method of connecting three-dimensional integrated circuit chips using trench technology.” Ex. 1008, Abstract, 1:8–11. Referring to Figures 2–8, Hsu’s fabrication process starts with etching deep trenches 16 on silicon substrate 10, which Hsu indicates can be composed of monocrystalline silicon. *Id.* at 2:50–61. Hsu’s integrated circuits consist of “one master chip and some subordinate chips.” *Id.* at 1:20–21. According Hsu, the master chip and subordinate chip each consist of a semiconductor substrate, preferably composed of monocrystalline silicon. *Id.* at 2:51–54, 3:42–45. These chips can be “stacked by interconnection through [a] pad window [. . .] during integrated circuit processing.” *Id.* at 1:28–31. Hsu further describes that the “bottom surface of the [subordinate] substrate is ground and polished so that only a thin portion of the substrate remains.” *Id.*

at 3:21–23.

2. Summary of Sakuta

Sakuta is a United States Patent that describes a semiconductor integrated circuit memory structure that uses “macro-cellulated circuit blocks.” Ex. 1067, Abstract, 1:11–17, 2:34–37, 5:52–54. Two embodiments of Sakuta’s semiconductor circuit blocks are shown below in Figures 1 and 3.

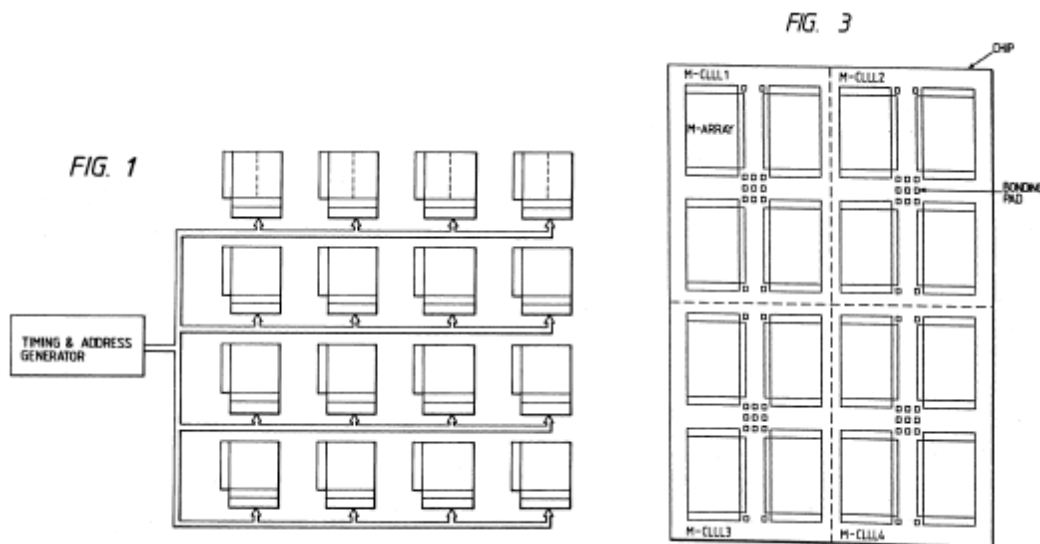


Figure 1 shows one embodiment of dynamic random access memory or RAM⁶ constructed such that macro-cellulated memory blocks are arranged in a matrix form. *Id.* at 5:35–36, 5:52–59. As shown in Figure 1, RAM having 64 Mbit storage capacity consists of sixteen macro-cellulated memory blocks arranged in four rows and in four columns. *Id.* at 5:35–37,

⁶ Ex. 1067, 1:14–15 (indicating “dynamic RAM (i.e., Random Access Memory)”).

5:52–59. Sakuta indicates that “the memory blocks specified [in Figure 1] are matrix-arranged together with the above-specified control circuit (i.e., the timing and address generator).” *Id.* at 5:68–6:3. “This control circuit exchanges signals with individual memory blocks through signal buses.” *Id.* at 6:3–5.

By contrast, Sakuta’s embodiment shown in Figure 3 “is not equipped with the aforementioned control circuit which is commonly used for the plural memory blocks.” *Id.* at 8:55–57. Rather, “each memory block of this embodiment is equipped with the address selection circuit, the input/output circuit, and the control circuit.” *Id.* at 8:58–60.

3. Analysis

Each of independent claims 1 and 5 recites a stacked memory integrated circuit comprising “a plurality of circuit layers comprising at least one control circuit layer and at least one memory circuit layer arranged in a stacked relationship.” A key aspect of each of independent claims 1 and 5 as a whole is partitioning at least one control layer and at least one memory circuit layer arranged in a stacked relationship. The plain language of independent claims 1 and 5 each requires a control layer in the stacked memory integrated circuit to be partitioned into a plurality of vertically interconnected circuit block stacks.⁷ Ex. 1001, 12:62–65, 13:44–47 (claims 1 and 5 each recite “wherein the at least one control layer *and* at

⁷ Petitioner refers to this limitation as “claim element 1c” and “claim element 5c,” respectively. See Pet. 33, 36.

least one memory circuit layers of the stacked memory integrated circuit *are* partitioned into a plurality of vertically interconnected circuit block stacks”) (emphases added).

A central issue concerns partitioning “the at least one control layer” recited in independent claims 1 and 5. Patent Owner contends that Petitioner “fails to address the recited partition feature of the control layer.” Prelim. Resp. 14. For the reasons that follow, we agree with Patent Owner.

a. Partitioned Circuit Control Layer Limitation

We look first to Petitioner’s contentions regarding the limitation “wherein the at least one control layer *and* at least one memory circuit layers of the stacked memory integrated circuit *are* partitioned into a plurality of vertically interconnected circuit block stacks,” as recited in independent claims 1 and 5. Pet. 33–36. Petitioner does not contend that either reference discloses or itself would have conveyed the required partitioned circuit control layer of a stacked memory integrated circuit. *See, e.g., id.* Indeed, Petitioner’s declarant, Dr. Franzon, acknowledges that Hsu does not teach or suggest a partitioned control layer in its three-dimensional integrated circuit technology. Ex. 1002 ¶ 147 (referring to limitations recited in “claim limitation 1c”) (“Hsu does not expressly disclose that wherein the at least one control layer and at least one memory circuit layer of the stacked memory integrated circuit are partitioned into a plurality of vertically interconnected circuit block stacks, wherein a plurality of said vertically

interconnected circuit block stacks can independently perform memory operations.”); *see also* Pet. 33 (citing Ex. 1002 ¶ 147).⁸

Apparently recognizing that Sakuta does not expressly disclose the required partitioned circuit control layer of a stacked memory integrated circuit, Petitioner asserts, without further explanation or analysis, that one of ordinary skill in the art “would have recognized that the stacked memory integrated circuits disclosed by Hsu, e.g., ROM and SRAM, are often partitioned into a plurality of circuit blocks. Ex. 1002 at ¶147.” *Id.* at 33 (quoting ¶ 147 of Dr. Franzon’s testimony (Ex. 1002)). Although Petitioner quotes Dr. Franzon’s testimony for support, Dr. Franzon’s testimony is unavailing because it is conclusory. Dr. Franzon’s testimony merely states, without providing further analysis or evidence, that one of ordinary skill in the art would have recognized stacked memory integrated circuits are often partitioned. As such, Dr. Franzon’s testimony does not disclose the facts underlying his conclusion or provide sufficient analysis or evidence to support his conclusion. Accordingly, Dr. Franzon’s testimony is entitled to

⁸ Without quoting, paraphrasing, or otherwise addressing, Petitioner cites to a single-numbered “paragraph” consisting of an eleven-page claim chart regarding the limitations of claim 1. At this time we take no position regarding whether this amounts to improper incorporation by reference. *See* 37 C.F.R. § 42.6(a)(3) (“Arguments must not be incorporated by reference from one document into another document.”); *Cisco Sys., Inc. v. C-Cation Techs., LLC*, Case IPR2014-00454 (PTAB Aug. 29, 2014) (Paper 12, 9) (Informative) (indicating the practice of citing a declaration to support conclusory statements that are not otherwise supported in the petition is incorporation by reference).

little or no weight. 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) (“[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.”).

Recognizing that neither reference itself would have conveyed the required control circuit layer partitioning, Petitioner relies on the combination of “the block-based memory design disclosed by Sakuta in the Hsu 3D memory structure” for conveying to one of ordinary skill in the art the recited “wherein the at least one control layer and the at least one memory circuit layer of the stacked memory integrated circuit are partitioned into a plurality of vertically interconnected circuit block stacks.” Pet. 35; *see id.* at 33–35 (addressing claim 1), 36 (addressing claim 5).

Petitioner’s reliance on Sakuta’s two-dimensional memory circuit design for the requisite partitioned control layer, however, does not distinguish sufficiently between Sakuta’s embodiment with a two-dimensional matrixed memory circuit that shares a control circuit (as shown in Sakuta’s Figure 1) and Sakuta’s embodiment with a two-dimensional matrixed memory circuit in which each memory block includes a control circuit (as shown in Sakuta’s Figure 3). *See* Pet. 33–34 (citing Ex. 1067, Abstract, 5:52–54 (discussing embodiment shown in Fig. 1), 5:60–68 (discussing embodiment shown in Fig. 1), 8:49–60 (discussing embodiment shown in Fig. 3), Figs. 1 and 3). Thus, Petitioner relies both on Sakuta’s

embodiment in which the control circuit arguably seems to be partitioned (Figure 3) and on Sakuta's embodiment in which the control circuit is not partitioned (Figure 1). *See, e.g.*, Ex. 1067, 6:34–35 (indicating the “control circuit” is the “timing and address generator of FIG. 1”), 8:49–60 (indicating Fig. 3 shows “each memory block of this embodiment” as being “equipped with . . . the control circuit”). Petitioner's reliance on both embodiments—only one of which arguably has a partitioned control circuit—undermines Petitioner's position that its proposed combination of Hsu and Sakuta would have conveyed to one of ordinary skill in the art the required partitioned control layer of a stacked memory integrated circuit.

Petitioner concludes its discussion of the partition limitation by repeating the claim language: “[w]hen combined, the resulting structure would include a stacked memory integrated circuit having one control layer and at least one memory circuit layer partitioned into a plurality of vertically interconnected circuit block stacks.” *Id.* at 35. For the reasons discussed previously, however, Petitioner's contention is not supported sufficiently. Furthermore, although Petitioner's cites to seven paragraphs of Dr. Franzon's declaration, Petitioner does not provide any explanation or analysis as to how the cited seven pages of Dr. Franzon's testimony purportedly support its conclusion. *Id.* at 35 (citing Ex. 1002 ¶¶ 120–126). For this additional reason, we determine that Petitioner has not supported, with sufficient evidence or analysis, its proposed combination involving Sakuta's purportedly partitioned control circuit.

Thus, we are not persuaded that Petitioner has shown sufficiently that Petitioner's proposed combination of Hsu and Sakuta would have conveyed to one of ordinary skill in the art the required partitioned circuit control layer of a stacked memory integrated circuit.

*b. Examples of Sakuta's "I/O Selector Ckt"
and "Refresh Address Counter RC"*

Second, we turn to Petitioner's examples combining, with Hsu's "master chip," either (i) Sakuta's "I/O selector ckt" shown in Figure 24 or (ii) Sakuta's "refresh address counter RC" shown in Figure 12. *Id.* at 28–29. In its purported reasons to combine Hsu and Sakuta, Petitioner asserts either of these combinations would have conveyed to one of ordinary skill in the art "a stacked integrated memory circuit including at least one control logic layer and one memory layer, wherein at least a portion of the stacked integrated memory circuit is partitioned into a plurality of circuit block stacks." *Id.* Petitioner, however, does not address (much less provide sufficient evidence to show) how one of ordinary skill in the art would have understood that either proposed combination would include Sakuta's partitioned control circuit. *See generally id.*

First, Sakuta characterizes Figure 24 as showing "yet another embodiment" of the described method and does not associate the embodiment in Figure 24 with Sakuta's embodiment in Figure 3 having a control circuit with each memory block. Ex. 1067, 5:4–6. Indeed, Petitioner's reliance on Sakuta's description that the circuit in Figure 24—including the RAM chips and the 'I/O selector ckt'—could be packaged as

“one module in the package” seems to undermine including a partitioned control circuit in its proposed combination of Hsu and Sakuta. Pet. 28 (citing Ex. 1067, 31:56–57.”). Sakuta’s statement expressly indicates one “I/O selector ckt” is packaged with multiple memory chips (“RAM chips”) in “the one module.” Similarly, because Sakuta’s Figure 24 shows a single “I/O selector ckt” and multiple memory chips, packing these components into a single module does not, on its face, without further explanation or evidence, convey an “I/O selector ckt” for each memory chip or otherwise suggest a partitioned control circuit. Neither Petitioner nor its declarant, Dr. Franzon, address (much less explain sufficiently) how one of ordinary skill in the art would have understood Sakuta’s “I/O selector ckt” or “refresh address counter RC” to be partitioned in some manner.

Although Petitioner cites a paragraph of Dr. Franzon’s testimony concerning Sakuta’s “I/O selector ckt” and “refresh address counter RC,” Dr. Franzon’s testimony does not provide sufficient analysis or further explain Petitioner’s position. Rather, Dr. Franzon’s testimony repeats the same conclusory contentions found in the Petition, which do not adequately address partitioning a control circuit. *Compare* Pet. 28, *with* Ex. 1002 ¶ 124 (both stating “One example of a candidate for inclusion on the ‘master chip’ is the ‘I/O selector ckt’ in Fig. 24 of Sakuta. Ex. 1067. Sakuta discusses that this circuit [including the RAM and the ‘I/O selector ckt’] could be packaged as ‘one module in the package.’ *Id.* at 31:56–57.”); *compare id.* at 29, *with* Ex. 1002 ¶ 124 (both stating “[a]n example for inclusion in the ‘master chip’ of Hsu is the ‘refresh address counter RC’ in Fig. 12 of Sakuta,

shown below. Ex. 1067 at 18:4–14. Sakuta discloses ‘the refreshing circuit can be shared to simplify the circuit structure.’ *Id.* at 18:8–9. Further simplification could be gained by placing the refreshing circuitry in [Hsu’s] ‘master chip.’”).

Notably, Petitioner and Dr. Franzon rely on Sakuta’s disclosure that “the refreshing circuit can be shared to simply circuit structure” (Pet. 29, Ex. 1002 ¶ 124). Petitioner’s reference to sharing “the refreshing circuit”—that is, a single refreshing circuit as shown in Figure 12)—seems to undercut Petitioner’s reliance on Sakuta’s embodiment in Figure 3 in which the control circuit is included in each memory cell for conveying to one of ordinary skill in the art a partitioned control circuit. Similarly, Petitioner’s statement that locating the refreshing circuitry in Hsu’s “master chip” also undermines its position relying on Sakuta for disclosing a partitioned control circuit. *See* Pet. 29.

Therefore, we are not persuaded by Petitioner’s discussion of Sakuta’s “I/O selector ckt” or Sakuta’s “refresh address counter RC” that Sakuta would have conveyed to one of ordinary skill in the art a partitioned control circuit, much less that the combination of Sakuta and Hsu would have conveyed to one of ordinary skill in the art a partitioned control layer.

c. Reasons to Combine

Third, we turn to Petitioner’s contentions regarding reasons one of ordinary skill in the art would have combined Hsu and Sakuta. *Id.* at 25. Petitioner’s contentions refer generally to “us[ing] *the block-based memory design* disclosed by Sakuta” and describing purported performance benefits

of “*the block-based design* disclosed by Sakuta.” *Id.* (“Furthermore, a person with ordinary skill in the art would have been motivated to use *the block-based memory design* disclosed by Sakuta in the Hsu 3D memory structure for several reasons.”) (emphasis added); *id.* at 26 (“[A] person having ordinary skill in the art would have recognized that *the block-based design* disclosed by Sakuta has potential to provide performance benefits by increasing the memory input/output bandwidth.”) (emphasis added).

In referring to “the block-based design” or “the block-based memory design” of Sakuta, Petitioner fails to distinguish between Sakuta’s various embodiments, only one of which even arguably discloses a partitioned control circuit (embodiment shown in Figure 3) for the reasons previously discussed. *See id.* at 33–34 (discussing embodiments shown in both Figures 1 and 3). This further demonstrates shortcomings in Petitioner’s position relying on Sakuta’s purported “memory circuit design that is partitioned into a plurality of circuit blocks” for a partitioned two-dimensional control circuit. *Id.*

Moreover, Petitioner does not address, much less sufficiently explain, why one of ordinary skill in the art would have combined, with Hsu’s three-dimensional memory structure, Sakuta’s embodiment that includes a control circuit in the memory block (as shown in Figure 3), rather than Sakuta’s embodiment that includes the memory blocks controlled by a shared control circuit (as shown in Figure 1). *See generally id.* at 25–30, 35.

For these reasons, we are not persuaded by Petitioner’s reasons to combine explain how Sakuta would have conveyed to one of ordinary skill

in the art a partitioned control circuit, much less how the combination of Sakuta and Hsu would have conveyed to one of ordinary skill in the art a partitioned control layer.

4. Conclusion

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, No. 2015-1693, 2016 WL 2620512, at *6 (Fed. Cir. May 9, 2016) (“It was [Petitioner]’s burden to demonstrate both that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.”) (internal quotation marks removed). Thus, Petitioner must explain how the combination of Hsu and Sakuta would have rendered the independent claims 1 and 5 unpatentable.

For the foregoing reasons, we determine that the Petition does not demonstrate sufficiently that Petitioner’s proposed combination of Hsu and Sakuta would have conveyed to one of ordinary skill in the art a control layer of the stacked memory integrated circuit partitioned into a plurality of vertically interconnected circuit block stacks as required by independent claims 1 and 5. Accordingly, after considering the information presented in

the Petition and Patent Owner's Preliminary Response, we conclude that the information presented does not show there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of independent claims 1 or 5 as obvious over Hsu and Sakuta.

*E. Asserted Grounds of Obviousness
over Hsu, Sakuta, and Other References*

Like independent claims 1 and 5, independent claims 113 and 133 each recites "wherein the at least one control layer and the at least one memory circuit layer of the stacked memory integrated circuit are partitioned into a plurality of vertically interconnected circuit block stacks." Similarly to independent claims 1 and 5, independent claim 12 recites a stacked memory integration circuit comprising a first integrated circuit controller layer and a plurality of memory layers of the stacked memory integrated circuit "wherein: the first integrated circuit controller layer and the plurality of memory layers of the stacked memory integrated circuit are partitioned into a plurality of vertically interconnected circuit block stacks."

For each of these independent claims, Petitioner relies on its analysis described above concerning Hsu and Sakuta. Pet. 3, 40 (regarding partitioning of a circuit controller layer as required by independent claim 12), 50 (regarding partitioning a control circuit layer as required by independent claim 113), 54 (regarding partitioning a control circuit layer as required by independent claim 133).

Accordingly, for similar reasons as those discussed previously with regard to independent claim 1, we determine that the Petition does not

demonstrate sufficiently that Petitioner's proposed combination of Hsu and Sakuta would have conveyed to one of ordinary skill in the art all of the elements recited in independent claims 12, 113, and 133, or recited in claims 36, 54, 78, 116, and 136, all of which depend from one of the challenged independent claims.

Similarly, concerning Petitioner's grounds asserted for a particular construction of low tensile stress dielectrics recited in some of the claims, Petitioner continues to rely on Hsu and Sakuta for the requisite partitioning of control circuit layers. *See generally id.* at 58–59. As such, we also determine that the Petition fails to show that this a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of the claims challenged in the alternative grounds relying on (i) Hsu, Sakuta, and Kowa and (ii) Hsu, Sakuta, Kowa, and Bertin '333. *Id.*

III. CONCLUSION

For the foregoing reasons, we determine that the information presented by Petitioner fails to establish a reasonable likelihood that Petitioner would prevail in showing that at least one of claims 1, 5, 12, 36, 54, 78, 113, 116, 133, and 136 of the challenged patent is unpatentable.

IV. ORDER

After due consideration of the record before us and for the foregoing reasons, it is:

ORDERED that the Petition is denied and no trial is instituted.

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