

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

DSS TECHNOLOGY MANAGEMENT, INC.,
Patent Owner.

Case IPR2016-00782
Patent 6,784,552 B2

Before BRYAN F. MOORE, BRIAN J. McNAMARA, and
MINN CHUNG, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

A. Introduction

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Samsung Electronics Co., Ltd. (“Petitioner”) challenges the patentability of claims 1–12 (the “challenged claims”) of U.S. Patent No. 6,784,552 B2 (Ex. 1001, “the ’552 patent”), owned by DSS Technology Management, Inc. (“Patent Owner”). The Board has jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. With respect to the grounds instituted in this trial, we have considered the papers submitted by the parties and the evidence cited therein. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–12 of the ’552 patent are unpatentable.

B. Procedural History

On March 18, 2016, Petitioner filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–12 (the “challenged claims”) of U.S. Patent No. 6,784,552 B2 (Ex. 1001, “the ’552 patent”). Petitioner also filed the Declaration of Dr. Richard Fair (Ex. 1003, “Fair Decl.”) in support of the Petition. Patent Owner did not file a Preliminary Response. On September 23, 2016, we instituted an *inter partes* review of claims 1–12 of the ’552 patent based on the following specific grounds (Paper 6, “Dec. on Inst.,” 27).

Claim(s) Challenged	Statutory Basis	Reference(s)
1, 2, 4–12	§ 102(b)	Kuesters ¹
3	§ 103(a)	Kuesters and Havemann ²
1, 2, 4–7	§ 103(a)	Kuesters and Heath ³
3	§ 103(a)	Kuesters, Heath, and Havemann

After institution, Patent Owner filed a Patent Owner Response (Paper 10, “PO Resp.”), to which Petitioner filed a Reply (Paper 12, “Pet. Reply”). Petitioner also filed the Declaration of Dr. Richard Fair in Support of Petitioner’s Reply (Ex. 1014, “Fair Reply Decl.”). An oral hearing was held on June 20, 2017. A transcript of the hearing is included in the record as Paper 17 (“Tr.”).

C. Related Proceedings

According to the parties, the ’552 patent is the subject of the following patent infringement cases: *DSS Tech. Mgmt., Inc. v. Samsung Elec. Co., Ltd.*, Case No. 15-cv-690 (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. Intel, Corp.*, Case No. 15-cv-130 (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. SK Hynix, Inc.*, Case No. 15-cv-691 (E.D. Tex.); and *DSS Tech. Mgmt., Inc. v. Qualcomm, Inc.*, Case No. 15-cv-692 (E.D. Tex.). Pet. 2; Paper 5, 2–3.

¹ Kuesters et al., *Self Aligned Bitline Contact For 4 Mbit dRAM*, PROCEEDINGS OF THE FIRST INTERNATIONAL SYMPOSIUM ON ULTRA LARGE SCALE INTEGRATION SCIENCE AND TECHNOLOGY 640–49 (1987) (“Kuesters”) (Ex. 1005).

² U.S. Patent No. 5,482,894 (Jan. 9, 1996) (“Havemann”) (Ex. 1006).

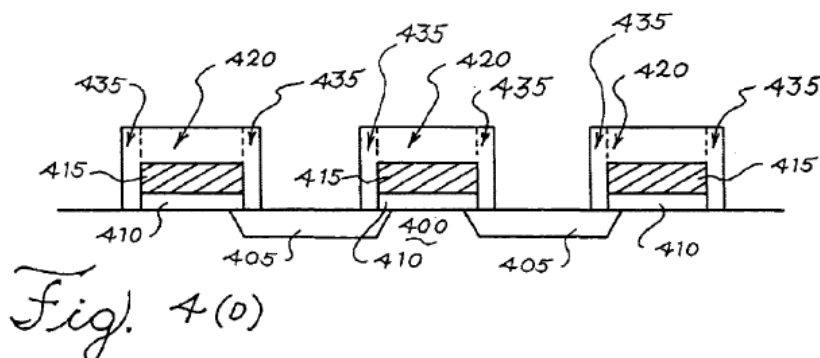
³ U.S. Patent No. 4,686,000 (Aug. 11, 1987) (“Heath”) (Ex. 1007).

The '552 patent was also the subject of instituted trial proceedings *Intel Corp. v. DSS Tech. Mgmt., Inc.*, Cases IPR2016-00287 and IPR2016-00288, in which we have entered final written decisions finding all of the claims of the '552 patent unpatentable.⁴ *Intel Corp. v. DSS Tech. Mgmt., Inc.*, Cases IPR2016-00287 and IPR2016-00288 (PTAB June 1, 2017) (Paper 25 in both cases). Patent Owner has timely filed a Notice of Appeal in each of Cases IPR2016-00287 and IPR2016-00288 (Paper 28 in each case).

II. THE '552 PATENT

A. Described Invention

The '552 patent describes a process of semiconductor device fabrication and a structure of a semiconductor device having “substantially rectangular” lateral insulating spacers adjacent to gate electrodes. Ex. 1001, Abstract. The '552 patent defines the term “substantially rectangular” to mean that “a side of the spacer has an angle relative to the substrate surface of more than 85°.” *Id.* at col. 8, ll. 40–42. Figure 4(D) of the '552 patent is reproduced below.



⁴ Cases IPR2016-01311 and IPR2016-01314 have been joined with IPR2016-00287 and IPR2016-00288, respectively.

Figure 4(D) illustrates a cross-sectional view of a series of gates 415 (also called conducting layers or polysilicon layers) completely encapsulated in insulating material 420, e.g., TEOS (tetraethyl orthosilicate glass), where spacers 435 of the insulating material adjacent to the gates have substantially rectangular profiles. *Id.* at col. 9, ll. 9–13; col. 11, ll. 40–46. As shown in Figure 4(D), gates 415 are insulated from sources or drains 405 by insulating dielectric layers 410. *See id.* at col. 10, ll. 49–50. The '552 patent describes a process of making high quality contacts to the sources or drains, such as “self-aligned” contacts, by etching structures over substrate 400 and sources or drains 405. *Id.* at col. 7, ll. 19–22; col. 8, ll. 4–6.

Figure 4(I) of the '552 patent is reproduced below.

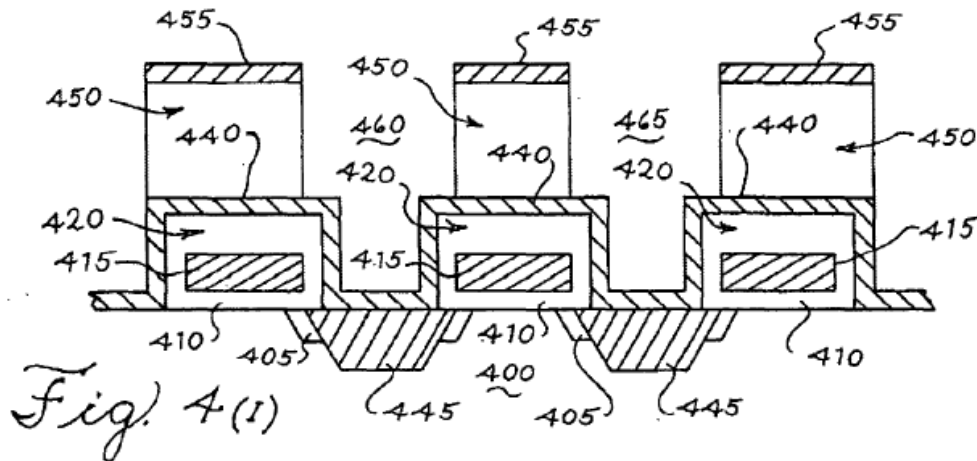


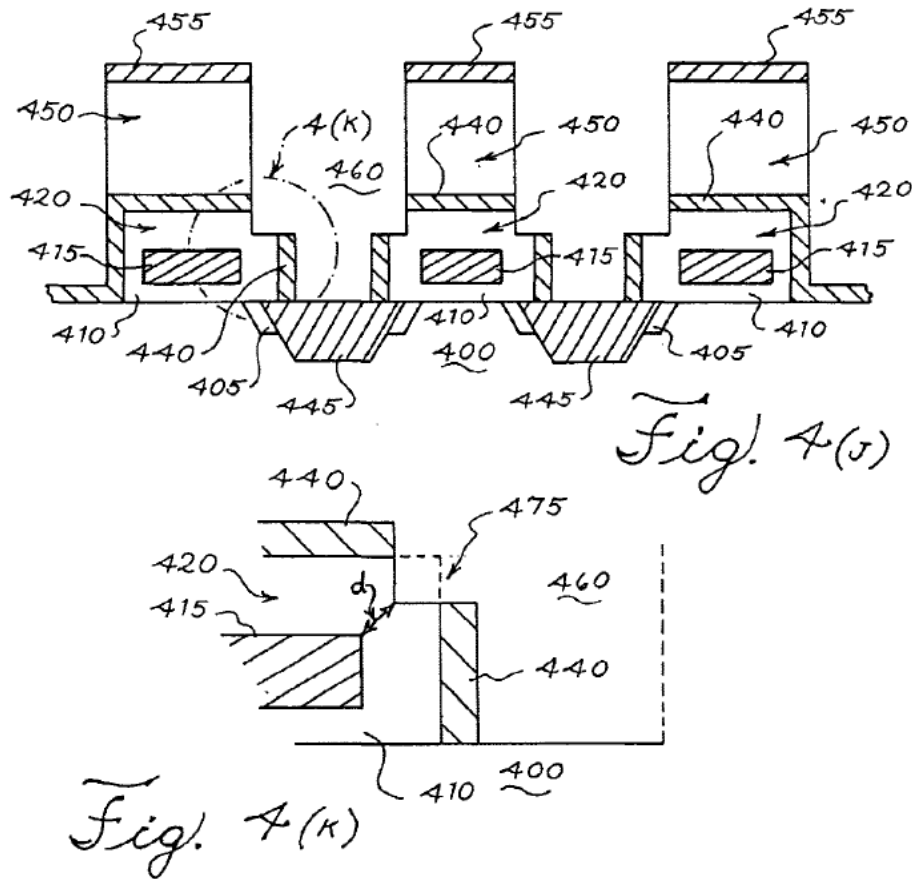
Figure 4(I) illustrates additional structures deposited and etched over the structure described in Figure 4(D), such as second dielectric layer 440 (called etch stop layer), blanket layer 450, and photoresist mask layer 455. *Id.* at col. 9, ll. 33–39; col. 11, ll. 63–65; col. 12, ll. 34–42. According to the '552 patent, etch stop layer 440, e.g., silicon nitride layer 440, depicted in Figure 4(I) is distinct or different from the underlying TEOS insulating

layer. *Id.* at col. 12, ll. 10–11. The etch stop layer protects the underlying TEOS layer when blanket layer 450 made of BPTEOS⁵ is etched away to create contact openings 460 and 465 above source or drain 445. *See id.* at col. 12, ll. 36–42; col. 4, ll. 41–59.

A second etch is then performed to remove etch stop layer 440 covering source or drain 445 in contact openings 460 and 465. *Id.* at col. 12, ll. 48–52; col. 7, ll. 43–45. The '552 patent describes that the second etch is “almost completely anisotropic,” which means that the etchant etches in the vertical direction, or perpendicular relative to the substrate surface. *Id.* at col. 7, ll. 45–48; col. 12, ll. 55–58. Hence, the etch removes the etch stop material covering the area of the contact openings or contact regions 460 and 465, but does not significantly etch the etch stop material adjacent to the spacer portions 435. *Id.* at col. 7, ll. 53–55; col. 12, ll. 58–61.

⁵ BPTEOS is an acronym for borophosphosilicate tetraethyl orthosilicate glass. *See* Ex. 1001, col. 11, ll. 6–7.

Figures 4(J) and 4(K) of the '552 patent are reproduced below.



Figures 4(J) and 4(K) illustrate the structure of the semiconductor device of the '552 patent after the second etch for removing the etch stop layer from the contact regions 460 and 465 is completed. As shown in Figures 4(J) and 4(K), due to the anisotropic or vertical nature of the second etch, only a small portion, i.e., portion 475, of the TEOS spacer portion 435 is removed during the etch. *Id.* at col. 13, ll. 6–9. Of primary significance, according to the '552 patent, is that the spacer portion 435 of the TEOS insulating layer 420 retains its substantially rectangular profile, in contrast to the conventional prior art method which transforms a substantially rectangular

spacer into a sloped spacer. *Id.* at col. 13, ll. 9–10; col. 7, ll. 48–51; col. 5, ll. 4–14.

B. Illustrative Claim

Of the challenged claims, claims 1 and 8 are independent. Claims 2–7 depend directly or indirectly from claim 1, and claims 9–12 depend directly or indirectly from claim 8. Claim 1 is illustrative of the challenged claims and is reproduced below with the key limitation (the “angle limitation”) emphasized in *italics*:

1. A structure, comprising:
 - (a) a conductive layer disposed over a substrate;
 - (b) a first insulating layer on the conductive layer;
 - (c) a contact region in said first insulating layer;
 - (d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and
 - (e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,wherein *a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.*

III. CLAIM CONSTRUCTION

The '552 patent has expired. PO Resp. 15; Pet. 13. Thus, we construe the claims in accordance with the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See In re CSB-Sys. Int'l, Inc.*, 832 F.3d 1335, 1341 (Fed. Cir. 2016) (“[W]hen an expired patent is subject to reexamination, the traditional *Phillips* construction standard

attaches.”) (citing *In re Rambus*, 694 F.3d 42, 46 (Fed. Cir. 2012)); *Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed. App’x 1019, 1024 (Fed. Cir. 2016) (unpublished) (holding that in an *inter partes* review, “[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in [*Phillips*]”). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

“Contact Region” and “Contact Opening”

In the Decision on Institution, applying the *Phillips* standard, we preliminarily interpreted the terms “contact region” and “contact opening” to mean “contact openings or via.” Dec. on Inst. 8–9. The parties do not dispute the meaning of these terms in their Patent Owner Response and Petitioner Reply. See PO Resp. 15–16. Upon considering the complete record, we discern no reason to deviate from our construction, which was adopted from the express and unambiguous definition of the terms in the ’552 patent (see Dec. on Inst. 8–9 (citing Ex. 1001, col. 1, ll. 38–41)), and maintain our construction of the terms “contact region” and “contact opening” as “contact openings or via.”

No other claim terms need to be construed expressly for purposes of this Final Written Decision. See *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (explaining that “claim terms need only be

construed ‘to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

IV. ANALYSIS OF PETITIONER’S PRIOR ART CHALLENGES

To prevail in challenging Patent Owner’s claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review).

A. Kuesters As a Printed Publication

In all instituted grounds in this trial proceeding, Petitioner relies on Kuesters (Ex. 1005) as the primary prior art reference. *See* Pet. 3–4. Petitioner contends that Kuesters is prior art to the ’552 patent under 35 U.S.C. § 102(b) because it was available to the public at Stanford

University Libraries no later than October 23, 1990.⁶ *Id.* at 3 (citing Ex. 1010). In support of its assertion, Petitioner submits a Declaration of Mariellen F. Calter (Ex. 1010), who is Associate University Librarian and Chief of Staff at the Stanford University Libraries located in Stanford, California. Pet. 3; Ex. 1010 ¶ 2.

In the Decision on Institution, upon consideration of Petitioner's argument and evidence, we preliminarily determined that Petitioner has demonstrated sufficiently that Kuesters was available to the public by October 23, 1990, and, therefore, constitutes prior art to the '552 patent under § 102(b). Dec. on Inst. 9–11. The parties do not dispute whether Kuesters qualifies as prior art in their Patent Owner Response and Petitioner Reply. Upon considering the complete record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that Kuesters constitutes prior art to the '552 patent as a printed publication under § 102(b).

B. Level of Ordinary Skill in the Art

The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In determining the level of ordinary skill in the art, various factors may be considered, including the types of problems encountered in the art, prior art solutions to those problems, the sophistication of the technology, rapidity with which

⁶ As noted by Petitioner, the '552 patent claims priority to a predecessor application filed on December 22, 1995. Pet. 5; Ex. 1001, 1 (Related U.S. Application Data).

innovations are made, and educational level of active workers in the field. *Id.* In a given case, one or more factors may predominate. *Id.* In addition, we may be guided by the level of ordinary skill in the art reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d. 1350, 1355 (Fed. Cir. 2001).

Relying upon the Declaration of Dr. Richard Fair, Petitioner asserts that, at the time of the invention claimed in the '552 patent, a person of ordinary skill in the art for the technology disclosed in the '552 patent would have had a Bachelor of Science degree in electrical engineering, chemistry, materials science, or physics, or a closely related field, along with at least 2 to 3 years of experience in semiconductor fabrication. Pet. 15 (citing Ex. 1003 ¶¶ 25–27). Patent Owner does not dispute Petitioner's definition of the level of ordinary skill in the art.

Upon considering the complete record, we are persuaded by Petitioner's argument and evidence, and determine that a person of ordinary skill in the art at the time of the invention of the '552 patent would have had a Bachelor of Science degree in electrical engineering, chemistry, materials science, or physics, or a related field, along with 2 to 3 years of experience in semiconductor fabrication.

C. Anticipation By Kuesters

Petitioner asserts that claims 1, 2, and 4–12 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Kuesters. Pet. 31–52. Petitioner provides detailed explanations and specific citations to Kuesters indicating where in the reference the claimed features are disclosed. *Id.* In addition,

Petitioner relies upon the Declaration of Dr. Richard Fair (Ex. 1003) to support its position. *Id.* Upon review of all of the parties' papers and supporting evidence discussed in those papers, we are persuaded that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1, 2, and 4–12 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Kuesters.

1. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 102 only if a single prior art reference expressly or inherently describes each and every limitation set forth in the claim. *See Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005); *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987). Further, a reference cannot anticipate “unless [it] discloses within the four corners of the document not only all of the limitations claimed[,] but also all of the limitations arranged or combined in the same way as recited in the claim.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be arranged in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). Moreover, the prior art reference is read from the perspective of one with ordinary skill in the art. *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) (“A reference anticipates a claim if it discloses the claimed invention such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.” (citation and quotation marks omitted)); *In re*

Preda, 401 F.2d 825, 826 (CCPA 1968) (“[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.”). We analyze this asserted ground based on anticipation with the principles identified above in mind.

2. Overview of Kuesters

Kuesters describes a process of fabricating a 4 Mbit dRAM semiconductor device with a 25% reduction in cell size, “achieved by a self aligned bitline contact.” Ex. 1005, 3.⁷

⁷ The page numbers for Exhibit 1005 refer to the page numbers inserted by Petitioner in the bottom, right-hand corner of each page.

Figure 2 of Kuesters is reproduced below.

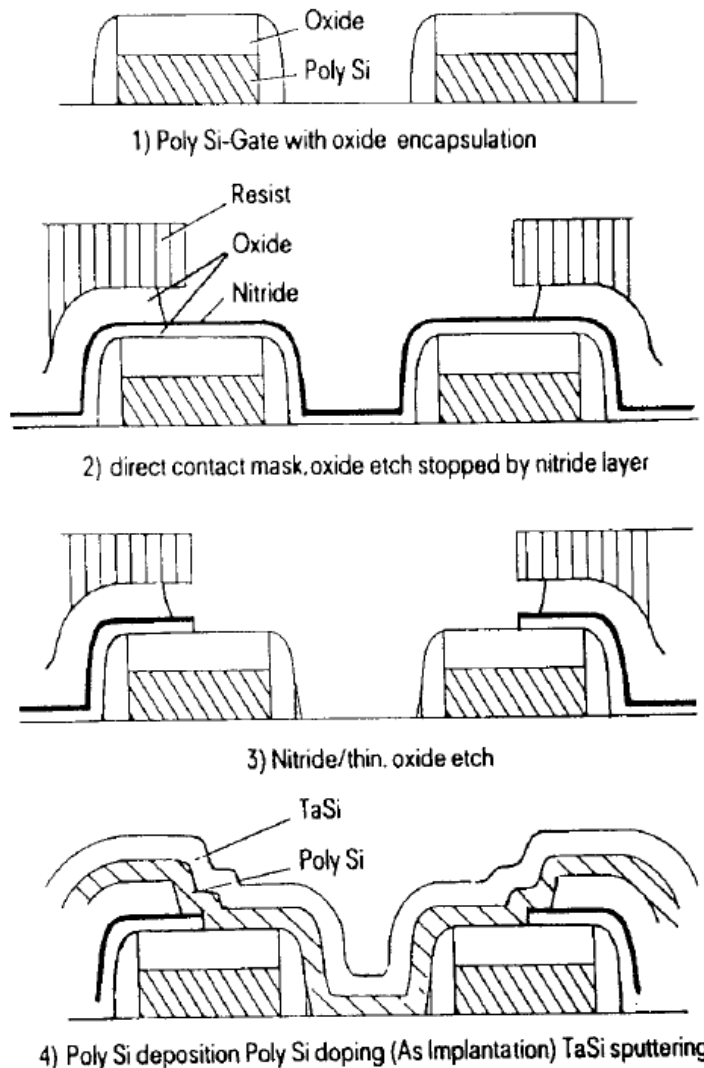


Fig.2:
Process for FOBIC
contact (wet etch of
top oxide as des-
cribed in 2.2.1, b)

**cross section of
bitline contact.**

Figure 2 depicts the process of fabricating a 4 Mbit dRAM with self-aligned, fully overlapping bitline contact (“FOBIC”), as disclosed in Kuesters. *Id.* at 3, 4. As shown in Figure 2-1 above, the process begins with the deposition of a polysilicon layer over a substrate to form a gate structure. *Id.* at 4. Then, an insulating oxide layer is deposited on the gate. *Id.* Next, an oxide spacer covering the sidewalls of the polysilicon/oxide layer is formed by oxide deposition and RIE etching. *Id.* According to Kuesters, “[a] vertical

etch profile of [the polysilicon/oxide layer] . . . is essential” when forming the oxide sidewall spacers. *Id.*

As illustrated in Figure 2-2, a triple layer of “thin oxide/nitride/oxide” is then deposited over the entire structure. *Id.* After patterning a contact hole mask on top of the structure, the top oxide is etched to create a contact hole using the nitride as an etch stop. *Id.* Subsequently, the nitride etch stop and the remaining thin oxide are etched anisotropically, resulting in the structure illustrated in Figure 2-3. *Id.* at 5. The contact area of the fabricated self-aligned contact is “defined by gate and field oxide edges.” *Id.* Figure 4a of Kuesters is reproduced below.

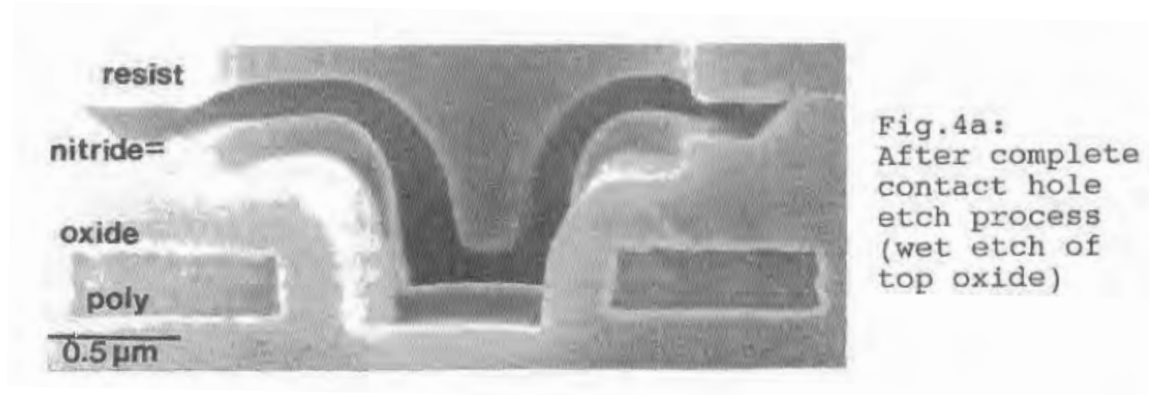


Figure 4a depicts the structure fabricated by Kuesters’s process illustrated in Figure 2 after the contact hole etch process is completed. *Id.* at 4–5.

Following the formation of the contact hole, the dRAM structure is completed by adding a bitline, which is accomplished by depositing conductive material (TaSi_2 on top of polysilicon that is doped by As or P implantation) in the contact hole, as illustrated in Figure 2-4. *Id.* at 6.

3. Discussion

Petitioner asserts that Kuesters describes a process and a structure for a 4 Mbit dRAM cell with a 25% reduction in cell size, “achieved by a self aligned bitline contact.” Pet. 15–16 (citing Ex. 1005, 3). Petitioner argues that Kuesters is directed to the same challenges as the ’552 patent because Kuesters describes a “new technique for etching the dielectric underneath the bitline” that “ensure[s] a good insulation of bitline to polysilicon gates (wordline) and substrate for the overlapping contacts.” *Id.* at 16 (citing Ex. 1005, 4).

a. Claim 1

As set forth above, claim 1 recites numbered elements labeled (a) to (e) followed by a wherein clause that recites “a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°,” i.e., the “angle limitation.” The parties’ dispute with respect to anticipation by Kuesters centers on the “angle limitation.” Petitioner asserts that Kuesters discloses every limitation of claim 1, including the “angle limitation.” Pet. 31–40. Patent Owner disagrees but argues it “will *only* address” the final element, i.e., the “angle limitation,” of claim 1. PO Resp. 27 (emphasis added). Patent Owner asserts that Kuesters does not anticipate claim 1 because the reference does not disclose the “angle limitation” recited in claim 1. *Id.* at 27–34. In what follows, because the “angle limitation” is claim 1’s final element that describes the structural relationship of earlier recited elements, we will

discuss the preamble and the numbered elements (a) to (e) first before addressing the “angle limitation” of claim 1.

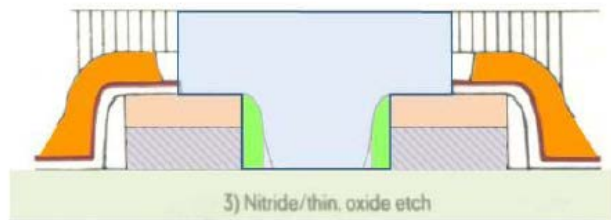
i. Preamble and Elements (a), (b), (c), (d), and (e)

Beginning with the preamble of claim 1, Petitioner cites Kuesters’s disclosure of a dRAM structure in Figures 2 and 4 as disclosing a “structure” recited in claim 1. Pet. 31–32 (citing Ex. 1005, 3–4, Figs. 2, 4). According to Petitioner, Figures 2 and 4a disclose a fully overlapping bitline contact (FOBIC) of a 4Mbit dRAM fabricated in accordance with the etching methods disclosed in Section 2.2.1(b) of Kuesters. *Id.* at 32.

We agree with Petitioner that Kuesters discloses a “structure” recited in claim 1 because, as noted by Petitioner, Kuesters describes “a self[-]aligned bitline contact” in a “4 Mbit dRAM cell” (*id.* at 31 (citing Ex. 1005, 3)) and “a trench capacitor cell with self[-]aligned, fully overlapping bitline contact (FOBIC)” (*id.* at 32 (citing Ex. 1005, 3)).

Petitioner next addresses the limitations recited in the body of claim 1. Claim 1 numbers from (a) to (e) the elements recited in the body of the claim and recites the numbered elements as follows: (a) a conductive layer disposed over a substrate; (b) a first insulating layer on the conductive layer; (c) a contact region in said first insulating layer; (d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and (e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer. Petitioner asserts that the structure depicted in Figures 2 and 4a of Kuesters discloses each of these numbered elements. *Id.* at 32–39.

Petitioner provides annotated versions of Figures 2-3 and 4a shown below.



SAMSUNG-1005, Kuesters at Figure 2 (with annotations)

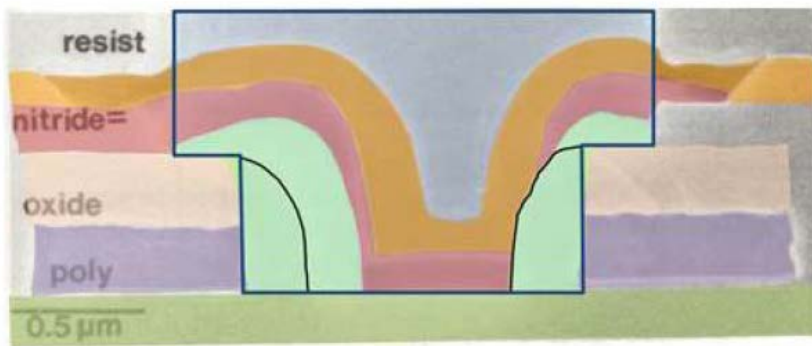


Fig.4a:
After complete
contact hole
etch process
(wet etch of
top oxide)

SAMSUNG-1005, Kuesters at Figure 4a (with annotations)

Annotated versions of Figures 2-3 and 4a in Petition

Id. at 33. According to Petitioner and Dr. Fair, Figure 4a depicts a cross-section scanning electron microscope (“SEM”) image of the actual structure fabricated in accordance with the etching methods disclosed in section 2.2.1(b) of Kuesters. *Id.* at 19, 32; Ex. 1003 ¶ 90. Petitioner argues that Figure 2 is a drawing depicting the same 4 Mbit dRAM structure according to the same etching process. *Id.* at 32. Petitioner asserts that Figure 2-3 is a two-dimensional illustration that highlights the structure at the center of the contact hole, whereas Figure 4a depicts a three-dimensional image that discloses the structure both at the center and along the back plane of the

contact region. *Id.* at 33 & n.7. The contact region is annotated in light blue in Annotated Figures 2 and 4a. *Id.* at 36.

Petitioner asserts that the polysilicon conductive gate layer formed over a substrate depicted in Figures 2-3 and 4a discloses “(a) a conductive layer disposed over a substrate,” as recited in claim 1. *Id.* at 32–34 (citing Ex. 1005, 4, Figs. 2, 4a). According to Petitioner, Annotated Figure 4a above shows a conductive polysilicon gate layer (annotated in purple) deposited over the substrate (annotated in dark green) in Kuesters’s dRAM structure. *Id.* at 33–34; Ex. 1003 ¶ 93. Petitioner further argues that Kuesters describes a “new technique for etching the dielectric underneath the bitline” that “ensure[s] a good insulation of bitline to *polysilicon gates* (wordline) and *substrate* for the overlapping contacts.” *Id.* at 16, 32 (quoting Ex. 1005, 4) (emphases added).

We are persuaded by Petitioner’s argument and evidence that Kuesters discloses “a conductive layer disposed over a substrate” as claimed because, as noted by Petitioner, Kuesters describes fabricating a contact region including a polysilicon gate layer and substrate (*id.* at 16, 32 (quoting Ex. 1005, 4)), and the structures identified by Petitioner in Figures 2-3 and 4a show that the polysilicon conductive gate layer is formed over the substrate.

Petitioner next asserts that the oxide insulating layer annotated in light orange in Annotated Figures 2-3 and 4a above discloses “(b) a first insulating layer on the conductive layer,” as recited in claim 1. *Id.* at 34–35. Petitioner notes that the oxide insulating layer is labeled “oxide” in the original Figure 4a of Kuesters. *Id.* at 35. Petitioner argues that Figures 2-3

and 4a show that the oxide insulating layer is formed on the polysilicon gate layer. *Id.* Petitioner further asserts Kuesters discloses a process of encapsulating the gate with an insulating layer and a subsequent etching process to form a contact hole that leaves the oxide insulating layer intact. *Id.* at 34–35 (citing Ex. 1005, 4–5).

We are persuaded by Petitioner’s argument and evidence that Kuesters discloses a completed contact hole structure with an oxide insulating layer formed on the conductive polysilicon gate layer because, as noted by Petitioner, Kuesters discloses that the “gate is encapsulated by oxide using an oxide spacer technique” (*id.* at 34 (quoting Ex. 1005, 3)) and that “[a]fter completing the process (see fig. 3c,4b,4c) an oxide insulation of the gate > 120 nm is obtained” (*id.* at 34–35 (quoting Ex. 1005, 5)). Further, the structures identified by Petitioner in Figures 2-3 and 4a show that the oxide insulating layer (annotated in light orange) is formed on the polysilicon conductive gate layer (annotated in purple). Thus, Petitioner demonstrates sufficiently that Kuesters discloses “(b) a first insulating layer on the conductive layer,” as recited in claim 1.

Next, Petitioner asserts that Kuesters’s contact hole or contact area extending through the oxide encapsulation discloses “(c) a contact region in said first insulating layer,” as recited in claim 1. *Id.* at 35–36. Petitioner identifies the area annotated in light blue in Annotated Figures 2 and 4a reproduced above as the claimed “contact region” disclosed in Kuesters. *Id.* at 36.

We are persuaded by Petitioner’s argument and evidence that Kuesters discloses a contact hole, i.e., the claimed “contact region,”

extending through the oxide insulating layer, i.e., the claimed “first insulating layer,” because, as noted by Petitioner, Kuesters discloses forming a contact hole by etching a triple layer of top oxide, nitride, and insulating oxide. *Id.* at 35–36 (quoting Ex. 1005, 4 (the first paragraph of Kuesters’s Section 2.2.1 titled “Contact hole etch”)). The Petitioner-cited portion of Kuesters discloses that “the top oxide is etched using the nitride as an etch stop” and, subsequently, “the underlying nitride/oxide is etched anisotropically” to form a contact hole without “significantly affect[ing] the oxide insulation of the gate.” *Id.* (quoting Ex. 1005, 4, 5). As noted by Petitioner, Kuesters also discloses that “[t]he contact area of the FOBIC contact is defined by gate and field oxide edges” (*id.* at 36 (quoting Ex. 1005, 5)), that is, the contact area is delineated by the oxide insulating layer. Thus, Petitioner demonstrates sufficiently that Kuesters discloses “(c) a contact region in said first insulating layer,” as recited in claim 1.

Petitioner next asserts that the oxide spacer of Kuesters encapsulating the polysilicon gate layer discloses “(d) at least one insulating spacer in the contact region adjacent to the first insulating layer,” as recited in claim 1. *Id.* at 37–38. Petitioner identifies the oxide spacer annotated in bright green in Annotated Figures 2-3 and 4a above as the claimed “insulating spacer in the contact region adjacent to the first insulating layer.” *Id.* at 38.

We are persuaded by Petitioner’s argument and evidence that Kuesters discloses an insulating oxide spacer encapsulating the polysilicon gate layer because, as noted by Petitioner, Kuesters describes that “[a]fter patterning a double layer of *poly Si/oxide* . . . an *oxide spacer* is formed by oxide deposition (TEOS) and RIE etching . . . [and] [t]he *poly gate* is

insulated by at least 0.15 μm oxide.” *Id.* at 37 (emphases added) (quoting Ex. 1005, 4 (the first paragraph of Kuesters’s Section 2.1 titled “Oxide encapsulation of the gate”)). We are persuaded that the insulating oxide spacer of Kuesters is adjacent to the oxide insulating layer, i.e., the claimed “first insulating layer,” because the Petitioner-cited portion of Kuesters quoted above describes that the polysilicon gate layer is encapsulated by the oxide insulating layer and the insulating oxide spacer. As noted by Petitioner, Kuesters also discloses that “gate is encapsulated by oxide using an oxide spacer technique.” *Id.* (quoting Ex. 1005, 3). Further, Annotated Figures 2-3 and 4a reproduced above show that the oxide spacer identified by Petitioner (annotated in bright green) is adjacent to the oxide insulating layer (annotated in light orange and labeled “Oxide” in Figure 4a), i.e., the claimed “first insulating layer,” and in the contact area (annotated in light blue), the claimed “contact region.” Thus, Petitioner demonstrates sufficiently that Kuesters discloses “(d) at least one insulating spacer in the contact region adjacent to the first insulating layer,” as recited in claim 1.

Petitioner further asserts that the nitride layer of Kuesters discloses “(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,” as recited in claim 1. *Id.* at 38–39. Petitioner asserts that the nitride layer of Kuesters is an etch stop material and is deposited over the oxide insulating layer and adjacent to the oxide spacer of Kuesters. *Id.* (citing Ex. 1005, 3, 4, 5). Petitioner identifies the nitride layer annotated in red in Annotated Figures 2-3 and 4a above as the claimed “etch stop material over said first insulating layer and adjacent to the insulating spacer.” *Id.* at

39. Petitioner further contends that nitride is a different material from the insulating spacers made of oxide. *Id.*

We are persuaded by Petitioner’s argument and evidence that the nitride layer of Kuesters is an etch stop material because, as noted by Petitioner, Kuesters discloses that “[a]fter patterning the contact hole mask the top oxide is etched using the nitride as an etch stop.” *Id.* at 38 (quoting Ex. 1005, 4). Further, Annotated Figures 2-3 and 4a show that the nitride layer (annotated in red) is formed over the oxide insulating layer, i.e., the claimed “first insulating layer” and adjacent to the oxide spacer, i.e., the claimed “insulating spacer.” Hence, we are persuaded that Kuesters discloses “(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,” as recited in claim 1.

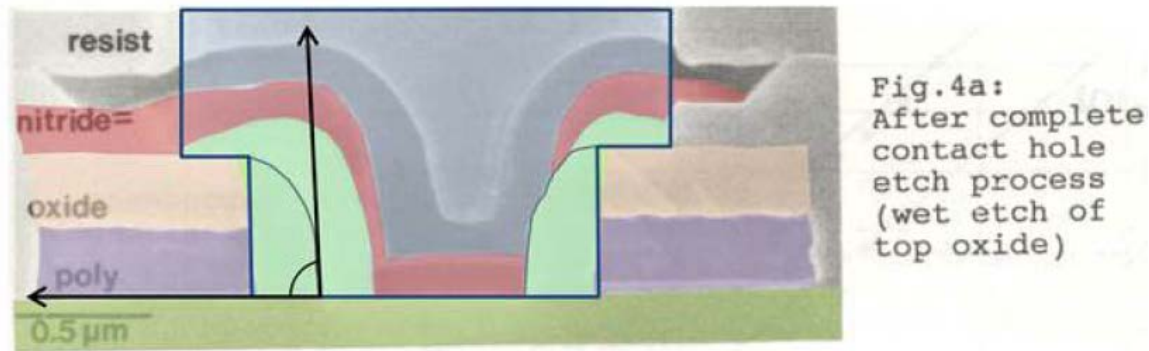
Patent Owner does not dispute specifically Petitioner’s contention that Kuesters discloses the preamble and numbered elements (a), (b), (c), (d), and (e) of claim 1. Upon considering the complete record, we determine Petitioner has demonstrated sufficiently that Kuesters discloses the preamble and elements (a), (b), (c), (d), and (e) of claim 1.

ii. The “Angle Limitation”

Citing the testimony of Dr. Fair, Petitioner contends that Figure 4a of Kuesters discloses the “angle limitation” recited in claim 1, i.e., the limitation reciting “a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.” Pet. 39–40 (citing Ex. 1003 ¶ 96). According to Dr. Fair, interpreting

and understanding an SEM image, such as the one shown in Figure 4a, requires a background on the SEM method and the reading of SEM images. Ex. 1003 ¶ 47. Referring to Annotated Figure 4a reproduced above, Dr. Fair testifies that the black line on the insulating spacers (annotated in bright green) denotes “the leading edge of the insulating spacer at the front plane of the SEM image (i.e., the center of the contact hole).” *Id.* ¶ 93. Dr. Fair further testifies that the region also annotated in bright green above the black line reflects “the sidewall spacer receding into the page toward the back plane of the contact hole,” which is an artifact of SEM imaging due to the fact that the incident angle of the electron beam of the SEM to the surface of the sidewall spacer in this area is not 90°. *Id.* Hence, according to Dr. Fair, for the actual fabricated structure of Kuesters depicted in Figure 4a, the angle of a side of the insulating spacer relative to the substrate surface can be measured where it contacts the pale green of the substrate, i.e., where the black line meets the upper edge of the horizontal substrate annotated in pale green. *Id.* ¶ 96.

Petitioner provides a version of Figure 4a further annotated by Dr. Fair, which is reproduced below.



SAMSUNG-1005, Kuesters at Figure 4a (with annotations)

Dr. Fair annotated version of Figure 4a in Petition

Pet. 40. Dr. Fair testifies that he has measured the angle of a side of the insulating spacer relative to the substrate surface in Kuesters, as illustrated in Dr. Fair Annotated Figure 4a shown above, and found the measured angle to be “between 86° and 87°.” Ex. 1003 ¶ 96.

Patent Owner disputes Dr. Fair’s angle measurement and asserts that the angle measured by Patent Owner on Annotated Figure 4a is less than 85°. PO Resp. 31–32. Patent Owner also asserts that the black line drawn by Dr. Fair to denote the leading edge of the insulating spacer in Annotated Figure 4a is not present in the original Figure 4a of Kuesters and that, because there is no clear distinction or demarcation between the layers shown in the SEM image of Figure 4a, Dr. Fair’s angle measurement is unreliable. *Id.* at 32–33. Patent Owner further asserts that the alleged lack of clear distinction or demarcation is in part due to the fact that, as

acknowledged by Dr. Fair, the SEM image of Figure 4a was “not taken at a 90° angle to the structure.” *Id.* at 25 (citing Ex. 1003, 37), 32–33.

In its Reply, Petitioner responds that Patent Owner’s contentions are unsupported attorney arguments because Patent Owner did not submit any expert declaration to contradict Dr. Fair’s declaration. Pet. Reply 1.

Petitioner also argues Patent Owner did not cross-examine Dr. Fair on his opinions or methods. *Id.* According to Petitioner, Patent Owner’s attorney simply made an erroneous angle measurement to obtain a different angle from Dr. Fair. *Id.* at 9–12.

Petitioner argues that interpreting and measuring an SEM image involves ordinary skill. *Id.* at 12. As discussed above, Dr. Fair opines that interpreting and understanding an SEM image, such as the one shown in Figure 4a, requires a background on the SEM method and the reading of SEM images. Ex. 1003 ¶ 47. In his Declaration in Support of Petitioner’s Reply, Dr. Fair further explains that one of ordinary skill in the art, having experience with and knowledge of semiconductor fabrication, would have experience in viewing and analyzing SEM images, including experience with identifying and locating the boundaries between adjacent elements or regions in a structure. Ex. 1014 ¶ 36. Dr. Fair opines that a layperson would not be expected to have such experience and knowledge, and, therefore, could not be expected to accurately or reliably interpret an SEM image or to locate the boundaries between adjacent elements or regions in a structure. *Id.*

Petitioner argues that Dr. Fair, as a person of ordinary skill in the art, analyzed the SEM image in Figure 4a of Kuesters, performed a standard

measurement on the image using accepted techniques, and annotated the figure to illustrate his measurement. Pet. Reply 2–3. Petitioner asserts that Dr. Fair measured the angle between the substrate and the sidewall from the SEM image itself in Figure 4a, and then annotated the image to illustrate what he measured and how he measured it. *Id.* at 5–6 (citing Ex. 1003, Appx. A, A-20). Citing the testimony of Dr. Fair, Petitioner further asserts that SEM images, such as the image in Figure 4a of Kuesters, are used routinely in the industry by those of ordinary skill to measure the lengths, widths, thicknesses, and relative angles between the layers of semiconductor structures. *Id.* at 7–8 (citing Ex. 1014 ¶ 35).

Dr. Fair testifies that he used techniques routinely used by those of ordinary skill to perform his measurements and that the SEM image in Figure 4a is sufficiently clear to allow a person of ordinary skill to locate the intersections between the edge of the left sidewall spacer and the substrate and to measure the angles between the surfaces at those intersections. Ex. 1014 ¶ 32. According to Dr. Fair, SEM images are used by those of ordinary skill in the art to determine the dimensions and relative positions of structures formed on a semiconductor substrate. *Id.* ¶ 35. Dr. Fair testifies that SEM images have been used for decades to determine angles formed between different structures on a semiconductor substrate, e.g., to determine whether a contact etch is sufficiently anisotropic and if the contact hole has sufficiently vertical sidewalls. *Id.* Dr. Fair also provides an extensive discussion of how an SEM image is formed and how a person of ordinary skill in the art would interpret SEM images. Ex. 1003 ¶¶ 48–53; Ex. 1014 ¶¶ 34–36.

Dr. Fair cites to his initial Declaration and testifies that he used techniques well-known to those of ordinary skill to measure, on the SEM image from Figure 4a itself, the angle at the intersection of the edge of the left sidewall spacer and the substrate surface, and then annotated Figure 4a with colors and lines to illustrate the angle he had measured. *Id.* ¶ 38 (citing Ex. 1003 ¶¶ 92, 96, Appx. A, A-20–A-21). Dr. Fair also provides the details of the techniques and the process he used to make the angle measurements. *Id.* ¶¶ 39–42. Dr. Fair testifies that the SEM image in Figure 4a of Kuesters discloses the angle he measured to a person of ordinary skill in the art. *Id.* ¶ 42. Dr. Fair further testifies that, to a person of ordinary skill in the art, the distinction between the surfaces shown in the SEM image of Figure 4a in the left side of the contact hole is clear, and the angle of intersection between the left sidewall spacer edge and the substrate can be readily located and measured from the SEM image itself. *Id.* ¶ 44. Dr. Fair opines that Figure 4a can reliably be used to discern properties of the various layers shown, such as the relative positions and relationships between the different layers in the structure, and that it would have been routine for one of ordinary skill to interpret the SEM image in Figure 4a accurately. *Id.*

Dr. Fair further testifies that the fact that the SEM image in Figure 4a was taken with the incident electron beam at an angle less than 90° to the dRAM structure in the azimuthal plane (i.e., in the horizontal plane to take a cross-sectional image) does not affect the vertical dimensions in the image and, therefore, does not affect the accuracy of the angle measurement, on the vertical plane, of the angle between the edge of the sidewall spacer and the substrate surface. *Id.* ¶¶ 45–46.

We credit Dr. Fair's testimony and find that Dr. Fair's angle measurement from the SEM image in Figure 4a of Kuesters provides persuasive evidence of how a person of ordinary skill would interpret the SEM image. We are persuaded that Dr. Fair's angle measurement was in accordance with the established, reliable method well-known to a person of ordinary skill in the art. We also agree with Petitioner that Patent Owner's arguments against Dr. Fair's angle measurement are unpersuasive as unsupported attorney arguments. Patent Owner's angle measurement is similarly unpersuasive as unsupported and lacking foundational showing that Patent Owner's measurement is based on established, reliable methods.

Patent Owner further asserts that Kuesters does not disclose explicitly the specific angle of a side of the insulating spacer relative to the substrate surface, as recited in claim 1. PO Resp. 29. As noted by Petitioner, however, Kuesters discloses that “[a] *vertical* etch profile of [the polysilicon/oxide layer] . . . is essential” when forming the oxide sidewall spacers (Pet. 37 (emphasis added) (quoting Ex. 1005, 4)) and that the “nitride/oxide is etched *anisotropically*” to form the contact hole of the self-aligned contact (*id.* at 36 (emphasis added) (quoting Ex. 1005, 5)). Hence, the result of Dr. Fair's angle measurement on Figure 4a is consistent with these express disclosures regarding the structure of the oxide spacer in Kuesters. As discussed above, the '552 patent also describes forming “substantially rectangular” lateral insulating spacers (Ex. 1001, col. 8, ll. 40–42) by an “anisotropic” etching (*id.* at col. 7, ll. 45–48, 53–55; col. 12, ll. 55–61).

Patent Owner further asserts that Kuesters does not disclose using “low-selectivity etching” to produce an adequately insulative lateral spacer portion which “retains a rectangular or ‘boxy’ profile” and has only “a small portion” removed during the etching process. PO Resp. 34 (citing Ex. 1001, col. 13, ll. 4–8). In its Reply, Petitioner responds that claim 1 does not recite the limitations argued by Patent Owner, and that it is improper to import such limitations from the Specification. Pet. Reply 14–16. We agree with Petitioner’s argument.

Patent Owner’s argument is unpersuasive because the ’552 patent Specification expressly states that the use of a low selectivity etch to form a spacer portion that retains a rectangular or “boxy” profile and has only “a small portion” removed is “exemplary” and does not limit the claimed invention. For example, the ’552 patent states as follows:

The etchant utilized to remove silicon nitride from the contact opening 460 has a low selectivity for etching the silicon nitride material compared to the underlying TEOS layer 420. . . . The *low selectivity etch yields a TEOS layer spacer portion 435 that retains a rectangular or “boxy” profile.* FIG. 4(K) illustrates that *only a small portion 475* (illustrated in ghost lines) of the TEOS layer spacer portion 435 *is removed* during the etch. *Of primary significance, the spacer portion 435 of the TEOS layer 420 retains its substantially rectangular profile.*

It is to be appreciated that *the described etch stop layer etch conditions* (i.e., *low selectivity, low bombardment/high neutral flux*) are *exemplary* of etch conditions that result in the retention of a boxy spacer.

Ex. 1001, col. 12, l. 66–col. 13, l. 14 (emphases added). The ’552 patent further specifies that “[t]he invention relates to these process conditions as

well as *others that result in the retention of a boxy spacer,*” and, therefore, “the etch-stop etch conditions should be regarded in an *illustrative rather than restrictive* sense.” *Id.* at col. 13, ll. 14–18 (emphases added).

Furthermore, the challenged claims do not recite using a low selectivity etch, or, for that matter, any limitations relating to the conditions or methods of the etching process. In general, “even if *all of the embodiments* discussed in the patent included a specific limitation, it would not be proper to import from the patent’s written description limitations that are not found in the claims themselves.” *Cadence Pharm. Inc. v. Exela PharmSci Inc.*, 780 F.3d 1364, 1369 (Fed. Cir. 2015) (emphasis added) (citations omitted) (internal quotation marks omitted). Further, “it is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited.” *Epos Techs. Ltd. v. Pegasus Techs. Ltd.*, 766 F.3d 1338, 1341 (Fed. Cir. 2014). In view of the passages of the ’552 patent quoted above that describe the use of a low selectivity etch as “exemplary” or “illustrative” and not restrictive, we find the disclosure of the ’552 patent cited by Patent Owner as purportedly limiting the invention does not rise to the level of a clear indication that the patentee intended to limit the challenged claims to require the use of a low selectivity etch or other limitations argued by Patent Owner that are not recited in the claims.

Patent Owner further argues that Kuesters does not disclose “using low-selectivity etching to produce an adequately insulative lateral spacer portion which . . . retains an additional insulating layer of ‘etch stop material

adjacent to the spacer portion.” PO Resp. 34 (citing Ex. 1001, col. 12, ll. 59–60). It is unclear what Patent Owner argues because Patent Owner does not provide any further explanation beyond the single sentence stating Patent Owner’s contention. As discussed above with respect to limitation (e) recited in claim 1, we are persuaded Petitioner has demonstrated sufficiently that Kuesters discloses the nitride layer, i.e., the claimed “etch stop material” is adjacent to the oxide spacer, i.e., the claimed “insulating spacer.”

Based on the complete record, we are persuaded Petitioner has demonstrated sufficiently that Kuesters discloses “a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°,” as recited in claim 1.

iii. Conclusion

Based on the complete record, we find that Petitioner has shown sufficiently Kuesters discloses each limitation of independent claim 1 as arranged in the claim. Accordingly, upon considering all of the evidence of record, we determine that Petitioner has demonstrated, by a preponderance of evidence, that claim 1 is unpatentable under 35 U.S.C. § 102(b) as anticipated by Kuesters.

b. Claim 8

Independent claim 8 is similar to claim 1 in that the claims recite similar limitations, although claim 8 recites “electrically insulative spacer” instead of “insulating spacer” recited in the corresponding limitations of claim 1. For example, both claims recite essentially the same “angle

limitation,” the only difference being that claim 8 recites “electrically insulative spacer” instead of “insulating spacer” recited in claim 1.

Tracking the language of the claims, the ’552 patent uses the terms “insulating spacer” and “insulative spacer” interchangeably throughout the written description. *See, e.g.*, Ex. 1101, col. 6, ll. 13–65; *see also id.* at col. 13, ll. 55–62 (using “the spacer portions of the insulating material” and “the spacer portions [of] insulative material” interchangeably). The parties also appear to use the terms “insulating spacer” and “insulative spacer” interchangeably in the Petition and the Patent Owner Response. *See, e.g.*, Pet. 37–38; PO Resp. 23–24. Upon considering the complete record, we deem the terms “insulating spacer” and “insulative spacer” to be interchangeable and to have no meaningful difference in their meaning in the context of the ’552 patent.

For similar limitations of claims 1 and 8, Petitioner relies on the same or similar structures disclosed in Kuesters for both claims. For example, for both “insulating spacer” recited in claim 1 and “electrically insulative spacer” recited in claim 8, Petitioner relies on the oxide spacer described in Kuesters, including the oxide spacer annotated in bright green in Annotated Figures 2-3 and 4a. Pet. 37–38 (claim 1), 48 (claim 8). Similarly, Petitioner maps both the “conductive layer disposed over a substrate” recited in claim 1 and the “second electrically conductive material formed on the substrate” recited in claim 8 to the polysilicon gate layer of Kuesters. *Id.* at 32–34 (claim 1), 47 (claim 8). Petitioner also relies on the nitride layer disclosed in Kuesters for both the “etch stop material over the electrically insulative spacer . . . the etch stop material being a different material from the

insulative spacer,” as recited in claim 8, and the “etch stop material over said first insulating layer . . . the etch stop material being a different material from the insulating spacer” recited in claim 1. *Id.* at 38–39 (claim 1), 49 (claim 8). In addition, Petitioner relies on Kuesters’s contact hole (or contact area) as disclosing both the “contact region” recited in claim 1 and the “contact opening” recited in claim 8. *Id.* at 35–36 (claim 1), 47 (claim 8). Thus, Petitioner demonstrates sufficiently that Kuesters discloses these limitations of claim 8 for the same reasons discussed above with respect to claim 1.

Similarly, for the angle limitations in claims 1 and 8, Petitioner relies on the same disclosure in Kuesters, including the angle measured on Figure 4a depicting an SEM image of the fabricated structure discussed above with respect to claim 1. *Id.* at 39–40 (claim 1), 50–51 (claim 8). Hence, Petitioner demonstrates sufficiently that Kuesters discloses the angle limitation recited in claim 8 for essentially the same reasons discussed above with respect to claim 1.

Petitioner also addresses the substantive differences between claims 1 and 8 and presents an analysis of how Kuesters discloses the different or additional limitations of claim 8, providing detailed explanations and specific citations to Kuesters. *Id.* at 46–51.

Petitioner asserts that Kuesters discloses “(a) a first electrically conductive material formed in and/or on a surface of a substrate,” as recited in claim 8. *Id.* at 46–47 (citing Ex. 1005, 4, Figs. 2-3, 2-4, 4a; Ex. 1003, Appx. A, A-32–A-35). Petitioner identifies electrically conductive n⁺ diffusion regions in the surface of the substrate in Figures 2 and 4a as the

claimed “first electrically conductive material formed in and/or on a surface of a substrate.” *Id.* (citing Ex. 1005, Figs. 2-3, 2-4, 4a).

We are persuaded by Petitioner’s argument and evidence that Kuesters discloses an “electrically conductive material formed in and/or on a surface of a substrate” as claimed because, as noted by Petitioner, Kuesters discloses “contacts connecting the polycide bitline to n⁺ diffusion (source/drain of transfer gates)” (*id.* at 46 (quoting Ex. 1005, 4)) and because Dr. Fair explains that a person of ordinary skill would understand that n⁺ diffusion regions that make up the source and drain of Kuesters’s dRAM cell (identified by Petitioner in Figures 2-3, 2-4, and 4a) are electrically conductive regions in the surface of the substrate (Ex. 1003, Appx. A, A-32–A-35).

Petitioner further asserts that Kuesters discloses “(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate,” as recited in claim 8. Pet. 47–48. As discussed above, the contact hole and the polysilicon conductive gate layer of Kuesters disclose the “contact opening” and the “second electrically conductive material formed on the substrate” recited in claim 8, respectively.

We are persuaded by Petitioner’s argument and evidence that Kuesters discloses a contact opening in a region adjacent to a second electrically conductive material, as recited in claim 8, because, as shown in Annotated Figures 2-3 and 4a reproduced in Claim 1 subsection above, the contact area of Kuesters (annotated in light blue in Annotated Figures 2-3 and 4a) is adjacent to the conductive gate layer (annotated in purple). *Id.* (citing Ex. 1005, Fig. 2; Pet. § 9.1.4).

Petitioner next asserts that Kuesters discloses “(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material,” as recited in claim 8. *Id.* at 48. As discussed above, the oxide spacer described in Kuesters discloses the “electrically insulative spacer” recited in claim 8.

We are persuaded by Petitioner’s argument and evidence that Kuesters discloses an “electrically insulative spacer in the contact opening” as claimed because, for the same reasons discussed above with respect to claim 1, Kuesters discloses that the oxide spacer is formed in the contact area. *Id.* (citing *id.* § 9.1.5). We are also persuaded that Kuesters discloses “an electrically insulative spacer . . . adjacent to the second electrically conductive material” because, as noted by Petitioner, Figures 2-3 and 4a of Kuesters show that the oxide spacer (annotated in bright green in Annotated Figures 2-3 and 4a) is adjacent to the conductive gate layer (annotated in purple). *Id.* (citing Ex. 1005, Figs. 2, 4a; Pet. § 9.1.5).

Next, Petitioner asserts that Kuesters discloses “(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer,” as recited in claim 8. *Id.* at 49. As discussed above, the nitride layer of Kuesters discloses “an etch stop material over the electrically insulative spacer . . . the etch stop material being a different material from the insulative spacer” as claimed.

We are persuaded Kuesters also discloses the etch stop material is “over . . . the first and second electrically conductive materials” as well because, as Petitioner argues, Figures 2-3 and 4a show that the nitride etch

stop layer (annotated in red in Annotated Figures 2-3 and 4a) extends over the n⁺ diffusion (source and drain) regions, i.e., the claimed “first electrically conductive material,” as well as over the conductive gate layer, i.e., the claimed “second electrically conductive material.” *Id.* (citing Ex. 1005, Figs. 2, 4a; Pet. § 9.1.6).

Petitioner further asserts that Kuesters discloses “(e) a blanket layer over the etch stop material,” as recited in claim 8. *Id.* at 49–50 (citing *id.* § 9.5.1 (Claim 6)). Petitioner contends that the top oxide layer of the triple oxide/nitride/oxide stack described in Kuesters (annotated in orange in Annotated Figures 2-3 and 4a reproduced above in Claim 1 subsection) discloses the limitation. *Id.* at 43–44 (citing Ex. 1005, 3, 4; Figs. 2, 4a).

We are persuaded that Kuesters discloses “a blanket layer over the etch stop material” because, as Petitioner notes, Kuesters discloses that “[t]he dielectric under the bitline consists of a triple layer of thin oxide/nitride/oxide” (*id.* at 43 (quoting Ex. 1005, 4)), and Figures 2-3 and 4a of Kuesters show that the top oxide layer (annotated in orange in Annotated Figures 2-3 and 4a), i.e., the claimed “blanket layer” is over the nitride layer (annotated in red), i.e., the claimed “etch stop material.”

Petitioner next asserts that Kuesters discloses “(f) an opening through a first part of the etch stop material to the first electrically conductive material,” as recited in claim 8 because Kuesters describes that, after the contact hole is opened, an anisotropic etch is performed to remove the nitride etch stop from the center of the contact hole, resulting in the structure depicted in Figure 2-3. *Id.* at 50 (citing *id.* § 8.1).

We are persuaded by Petitioner’s argument and evidence because Petitioner-cited portion of Kuesters describes that, after the top oxide of the triple oxide/nitride/oxide layer is wet etched to open the contact hole, the nitride etch stop, i.e., the claimed “etch stop material,” and the thin oxide layer underneath the nitride layers are dry etched to form the contact area of the FOBIC contact. *Id.* at 18–19 (citing Ex. 1005, 5, Figs. 2-2, 2-3). We are also persuaded that the resulting structure depicted in Figure 2-3 of Kuesters shows that the contact area provides an opening to the n+ diffusion (source and drain) region, i.e., the claimed “first electrically conductive material.” *Id.* at 50 (citing Ex. 1005, Fig. 2-3). Hence, Petitioner demonstrates sufficiently that Kuesters discloses “(f) an opening through a first part of the etch stop material to the first electrically conductive material,” as recited in claim 8.

Therefore, based on the complete record, we are persuaded Petitioner has shown Kuesters discloses each limitation of independent claim 8 as arranged in the claim. Patent Owner does not respond separately, with specificity, to Petitioner’s challenge to claim 8 beyond Patent Owner’s arguments advanced with respect to claim 1 discussed above. *See* PO Resp. 34–35. Upon considering the complete record, we determine that Petitioner has demonstrated, by a preponderance of evidence, that claim 8 is unpatentable under 35 U.S.C. § 102(b) as anticipated by Kuesters.

c. Dependent Claims 2, 4–7, and 9–12

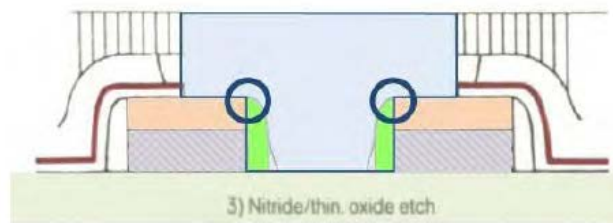
Claims 2 and 4–7 depend from claim 1, and claims 9–12 depend from claim 8. Regarding these dependent claims, Petitioner provides detailed

explanations and specific citations to Kuesters indicating where in the reference the additionally recited limitations of the dependent claims are disclosed. Pet. 40–45, 51–52.

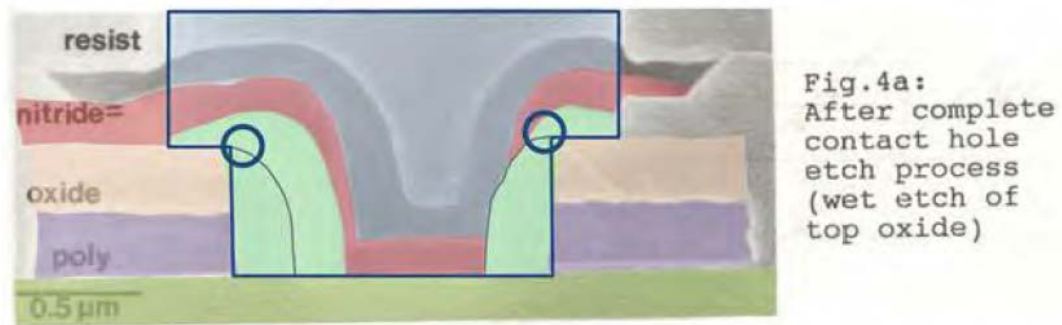
With respect to claim 2, which depends from claim 1 and further recites “said etch stop material comprises silicon nitride,” Petitioner asserts that the nitride etch stop layer of Kuesters discussed above comprises silicon nitride. *Id.* at 40–41 (citing Ex. 1005, 3, 4, 5). We are persuaded that Kuesters discloses “said etch stop material comprises silicon nitride,” as recited in claim 2, because, as noted by Petitioner, Kuesters discloses that the “nitride [layer] serves as an etch stop for top oxide etch.” *Id.* at 40 (quoting Ex. 1005, 3).

Claim 4 depends from claim 1 and further recites “the insulating spacer has a surface portion in the contact region without overlying etch stop material.” Claim 5 depends from claim 4 and additionally recites “the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate.” Claims 9 and 10, which depend from claim 8, recite additional limitations similar to claims 4 and 5, respectively, with claims 9 and 10 reciting “electrically insulative spacer” instead of “insulating spacer” recited in claims 4 and 5. Referencing further annotated versions of Figures 2-3 and 4a, Petitioner points to the structures depicted in Figures 2-3 and 4a of Kuesters and asserts that Kuesters discloses these additionally recited limitations, providing description of the relevant structures and explanations in support of its argument. *Id.* at 41–43 (citing Ex. 1005, Figs. 2-3, 4a), 51–52.

Petitioner provides further annotated versions of Figures 2-3 and 4a shown below.



SAMSUNG-1005, Kuesters at Figure 2 (with annotations)



SAMSUNG-1005, Kuesters at Figure 4a (with annotations)

Further annotated versions of Figures 2-3 and 4a in Petition

Id. at 41–42. Petitioner identifies the portions of the oxide spacer annotated with a blue circle in Further Annotated Figures 2-3 and 4a reproduced above, and asserts that the identified portions disclose a surface portion of the oxide spacer without an overlying nitride material, as recited in claims 4 and 9. *Id.* at 41–42, 51. Petitioner argues that Figure 4a shows the nitride adjacent to the oxide spacer along the back plane of the contact hole, but not in the center of the contact hole. *Id.* at 42, 21–22 (citing Ex. 1003 ¶¶ 91, 94). Thus, according to Petitioner, the surface area at the top edge of the oxide spacer in the center of the contact hole does not have overlying nitride

material. *Id.* at 42. Petitioner further argues that this interpretation is consistent with the corresponding drawings of Figure 2. *Id.* Petitioner further asserts that the same portions of the oxide spacer annotated with a blue circle are the insulating spacer surface portions most distant from the substrate, as recited in claims 5 and 10. *Id.* at 42–43, 51–52.

We credit Dr. Fox’s testimony and are persuaded that the nitride layer shown in Figure 4a (annotated in red in Further Annotated Figure 4a above) is in the back plane of the contact hole, and, therefore, does not overly the oxide spacer (annotated in light green). Based on the complete record and upon reviewing Figures 2-3 and 4a and the structures or geometries shown in the figures, we are persuaded that Petitioner has demonstrated sufficiently that Kuesters discloses the limitations recited in claims 4, 5, 9, and 10.

Claims 6 and 11 depend from claims 1 and 8, respectively, and each further recite “further comprising a second insulating layer on the etch stop layer and over the conductive layer.” Petitioner asserts that the top oxide layer of the triple oxide/nitride/oxide stack shown in Figures 2-3 and 4a discloses the additionally recited limitations. *Id.* at 43–44 (citing Ex. 1005, 3, 4), 52.

Petitioner relies on the same top oxide layer of the triple oxide/nitride/oxide stack described in Kuesters as disclosing both the “blanket layer over the etch stop material” recited in claim 8 and the “second insulating layer on the etch stop layer” recited in claims 6 and 11. *Id.* at 49–50 (citing *id.* § 9.5.1 (Claim 6)). Hence, we are persuaded that Kuesters discloses “a second insulating layer on the etch stop layer,” as recited in

claims 6 and 11, for the same reasons discussed above with respect to claim 8.

We are also persuaded that the top oxide layer is “over the conductive layer,” as recited in claim 6, because Figures 2-3 and 4a cited by Petitioner show that the top oxide layer is formed over the polysilicon conductive gate layer, i.e., the “conductive layer” recited in claim 6. *Id.* at 44 (citing Ex. 1005, Figs. 2-3, 4a). Although Petitioner does not address the apparent ambiguity in claim 11 as to whether “the conductive layer” recited in claim 11 refers to the “first electrically conductive material” or the “second electrically conductive material” of base claim 8, we are persuaded that Kuesters discloses the recited limitation of claim 11 under either interpretation because Figures 2-3 and 4a cited by Petitioner show that the top oxide layer is formed over the n+ diffusion (source and drain) region, i.e., the claimed “first electrically conductive material,” as well as over the polysilicon conductive gate layer, i.e., the claimed “second electrically conductive material.” *See id.* at 44, 52.

Claims 7 and 12 depend from claims 6 and 11, respectively, and each additionally recite “further comprising a second conductive material in the contact region.” Petitioner contends that Kuesters discloses the additionally recited limitations of claims 7 and 12 because Kuesters describes a “contact between polycide (TaSi) bitline” and the diffusion region of the substrate (*id.* at 44–45 (citing Ex. 1005, 3)) and “a low resistivity polycide (poly Si/TaSi₂) layer,” which is “used for bitlines and local peripheral interconnects” (*id.* at 45 (citing Ex. 1005, 4)).

We are persuaded by Petitioner's argument because a polysilicon/ TaSi₂ layer used to connect the bitline to the source/drain region in the structure disclosed in Kuesters would constitute "a second conductive material in the contact region" of claim 6, distinct from the polysilicon gate layer of Kuesters, i.e., the conductive material recited in claim 1 (*id.* at 32–34).

Petitioner does not address the potential ambiguity in claim 11 as to whether "a second conductive material in the contact region" recited in claim 11 refers to the "second electrically conductive material" recited in base claim 8 or yet another conductive material in addition to claim 8's first and second electrically conductive materials. Nonetheless, we are persuaded Kuesters discloses the recited limitation of claim 11 under either interpretation because Petitioner-cited portions of Kuesters disclose a polysilicon conductive gate layer, i.e., the "second electrically conductive material" recited in base claim 8, formed in the contact area, i.e., the claimed "contact region," of Kuesters, as discussed above with respect to claim 8, as well as a conductive polysilicon/ TaSi₂ layer used to connect the bitline to the source/drain region, distinct from the polysilicon gate layer of Kuesters, as discussed above with respect to claim 6.

Patent Owner does not respond separately, with specificity, to Petitioner's challenge to dependent claims 2, 4–7, and 9–12 beyond Patent Owner's arguments advanced with respect to claim 1 discussed above. PO Resp. 35. Upon considering the complete record, we determine that Petitioner has demonstrated, by a preponderance of evidence, that claims 2,

4–7, and 9–12 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Kuesters.

D. Obviousness Based on the Combination of Kuesters and Havemann

Claim 3 depends from claim 1 and further recites “said etch stop material comprises silicon dioxide.” Petitioner asserts that claim 3 is unpatentable under 35 U.S.C. § 103(a) over the combination of Kuesters and Havemann (Ex. 1006). Pet. 52–54.

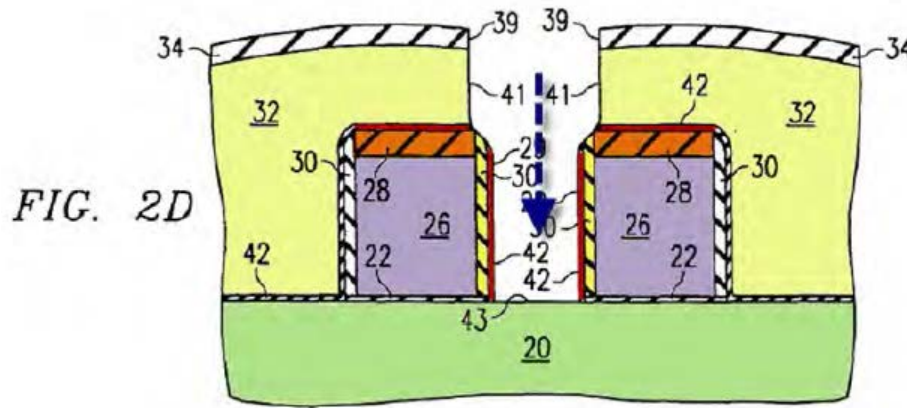
1. Overview of Havemann

Havemann describes a semiconductor device and a process of making a semiconductor device which incorporates organic dielectric materials to form self-aligned contacts reliably. Ex. 1006, Abstract. Havemann discloses at least two embodiments—the first embodiment is illustrated in Figures 1A to 1I (*id.* at col. 3, ll. 38–40; col. 3, l. 53–col. 5, l. 1), whereas the second embodiment is depicted in Figures 2A to 2D (*id.* at col. 3, ll. 41–43; col. 5, ll. 2–31).

2. Discussion

Petitioner acknowledges Kuesters does not disclose explicitly that the etch stop material comprises silicon dioxide, but asserts that this limitation would have been rendered obvious by the combination of Kuesters and Havemann. Pet. 53.

Figure 2D of Havemann, as annotated by Petitioner in colors, is reproduced below.



Annotated version of Figure 2D of Havemann in Petition

Id. at 24. Referencing Annotated Figure 2D, Petitioner identifies conductor cap 28 (annotated in orange) as the insulating cap, conformal layer 30 (annotated in yellow) as the sidewall spacer, and conformal dielectric overlayer 42 (annotated in red) as the etch stop material. *Id.* at 23–24 (citing Ex. 1006, col. 2, ll. 40–49, 52–54, col. 5, ll. 10–15, col. 6, ll. 11–14).

Petitioner asserts that Havemann teaches an etch stop material comprising silicon dioxide, as recited in claim 3, because Havemann describes that a thermally grown silicon dioxide can be used for the etch stop material. *Id.* at 53 (citing Ex. 1006, col. 5, ll. 9–21; col. 6, ll. 14–19, 31–33). Petitioner further asserts that Havemann teaches the insulating cap and sidewall spacers may comprise silicon nitride or silicon oxynitride, which are different materials from silicon dioxide. *Id.* (citing Ex. 1006, col. 5, ll. 9–15; col. 6, ll. 14–19). Petitioner argues, therefore, applying this teaching of Havemann to Kuesters would have resulted in the structure of

claim 1 with an etch stop material of silicon dioxide and an insulating layer and insulating spacer made of silicon nitride or silicon oxynitride. *Id.*

Relying upon the testimony of Dr. Fair, Petitioner argues that a person of ordinary skill in the art would have been motivated to combine Kuesters and Havemann because the references are in the same field and use similar methods to create similar structures and to solve the same problem, i.e., fabricating dRAM cells with reliable self-aligned contacts. *Id.* at 27–28 (citing Ex. 1005, 3, Fig. 2; Ex. 1006, col. 1, ll. 23–25, col. 2, ll. 15–20, Fig. 2; Ex. 1003 ¶¶ 113, 114). Petitioner further asserts that it would have been obvious to one skilled in the art to make the simple substitution of the silicon dioxide etch stop and silicon oxynitride spacer materials disclosed in Havemann for the nitride etch stop and oxide insulating spacer materials of the Kuesters’s semiconductor structure, and that such simple substitution of known materials would have produced predictable results. *Id.* at 28–29 (citing Ex. 1003 ¶¶ 114–116). Dr. Fair explains Havemann teaches that the substitution proposed by Petitioner would produce predictable and successful results. Ex. 1003 ¶ 115 (citing Ex. 1006, col. 6, ll. 5–34).

Upon reviewing Petitioner’s argument and evidence, we are persuaded that the proposed combination of Kuesters and Havemann teaches an insulating spacer formed of silicon nitride and an etch stop material made of silicon dioxide. As argued by Petitioner (Pet. 53), Havemann discloses an embodiment where the insulating cap (28) and sidewall spacer (30) are formed of silicon nitride (or silicon oxynitride) and the etch stop layer (42) is made of thermal-grown silicon oxide (Ex. 1006, col. 6, ll. 5–34).

We also agree with Petitioner that Kuesters and Havemann are in the same field and use similar methods to create similar structures and to solve the same problem. As Dr. Fair explains, both Kuesters and Havemann describe fabricating dRAM cells with self-aligned contacts. Ex. 1003 ¶ 114 (citing Ex. 1005, 3; Ex. 1006, col. 1, ll. 23–25, col. 2, ll. 15–20). As discussed above, the '552 patent is also directed to making high quality contacts in semiconductor devices, such as “self-aligned” contacts. Ex. 1001, Abstract, col. 7, ll. 19–22, col. 8, ll. 4–6. Hence, we are persuaded that a person of ordinary skill in the art would have been motivated to look to the teachings of Havemann when considering the materials to use for insulating layers and etch stop layers in the process of making contact openings in a multi-layer structure of a semiconductor device, such as the “self-aligned” contacts described in the '552 patent and Kuesters. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007) (“any need or problem known in the field and addressed by the patent can provide a reason for combining the elements in the manner claimed”).

We are also persuaded that a person of ordinary skill in the art would have had a reason to substitute the silicon dioxide etch stop and silicon oxynitride spacer materials disclosed in Havemann for the nitride etch stop and oxide insulating spacer materials of the Kuesters’s semiconductor structure because Havemann teaches explicitly the interchangeable use of silicon dioxide and silicon nitride for the etch stop layer and the insulating spacer as alternative embodiments. *See* Ex. 1006, col. 6, ll. 5–34 (describing alternative embodiments, including the interchangeable use of silicon dioxide and silicon nitride for layer 30 and overlayer 42). Based on the

complete record, we credit the testimony of Dr. Fair and are persuaded that it would have been obvious to a person of ordinary skill in the art to combine Kuesters and Havemann to make a structure recited in claim 3, including an “etch stop material” comprising silicon dioxide and an “insulating spacer” made of a different material from the etch stop material, such as silicon nitride or silicon oxynitride. *See KSR*, 550 U.S. at 416 (when a patent claims a structure already known in the prior art that is altered by mere substitution of one element for another known in the field, the result is likely to be obvious if the combination does no more than yield predictable results).

Patent Owner asserts that the proposed combination of Kuesters and Havemann would not have rendered claim 3 obvious because Havemann does not cure Kuesters’s deficiencies alleged by Patent Owner with respect to claim 1. PO Resp. 44–46 & nn.14–15. We are not persuaded by Patent Owner’s argument for the reasons discussed above with respect to claim 1.

Upon considering the complete record, we determine that Petitioner has demonstrated, by a preponderance of evidence, that the subject matter of claim 3 would have been obvious under 35 U.S.C. § 103(a) based on the combination of Kuesters and Havemann.

E. Obviousness Based on the Combination of Kuesters and Heath

Petitioner contends that, to the extent the etch stop material disclosed in Kuesters is deemed to be not adjacent to the insulating spacer, claims 1, 2, and 4–7 are unpatentable under 35 U.S.C. § 103(a) over the combination of Kuesters and Heath (Ex. 1007). Pet. 54–59.

1. Overview of Heath

Heath describes a process for forming a self-aligned contact window in a semiconductor device, such as an integrated circuit. Ex. 1007, Abstract. Heath describes a two-step etching process which comprises the steps of first etching a dielectric layer down to a silicon nitride etch stop layer, and then etching the etch stop, leaving a “stick” of the etch stop material on the vertical sidewall of the layer to be protected. *Id.* Figure 8B of Heath is reproduced below.

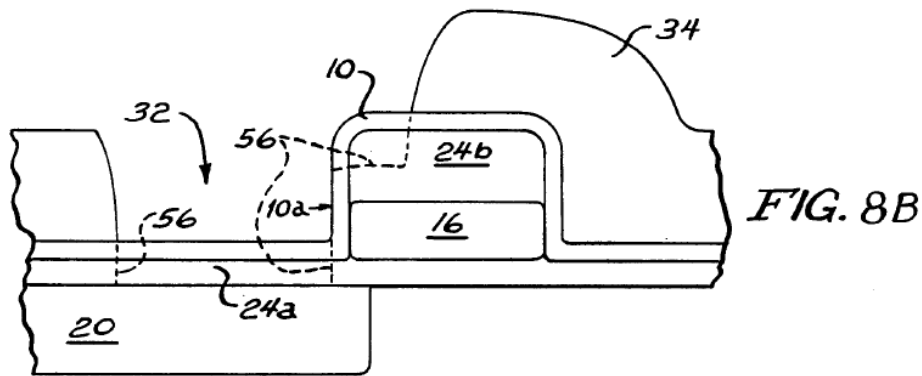


Figure 8B depicts a cross-sectional view of a semiconductor structure after the first etching step, including gate electrode 16 insulated from contact window 32 and source or drain 20 by silicon nitride layer 10. *See id.* at col. 9, ll. 50–67. In the second etching step, etch stop layer 10 is removed to open contact window 32 to source or drain 20. Heath describes that, because the nitride removal is anisotropic, vertical “stick” 10a of nitride layer 10 will remain on the side of gate electrode 16 so that no electrical short occurs between the gate electrode and the contact window or the source or drain region. *Id.* at col. 10, ll. 1–11.

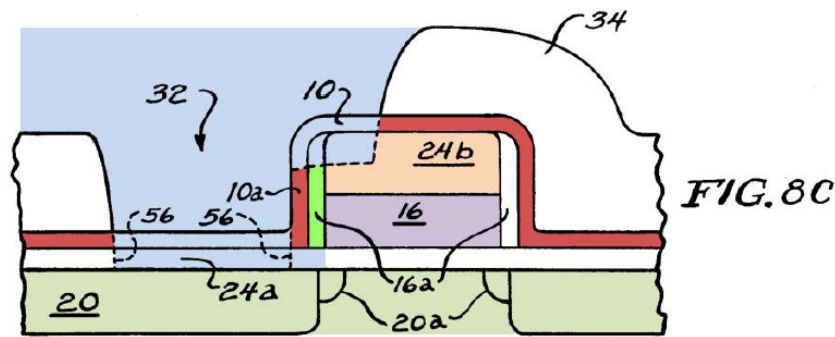
2. Discussion

As discussed above in the context of Petitioner's ground of challenge based on anticipation by Kuesters, Kuesters describes depositing a triple layer of thin oxide/nitride/oxide over the insulating oxide and the oxide spacer. According to Petitioner, the thin oxide beneath the nitride layer is a liner layer that protects the substrate in the contact area from the nitride etch stop material (Pet. 17) presumably to protect the source/drain region created or to be created on the silicon substrate from contamination (*see id.* at 46–47). Petitioner asserts that, when the contact hole is created by a wet etch of the top oxide followed by an anisotropic dry etch of the nitride/oxide layer, the remaining thin oxide on the oxide spacer after the nitride is etched away becomes part of the insulating oxide spacer in the contact area. *Id.* at 17–19, 37–38. Petitioner argues that this thin oxide remaining on the original oxide spacer becomes part of the insulating spacer in the contact region because the thin oxide is made of the same material as the oxide spacer. *Id.* at 17. Petitioner further asserts that the thin oxide and the oxide spacer are indistinguishable in the SEM image shown in Figure 4a. *Id.* at 17, 38 (citing Ex. 1003 ¶ 86).

Petitioner asserts that, to the extent the nitride etch stop layer of Kuesters is deemed not adjacent to the oxide insulating spacer due to the intervening thin oxide layer, the combination of Kuesters and Heath teaches this limitation. Pet. 56. In other words, in this asserted ground of obviousness over Kuesters and Heath, Petitioner relies on the teachings of Heath only for the limitation reciting “(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer.” For all other

limitations of claims 1, 2, and 4–7, Petitioner asserts that Kuesters teaches the limitations for the same reasons discussed above in the context of Petitioner’s challenge based on anticipation by Kuesters. *Id.* at 54–58.

Petitioner provides an annotated version of Figure 8C of Heath shown below.



SAMSUNG-1007, Heath at Figure 8C (with annotations)

Annotated Figure 8C in Petition

Id. at 57. Annotated Figure 8C above depicts a cross-sectional view of a semiconductor structure at the same stage of processing as Figure 8B, combined with the addition of a sidewall spacer 16a, preferably formed of oxide. Ex. 1007, col. 10, ll. 14–19, 23–24. Referencing Annotated Figure 8C, Petitioner asserts that light green denotes the substrate, purple denotes the conductive layer, orange denotes the first insulating layer, blue denotes the contact region, bright green denotes the insulating spacer, and red denotes the etch stop material. Pet. 57. As shown in Figure 8C, vertical “stick” 10a of etch stop nitride layer 10 is adjacent to insulating spacer 16a made of oxide. See *id.* at 56–58.

Petitioner asserts that Heath differs from Kuesters in that Heath uses the previously deposited oxide layer 24a to protect the silicon substrate at

the bottom of the contact hole from the silicon nitride etch stop material without the need for an additional oxide liner layer. *Id.* at 57. Hence, according to Petitioner, applying Heath's teaching to Kuesters would result in the same structure as otherwise disclosed in Kuesters, but without the oxide liner layer beneath the etch-stop material. *Id.* Petitioner argues, therefore, the proposed combination of Kuesters and Heath teaches each limitation of claim 1, including the limitation reciting "(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer." *Id.* at 57–58.

Regarding the rationale to combine Kuesters with Heath, Petitioner asserts, citing the testimony of Dr. Fair, that both Kuesters and Heath are in the same field and use similar methods to create similar structures and to solve the same problem, i.e., fabricating dRAM cells with improved self-aligned contacts. *Id.* at 29 (citing Ex. 1005, 3, Fig. 2; Ex. 1007, Abstract, col. 6, ll. 35–36, Fig. 8C; Ex. 1003 ¶ 118). Petitioner argues that the structures of Kuesters and Heath are essentially identical except that Heath differs from Kuesters in that Heath uses the previously deposited oxide layer 24a to protect the silicon substrate at the bottom of the contact hole from the silicon nitride etch stop material without the need for an additional oxide liner layer used in Kuesters. *Id.* at 30. Petitioner argues, therefore, a person of ordinary skill in the art would have been motivated to apply the known technique of omitting an additional thin oxide liner layer when using a silicon nitride etch stop taught in Heath to improve the similar device disclosed in Kuesters and eliminate the additional thin oxide liner layer used in conjunction with the etch stop material in Kuesters. *Id.* at 29–30 (citing

Ex. 1005, 3, Figs. 2, 4a; Ex. 1007, col. 6, ll. 35–36, Fig. 8C; Ex. 1003 ¶¶ 119–120). Petitioner further argues that Heath teaches explicitly that the proposed combination is compatible. *Id.* at 30 (citing Ex. 1007, col. 5, ll. 3–6, col. 9, ll. 52–55).

Upon reviewing Petitioner’s argument and evidence, we are persuaded that the proposed combination of Kuesters and Heath teaches the limitation reciting “(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer.” We are persuaded that, as shown in Figure 8C, Heath teaches doing away with an additional thin oxide liner layer underneath the nitride layer and protecting the silicon substrate at the bottom of the contact hole using a previously deposited oxide layer 24a. *See* Ex. 1007, col. 9, ll. 52–54 (“Oxide layer 24 covers the active area 20 and the top of gate electrode 16. It is relatively thin over the source/drain 20 as shown at 24a.”).

We also agree with Petitioner that Kuesters and Heath are in the same field and use similar methods to create similar structures and to solve the same problem. As Dr. Fair explains, both Kuesters and Heath describe fabricating dRAM cells with improved self-aligned contacts. Ex. 1003 ¶ 118 (citing Ex. 1005, 3, Figs. 2, 4a; Ex. 1007, Abstract, col. 6, ll. 35–36, Fig. 8C). As discussed above, the ’552 patent is also directed to making high quality contacts in semiconductor devices, such as “self-aligned” contacts. Ex. 1001, Abstract, col. 7, ll. 19–22, col. 8, ll. 4–6. Hence, we are persuaded that a person of ordinary skill in the art would have been motivated to look to the teachings of Heath when considering advantages and disadvantages of alternative methods of making contact openings in a

multi-layer structure of a semiconductor device, such as the “self-aligned” contacts described in the ’552 patent and Kuesters. *See KSR*, 550 U.S. at 420.

We are also persuaded, as shown in Figure 2 of Kuesters and Figure 8C of Heath and their accompanying text, the structures of Kuesters and Heath are similar except that the references employ different methods to protect the silicon substrate in the contact area in the process of fabricating the disclosed semiconductor structures. Hence, we credit Dr. Fair’s testimony and are persuaded that a person of ordinary skill in the art would have been motivated to apply the teachings of Heath to Kuesters to substitute Kuesters’s protection method with the method of Heath and eliminate the extra oxide layer used in Kuesters. Ex. 1003 ¶ 119. As Petitioner and Dr. Fair explain (Pet. 30; Ex. 1003 ¶ 119), Heath expressly contemplates alternative embodiments using Kuesters’s extra oxide layer. For example, Heath teaches as follows:

The process should also tolerate, on the other hand, *the addition of any amount of oxide to the sidewall* for any purpose such as isolation from a later established inter connect or other element, or the addition of any material to the sidewall for the purpose of providing a spacer to fabricate optimized VLSI transistor structures.

Ex. 1007, col. 5, ll. 2–8 (emphasis added). Thus, we agree with Petitioner that it would have been obvious to combine the teachings of Heath with Kuesters to modify the same or similar structures with a known technique with predictable results. Pet. 57; *see also KSR*, 550 U.S. at 416 (“The

combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”).

Based on the complete record, we credit the testimony of Dr. Fair and are persuaded that it would have been obvious to a person of ordinary skill in the art to combine Kuesters and Heath to teach or render obvious all limitations of claim 1, including the limitation reciting “(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer.”

Patent Owner asserts that the combination of Kuesters and Heath does render claim 1 obvious because Heath purportedly teaches that there is no need for a sidewall insulating spacer because insulation of the conductive contact is “derived from the *stick* layer of etch stop material.” PO Resp. 41.

In its Reply, Petitioner responds that Patent Owner’s argument is misguided because Petitioner’s proposed combination does not rely on Heath for its teaching of a sidewall spacer, but, rather uses Kuesters’s sidewall spacer and relies on Heath for its teaching of a way to eliminate the extra oxide liner of Kuesters. Pet. Reply 4. Petitioner further argues that even if insulation of the conductive contact is achieved by a stick of etch stop material in Heath, it does not negate Heath’s teaching and embodiments using a sidewall spacer.

We agree with Petitioner’s argument and find Patent Owner’s argument unpersuasive because Patent Owner does not address the specific combination proposed by Petitioner, i.e., using Kuesters’s sidewall spacer and relying on Heath for its teaching of a way to eliminate the extra oxide liner of Kuesters. Further, to the extent Patent Owner argues Heath teaches

away from the proposed combination, Patent Owner's argument is unpersuasive because "the 'mere disclosure of more than one alternative' does not amount to teaching away from one of the alternatives where the reference does not 'criticize, discredit, or otherwise discourage the solution claimed.'" *SightSound Techs., LLC v. Apple Inc.*, 809 F.3d 1307, 1320 (Fed. Cir. 2015) (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)).

Patent Owner further asserts that the combination of Kuesters and Heath does not render the challenged claims obvious because Heath does not cure Kuesters's deficiencies alleged by Patent Owner with respect to the ground based on anticipation by Kuesters. PO Resp. 42–43. We are not persuaded by Patent Owner's argument for the same reasons discussed above in our analysis of the ground based on anticipation by Kuesters.

As discussed above, in this asserted ground of obviousness over Kuesters and Heath, Petitioner relies on the teachings of Heath only for the limitation reciting "(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer." For all other limitations of claims 1, 2, and 4–7, Petitioner persuasively relies on Kuesters to teach the limitations for the same reasons discussed above in the context of Petitioner's challenge based on anticipation by Kuesters.

Patent Owner does not respond separately, with specificity, to Petitioner's challenge to dependent claims 2 and 4–7 beyond Patent Owner's arguments advanced with respect to claim 1 discussed above. See PO Resp. 43.

Accordingly, upon considering the complete record, we determine that Petitioner has demonstrated, by a preponderance of evidence, that the

subject matter of claims 1, 2, and 4–7 would have been obvious under 35 U.S.C. § 103(a) based on the combination of Kuesters and Heath.

*F. Obviousness Based on the Combination of
Kuesters, Heath, and Havemann*

Claim 3 depends from claim 1, and, in an asserted ground of obviousness as to claim 3, Petitioner adds the teachings of Havemann to the basic combination of Kuesters and Heath to teach the additionally recited limitation of claim 3. Pet. 60. Citing the testimony of Dr. Fair, Petitioner argues that the reasons for combining Kuesters with Heath or Havemann individually discussed above are equally applicable to the three-way combination of Kuesters, Heath, and Havemann. *Id.* at 30–31 (citing Ex. 1003 ¶¶ 121–123).

Similar to Patent Owner’s response to the grounds based on the combination of Kuesters and Heath or Kuesters and Havemann, Patent Owner asserts that the combination of Kuesters, Heath, and Havemann does not render claim 3 obvious because neither Heath nor Havemann cures the deficiencies in Kuesters alleged by Patent Owner with respect to the ground based on anticipation by Kuesters. PO Resp. 44–46 & nn.14–15. We are similarly unpersuaded by Patent Owner’s argument for the same reasons discussed above in our analysis of the ground based on anticipation by Kuesters.

Upon considering the complete record, we determine that Petitioner has demonstrated, by a preponderance of evidence, that the subject matter of

claim 3 would have been obvious under 35 U.S.C. § 103(a) based on the combination of Kuesters, Heath, and Havemann.

V. CONCLUSION

Petitioner has met its burden of proof, by a preponderance of the evidence, in showing that the claims of the '552 patent are unpatentable based on the following grounds:

1. Claims 1, 2, and 4–12 as anticipated under 35 U.S.C. § 102(b) by Kuesters;
2. Claim 3 as obvious under 35 U.S.C. § 103(a) over the combination of Kuesters and Havemann;
3. Claims 1, 2, and 4–7 as obvious under 35 U.S.C. § 103(a) over the combination of Kuesters and Heath; and
4. Claim 3 as obvious under 35 U.S.C. § 103(a) over the combination of Kuesters, Heath, and Havemann.

VI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–12 of the '552 patent are *unpatentable*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 6,784,552 B2

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