

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., HTC CORPORATION, and HTC AMERICA, INC.,
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,
Patent Owner.

Case IPR2016-00924¹
Patent 5,960,464

Before MICHAEL R. ZECHER, JAMES B. ARPIN, and
MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Case IPR2016-00848 has been joined with this proceeding.

I. INTRODUCTION

Apple Incorporated (“Petitioner”), filed a Petition requesting an *inter partes* review of claims 1–4, 7–13, 16–24, 32–36, and 40 of U.S. Patent No. 5,960,464 (Ex. 1001, “the ’464 patent”). Paper 2 (“Pet.”). Petitioner also filed a Motion for Joinder with *Samsung Electronics Co. v. Parthenon Unified Memory Architecture LLC*, Case IPR2015-01946. Paper 3 (dismissed without prejudice after Case IPR2015-01946 was terminated). Parthenon Unified Memory Architecture Limited Liability Corporation (“Patent Owner”), waived its right to file a Preliminary Response. Paper 8. On August 23, 2016, we instituted an *inter partes* review of claims 1–4, 7–13, 16–24, 32–36, and 40 (“the instituted claims”) of the ’464 patent on certain grounds of unpatentability alleged in the Petition. Paper 10 (“Dec. to Inst.” or “Inst. Dec.”). Also, on the same day, we instituted an *inter partes* review of the same claims of the ’464 patent in *HTC Corporation v. Parthenon Unified Memory Architecture LLC*, Case IPR2016-00848, and joined that proceeding with this proceeding. Paper 12.

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 22, “PO Resp.”), to which Petitioner filed a Reply (Paper 27, “Pet. Reply”).

We held a consolidated hearing on May 18, 2017, for this case and related Case IPR2016-0923, and a transcript of the hearing is included in the record. Paper 38 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner has shown, by a

preponderance of the evidence, that the challenged claims of the '464 patent, upon which we instituted review, are unpatentable.

A. Related Proceedings

The '464 patent is involved in the following district court cases:

(1) *Parthenon Unified Memory Architecture LLC v. Huawei Technologies Co.*, No. 2:14-cv-00687-JRG-RSP (E.D. Tex.); (2) *Parthenon Unified Memory Architecture LLC v. Motorola Mobility, Inc.*, No. 2:14-cv-00689-JRG-RSP (E.D. Tex.); (3) *Parthenon Unified Memory Architecture LLC v. HTC Corp.*, No. 2:14-cv-00690-RSP (E.D. Tex.); (4) *Parthenon Unified Memory Architecture LLC v. LG Electronics, Inc.*, No. 2:14-cv-00691-JRG-RSP (E.D. Tex.); (5) *Parthenon Unified Memory Architecture LLC v. Samsung Electronics Co.*, No. 2:14-cv-00902-JRG-RSP (E.D. Tex.); (6) *Parthenon Unified Memory Architecture LLC v. Qualcomm Inc.*, No. 2:14-cv-00930-JRG-RSP (E.D. Tex.); (7) *Parthenon Unified Memory Architecture LLC v. ZTE Corp.*, No. 2:15-cv-00225-JRG-RSP (E.D. Tex.); and (8) *Parthenon Unified Memory Architecture LLC v. Apple Inc.*, No. 2:15-cv-00621-JRG-RSP (E.D. Tex.). Pet. 1–2;² Paper 7, 2. Petitioner also filed another petition challenging the patentability of a certain subset of claims in related U.S. Patent No. 5,812,789 (Case IPR2016-00923).

² The Petition and supporting evidence filed by HTC in Case IPR2016-00848 are essentially the same as the Petition and supporting evidence filed by Apple in Case IPR2016-00924. For clarity and ease of citation, all references to the Petition and supporting evidence throughout this Final Written Decision are to the Petition and supporting evidence filed by Apple in Case IPR2016-00924.

B. The '464 patent

The '464 patent, entitled “Memory Sharing Architecture for a Decoding in a Computer System,” issued September 28, 1998, from U.S. Patent Application No. 08/701,890, filed on August 23, 1996. Ex. 1001 at [54], [45], [21], [22]. Because the application that led to the '464 patent was filed August 23, 1996, the '464 patent expired on August 23, 2016.

The '464 patent generally relates to “a memory management system that can be used with applications requiring a large contiguous block of memory, such as video decompression techniques (e.g., [Motion Picture Expert Group 2 (MPEG 2)] decoding).” *Id.* at Abstract. Existing MPEG 2 decompression chip sets could be expensive because they required two megabytes of dynamic random-access memory. *Id.* at 2:18–24. As a result, it was desirable to employ the main memory of the computer. *Id.* However, because typical operating systems allocate memory in four-kilobyte blocks, it was difficult to obtain two megabytes of contiguous memory. *Id.* at 2:51–63. To address these and other problems, the disclosed memory management module requests and employs approximately 500 four-kilobyte pages of the main memory, some of which are in noncontiguous blocks of pages, to construct a single, contiguous two-megabyte block of memory. *Id.* at 3:8–15.

Figure 2 of the '464 patent is reproduced below.

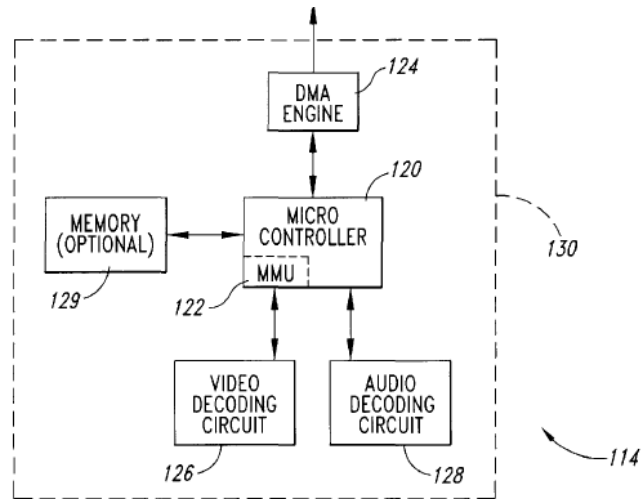


Fig. 2

Figure 2 is a block diagram of MPEG 2 decoder 114. *Id.* at 4:1–2, 4:42–43. MPEG 2 decoder 114 includes direct memory access (DMA) engine 124, video decoding circuit 126, and audio decoding circuit 128, each of which is conventional. *Id.* at 4:51–54, 5:3–7. MPEG 2 decoder 114 further includes microcontroller 120, which, in turn, includes memory management unit (MMU) 122. *Id.* at 4:43–46. Microcontroller 120 directly accesses main memory 106 through DMA engine 124. *Id.* at 4:46–54. Microcontroller 120 performs memory sharing routine 200 (illustrated in the flowchart of Figure 4) to request a two megabyte portion of main memory 106 (not illustrated in Figure 2 above). *Id.* at 6:63–66. If two megabytes of contiguous memory is not available, microcontroller 120 can request two, one-megabyte blocks. *Id.* at 7:16–27. If two, one-megabyte blocks of contiguous memory are not available, microcontroller 120 can request four 500-kilobyte blocks. *Id.* In a worst-case scenario, microcontroller 120 can request 500 four-kilobyte blocks of memory. *Id.* at 7:56–63. “[M]icrocontroller 120 programs or creates a lookup table to translate or map the 500 pages to a contiguous string of memory locations beginning at a set address and increasing

contiguously therefrom to an address 2 megabytes later” (*id.* at 7:46–50) using conventional lookup table techniques (*id.* at 8:30–35).

C. Illustrative Claim

Of the challenged claims, claims 1, 10, 19, and 32 are independent. Claims 2–4 and 7–9 depend from independent claim 1. Claims 11–13 and 16–18 depend from independent claim 10; claims 20–24 depend from independent claim 19; and claims 33–36 and 40 depend from independent claim 32. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

1. In a computer system having a main memory, a storage device having encoded data stored therein and a processor controlled by an operating system, an electronic device comprising:

a decoding circuit coupled to receive and decode the encoded data from the storage device; and

a control circuit coupled to the decoding circuit, the processor and the main memory, the control circuit being configured to request continuous use of several portions of the main memory from the operating system, the portions of the main memory having noncontiguous addresses, and being configured to translate the noncontiguous addresses to contiguous addresses of a block of memory, and

wherein the decoding circuit is configured to request at least some of the contiguous addresses of the block of memory, and wherein the control circuit translates the requested contiguous addresses of the block of memory to requested noncontiguous addresses and permits the decoding circuit to access the portions of the main memory.

Ex. 1001, 9:60–10:13.

D. Prior Art Relied Upon

Petitioner relies upon the following prior art references:

Selliah Rathnam & Gert Slavenburg, *An Architectural Overview of the Programmable Multimedia Processor, TM-1*, 1996 IEEE PROC. COMPCON '96, at 319 (Ex. 1005, "Rathnam").

Gordon E. Moore, *Cramming More Components onto Integrated Circuits*, 38 ELECTRONICS 114 (1965) (Ex. 1035, "Moore").

Notarianni³ US 5,404,511 Apr. 4, 1995 Ex. 1031
(Filed June 26, 1992)

Pet. 3–4. Petitioner also relies upon the Declaration of Harold S. Stone, Ph.D. ("Stone Decl.") (Ex. 1030) and the Reply Declaration of Harold S. Stone, Ph.D. ("Stone Reply Decl.") (Ex. 1044). Patent Owner relies upon the Declaration of Mitchell A. Thornton, Ph.D., P.E. (Ex. 2003).

E. The Instituted Grounds of Unpatentability

We instituted *inter partes* review of the challenged claims of the '464 patent based upon the following grounds (Dec. to Inst. 18):

Reference(s)	Basis	Claim(s) challenged
Notarianni	§ 102(b)	1, 3, 4, 8–10, 12, 13, 16–21, 23, 24, 32, 33, 35, 36, and 40
Notarianni	§ 103(a)	7 and 22
Notarianni and Moore	§ 103(a)	2 and 11
Notarianni and Rathnam	§ 103(a)	34

³ We understand references to "Notorianni" in the Petition to be typographical mistakes. See Ex. 1031 at [75].

II. ANALYSIS

A. Claim Construction

Petitioner alleged that the '464 patent would expire in August 2016. Pet. 9–10. Patent Owner does not dispute the allegation. *See generally* PO Resp. *passim*. We agree that the '464 patent has expired.

As a result, we construe the claims in accordance with the principles followed in district court. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc); *Toyota Motor Corp. v. Cellport Sys., Inc.*, Case IPR2015-00633, slip op. at 8–10 (PTAB Aug. 14, 2015) (Paper 11); *cf. In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (“While claims are generally given their broadest possible scope during prosecution, the Board’s review of the claims of an expired patent is similar to that of a district court’s review.”) (internal citation omitted). Moreover, Petitioner argues that its proposed construction will remain the same even if we apply the district court claim construction principles, such as those set forth in *Phillips*. Pet. 10.

In our Decision on Institution, we construed “translate” to mean “convert,” and we construed “algorithmically translate the noncontiguous addresses to the contiguous addresses” to mean “convert using at least one mathematical operation.” Inst. Dec. 9–10. Patent Owner does not dispute our determinations or propose additional terms for construction. *See* Paper 11, 3 (“The patent owner is cautioned that any arguments for patentability not raised in the response will be deemed waived.”). Petitioner does not address our determinations in this regard in its Reply. *See* 37 C.F.R. § 42.23(b) (“A reply may only respond to arguments raised in the

corresponding . . . patent owner response.”). Based on the record developed during this proceeding, we continue to apply these constructions.

To the extent it is necessary, we discuss below certain other claims terms in the context of analyzing whether the prior art renders the challenged claims unpatentable.

B. Anticipation by Notarianni

Petitioner contends that claims 1, 3, 4, 8–10, 12, 13, 16–21, 23, 24, 32, 33, 35, 36, and 40 of the ’464 patent are anticipated under § 102(b) by Notarianni. Pet. 11–25. Petitioner explains how Notarianni describes the subject matter of each challenged claim (*id.*), and relies upon the Declarations of Dr. Stone (Ex. 1030 ¶¶ 47–67; Ex. 1044 ¶¶ 2–17) to support its contentions. In its Patent Owner Response, Patent Owner presents four arguments with respect to independent claim 1, one argument with respect to dependent claims 3, 4, 20, and 21, and one argument with respect to dependent claim 16. PO Resp. 6–35. Patent Owner relies upon the Declaration of Dr. Thornton, to support its positions. Ex. 2003 ¶¶ 37–77.

We begin our analysis with the principles of law that generally apply to a ground based on anticipation, followed by a brief overview of Notarianni, and we then address the parties’ contentions.

1. Principles of Law

To establish anticipation, “all of the elements and limitations of the claim must be shown in a single prior reference, arranged as in the claim.” *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). When evaluating a single prior art reference in the context of anticipation, the reference must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475,

1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). “[T]he dispositive question regarding anticipation [, therefore, i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference’s] teaching’ that every claim element was disclosed in that single reference.” *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) (alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991)). We analyze this asserted ground based on anticipation with the principles stated above in mind.

2. Notarianni Overview

Notarianni generally relates to a fragmented memory manager module to alleviate the problem of memory fragmentation when reading image and audio files from a compact disc read-only memory (“CD-ROM”) disc and decoding them in real-time. Ex. 1031, Title, Abstract. According to Notarianni,

[t]his fragmentation might mean, for example, that a request for the allocation of 60 kilobytes of buffer space cannot be satisfied because there is no single unallocated block larger than 50 kilobytes. At the same time, adding up all the small fragments, there may in fact be hundreds of kilobytes of unallocated memory.

Id. at 1:49–55. “By managing the memory . . . as a set of many small fragments, any small fragment can be [utilized] to contribute to any allocation of buffer space, large or small (minimum size: one fragment).”

Id. at 2:11–14. “[T]he allocated buffer may be the sum of many fragments dispersed randomly throughout the physical memory space.” *Id.* at 2:15–17. “[T]he total of available buffer space in the memory is divided into a plurality of fragments, each fragment containing a relatively small

“[T]he formatting of memory into a linked list of small fragments allows the use of all available memory for real-time buffers, even if such memory is severely fragmented and dispersed at random throughout the physical memory space.” *Id.* at 9:67–10:3. In other embodiments, “the augmented [Play Control Lists] of the fragmented memory could even be gathered together in physical memory.” *Id.* at 11:10–13. At the outset, the FRAGM secures an allocation of buffer space sufficient for all requirements of the application module, and partitions the allocation into small units of buffer space (fragments), which are linked into a list by respective list pointers. *Id.* at Abstract. Any subsequent requirement for buffer space is met by the FRAGM, by un-linking the requisite number of fragments from the list of unallocated fragments. *Id.*

3. Level of Skill in the Art

There is evidence in the record before us that enables us to determine the knowledge level of a person of ordinary skill in the art. Relying on the testimony of its declarant, Dr. Stone, Petitioner asserts that a person of ordinary skill in the art at the time of the invention of the '464 patent would be an individual who possesses (1) an accredited Bachelor's degree in electrical engineering, computer science, or computer engineering; and (2) at least three years of experience in the fields of data compression and overall computer system architecture. Pet. 10 (citing Ex. 1030 ¶¶ 46–46). Patent Owner's declarant, Dr. Thornton, testifies that a person of ordinary skill in the art at the time of the invention of the '789 patent would be an individual who possesses (1) an accredited Bachelor's degree in electrical engineering, computer engineering, *or an equivalent degree*; and (2) at least two to three years of experience in signal/image processing and computer architecture at

both the systems and micro-architecture levels. Ex. 2003 ¶ 27.

Dr. Thornton further testifies that, in lieu of the two to three years of experience, a person of ordinary skill in the art at the time of the invention of the '464 patent may hold a Master's or other graduate degree in electrical or computer engineering with a focus in computer architecture and signal/image processing, along with one year of relevant experience. *Id.*

Putting aside the subtle distinctions in the assessments of the level of skill in the art put forth by both declarants, Dr. Thornton testifies that, if he were to apply Dr. Stone's assessment of the level of skill in the art, his "analysis and conclusions would remain unchanged." Ex. 2003 ¶ 28. Because Dr. Stone's assessment of the level of skill in the art is consistent with the '464 patent and the asserted prior art, we adopt it and apply it to our evaluation below, but note that our conclusions would remain the same under Dr. Thornton's assessment.

4. Claim 1

Petitioner relies upon Notarianni's video decoder and adaptive pulse code modulation decoder to describe the "decoding circuit" recited in independent claim 1, and relies upon Notarianni's access controller to describe the "control circuit" recited in independent claim 1. Pet. 11–14.

With respect to the control circuit "being configured to request continuous use of several portions of the main memory from the operating system, the portions of the main memory having noncontiguous addresses," Petitioner relies upon Notarianni's disclosure that "memory manager module 210 of CDRTOS allows the application module 202 to reserve blocks of memory in a desired plane of the memory 200, which can be used as buffers storing the video/audio data for a given play operation." *Id.* at 12 (citing

Ex. 1031, 4:3–41; Ex. 1030 ¶ 47). With respect to the control circuit “being configured to translate the noncontiguous addresses to contiguous addresses of a block of memory,” Petitioner argues that Notarianni’s FRAGM 212 “finds small, non-contiguous fragments of the memory and creates a list of links to the small memory locations,” and that “[t]he linked listing is then a contiguous block of memory.” *Id.* at 12–13.

With respect to the decoding circuit being “configured to request at least some of the contiguous addresses of the block of memory,” Petitioner relies upon Notarianni’s disclosure of an “application module” that is designed “to cause the decoders 206 to read [audio, video, and program data from the disc] for the generation of desired audio and video presentations.” *Id.* at 13 (emphasis omitted) (quoting Ex. 1031, 4:19–24).

With respect to the control circuit “translat[ing] the requested contiguous addresses of the block of memory to requested noncontiguous addresses and permits the decoding circuit to access the portions of the main memory,” Petitioner argues that Notarianni’s FRAGM 212 translates the requests from decoders 206 to the noncontiguous addresses of the various memory fragments. *Id.* at 13–14 (citing Ex. 1031, 6:49–51, 6:67–7:17, Figs. 6, 7).

In its Patent Owner Response, Patent Owner responds that Notarianni does not anticipate claim 1 for the following four reasons: (1) Notarianni does not disclose a control circuit configured to request “continuous use” of several portions of main memory (PO Resp. 6–12); (2) Notarianni does not disclose a control circuit that “translates the requested contiguous address . . . to requested noncontiguous address” (*id.* at 12–26); (3) Petitioner relies upon three separate components of Notarianni as the “control circuit”

because it does not disclose a “control circuit” (*id.* at 26–31); and (4) Notarianni does not disclose a “decoding circuit” that is “configured to request at least some of the contiguous addresses of the block of memory” (*id.* at 31–34). We address each argument in turn.

a. Continuous use

Independent claim 1 recites, in relevant part, “the control circuit being configured to request continuous use of several portions of the main memory from the operating system.”

Patent Owner argues that requesting “continuous use” requires static allocation of memory (i.e., an “allocation of the memory to be used solely by an application over the timespan of that application’s execution”). PO Resp. 9. According to Patent Owner, “[i]n contrast to the static allocation of memory for ‘continuous use’ as recited by the claims of the ’464 Patent, in Notarianni free memory is dynamically allocated during the operation of the disclosed system.” *Id.* at 10 (emphasis omitted) (citing, *inter alia*, Ex. 1031, 1:5–6). Specifically, Patent Owner contends that “Notarianni supports dynamic usage of free memory by allowing manipulation of the list where such manipulation includes inserting and deleting entries corresponding to available blocks of free memory and whereby such manipulation occurs during the execution of the application.” *Id.* at 11 (citing Ex. 1031, 5:35–37; Ex. 2003 ¶ 44). Thus, concludes Patent Owner, “instead of ‘locking down’ memory for ‘continuous use’ as recited in the claims, Notarianni discloses dynamic and on-demand allocation of free memory.” *Id.* at 11 (citing Ex. 1031, 1:60–64, 2:3–10, 5:35–37, 6:15–18, 6:29–34, 7:52–8:11, 9:11–40, 10:14–22; Ex. 2003 ¶ 45).

Petitioner counters that Patent Owner’s attempt to import “static allocation” into the claims requiring “continuous use” is improper because “[t]he claims do not recite any language requiring that all of the memory be allocated in a particular way (i.e., static v. dynamic),” “at a particular time (i.e., at initiation v. while processing)” or “using a particular technique (i.e., locked down v. some other memory reservation technique).” Pet. Reply 4–6. We agree. The ’464 patent does not define “continuous use.” Outside of the claims, that phrase is used twice throughout the specification of the ’464 patent, only in the “Summary of the Invention” section, and neither use amounts to a definition. Moreover, Patent Owner does not propose a construction of the term explicitly. As a result, upon reviewing the claims and specification of the ’464 patent, we agree with Petitioner that the phrase “continuous use” does not require static allocation.

Even assuming that “continuous use” requires “memory to be used solely by an application over the timespan of that application’s execution,” as Patent Owner contends (PO Resp. 9), we are persuaded by Petitioner’s argument that Notarianni discloses such use. Pet. Reply 2–3, 6–7 (“Notarianni’s memory allocation has the same effect and works in the same manner as the ‘static’ allocation in the ’464 patent.”). Specifically, Petitioner argues that Notarianni discloses a “[FRAGM that] secures *at the outset* an allocation of buffer space sufficient for all requirements of the application module.” Pet. Reply 2 (quoting Ex. 1031, Abstract (emphasis added)). Notarianni, “first finds at 702 the *maximum amount* of memory it will require in each plane” (Ex. 1031, 7:8–10 (emphasis added)) and passes that maximum amount “as a parameter to FRAGM . . . in a call to the function FRAG_INIT” (*id.* at 7:12–16), which in turn “requests CDRTOS

memory manager 210 to allocate *at once* the memory space required MAXN fragments” (*id.* at 7:18–25 (emphasis added)). Pet. Reply 2–3. According to Petitioner,

Patent Owner’s expert admits that the FRAGM module in Notarianni requests all of the memory . . . that may be used for decoding at the beginning of the decoding process, and that the memory remains ‘locked down’ for the duration of decoding, resulting in a ‘static’ allocation of memory under the expert’s own definition. *See* Ex. 1043 at 60:16-61:9, 62:5-18, 64:18-65:4, 65:23-66:5

Pet. Reply 6–7. We have reviewed this testimony and agree that it supports Petitioner’s characterization. In particular, we find persuasive the following exchange between Petitioner’s counsel and Patent Owner’s declarant:

Q. . . . It’s fair to say that between the allocation step 804 and the completion of FRAG_SHUTDOWN in step 860, the memory remains locked down for use by the application module?

A. Yes.

Ex. 1043, 65:25–66:5.

With respect to Patent Owner’s reliance on Notarianni’s reference to “dynamic allocation of buffer space” (Ex. 1031, 1:5–6), Petitioner argues that this disclosure “references the use of the memory by Notarianni’s decoder, not the allocation of the memory at the beginning of an application process. . . .” Pet. Reply 7. According to Petitioner, the “use” is not relevant to the limitation because it is the allocation that matters, and “the point at which all of the memory is requested by FRAGM prior to decoding is step 804.” *Id.* at 7–8. We agree.

For the foregoing reasons, we are persuaded that Notarianni discloses the “continuous use” limitation of the independent claims.

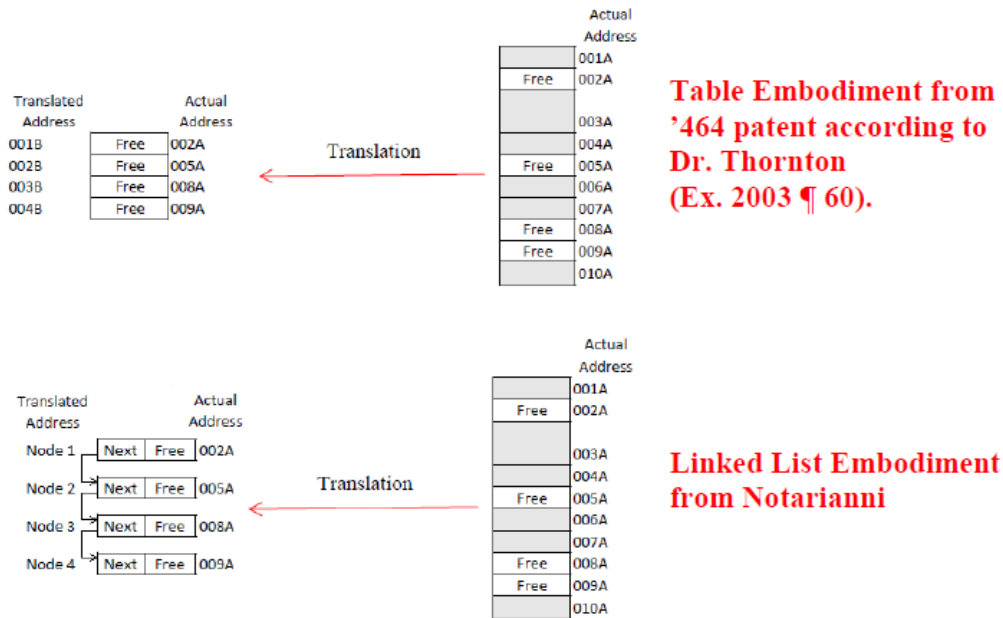
b. Translation

Independent claim 1 recites, in relevant part, “translat[ing] the noncontiguous addresses to contiguous addresses of a block of memory.”

Patent Owner argues that Notarianni does not disclose a circuit configured to “translate”—or “convert,” as we have construed “translate” to mean—because “a [person of ordinary skill in the art] would understand that [Notarianni’s] creation of a ‘linked list’ of memory fragments is not the same as ‘translating’ or ‘converting’ the addresses of the memory fragments to create a memory block having contiguous addresses.” PO Resp. 14–18; *see also id.* at 18–21 (analogizing the difference between the ’464 patent and Notarianni to the difference between taking a number upon arrival and a sign-in sheet). In particular, Patent Owner argues that, in Notarianni’s linked list, “there is no translation or conversion to an alias or alternative value wherein those values are sequential or contiguous,” and that “it is the order present in the list that dictates order of service whereby in the alternative method, where aliases or contiguous values are assigned, it is the value of the alias that dictates the order of the service.” *Id.* at 21. According to Patent Owner, Notarianni’s “linked list contains the **non-translated** addresses of the actual fragmented free memory blocks,” and those actual addresses of fragmented free memory blocks are not “translated” or “converted,” but merely sequenced by use “of a pointer linking one fragment address to the next.” *Id.* at 22.

Petitioner counters that “‘translating’ is done in Notarianni by creation of a linked list that maps the noncontiguous memory fragments to nodes of the list.” Pet. Reply 9; *see also id.* (“Notarianni ‘translates’ the noncontiguous memory fragment addresses into contiguous nodes of a

linked list.”) (citing Ex. 1031, 7:23–25 (“allocate at once the memory space required for MAXN fragments”), 7:29–31 (formatting “to create a linked list of empty FRAG structures”), 9:67–10:3 (“[T]he formatting of memory into a linked list of small fragments allows the use of all available memory for real-time buffers, even if such memory is severely fragmented and dispersed at random throughout the physical memory space.”)). Petitioner argues that Notarianni’s linked list “performs the same function of translating noncontiguous addresses to continuous addresses as stated in the claim,” and cites Figure 8 of Notarianni as showing “physically noncontiguous blocks of memory as forming one contiguous memory space F1 through F12.” Pet. Reply 10–11. Petitioner adapts and annotates a figure, reproduced below, from page 24 of Patent Owner’s Response:



Pet. Reply 11. About this figure, Petitioner states

while the table implementation uses an index or table position as the continuous address that holds the translation of a noncontiguous address, the linked list implementation uses the link position (node 1-4) to hold the result of the same translation.

Id. For both implementations, the data structures are later used to translate the contiguous addresses (table index or node position) to the actual addresses of noncontiguous memory blocks. *Id.*

Pet. Reply 11–12.

We agree with Petitioner. In particular, we are persuaded that the node positions in Notarianni’s linked list are “contiguous addresses,” as recited in the claims, because they have a sequence, and that those contiguous addresses are “translated” or “converted” to the noncontiguous addresses of the memory fragments by traversing those nodes from one to the next. We are not persuaded by Patent Owner’s argument that “[a] linked list contains the non-translated addresses” (PO Resp. 22) because the same is true of a lookup table and Petitioner is relying upon the node position, not the address of the memory fragment, as the contiguous address. We also are not persuaded by Patent Owner’s argument that “the fragment addresses are not ‘translated’ or ‘converted’ [because]. . . Notarianni retains and uses the individual fragment addresses in the form of a pointer linking one fragment address to the next” (*id.*) because, again, Petitioner is relying upon the node position in the linked list, not the pointer to the next noncontiguous address, as the contiguous address.

Patent Owner also argues that “step 206 of Figure 4 in the ’464 patent (i.e., ‘. . . the microcontroller 120 programs or creates a lookup table . . .’) is never performed, required or needed in Notarianni.” PO Resp. 22. This argument is not persuasive because it is not commensurate with the claim language, which recites “translate” and is not limited to using a lookup table to “translate.” See Pet. Reply 12–14 (arguing that Patent Owner attempts improperly to import a limitation from an embodiment in the Specification,

and that independent claims 1, 10, and 32 must be broader than dependent claims 6, 15, and 37, each of which recites “a look up table, the look up table [mapping/translating] the noncontiguous addresses to the contiguous addresses.”); *see also In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (explaining that limitations not appearing in the claims cannot be relied upon for patentability).

Patent Owner also argues that “the words ‘translate’ and ‘convert’ or the concept of translation/conversion never appear in Notarianni.” PO Resp. 23. This argument is not persuasive because there is no *ipsissimis verbis* test for determining whether a reference discloses a claim element (i.e., identity of terminology is not required). *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990).

Patent Owner also argues that “Notarianni does not disclose an initial step of translating or converting the non-contiguous addresses to contiguous addresses of a block of memory as recited in independent claims 1, 10, 19, and 32.” PO Resp. 23. This argument is not persuasive because claims 1, 10, and 19 are system, not method, claims, and because claim 32, although a method claim, does not include any language that requires “translating” to be the “initial” step of the claimed method.

Finally, Patent Owner argues that the recited “translation” or “conversion” “effectively require[s] construction of what appears to be a single contiguous block of memory such that the decoder perceives the available non-contiguous smaller memory blocks to be a larger contiguous block of memory through use of the created ‘lookup table’ in the ’464 patent” (PO Resp. 23), that Notarianni does not disclose a lookup table (*id.* at 24), and that its “linked list of actual non-contiguous free memory block

addresses is not equivalent to the lookup table containing translated or mapped memory addresses.” *Id.*; *see also id.* at 24–25 (elaborating on why Notarianni’s linked list does not disclose, and is not equivalent to, a lookup table). This argument is not persuasive because it is not commensurate with the claim language, which recites “translate” and is not limited to using a lookup table. *See Self*, 671 F.2d at 1348. As discussed above, we are persuaded by Petitioner’s argument that Notarianni converts the non-contiguous addresses of memory fragments into contiguous addresses by sequencing them using a linked list. Because the linked list makes the fragments appear contiguous, “the fragmentation becomes effectively transparent to the play control module 208 of CDRTOS.” Ex. 1031, 6:26–37.

c. Control circuit

Independent claim 1 recites, in relevant part, “a control circuit.”

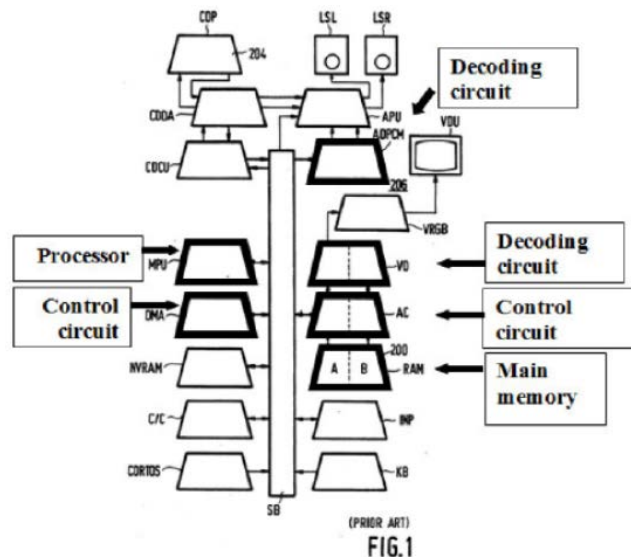
Patent Owner argues Petitioner “relies on three separate components in Notarianni with regard to the recited features of the control circuit.” PO Resp. 26. Patent Owner argues that no single component in Notarianni demonstrates that

(1) it is coupled to the “decoding circuit, the processor and the main memory” (claim 1)/“processor and the main memory” (claims 10 and 19); (2) it is configured to request continuous use of several portions of the main memory from the operating system (claims 1, 10, 19); and (3) it is configured to translate the noncontiguous addresses to contiguous addresses of a block of memory (claims 1, 10, 19).

Id. According to Patent Owner, Petitioner relies on Notarianni’s access controller, application module 202, and FRAGM, but that none of these

components—either individually or together—teach the recited “control circuit.” *Id.* at 26–31 (citing Pet. 12–13).

Petitioner counters that Notarianni’s “access controller executes the FRAGM program, which performs the address translation,” and, therefore, “Notarianni’s access controller and its FRAGM software [together] disclose the control circuit. . . .” Pet. Reply 15. With respect to being coupled to the decoding circuit, processor, and main memory, Petitioner provides the following annotated figure to show how access controller “AC” is coupled to the decoding circuit, processor, and main memory, via system bus SB:



Id. We agree that Notarianni’s AC is coupled to the decoding circuit, processor, and main memory via system bus SB.

With respect to being configured to request continuous use of several portions of main memory, Petitioner counters that “the access controller executes the FRAGM software, which . . . is configured to request continuous use,” and that Patent Owner mischaracterizes the argument presented in the Petition by suggesting that Petitioner relies on application module 202. Pet. Reply 16–17. In the paragraph addressing “continuous

use” in the Petition, Petitioner quotes from column 4, lines 37 to 41, of Notarianni. Pet. 12. Patent Owner is correct that this particular disclosure relates to the memory operation of application module 202. Ex. 1031, 4:37–41. Nevertheless, as discussed above extensively, we are persuaded that Notarianni discloses FRAGM requesting “continuous use” of portions of main memory based on Notarianni’s disclosure that it “first finds at 702 the *maximum amount* of memory it will require in each plane” (Ex. 1031, 7:8–10 (emphasis added)) and passes that maximum amount “as a parameter to FRAGM . . . in a call to the function FRAG_INIT” (*id.* at 7:12–16), which, in turn, “requests CDRTOS memory manager 210 to allocate *at once* the memory space required MAXN fragments” (*id.* at 7:18–25 (emphasis added)). Pet. Reply 2–3.

With respect to being configured to translate the contiguous addresses to noncontiguous addresses, Petitioner counters that FRAGM uses a linked list to do so. Pet. Reply 17. We are persuaded that FRAGM’s use of a linked list “translates” addresses for the same reasons discussed above.

Finally, with respect to Patent Owner’s argument that Notarianni’s access controller executing FRAGM software is not a “single element,” Petitioner counters that the ’464 patent itself contemplates the recited “control circuit” implemented as a hardware component executing a software routine. Pet. Reply 18 (citing Ex. 1001, 4:43–46 “a memory management unit 122 (MMU) [that] operates under a routine described below to decode audio and video from the DVD CD-ROM player 112). We agree that the recited “control circuit” encompasses a hardware component executing a software routine, such as Notarianni’s access controller executing FRAGM software.

d. Decoding circuit

Independent claim 1 recites, in relevant part, “the decoding circuit is configured to request at least some of the contiguous addresses of the block of memory.”

Patent Owner argues that “the Petition has identified nothing in Notarianni suggesting that the video decoder (VD) or the adaptive pulse code modulation decoder (ADPCM) are ‘configured to request at least some of the contiguous addresses of the block of memory,’” as recited in independent claim 1. PO Resp. 33. Patent Owner further argues that Petitioner’s reliance on Notarianni’s application module is misplaced because the application module is not what Petitioner identified as the recited “decoding circuit” and it does not request “contiguous addresses of the block of memory.” PO Resp. 33–34.

Petitioner counters that the Petition describes how Notarianni’s decoder 206 reads audio and video data from the memory for the generation of desired audio and video presentation. Pet. Reply 19 (citing Pet. 13–14 (quoting Ex. 1031, 4:19–24 (“cause the decoders 206 to read [audio, video, and program data from the disc] for the generation of desired audio and video presentations.”))). Petitioner argues that “the decoder accesses links in the list (i.e., “requests some of the contiguous addresses”) as it sequentially traverses each link to process the stored audio and video data.” *Id.* With respect to the application module, Petitioner states that it “is merely the component that initiates the play operation,” and that “the decoder is given a pointer to the linked list so that it can generate the audio and video presentation from the data stored in memory.” *Id.* at 20.

We agree with Petitioner. The Petition states that:

The FRAGM translates the requested contiguous addresses of the block of memory to requested noncontiguous addresses *and permits the decoding circuit to access the portions of the main memory*. See, e.g., Ex. 1031 at 6:67-7:17; see also *id.*, Fig. 6 (depicting the operation of the application module), Fig. 7 (depicting the FRAGM translating contiguous addresses into the fragmented non-contiguous addresses in the main memory)

Pet. 13–14 (emphasis added). Although Petitioner relies on FRAGM for translating, the Petition indicates that FRAGM does not request, but merely “permits the decoding circuit to access the portions of the main memory.” *Id.* at 14. As a result, we are persuaded that the Petition explains sufficiently how Notarianni’s video decoder and adaptive pulse code modulation decoder are “configured to request at least some of the contiguous addresses of the block of memory.” Moreover, we are not persuaded that Petitioner’s citation to the operation of application module 202 is misplaced. Petitioner explains how application module 202 merely initiates the play operation, but the decoder itself traverses the linked list. Pet. Reply 20. This is consistent with Petitioner’s position that it is Notarianni’s video decoder and adaptive pulse code modulation decoder that teach the recited “decoding circuit.”

e. Summary

We conclude that Petitioner has demonstrated, by a preponderance of the evidence, that the subject matter of independent claim 1 is anticipated by Notarianni.

5. Claims 3, 4, 8–10, 12, 13, 16–21, 23, 24, 32, 33, 35, 36, and 40

We have reviewed Petitioner’s explanations and supporting evidence regarding claims 3, 4, 8–10, 12, 13, 16–21, 23, 24, 32, 33, 35, 36, and 40,

and we agree with and adopt Petitioner’s analysis showing that Notarianni discloses the limitations recited in these claims. *See* Pet. 14–25.

In its Patent Owner Response, Patent Owner responds that Notarianni does not disclose a “video decoding circuit,” as recited in claims 3 and 20, or an “audio decoding circuit,” as recited in claim 4 and 21. PO Resp. 34–35. These arguments, however, merely repeat Petitioner’s contention with respect to claim 1 that “no [] contiguous addresses are ever constructed in Notarianni.” *Id.* That argument is not persuasive for the reasons discussed above in the context of claim 1.

Patent Owner also argues that Notarianni does not disclose claim 16 because Notarianni does not disclose a memory management module “configured to translate the noncontiguous addresses to the contiguous addresses,” as recited in claim 16. PO Resp. 35. This argument repeats Patent Owner’s argument that Notarianni does not “translate” for the same reasons argued with respect to claim 1, and is not persuasive for the reasons discussed above.

We conclude that Petitioner has demonstrated, by a preponderance of the evidence, that the subject matter of claims 3, 4, 8–10, 12, 13, 16–21, 23, 24, 32, 33, 35, 36, and 40 is anticipated by Notarianni

C. Claims 7 and 22 — Obviousness over Notarianni

Petitioner argues that claims 7 and 22 are unpatentable under § 103(a) as obvious over Notarianni. Pet. 25–27. Petitioner explains how Notarianni describes the subject matter of each challenged claim (*id.*), and relies upon the Declaration of Dr. Stone (Ex. 1030 ¶ 68) to support its contentions. In its Patent Owner Response, Patent Owner presents one argument with respect to dependent claims 7 and 22. PO Resp. 35–38. Patent Owner relies

upon the Declaration of Dr. Thornton, to support its positions. Ex. 2003 ¶¶ 80–83.

We begin our analysis with the principles of law that generally apply to a ground based on obviousness, and then we address the parties' contentions with respect to dependent claims 7 and 22.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

2. Analysis

Each of claims 7 and 22 recites “wherein the control circuit includes a memory management unit that is configured to algorithmically translate the noncontiguous addresses to the contiguous addresses.” We construed “algorithmically translate” to mean “convert using at least one mathematical operation.”

Petitioner relies upon Notarianni's teaching of FRAGM to create a linked list of small, non-contiguous memory locations. Pet. 25. Petitioner

acknowledges that Notarianni “does not explicitly describe that the translation of noncontiguous addresses to contiguous addresses includes ‘algorithmically translat[ing] the noncontiguous addresses to the contiguous addresses,’” but argues that it would have been obvious to a person of ordinary skill in the art:

In particular, according to *Not[a]rianni*, each noncontiguous fragment of memory 200 is mapped to a corresponding fragment within a buffer of contiguous addresses, and the base addresses of successive contiguous fragments in a buffer differ by an offset in the contiguous address space. *See, e.g.*, Ex. 1031 at 5:58-63, 6:26-28, 9:67-10:13, Fig. 8c, Abstract. One of ordinary skill in the art would have understood that there would have been a finite number of options for obtaining this arrangement. Ex. 1030 at ¶ 68. For example, one of ordinary skill would have understood that addition of an offset (i.e., a mathematical operation) to successive base addresses could be used to produce the base address of the next contiguous fragment within a buffer into which a noncontiguous fragment of memory 200 is mapped. Ex. 1030 at ¶ 68; *see also* Ex. 1040 at Fig. 2 (depicting an exemplary addition operation using an offset). Therefore, given the design need for mapping noncontiguous fragments of memory 200 to corresponding contiguous fragments within a buffer disclosed by *Notarianni*, one of ordinary skill in the art would have had good reason to pursue the known option of using mathematical operations to translate the noncontiguous addresses to the contiguous addresses. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007); Ex. 1030 at ¶ 68. Indeed, the use of such mathematical operations would have been common sense and predictable to one of ordinary skill in the art. *See KSR*, 550 U.S. at 421; Ex. 1030 at ¶ 68; *see also* Ex. 1001 at 8:30-34 (admitting that “[l]ookup table techniques, memory mapping techniques, and the operation of memory management units are conventional”)

Pet. 26–27.

Patent Owner argues that a person of ordinary skill in the art would have understood that “the use of [Notarianni’s] linked listing of fragments does not involve a conversion ‘using at least one mathematical operation,’” as we construed “algorithmically translate” to require. PO Resp. 36–38 (citing Ex. 2003 ¶ 81). This argument is not persuasive, however, because it is conclusory. Petitioner argues credibly that a person of ordinary skill in the art would have known to use a mathematical operation, such as the addition of an offset, to traverse Notarianni’s linked list. Neither Patent Owner nor Dr. Thornton explain why a person of ordinary skill in the art would not have known to do so.

Patent Owner also argues that “[i]t would not be obvious to augment or replace the functionality of FRAGM to include the additional step of creating a lookup table of translated, converted, or mapped contiguous addresses. . . .” PO Resp. 37. That argument is not persuasive because the claims do not require creating a lookup table. *See Self*, 671 F.2d at 1348.

3. Summary

We conclude that Petitioner has established, by a preponderance of the evidence, that the subject matter of dependent claims 7 and 22 would have been obvious over Notarianni.

D. Claims 2 and 11 — Obviousness over Notarianni & Moore

Petitioner argues that claims 2 and 11 are unpatentable under § 103(a) as obvious over Notarianni and Moore. Pet. 27–28. Petitioner explains how Notarianni describes the subject matter of each challenged claim (*id.*), and relies upon the Declaration of Dr. Stone (Ex. 1030 ¶ 70) to support its contentions. In its Patent Owner Response, Patent Owner presents one argument with respect to dependent claims 2 and 11. PO Resp. 38. Patent

Owner relies upon the Declaration of Dr. Thornton, to support its positions. Ex. 2003 ¶ 84.

We begin our analysis with a summary of Moore, and then we address the parties' contentions with respect to dependent claims 2 and 11.

1. Moore (Ex. 1035)

Moore, dated April 19, 1965, states that “[i]ntegrated electronics is established today.” Ex. 1035, 2. According to Moore, “[r]educd cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate.” *Id.*

2. Analysis

Each of claims 2 and 11 recites “wherein the [decoding circuit / main memory] and the control circuit are monolithically integrated.”

Petitioner relies upon Moore’s teaching, as far back as the 1960s, that integrated electronics was established, and that integration reduced cost. Pet. 27–28 (citing Ex. 1035). Petitioner concludes that “monolithically integrating the decoding circuit and the control circuit in *Not[a]rianni*, or the main memory and control circuit in *Not[a]rianni* similar to the manner described in Moore, would have been nothing more than a combination of familiar elements that would have yielded predictable results.” Pet. 28 (citing *KSR*, 550 U.S. at 416). We agree with Petitioner and are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness. See *KSR*, 550 U.S. at 418.

Patent Owner argues that claims 2 and 11 would not have been obvious over Notarianni and Moore for the same reasons that independent

claims 1 and 10, from which they depend respectively, are not anticipated by Notarianni. PO Resp. 38. This argument is not persuasive because, as we discussed above, we are persuaded that Notarianni anticipates the subject matter of independent claims 1 and 10.

3. Summary

We conclude that Petitioner has established, by a preponderance of the evidence, that the subject matter of claims 2 and 11 would have been obvious over Notarianni and Moore.

E. Claim 34 — Obviousness over Notarianni & Rathnam

Petitioner argues that claim 34 is unpatentable under § 103(a) as obvious over Notarianni and Rathnam. Pet. 29–30. Petitioner explains how Notarianni describes the subject matter of claim 34 (*id.*), and relies upon the Declarations of Dr. Stone (Ex. 1030 ¶ 71) to support its contentions. In its Patent Owner Response, Patent Owner argues that claim 34 is patentable for the same reasons as independent claim 32, from which it depends. PO Resp. 38–39. Patent Owner relies upon the Declaration of Dr. Thornton, to support its positions. Ex. 2003 ¶ 85.

We begin our analysis with a brief overview of Rathnam, and then we address the parties’ contentions with respect to dependent claim 34.

1. Rathnam (Ex. 1005)

Rathnam describes a programmable multimedia processor called TM-1. Ex. 1005, Title, Abstract. TM-1 has a high performance VLIW-CPU core with video and audio peripheral units designed to support popular multimedia applications. *Id.* at Abstract. “TM-1 easily implements popular multimedia standards such as MPEG-1 and MPEG-2, but its orientation around a powerful general-purpose [central processing unit (CPU)] makes it

capable of implementing a variety of multimedia algorithms, whether open or proprietary.” *Id.* at 319.

Figure 1 of Rathnam is reproduced below.

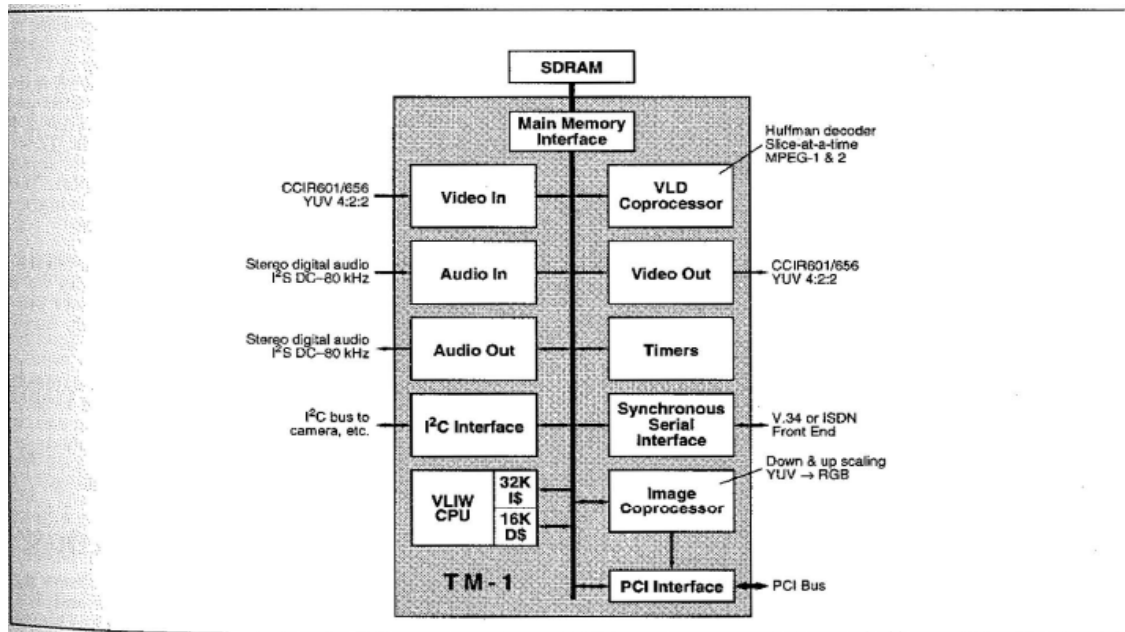


Figure 1. TM-1 block diagram.

Figure 1 shows a block diagram of TM-1. *Id.* at 320. The CPU and peripherals are time-shared and communication between units is through the synchronous dynamic random access memory (SDRAM). *Id.* at 320–321. “The internal data bus connects all internal blocks together and provides access to internal control registers (in each on-chip peripheral units), external SDRAM, and the external [peripheral component interconnect (PCI)] bus.” *Id.* at 322. “Access to the internal bus is controlled by a central arbiter, which has a request line from each potential bus master.” *Id.*

In operation, “[t]he TM-1 CPU can enlist the [Image Coprocessor (ICP)] and video-in units to help with some of the straightforward, tedious tasks associated with video processing.” *Id.* at 321. “A typical mode of operation for a TM-1 system is to serve as a video-decompression engine on

a PCI card in a [personal computer (PC)].” *Id.* “Video decompression begins when the PC operating system hands the TM-1 a pointer to compressed video data in the PC’s memory” *Id.* “The TM-1 CPU fetches data from the compressed video stream via the PCI bus, decompresses frames from the video stream, and places them into local SDRAM.” *Id.* “Decompression may be aided by the VLD (variable-length decoder) unit, which implements Huffman decoding and is controlled by the TM-1 CPU.” *Id.* “The TM-1 CPU hands the VLD a pointer to a Huffman-encoded bit stream, and the VLD produces a tokenized bit stream that is very convenient for the TM-1 image decompression software to use.” *Id.* at 324.

2. Analysis

We are persuaded by Petitioner’s arguments and cited evidence that the combined teachings of Notarianni and Rathnam account for each of the recited limitations of claim 34. Pet. 29–30 (citing Ex. 1030 ¶ 71). Petitioner contends as follows that a person of ordinary skill in the art would have found it obvious to combine the teachings of Notarianni and Rathnam.

An ordinary artisan would have understood the benefits of adding the MPEG-2 decoding ability disclosed in *Rathnam* to the system disclosed in *Not[a]rianni*. The ’464 admits that MPEG 2 decoding was known prior art. *See, e.g.*, Ex. 1001 at 1:45-50. MPEG 2 was an industry standard codec. Ex. 1030 at ¶ 71. An ordinary artisan would have understood implementing MPEG 2 decoding would increase the functionality of the video decoding circuit because it was compatible with a popular video codec. Ex. 1030 at ¶ 71. Thus, an ordinary artisan would have applied the well-known engineering technique of MPEG-2, as taught by *Rathnam*, to modify *Not[a]rianni*’s decoder to support MPEG-2. A person of ordinary skill would have found that modifying *Not[a]rianni* in this way would have been a simple and

commonsense combination of known prior art elements according to known methods to yield predictable results. *See KSR*, 550 U.S. at 401, 417; *see also* Ex. 1030 at ¶ 71.

Id. at 30. We agree with Petitioner and are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness. *See KSR*, 550 U.S. at 418.

Patent Owner argues that claim 34 is patentable based on the same reasons as the independent claim 32, from which it depends. PO Resp. 38. As discussed above, however, we remain persuaded by Petitioner's arguments that the subject matter of independent claim 32 is anticipated by Notarianni.

3. Summary

We conclude that Petitioner has established, by a preponderance of the evidence, that the subject matter of dependent claim 34 would have been obvious over the combined teachings of Notarianni and Rathnam.

III. CONCLUSION

Petitioner has demonstrated, by a preponderance of the evidence, that (1) claims 1, 3, 4, 8–10, 12, 13, 16–21, 23, 24, 32, 33, 35, 36, and 40 of the '464 patent are unpatentable under § 102(b) as anticipated by Notarianni; (2) claims 7 and 22 of the '464 patent are unpatentable under § 103(a) as obvious over the teachings of Notarianni; (3) claims 2 and 11 of the '464 patent are unpatentable under § 103(a) as obvious over the combined teachings of Notarianni and Moore; and (4) claim 34 of the '464 patent is unpatentable under § 103(a) as obvious over the combined teachings of Notarianni and Rathnam.

IV. ORDER

Accordingly, it is

ORDERED that claims 1–4, 7–13, 16–24, 32–36, and 40 of the '464 patent are determined to be *unpatentable*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2016-00924
Patent 5,960,464

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