

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION,
Petitioner,

v.

COLLABO INNOVATIONS, INC.,
Patent Owner.

Case IPR2016-00938
Patent 7,944,493 B2

Before DAVID C. McKONE, GREGG I. ANDERSON, and
JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

McKONE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Sony Corporation (“Petitioner”) filed a Petition (Paper 2, “Pet.”) to institute an *inter partes* review of claims 1–4 and 6–9 of U.S. Patent No. 7,944,493 B2 (Ex. 1001, “the ’493 patent”). Collabo Innovations, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

Pursuant to 35 U.S.C. § 314, in our Institution Decision (Paper 7, “Dec.”), we instituted this proceeding as to claims 1–3 and 6–9, but not claim 4.

Patent Owner filed a Patent Owner’s Response (Paper 12, “PO Resp.”), and Petitioner filed a Reply to the Patent Owner’s Response (Paper 15, “Reply”).

Petitioner relies on the Declaration of R. Michael Guidash (Ex. 1002, “Guidash Decl.”). Patent Owner relies on the Declaration of Martin Afromowitz, Ph.D. (Ex. 2003, “Afromowitz Decl.”).

An oral argument was held on July 11, 2017 (Paper 21, “Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–3 and 6–9. Based on the record before us, Petitioner has demonstrated, by a preponderance of the evidence, that claims 1–3 and 6–9 of the ’493 patent are unpatentable.

The ’493 patent describes solid-state imaging devices used, for example, to capture images in a digital camera. The challenged claims recite specific transistor components in active regions and electrical contacts arranged in a certain way. Petitioner contends that the Guidash patent describes a solid-state imaging device with the same components arranged

nearly the same way, and that it would have been obvious to modify the layout shown in the Guidash patent to meet the limitations of the challenged claims. Patent Owner argues that the art is unpredictable and that Petitioner's proposed modifications actually would have been disadvantageous. Patent Owner also argues that the Guidash patent does not teach an "active region" under Patent Owner's construction of that term. For the reasons given below, we agree with Petitioner that the challenged claims would have been obvious over the Guidash patent.

B. Related Matters

The parties indicate that the '493 patent has been asserted in *Collabo Innovations, Inc. v. Sony Corp.*, Case No. 1-15-cv-01094 (D. Del.), and *Collabo Innovations, Inc. v. Omnivision Technologies, Inc.*, Case No. 1-16-cv-00197-UNA (D. Del.). Pet. 1; Paper 5, 1. Different claims of the '493 patent are the subject of an additional *inter partes* review petition in IPR2016-00939. Pet. 1; Paper 5, 1.

C. Asserted Prior Art References

Petitioner relies on the following prior art:

Ex. 1003 ("Guidash patent")	US 6,657,665 B1	Dec. 2, 2003
Ex. 1006 ("Suzuki")	US 2003/0025160 A1	Feb. 6, 2003
Ex. 1008 ("Sakurai")	EP 0 926 738 A2	June 30, 1999

D. The Instituted Grounds

We instituted a trial on the following grounds of unpatentability (Dec. 39):

Reference	Basis	Claims Challenged
Guidash patent	§ 103(a)	1–3 and 6–9
Suzuki	§§ 102(a) and (e)	8 and 9
Sakurai	§ 103(a)	8 and 9

Because we conclude that each of claims 1–3 and 6–9 would have been obvious over the Guidash patent, as detailed below, we do not reach whether claims 8 and 9 would have been anticipated by or obvious over Suzuki or Sakurai.

E. The '493 Patent

The '493 patent describes metal-oxide semiconductor (“MOS”)-type¹ solid-state imaging devices to be used with equipment such as home video cameras, digital still cameras, and cameras incorporated in cellular phones.

¹ MOS-type transistors have three terminals: a “source,” “from which charge carrie[r]s flow into channel toward the drain”; a “drain,” “into which charge carriers flow from the source through the channel”; and a “gate,” which “controls the current between source and drain by a voltage applied to its terminal.” IEEE 100, *The Authoritative Dictionary of IEEE Standards Terms* 337, 476, 1074 (7th ed. 2000) (Ex. 3003); *see also* Ex. 1009, 103 (“**drain** In a *field-effect transistor* the connection to the *channel* which *majority carriers* enter on leaving the channel.”); 301 (“**source** Of a *field-effect transistor* the connection to the channel from which *majority carriers* enter the channel.”).

Ex. 1001, 1:15–19. Although the embodiments of the '493 patent include components typical in such solid-state imaging devices (e.g., photodiodes, floating diffusion layer sections, transfer gates, and reset, amplifier, and address transistors), as detailed in the patent's Background of the Invention and shown in the prior art circuit diagram of Figure 9, the patent describes and claims particular physical layouts of those components. *Id.* at 1:20–3:12; Pet. 2–5; Prelim. Resp. 5–7. According to the '493 patent,

[i]n general, as the circuit size is smaller, yields of the circuit are improved more, thereby reducing the cost of the circuit. Therefore, laying out a circuit according to predetermined design rules is an important technical task in designing the semiconductor integrated circuit. However, as for a sensor in which photosensitive cells are each formed by three transistors, no specific layout of these photosensitive cells has been clearly known to public.

Ex. 1001, 3:15–23.

Figure 7, reproduced below, depicts one such layout:

FIG. 7

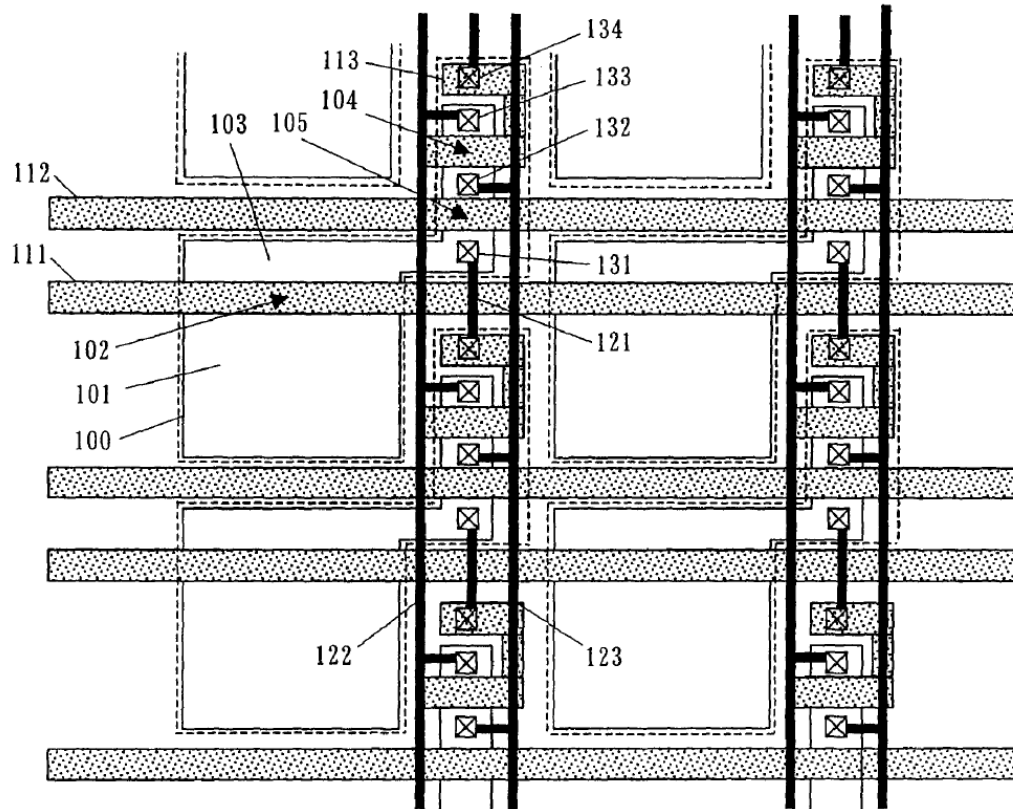


Figure 7 is a diagram illustrating two columns and two rows (out of many) of photosensitive cells of a layout pattern for a sensor. *Id.* at 5:37–38, 11:3–6; *see also id.* at 1:30–34 (“Note that, for the purpose of simplifying descriptions, it is assumed herein that the photosensitive cells are arranged in a 2×2 matrix. In practice, however, the photosensitive cells are arranged in a matrix with several tens to thousands of rows and columns.”). A particular cell includes active region 100. *Id.* at 11:5–6. At the three portions in which active region 100 and polysilicon wires 111, 112, and 113 overlap, transistors are formed. *Id.* at 11:6–9, 12–15. These include transfer gate 102 separating active region 100 into photodiode 101 and floating diffusion layer

section 103. *Id.* at 11:19–25. Reset transistor 105 and amplifier transistor 104 also are included. *Id.* at 11:12–18.

In operation, the reset transistors are controlled by a vertical shift register to first reset the floating diffusion layer sections. *Id.* at 1:42–45. The amplifier transistors produce outputs on vertical signal lines. *Id.* at 1:45–49. The transfer gates are controlled by the vertical shift registers to transfer electric charges stored in the photodiodes to the floating diffusion layer sections, causing signal voltages corresponding to the electric charges to appear on the vertical signal lines. *Id.* at 1:52–59.

The components are further connected by metal wires 121–123 and contact holes 131–134. *Id.* at 12:33–36. Floating diffusion layer section 103 is connected to the gate of amplifier transistor 104 by contact hole 131 and metal wire 121. *Id.* at 12:36–39, 12:56–58. Contact hole 132 is provided on a common drain shared by amplifier transistor 104 and reset transistor 105, and connects the common drain to metal wire 123 (a power supply line). *Id.* at 12:39–42. Contact hole 133 connects the source of amplifier transistor 104 to metal wire 122 (a vertical signal line). *Id.* at 12:43–45. Contact hole 134 connects the gate of amplifier transistor 104 to the floating diffusion layer of the next cell in the up direction. *Id.* at 12:45–49. Inferring from the repetition in Figure 7, the unlabeled wire connected to contact hole 134 corresponds to a wire 121 of the cell immediately above and the unlabeled contact hole connected to wire 121 opposite that of contact hole 131 corresponds to a contact hole 134 connected to the gate of the amplifier transistor of the cell immediately below.

In the embodiment of Figure 7, contact holes 131–134 are aligned approximately in one straight line. *Id.* at 12:49–51. According to the '493

patent, “[t]his can reduce an area required for layout of these four contact holes. Therefore, it is possible to reduce the size of the laid-out photosensitive cells, thereby reducing the circuit size of the entire sensor.” *Id.* at 12:52–55.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. An imaging device formed in a semiconductor substrate, the imaging device comprising:
 - a plurality of photodiodes arranged in rows and columns, each photodiode for a given row of photodiodes formed in a corresponding active region of the semiconductor substrate;
 - a transfer gate disposed over the first active region so as to define an associated photodiode on one side of the transfer gate and an associated floating diffusion element on another side of the transfer gate;
 - an amplifier transistor;
 - a reset transistor;
 - a first wire electrically connecting the associated floating diffusion element to a gate electrode of the amplifier transistor;
 - a second contact hole connecting a drain of the reset transistor to a third wire disposed over the first semiconductor substrate;
 - a third contact hole connecting the associated floating diffusion element to the first wire; and
 - a fourth contact hole connecting the gate electrode of the amplifier transistor to the first wire, wherein:
 - the amplifier transistor is formed in another active region which is separated from the corresponding active region where the associated floating diffusion

element connected to the gate of the amplifier transistor is formed,
the first wire is disposed in a column direction between the associated floating diffusion element and the gate electrode of the associated amplifier transistor, and
the second, third and fourth contact holes are aligned substantially in a straight line.

II. ANALYSIS

A. *Claim Construction*

We interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–45 (2016). In applying a broadest reasonable construction, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In the Institution Decision, we preliminarily construed the terms “active region,” appearing in independent claims 1 and 8, and “share a common drain,” appearing in dependent claims 7 and 9. Dec. 8–14. Patent Owner continues to contest both of these constructions, PO Resp. 13–35, while Petitioner contends that we should maintain them, Reply 7–20. We address the parties’ arguments as to “active region” below. Nevertheless, as to “share a common drain,” Patent Owner concedes that the Guidash patent teaches this limitation even under Patent Owner’s proposed construction. Tr. 32:18–33:3. Because we conclude that the Guidash patent teaches each

limitation of claims 7 and 9, we do not reach whether Suzuki or Sakurai teach the limitations of claim 9. Accordingly, we need not revisit our construction of “share a common drain” to resolve the parties’ dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

As to “active region,” the dispute is whether an active region must have a boundary across which charges cannot flow. In our Institution Decision, we preliminarily construed “active region” to mean “a contiguous region of the substrate through which charges can flow and where components such as photodiodes, diffusion layers, and portions of transistors are formed.” Dec. 12. We rejected the construction Patent Owner proposed in the Preliminary Response, namely, “an area where active transistors, photodiodes, and/or diffusion layers are formed that is surrounded by a device insulation region.” *Id.* at 9 (quoting Prelim. Resp. 13). We reasoned that the claims do not recite insulation as part of an active region and, indeed, the specification of the ’993 patent describes an insulation region as a component separate from an active region. *Id.* at 10–11 (citing Ex. 1001, 3:64–4:1 (“In each photosensitive cell, the photodiode, the transfer transistor, the floating diffusion layer section, the amplifier transistor, and the reset transistor are formed in one active region surrounded by a device insulation region . . .”))). We concluded that reading an insulation region as part of the claimed active region would be importing an extraneous limitation into the claims improperly. *Id.* at 11 (citing *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988) (“By ‘extraneous,’ we mean a limitation read into a claim from the

specification wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim. Where a specification does not require a limitation, that limitation should not be read from the specification into the claims.”)).

In its Response, Patent Owner argues that “active region” should be construed to mean “a contiguous region of the substrate through which charges can flow, having a boundary across which charges cannot flow, and where components such as photodiodes, diffusion layers, and portions of transistors are formed.” PO Resp. 34–35. Thus, Patent Owner would start with our construction and add to it “having a boundary across which charges cannot flow.” Based on Patent Owner’s response to questioning at the oral argument, it is unclear whether Patent Owner still contends that an active region includes an insulation region. Tr. 39:8–13 (“The insulation is the boundary of the active region, and which is reflected in the proposed construction, that it has a boundary. No, so, I wouldn’t say that the -- the insulation region is part of the active region. It is certainly what forms the boundary of the active region.”), 39:18–21 (“[Y]ou don’t have to have an insulation region, necessarily, in those terms, but you need something that confines the charge because the active region is defined by the region in which the charge is confined.”), 40:5–8 (“We’re defining the ‘active region’ by what this attribute of an active region that is required for the charge to be confined. And within that, there has to be a boundary for the active region.”). As explained below, the only boundary Patent Owner considers sufficient is an insulation region.

In essence, Patent Owner argues that (1) the ’493 patent describes the active region of the invention as including an insulation region and

(2) Dr. Afromowitz testifies that, to be usable, an active region must be maximally isolated from other regions and that, to achieve maximum isolation, an insulation region, in particular an oxide insulation, must be used.

Regarding the specification, the '493 patent states in its Abstract that certain components “are formed in one active region surrounded by a *device isolation region*.” Ex. 1001, Abstract (emphasis added). In the Summary of the Invention section, the specification states that certain components “are formed in one active region surrounded by a *device insulation region*.” *Id.* at 3:64–4:1 (emphasis added). Later, in its Description of the Preferred Embodiment section, in describing the embodiment of Figure 4, the specification states that “active region 200 is surrounded by a *device isolation region* (not shown).” *Id.* at 8:56–57 (emphasis added). The remaining references to active regions in the specification do not mention either isolation or insulation.

Patent Owner argues that these references to “isolation” and “insulation” in the specification show that charge is confined in the active region. PO Resp. 25–26. Patent Owner argues that because the Summary of the Invention and the Abstract use “insulation” and “isolation” similarly, the patent uses those terms interchangeably. *Id.* at 26. Relying on the Afromowitz Declaration, Patent Owner contends that the specification uses both “insulation” and “isolation” to mean the more restrictive “insulation” rather than the broader “isolation”; in other words, “one having ordinary skill in the art would have understood from the specification that the claimed active regions are all isolated by an insulation region.” *Id.* at 27 (citing

Ex. 2003 ¶ 31). Neither Patent Owner nor Dr. Afromowitz states why the more restrictive option is required.

In reply, Petitioner argues that the specification uses “active region” dozens of time and only once states that it is surrounded by a device insulation region. Reply 10. Petitioner further argues that the claims do not specify the character of the boundary of an active region and that the specification repeatedly refers to an active region without referring to what surrounds it. *Id.* As to the specific references to “insulation” and “isolation,” Petitioner argues that they reinforce our preliminary construction because they expressly describe insulation and isolation regions as being separate from the active regions. *Id.* at 10–11.

We agree with Petitioner. The challenged claims recite an “active region” without a recitation of an isolation region or an insulation region. Thus, the plain language of the claims does not require an insulation region serving as a border for an active region. As to the specification, it merely describes a device isolation region, specifically not shown, as an example region surrounding an active region of the preferred embodiment, but does not indicate that an isolation region is a part of an active region or necessarily accompanies an isolation region. Ex. 1001, 8:56–58. We are not persuaded that the ’493 patent’s one reference to “insulation” redefines active region or narrows the term “isolation” used elsewhere in the specification. We maintain our conclusion (Dec. 11) that reading an insulation region as part of the claimed active region (or necessarily accompanying an active region) based on the disclosure in the specification would be importing an extraneous limitation into the claims improperly. *See E.I. du Pont de Nemours*, 849 F.2d at 1433.

As noted above, Patent Owner also relies on the testimony of Dr. Afromowitz to provide technical reasons why an active region must have a border, such as an insulation region, across which charge cannot flow. Patent Owner contends that “[i]n order to serve its function in the imaging device, the active region must be insulated/isolated from other regions of the chip.” PO Resp. 28 (citing Ex. 2003 ¶ 32). Patent Owner again ties this to an insulation region, arguing that, “[i]n the context of MOS image sensor devices, this means that a dielectric, or non-conducting material or barrier is used to prevent the flow of an electric current under the influence of an electric field or a voltage difference.” *Id.* (citing Ex. 2003 ¶ 32). In his testimony, Dr. Afromowitz relies on the American Heritage Dictionary to conclude that “isolation” implies being apart or separate, that “insulate” means to prevent the passage of electricity, and, therefore, “an active region as envisioned by the inventor is a region that, by its intrinsic nature, is maximally isolated from other regions and in addition prevents, to the greatest possible degree, electric current from entering or leaving contiguous regions of the substrate.” Ex. 2003 ¶ 32 (citing Ex. 2012). Dr. Afromowitz does not explain how the dictionary definitions he relies upon support his conclusion with respect to the term “active region.” We find that the dictionary definitions do not adequately support Dr. Afromowitz’s testimony, that his conclusions do not logically follow from this evidence, and, therefore, that his testimony is not credible on this point.

Again relying on Dr. Afromowitz, and additionally on treatises, Patent Owner argues that it was known in the art that “the active region is usually physically defined by the isolation material surrounding it.” PO Resp. 28–30 (citing Ex. 2003 ¶ 34; Ex. 2009; Ming Bo Lin, *Introduction to VLSI*

Systems: A Logic, Circuit, and System Perspective, 203–04 (2012) (not introduced as an exhibit)). According to Dr. Afromowitz,

a person of ordinary skill in the art understands that this term of art applies to specifically bounded regions of the device across whose boundary charges cannot flow. The boundary is physically exhibited, at least, as an area where charge is confined. If the construction permits charge flow across the boundary, then an essential feature of the active region is missing, and the construction would be in contradiction to the purpose of the active region.

Ex. 2003 ¶ 34. Dr. Afromowitz does not cite to or explain the bases for this testimony. We find this testimony conclusory and unpersuasive and, accordingly, give it little weight. See 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

As to the cited treatises, Patent Owner concedes that “[a] person of ordinary skill in this field would know that there are different methods that have been used to isolate active regions of a semiconductor device,” but argues that only insulation, such as the use of dielectric materials or oxide described in Exhibit 2009, is consistent with the use of “active region” in the ’493 patent. PO Resp. 30–31 (citing Ex. 2003 ¶ 35). Patent Owner argues that other forms of isolation, such as p/n junction isolation (purportedly used in the prior art), are not consistent with the active regions of the patent, because they would result in charge being leaked away from the photodetectors, “making the device unusable for all practical purposes.” *Id.* at 31–32 (citing Ex. 2003 ¶¶ 35–37). Dr. Afromowitz repeats these arguments in his testimony, but, once again, does not state the bases for these opinions. Ex. 2003 ¶¶ 35–37. In particular, Dr. Afromowitz does not

explain how Patent Owner's cited treatises (Ex. 2009; Ex. 2010; Lin) support his conclusions. Moreover, as Petitioner points out (Reply 14), Dr. Afromowitz admitted on cross-examination that prior art active regions were isolated by p/n junctions and that he did not know whether, at the time of the invention, such p/n junction isolation was more or less common than the insulation his Declaration states was necessary to make a device that was not unusable. Ex. 1015, 57:2–58:17. In light of the lack of supporting factual bases for the conclusory opinions in his Declaration and his cross-examination testimony indicating a lack of knowledge in the subject matter area, we find Dr. Afromowitz's testimony on this point to lack credibility. Accordingly, we give it little weight.

Moreover, we have reviewed Patent Owner's extrinsic evidence and find that it does not support Patent Owner's conclusion that isolation regions other than insulation regions (including p/n junction isolation) are inconsistent with the '493 patent's teachings or that such isolation would have rendered devices unusable. To the contrary, as Petitioner argues (Reply 12–14), these extrinsic references show that it was known to use active regions with isolation regions other than dielectric and oxide insulation. This further undermines Dr. Afromowitz's testimony that such isolation would have rendered devices unusable.

In sum, the claim language itself does not restrict “active region” to a region bounded by insulation, maximally isolated, or otherwise including a boundary across which charges cannot flow.² Likewise, the '493 patent's

² We note that Patent Owner was unable to quantify the effectiveness of an insulation that provides maximal isolation. Tr. 45:1–19.

reference to a device insulation region is, at best, a non-limiting example of a device isolation region described as part of the patent's preferred embodiment. We see no indication that this reference is a lexicographic definition or statement of disavowal. We have considered Patent Owner's extrinsic evidence but find it unpersuasive. Patent Owner's treatises support Petitioner's position that active regions were known in the art with or without insulation regions. Patent Owner's expert declaration is contradicted by the language of the claims, the specification, Patent Owner's treatises, and the witness's own cross-examination testimony. Thus, it is entitled to little weight. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (en banc) (internal quotation marks and citation omitted) (“[C]onclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court. Similarly, a court should discount any expert testimony that is clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent.”).

On the complete record, we maintain our construction of “active region,” namely, “a contiguous region of the substrate through which charges can flow and where components such as photodiodes, diffusion layers, and portions of transistors are formed.”

B. Alleged Obviousness of Claims 1–3 and 6–9 over the Guidash Patent

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are “such that the subject matter as a whole would have been obvious at the time the invention

was made to a person having ordinary skill in the art to which said subject matter pertains.” We resolve the question of obviousness on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.³ See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In an obviousness analysis, some reason must be shown as to why a person of ordinary skill would have combined or modified the prior art to achieve the patented invention. See *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008). A reason to combine or modify the prior art may be found explicitly or implicitly in market forces; design incentives; the “interrelated teachings of multiple patents”; “any need or problem known in the field of endeavor at the time of invention and addressed by the patent”; and the background knowledge, creativity, and common sense of the person of ordinary skill. *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1328–29 (Fed. Cir. 2009) (quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–21 (2007)).

1. Level of Ordinary Skill

Petitioner does not state in the Petition its contention as to the level of ordinary skill in the art. Rather, Petitioner states that it is discussed in the Guidash Declaration. Pet. 11. Mr. Guidash testifies that a skilled artisan

³ The record does not include arguments or evidence regarding objective indicia of nonobviousness.

would have had “a Bachelor’s degree in electrical engineering, physics, or material science and approximately 3–5 years of industrial experience or equivalent research or teaching experience, or a Master’s degree in the same fields and 1–3 years of industrial experience or equivalent research or teaching experience in the field of semiconductor image sensor design and fabrication.” Ex. 1002 ¶ 45. Patent Owner argues that Petitioner did not reproduce Mr. Guidash’s opinion in the Petition. PO Resp. 62.

Nevertheless, Patent Owner does not provide a statement of the level of skill in the art and, when asked at the oral hearing, confirmed that it does not dispute Mr. Guidash’s opinion. Tr. 36:18–37:10. In any case, Mr. Guidash’s opinion as to the state of the art is consistent with the level of skill indicated by the prior art of record in this proceeding—namely the Guidash patent, Suzuki, Sakurai, and Hashimoto (Ex. 1013, EP 0954032A2). *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Nevertheless, the parties dispute the level of predictability in the art. Mr. Guidash testifies that “changes to integrated circuit layouts could be predictably implemented using techniques readily available to most engineers in the field at the time the ’493 patent was filed” and that “the standard principles involved concerning the interaction between various integrated circuit elements, their sizes and proximities were well-understood and predictable by 2003.” Ex. 1002 ¶ 48. Relying, for example, on the Mead & Conway treatise (Ex. 1005, 116–68), Mr. Guidash testifies that various software tools existed to help skilled artisans in the design and layout process and that such software “allowed numerical simulations to be performed of both the circuit diagram and the layout, allowing the effect of

changes to the layout to be predicted easily and with good accuracy.”

Ex. 1002 ¶ 48.

Patent Owner, relying on Dr. Afromowitz, argues that, because pixel design and layout includes human intervention that must be checked by computer aided design (CAD) algorithms, “it is not possible to predict with any degree of assurance that the circuit would work as hoped since simulation models are generally based on a set process” and that “applying a design in one fabrication process to another fabrication process would likely cause a change in the design rules and subsequently require the re-layout of a circuit.” PO Resp. 5 (citing Ex. 2003 ¶¶ 64–65, 74). According to Patent Owner, “[o]utcomes were by no means predictable at the time frame of the ’493 Patent’s priority date.” *Id.* at 6 (citing Ex. 2003 ¶ 74). Dr. Afromowitz additionally testifies that “[a]nalog integrated circuit design in general, and image sensor pixel circuit design and layout in particular, has always been regarded as something of a black art” and that his reason for this conclusion is that “there are not many automated computerized tools available even today to guarantee success of analog IC designs.” Ex. 2003 ¶ 66.

In support, Dr. Afromowitz cites primarily to Mr. Guidash’s deposition regarding reasons why an image sensor designer would perform a custom layout rather than an automated placement layout (Ex. 2003 ¶ 64 (citing Ex. 2011, 69:4–16)) and reasons why the designer would waive design rules (*id.* ¶ 65 (citing Ex. 2011, 73:15–17)). Dr. Afromowitz also relies on comments posted on the website www.quora.com, allegedly by skilled artisans, that analog circuit design is complex and unpredictable. *Id.* ¶¶ 69–73. Aside from the obvious hearsay problems, Dr. Afromowitz fails to connect these general statements about analog circuit design to the

particular art at issue in this case and fails to establish that such statements on message boards are the type of information experts in this field would reasonably rely on.

In reply, Petitioner urges us to resolve the dispute between the experts on the predictability in the art by considering their respective backgrounds. Reply 5. Petitioner argues that Mr. Guidash has decades of experience designing pixel layouts for commercial image sensors and holds numerous patents related to image sensor design. *Id.* We have considered Mr. Guidash's qualifications and agree that Mr. Guidash has the experience that Petitioner asserts. Mr. Guidash lists numerous such examples in his declaration. Ex. 1002 ¶¶ 9–11. Included in this is over a decade managing R&D and product development of CMOS Image Sensor programs at Kodak. *Id.* ¶ 11. This experience is stated in more detail in Mr. Guidash's curriculum vitae (CV), Ex. 1014, 1–3. In addition to his experience at Kodak, Mr. Guidash has written several technical publications related to pixel design and has dozens of patents in this art. Ex. 1014, 3–4. Mr. Guidash also was questioned extensively about his design experience on cross-examination. Ex. 2011, 10:17–17:10, 18:13–19:18. It is clear that Mr. Guidash has extensive experience designing and managing the design of the type of CMOS image sensors at issue in this proceeding.

In contrast, Petitioner argues, Dr. Afromowitz “has no relevant industrial experience, and very little relevant academic experience” and “has never been involved in the design of an image sensor.” Reply 5. We have considered Dr. Afromowitz's qualifications and agree with Petitioner's position. According to his Declaration, Dr. Afromowitz has extensive experience designing light-emitting diodes, lasers, and optical fiber sensors,

but we see little experience with solid state imaging devices or pixel design and layout. Ex. 2003, ¶¶ 4–6. This is confirmed by his CV, which lists his industry experience as “primarily involved with materials characterization (optical, thermal, lattice matching, etc.).” *Id.* at Appendix A, 1. His research interests, publications, and patents also do not appear to bear directly on the issues of this proceeding. *Id.* at Appendix A, 2–6. Dr. Afromowitz confirmed on cross-examination that he has never designed, simulated, or tested a pixel design or layout and that none of his publications or patents was related to pixel design. Ex. 1015, 29:6–30:13, 31:22–32:15. Dr. Afromowitz’s most relevant experience in this art was teaching an undergraduate-level class and a graduate-level class that included pixel layouts and a description of simulation tools as part of the lecture and homework assignments, of which only one or two lectures would deal with specific layouts for the design of pixels. *Id.* at 29:6–30:2, 32:16–33:15, 71:9–72:3. Although we have no reason to doubt that Dr. Afromowitz has extensive expertise in the fields in which he worked and researched extensively, those fields are not particularly relevant to the issues of this proceeding.

Given his extensive experience in the subject matter area of this proceeding, Mr. Guidash is very qualified to testify regarding the predictability of the art and, accordingly, we find his testimony highly credible. In contrast, given his relative lack of experience in the subject matter area of this proceeding, we find Dr. Afromowitz only minimally qualified and, therefore, find his testimony much less credible. We believe Mr. Guidash when he testifies that an engineer with 3–5 years of experience in this field “would have been familiar with semiconductor fabrication

techniques to build semiconductor image sensors, including various design rules used by different fabrication facilities” and “would have known how to make changes to a layout by re-routing signal lines, adding or removing transistors, moving or rearranging transistors, etc., and would have been able to predict the outcome of these changes.” Ex. 1002 ¶ 47.

2. Scope and Content of the Prior Art - Overview of the Guidash Patent

The Guidash patent describes solid-state image sensors having a plurality of pixels arranged in a series of rows and columns. Ex. 1003, Abstract, 1:7–13. Figure 4, reproduced below, illustrates an example.

Fig.4

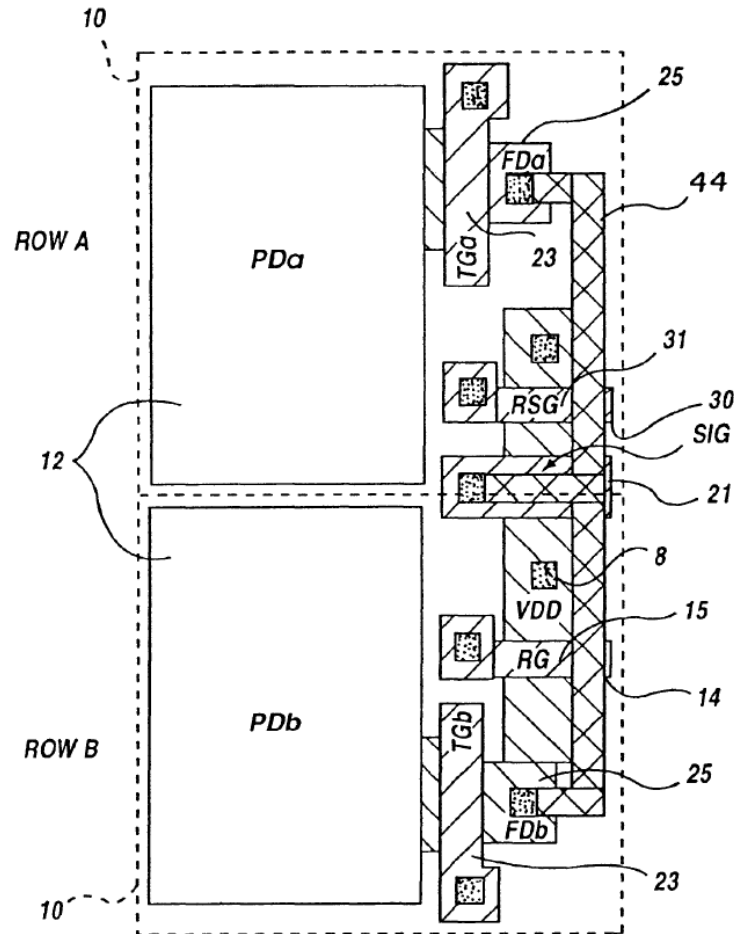


Figure 4 is a top view of two row-adjacent pixels, showing how the two physically separate floating diffusions in each pixel are interconnected to each other and to a source follower input transistor. *Id.* at 3:48–56.

Pixel 10 includes photodiode photodetectors 12 and floating diffusions 25 separated by transfer gates 23. *Id.* at 3:57–58. Floating diffusions 25 are physically and spatially isolated from each other and are electrically connected to one another, and to the gate of source follower input signal transistor 21, by conductive interconnect layer 44. *Id.* at 3:65–

4:4. Both source follower input transistor 21 and reset transistor 14 are connected to voltage supply 8 (“VDD”). *Id.* at 3:60–62.

3. *Comparison of the Guidash patent to the challenged claims; differences between the challenged claims and the Guidash patent*

a. *Claims 1 and 8*

Regarding claim 1, Petitioner contends that the Guidash patent teaches an imaging device formed in a semiconductor substrate, comprising a plurality of photodiodes arranged in rows and columns, citing to the Abstract of the Guidash patent. Pet. 13 (citing Ex. 1003, Abstract (“An image sensor having a plurality of pixels arranged in a series of row and columns comprising a semiconductor substrate”)). Based on this evidence, we agree.

Petitioner contends that photodiode PDa and floating diffusion FDa (shown in Figure 4, reproduced above), together, constitute an “active region of the semiconductor substrate.” Pet. 13–14. Similarly, Petitioner contends that photodiode PDb and floating diffusion FDb, together, constitute another active region physically separated from the other active region by isolating regions. *Id.* We agree that the Guidash patent describes two contiguous regions over which charge can flow (PDa + FDa and PDb + FDb), each at least isolated from the other. For example, the Guidash patent explains that “[i]n FIG. 4 the floating diffusions 25, are physically and spatially isolated from each other and are electrically connected to each other and the source follower input transistor 21 by means of a conductive interconnect layer 44.” Ex. 1003, 3:67–4:4; *see also id.* at 4:7–13 (“Floating diffusion 25, FDa, while on the same electrical node as floating diffusion FDb, is spatially isolated from floating diffusion 25 FDb. Therefore, floating diffusion 25

FDA while on the same electrical node as, floating diffusion 25 FDB, does not serve as the source 16 for the reset transistor 14, while floating diffusion FDB does serve as the source 16 of the reset transistor 14.”).

Patent Owner contends that the Guidash patent does not teach active regions because Petitioner has not shown anything in the Guidash patent that would indicate an active region having a boundary across which charges cannot flow. PO Resp. 47. Rather, Patent Owner argues, the Guidash patent “is silent as to what defines its active regions and is silent as to having any boundaries to any region confining charges.” *Id.* at 48. Patent Owner further contends that, in the imaging device of the Guidash patent, “each pixel’s floating diffusion region is merely spatially separated.” *Id.* (citing Ex. 1003, 3:63–67, 4:7–9). Although the Guidash patent states that the two regions depicted in Figure 4 are “physically and spatially isolated from each other,” Ex. 1003, 4:1–2, we need not determine whether such physical separation in addition to spatial separation indicates an insulation region. Rather, as explained in Section II.A above, an “active region” is “a contiguous region of the substrate through which charges can flow and where components such as photodiodes, diffusion layers, and portions of transistors are formed,” and need not (a) be maximally isolated, (b) include an insulation region, or (c) include a boundary over which charge cannot pass. Under our construction, we find that PDA and FDA, together, are an active region and that PDB and FDB, together, are another active region.

Petitioner further contends that transfer gate TGA is disposed over the active region of PDA and FDA and defines a photodiode (PDA) on one side and an associated floating diffusion element (FDA) on the other. Pet. 14–15. We agree that this is shown in Figure 4 of the Guidash patent, reproduced

above. Thus, we find that the Guidash patent teaches “a transfer gate disposed over the first active region so as to define an associated photodiode on one side of the transfer gate and an associated floating diffusion element on another side of the transfer gate,” as recited in claim 1.

Petitioner identifies source follower transistor 21 and reset transistor 14, both formed on floating diffusion FDb, respectively as an “amplifier transistor” and “reset transistor,” as recited in claim 1. *Id.* at 15.

Mr. Guidash testifies that source follower transistor 21 is an amplifier transistor. Ex. 1002 ¶ 80. We credit this testimony, which is undisputed. We find that the Guidash patent teaches “an amplifier transistor” and “a reset transistor,” as recited in claim 1.

As shown in Figure 4 of the Guidash patent, conductive interconnect layer 44 connects floating diffusion FDa to the gate electrode of source follower input signal transistor 21 (the amplifier transistor). Pet. 15–16. As noted above, the Guidash patent explains that “[i]n FIG. 4 the floating diffusions 25, are physically and spatially isolated from each other and are electrically connected to each other and the source follower input transistor 21 by means of a *conductive interconnect layer 44*.” Ex. 1003, 3:67–4:4 (emphasis added). We find that the conductive interconnect layer 44 of the Guidash patent is “a first wire electrically connecting the associated floating diffusion element to a gate electrode of the amplifier transistor,” as recited in claim 1.

Petitioner identifies, in Figure 4, the square contact labeled VDD (voltage supply 8) as a “second contact hole,” as recited in claim 1, connecting the drain of reset transistor 14 to a third wire disposed over the semiconductor substrate. Pet. 16–17. The Guidash patent does not specify

whether the transistors of Figure 4 are NMOS or PMOS transistors. Nevertheless, relying on other examples in the Guidash patent, Mr. Guidash testifies that NMOS transistors would have been the obvious choice. *Id.* at 17 (citing Ex. 1002 ¶ 86). If NMOS technology is used, Petitioner argues, electrons in reset transistor 14 would flow toward VDD, making it the drain. *Id.* (citing Ex. 1002 ¶ 87). Mr. Guidash further testifies that it would have been obvious to deliver VDD using a conductor in the metal layer, which Petitioner argues would be a “third wire,” as recited in claim 1. *Id.* (citing Ex. 1002 ¶ 87). We credit Mr. Guidash’s testimony, which is undisputed. Accordingly, we find that the Guidash patent teaches “a second contact hole connecting a drain of the reset transistor to a third wire disposed over the first semiconductor substrate,” as recited in claim 1.

As Petitioner argues (Pet. 17–18), Figure 4 shows a square contact hole (“third contact hole”) connecting floating diffusion FDa to conductive interconnect layer 44 (the first wire). Mr. Guidash testifies that the dark square in Figure 4 is a contact hole that extends vertically between FDa upward toward interconnect layer 44 in the metal layer. Ex. 1002 ¶ 88. We credit that testimony, which is undisputed. We find that this teaches “a third contact hole connecting the associated floating diffusion element to the first wire,” as recited in claim 1.

Similarly, Petitioner identifies a square contact hole (“fourth contact hole”) connecting the gate electrode of source follower transistor 21 (the amplifier transistor) to conductive interconnect layer 44 (the first wire). Pet. 18. We agree that this is shown in Figure 4. Thus, we find that the Guidash patent teaches “a fourth contact hole connecting the gate electrode of the amplifier transistor to the first wire,” as recited in claim 1.

As shown in Figure 4, source follower transistor 21 (the amplifier transistor) is formed on the active region of PDb and FDb, which, we explain above, is “another active region which is separated from the corresponding active region where the associated floating diffusion element [FDa] connected to the gate of the amplifier transistor is formed,” as recited in claim 1. Ex. 1003, 3:67–4:13. Thus, we find that the Guidash patent teaches “the amplifier transistor is formed in another active region which is separated from the corresponding active region where the associated floating diffusion element connected to the gate of the amplifier transistor is formed,” as recited in claim 1.

Petitioner acknowledges (Pet. 19–20) that the VDD contact hole (second contact hole), the gate of source follower input signal transistor 21 (the third contact hole), and the contact hole for FDa (the fourth contact hole) are not aligned substantially in a straight line, as recited in claim 1. As explained below, Petitioner argues that aligning the holes would have been obvious.

Claim 8 is substantially the same as claim 1, except that (1) claim 8 does not recite a “second contact hole”; (2) claim 8 recites “the first wire is disposed in approximately a straight line between the associated floating diffusion element and the gate electrode of the amplifier transistor”; and (3) rather than reciting that a second, third, and fourth contact holes are aligned substantially in a straight line, claim 8 recites that “the third contact hole and [t]he fourth contact hole are aligned in the column direction.” As to the limitations of claim 8 that overlap with those of claim 1, Petitioner refers to its evidence and argument for claim 1. Pet. 25–27. Based on this evidence, and for the reasons given for claim 1, we find that the Guidash

patent teaches the limitations of claim 8 that overlap with the limitations of claim 1.

Petitioner appears to acknowledge that Guidash's first wire (conductive interconnect 44) is not "disposed in approximately a straight line between the associated floating diffusion element and the gate electrode of the amplifier transistor" and that the third and fourth contact holes are not "aligned in the column direction," as recited in claim 8. Pet. 26–27. We find that they are not. As shown in Figure 4, conductive interconnect 44 takes two ninety-degree bends from the third contact hole to the fourth. As explained below, however, Petitioner argues that aligning the holes, with a first wire that is approximately a straight line between the holes, would have been obvious.

b. Claim 6

Claim 6 recites that "the reset transistor and the amplifier transistor are arranged between adjacent photodiodes in a row direction." As explained above, the pixel shown in Figure 4 is one of many rows and columns of pixels. Petitioner argues that reset transistor 14 and source follower input signal transistor (the amplifier transistor) 21 are arranged between the pixel shown in Figure 4 and an adjacent pixel in a row direction. Pet. 23–24.

Referring to Figure 4 of the '493 patent, Patent Owner argues that, to be arranged between adjacent photodiodes, the reset transistor and amplifier transistor must be substantially in the middle of the region between two adjacent photodiodes. PO Resp. 45. Figure 4 of the '493 patent is reproduced below:

F I G. 4

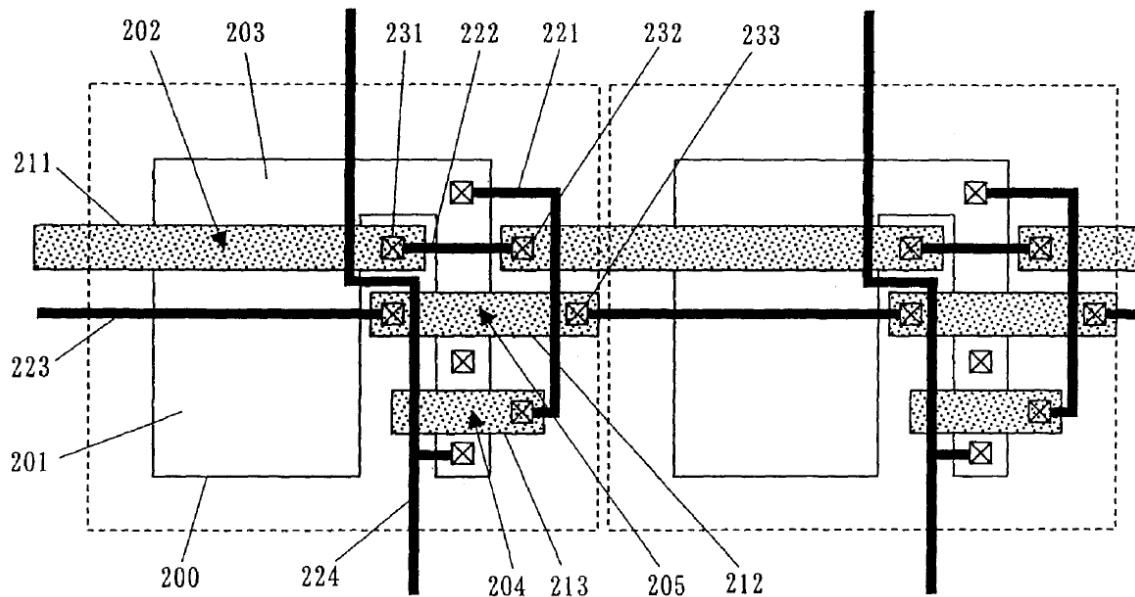


Figure 4 is a diagram of a layout pattern of photosensitive cells in a sensor. Ex. 1001, 5:29–30, 8:45–48. In Figure 4, reset transistor 205 is substantially in the middle of the space between active region 200 and an adjacent active region, while amplifier transistor 204 is formed near the bottom of the space between the active regions. *Id.* at 8:62–9:7. Patent Owner compares this to Figure 4 of the Guidash patent, reproduced above, in which reset transistor 14 is formed substantially in the middle of the space between active region PDb and an adjacent active region and amplifier transistor 21 is formed near the bottom of the space between active region PDa and an adjacent active region. PO Resp. 45–46. Patent Owner argues that “the amplifier transistor SIG [21] is situated on a line between the two photodiodes shown in part on the left of the figure [4 of the Guidash patent]” and that, because of this, a skilled artisan “would not have understood Guidash 665’s Amplifier to be ‘arranged between adjacent photodiodes in a row direction.’” *Id.* at 45. Patent Owner cites to the Afromowitz Declaration, but omits a paragraph

number. We presume Patent Owner intended to cite paragraph 105, which substantially repeats this argument. Ex. 2003 ¶ 105.

In reply, Petitioner argues that we should construe claim 6 in conjunction with Figure 7 of the '493 patent (reproduced above), rather than Figure 4. Reply 21. As shown in Figure 7, as Petitioner argues, reset transistor 105 is between columns of photodiodes, but is not between individual photodiodes. *Id.* The '493 patent describes Figure 7 in terms of regions of cells, in which the photodiode is in a first region of a cell, the amplifier and reset transistors are in a second region of the cell, and the second region of the cell is between the first region of that cell and the first region of an adjacent cell:

Here, consider a case where each photosensitive cell is divided into a first region and a second region, the first region including the photodiode 101, the transfer gate 102, and a part of the floating diffusion layer section 103 (in FIG. 7, a region on the left side of the metal wire 122) and the second region including the remaining floating diffusion layer section 103, the amplifier transistor 104, and the reset transistor 105 (in FIG. 7, a region on the right side of the metal wire 122). In this case, broadly speaking, the second region of the photosensitive cell C is laid out between the first region of the photosensitive cell A and the first region of the photosensitive cell B.

Ex. 1001, 11:64–12:8. According to Petitioner, this “supports a construction of claim 6 that requires a reset and amplifier transistor to be between adjacent columns of photodiodes, but not necessarily strictly between two photodiodes.” Reply 22.

We agree with Petitioner. Reading claim 6 in light of both Figures 4 and 7 of the '493 patent, it is clear that “arranged between adjacent photodiodes in a row direction” means “between adjacent columns of

photodiodes,” as shown in both figures. Indeed, Patent Owner appears to acknowledge, and we agree, that Figure 7 most closely aligns with the challenged claims. *See* PO Resp. 7 (“The ’493 Patent’s Figure 7 below illustrates a representative embodiment of some additionally novel features as expressed in claims 1–9 of the ’493 Patent.”). Patent Owner’s interpretation of claim 6 would read out the embodiment of Figure 7. Patent Owner offers no persuasive evidence or argument that this is appropriate under a broadest reasonable interpretation.

As shown in Figure 4 of the Guidash patent, amplifier transistor 204 and reset transistor 205 are arranged between adjacent columns of photodiodes. Accordingly, we find that the Guidash patent teaches the additional limitation of claim 6.

c. Claims 2, 3, 7, and 9

Claim 2 recites that “the first wire includes a straight portion disposed in the column direction” and claim 3 recites that “the first wire includes a portion disposed in a direction traversing column direction.” We find that Figure 4 of the Guidash patent shows such portions of conductive interconnect layer 44, the alleged “first wire,” with portions of conductive interconnect layer 44 running from left to right and a portion running up to down. Thus, we find that the Guidash patent teaches the additional limitations of claims 2 and 3.

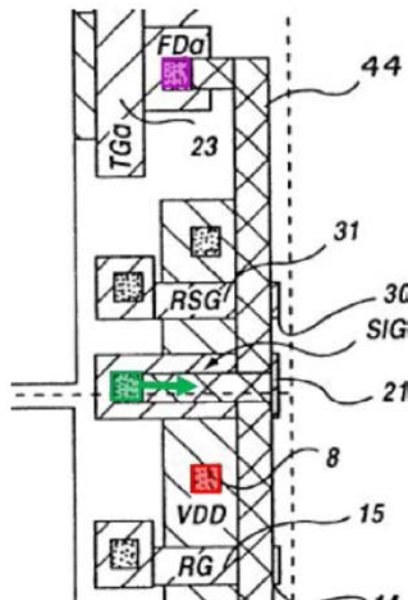
Claim 7 depends from claim 1. Claim 9 depends from claim 8. Both claims 7 and 9 recite “wherein the amplifier transistor and the reset transistor share a common drain.” Petitioner argues that, as shown in Figure 4, both source follower input signal transistor 21 and reset transistor 14 share VDD

as their drain. Pet. 24. Specifically, Petitioner argues that, because transistor 21 is described as a source-follower type, VDD 8 is the drain and the output side facing the row-select transistor RSG is the source. *Id.* As with claim 1, above, Petitioner contends that the reset and amplifier transistors are implemented using NMOS transistors. *Id.* at 24–25.

We find that Figure 4 shows that VDD 8 is in a portion of the active region physically shared by both the reset transistor 14 and the source follower input signal transistor 21. Thus, we find that the reset transistor and amplifier transistor shown in Figure 4 share a common drain. Patent Owner concedes that the Guidash patent teaches the additional limitation of claims 7 and 9. Tr. 32:18–33:3.

4. Reasons to Modify the Guidash Patent

Petitioner contends that it would have been obvious to move the Guidash patent's fourth hole into alignment with the second and third holes, as illustrated in portions of Figure 4 Petitioner has annotated:



The figure above is a portion of Figure 4 of the Guidash patent annotated by Petitioner to color in the boxes for the second, third, and fourth contact holes and include an arrow pointing from the fourth contact hole to the right, showing where the fourth contact hole would be moved. Petitioner argues that “a person of ordinary skill would have recognized that moving the fourth contact to the right would have placed the contact over the channel of the amplifier transistor, and thus over the gate oxide.” Pet. 20. Petitioner later refers to this with the shorthand “metal-to-poly,” or metal-to-polysilicon, contact. *See, e.g.*, Reply 27. In other words, one issue is whether a skilled artisan would have placed a metal-to-poly contact directly over a transistor channel, which would be the result of moving the fourth contact in the manner proposed by Petitioner.

Petitioner argues that this was not done in the Guidash patent because the design described in that patent was implemented using a set of design rules that would have prevented it. *Id.* at 20–21. Specifically, relying on Mr. Guidash (Petitioner’s expert and the named inventor on the Guidash patent), Petitioner argues, “in the relevant timeframe, certain fabricators had design rules that did not allow gate contacts to be made directly over the transistor channel, while certain fabricators *did* allow that.” *Id.* at 20. Mr. Guidash cites the Mead & Conway treatise (Ex. 1005) as teaching an example of a metal-to-poly contact over a transistor channel, in support of his testimony that “[w]hether a contact was allowed to be over a transistor channel was dependent on the technology available in the production line.” Ex. 1002 ¶ 95. As Patent Owner notes (PO Resp. 39–40), Mr. Guidash testified in deposition that he did not include such an example in the Guidash patent because “[a]t the time of the invention and the process being used,

there was a design rule constraint in the particular process that the contact to a gate could not be made to the poly over the active region” and “[i]n applying for a patent, we chose to include a -- an embodiment that had been demonstrated and this was at the time, given the constraint of contact placement I just mentioned, the best embodiment for those constraints.” Ex. 2011, 74:18–75:2.

Petitioner further argues that, in the case of fabricators that did allow gate channels to be made directly over the transistor channel, bringing the three holes into alignment would have shortened the polysilicon gate, saving space, and “would allow for the photodiode PDA to be enlarged, which in turn would increase the ‘fill factor,’ allowing the photodiode to receive more light.” Pet. 20–21 (citing Ex. 1002 ¶¶ 95–96). According to Petitioner, increasing the fill factor would have been desirable “because it would increase the sensitivity and saturation signal of the sensor, improving performance.” *Id.* at 21 (citing Ex. 1002 ¶ 96; Ex. 1003, 1:45–65). Relying on Mr. Guidash’s testimony, Petitioner argues that “[a] person of ordinary skill would further have known that minor variations in contact hole placement would not have materially affected the performance of the device.” *Id.* (citing Ex. 1002 ¶ 97).

Patent Owner argues that a skilled artisan would not have modified the Guidash patent in the manner proposed by Petitioner because “the gain would be insignificant and would not outweigh the problems associated with doing so.” PO Resp. 44. Patent Owner first takes issue with Mr. Guidash’s opinion that a skilled artisan would have used technology with different design rules to implement a pixel layout in which the fourth contact hole is moved into alignment with the second and third contact holes. PO Resp.

39–41. In particular, Patent Owner argues that Mr. Guidash’s reliance on the Mead & Conway treatise (Ex. 1005) is misplaced because it describes technology that was 20 years old at the time the ’493 patent was filed. *Id.* at 40–41. Patent Owner, relying on Dr. Afromowitz’s testimony, argues that reliance on this technology “would have undoubtedly resulted in a device that was far larger than one fabricated in 2003 when the ’493 patent was filed.” *Id.* at 41 (citing Ex. 2003 ¶ 91). Dr. Afromowitz repeats this argument in his testimony but does not state the basis for his opinion. Ex. 2003 ¶ 91.

In reply, Petitioner argues that Dr. Afromowitz’s testimony should be discounted because, in deposition, he testified that he did not know whether fabrication facilities allowed metal-to-poly contacts in the relevant timeframe or whether that technique is possible today. Reply 27 (citing Ex. 1015, 93:23–94:6, 97:18–23). Petitioner argues that Dr. Afromowitz further undermined his testimony by submitting an exhibit at paragraph 53 of his Declaration (in supporting the construction of an unrelated term) that shows such metal-to-poly contacts. Reply 27–30 (discussing Ex. 2006).

Patent Owner argues that a skilled artisan would not have seen an advantage in moving the fourth contact hole of the Guidash patent to save space and increase fill factor, allowing the photodiode to receive more light; rather, Patent Owner argues, any small increase in fill factor would have been outweighed by problems arising from “any effort to stray away from a symmetrical rectangular shape” of a photodiode. PO Resp. 41–43. Patent Owner argues that such use of asymmetrical photodiodes “goes against the stated improvement in Guidash 665 over the prior art.” *Id.* at 43. Specifically, Patent Owner argues that the Guidash patent (Ex. 1003, 2:15–

18, 2:37–64) disparages such asymmetry. *Id.* at 42–44 (citing Ex. 2003 ¶ 86).

We have reviewed the portions of the Guidash patent cited by Patent Owner and agree with Petitioner (Reply 30) that they discuss problems associated with the asymmetrical location of photodiodes among cells rather than the asymmetrical or non-rectangular shapes of individual photodiodes. Ex. 1003, 2:15–17 (“Non identical *placement of the photodetector within each pixel* can lead to aliasing artifacts.”), 2:48–53 (“[T]here remains a need within the art to provide an alternative pixel architecture that has a large fill factor . . . and with *identical placement of the photodetector within each pixel.*”), 2:60–64 (“eliminating the need for . . . asymmetry of adjacent photodetector placements within the array of pixels”). Moreover, as Petitioner notes (Reply 30), Figure 4 of the Guidash patent shows non-rectangular asymmetrical photodiodes. Thus, Patent Owner’s argument, and Dr. Afromowitz’s testimony in support thereof, are contrary to the description in the Guidash patent and unpersuasive.

Patent Owner also argues that a lens system sitting over a pixel modified per Petitioner’s proposal would not have been able to focus light on the additional areas resulting from moving the fourth contact hole. PO Resp. 42–43. Patent Owner relies on Dr. Afromowitz, who essentially repeats the argument without stating the basis for his opinions. Ex. 2003 ¶ 86. As Petitioner points out (Reply 30), however, Dr. Afromowitz admitted during cross-examination that he does not know where a lens system would focus light in a photodiode. Ex. 1015, 87:20–88:20. This admission undermines the credibility of his testimony.

Petitioner’s proposed reasons to modify the design shown in the Guidash patent— increasing the fill factor and improving sensor performance by increasing the sensitivity and saturation signal of the sensor—have a rational underpinning. We have considered the competing expert testimony regarding whether it would have been possible to move the fourth contact hole of Figure 4 of the Guidash patent and whether, if done, it would have had disadvantages contrary to the teaching of the Guidash patent. Although, for the reasons given above, we do not find that the art is a “black art” to an artist with the requisite experience, it is complex enough where it is appropriate for us to give expert testimony careful consideration. *Centricut, LLC v. The Esab Group, Inc.*, 390 F.3d 1361, 1369–70 (Fed. Cir. 2004) (internal citation omitted) (“Expert testimony may be similarly important in patent cases involving complex technology such as this one. Where the field or art is complex, we have repeatedly approved the use of expert testimony to establish infringement. We have also noted that ‘typically’ expert testimony will be necessary in cases involving complex technology.”).

In general, as explained in Section II.B.1 above, we find that Mr. Guidash, due to his extensive experience in the relevant art, is in a much better position to testify as to the effects of modifying the layout of Figure 4 than is Dr. Afromowitz who has a relative lack of experience in the subject matter area of this proceeding. As to the testimony specific to this issue, Mr. Guidash has provided an example (Ex. 1005, Mead & Conway) to show that fabricators did allow gate channels to be made directly over the transistor channel. Dr. Afromowitz’s testimony, on the other hand, is based on a misreading of the Guidash patent and also admits to a lack of specific

knowledge as to where lenses focus light onto photodiodes in the systems at issue in this proceeding. We credit the testimony of Mr. Guidash and give it substantial weight. In contrast, we do not credit Dr. Afromowitz's testimony and give it little weight.

In sum, we find that a skilled artisan would have found it obvious to modify the system shown in Figure 4 of the Guidash patent to move the fourth contact hole into alignment with the second and third contact holes. The skilled artisan would have done so, in the context of a fabricator that allowed such placement, in order to increase the fill factor and improve sensor performance by increasing the sensitivity and saturation signal of the sensor. As explained in Section II.B.1 above, we find that a skilled artisan would have been familiar with various design rules used by different fabrication facilities, would have known how to make changes to a layout, and would have been able to predict the outcome of these changes. *See Ex. 1002 ¶ 47.* We find that a skilled artisan would have known how to move the fourth contact hole into alignment with the second and third contact holes, would have been able to predict the outcome of doing so, and would have had a reasonable expectation of success. So modified, we find that the Guidash patent teaches "the second, third and fourth contact holes are aligned substantially in a straight line," as recited in claim 1.

As explained above, the Guidash patent does not disclose "the first wire is disposed in approximately a straight line between the associated floating diffusion element and the gate electrode of the amplifier transistor, and the third contact hole and [t]he fourth contact hole are aligned in the column direction," as recited in claim 8. Petitioner incorporates its reasoning as to claim 1 for moving the fourth contact hole into alignment

with the third contact hole. Pet. 27. As to “the first wire is disposed in approximately a straight line between the associated floating diffusion element and the gate electrode of the amplifier transistor,” Petitioner notes that Figure 4 shows conductive interconnect layer 44 with a straight portion between FDa and source follower input signal transistor 21 (the amplifier transistor). *Id.* at 26. Petitioner argues that, if the fourth contact hole (at the gate of transistor 21) is moved, as Petitioner proposes above, conductive interconnect layer 44 would be approximately in a straight line for its entire length. *Id.* at 26–27. Patent Owner does not dispute Petitioner’s allegations for these limitations. For the reasons given for claim 1, above, we find that a skilled artisan would have found it obvious to modify the system shown in Figure 4 of the Guidash patent to move the fourth contact hole into alignment with the third contact hole in the column direction. We further find that, with this change, the first wire would be disposed in approximately a straight line between the floating diffusion FD and amplifier transistor 21. Accordingly, we find that the Guidash patent teaches these limitations of claim 8.

5. Conclusion of Obviousness

As explained above, the Guidash patent teaches each limitation of claims 1–3 and 6–9 except for the alignment of the contact holes recited in claims 1 and 8. Petitioner has introduced persuasive evidence that a skilled artisan would have had reasons to modify the design shown in Figure 4 of the Guidash patent to align the contact holes in the manner recited in claims 1 and 8. We have weighed the respective backgrounds and experiences of the parties’ expert witness and find that Petitioner’s expert witness,

Mr. Guidash, is more qualified to opine on the subject matter than Patent Owner's expert witness, Dr. Afromowitz. We also have analyzed the testimony of the respective experts and find that Mr. Guidash's testimony is more consistent with the other evidence in the record. Accordingly, we find Mr. Guidash's testimony more credible, as discussed in detail above. Patent Owner does not argue or introduce evidence of objective indicia of nonobviousness. In sum, upon consideration of all the evidence, we conclude that Petitioner has proved by a preponderance of the evidence that claims 1–3 and 6–9 would have been obvious over the Guidash patent.

III. CONCLUSION

Petitioner has demonstrated, by a preponderance of the evidence, that claims 1–3 and 6–9 are unpatentable over the Guidash patent.

IV. ORDER

For the reasons given, it is:

ORDERED, based on a preponderance of the evidence, that claims 1–3 and 6–9 are unpatentable; and

FURTHER ORDERED, because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2016-00938
Patent 7,944,493 B2

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