

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION,
Petitioner,

v.

COLLABO INNOVATIONS, INC.,
Patent Owner.

Case IPR2016-00939
Patent 7,944,493 B2

Before DAVID C. McKONE, GREGG I. ANDERSON, and
JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

McKONE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Sony Corporation (“Petitioner”) filed a Petition (Paper 2, “Pet.”) to institute an *inter partes* review of claims 10–22 of U.S. Patent No. 7,944,493 B2 (Ex. 1001, “the ’493 patent”). Collabo Innovations, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

Pursuant to 35 U.S.C. § 314, in our Institution Decision (Paper 7, “Dec.”), we instituted this proceeding as to claims 10–22.

Patent Owner filed a Patent Owner’s Response (Paper 12, “PO Resp.”), and Petitioner filed a Reply to the Patent Owner’s Response (Paper 15, “Reply”).

Petitioner relies on the Declaration of R. Michael Guidash (Ex. 1002, “Guidash Decl.”). Patent Owner relies on the Declaration of Martin Afromowitz, Ph.D. (Ex. 2003, “Afromowitz Decl.”).

An oral argument was held on July 11, 2017 (Paper 21, “Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of claims 10–22. Based on the record before us, Petitioner has demonstrated, by a preponderance of the evidence, that claims 10–22 of the ’493 patent are unpatentable.

The ’493 patent describes solid-state imaging devices used, for example, to capture images in a digital camera. The challenged claims recite specific transistor components in active regions and electrical contacts arranged in a certain way. Petitioner contends that three references, the Guidash patent, Sakurai, and Tanaka, each describe a solid-state imaging device with the same components arranged in the same way, and that any

aspects of the challenged claims not expressly described in those references would have been inferred by a skilled artisan implementing the designs with the most appropriate technology. Patent Owner argues that none of these references teaches an “active region” under Patent Owner’s construction of that term. For the reasons given below, we agree with Petitioner that the challenged claims would have been obvious over the Guidash patent, Sakurai, and Tanaka.

B. Related Matters

The parties indicate that the ’493 patent has been asserted in *Collabo Innovations, Inc. v. Sony Corp.*, Case No. 1-15-cv-01094 (D. Del.), and *Collabo Innovations, Inc. v. Omnivision Technologies, Inc.*, Case No. 1-16-cv-00197-UNA (D. Del.). Pet. 1; Paper 5, 1. Different claims of the ’493 patent are the subject of an additional *inter partes* review petition in IPR2016-00938. Pet. 1; Paper 5, 1.

C. Asserted Prior Art References

Petitioner relies on the following prior art:

Ex. 1003 (“Guidash patent”)	US 6,657,665 B1	Dec. 2, 2003
Ex. 1008 (“Sakurai”)	EP 0 926 738 A2	June 30, 1999
Ex. 1012 (“Tanaka”) ¹	H10-256520	Sept. 25, 1998

¹ Exhibit 1012 is a certified English translation of Exhibit 1011, a Japanese Publication of Unexamined Patent Application. Our citations are to Exhibit 1012. We note that Iida, rather than Tanaka, is the first named inventor. Nevertheless, Petitioner referred to this reference as “Tanaka” in the Petition, a convention Patent Owner followed in the Response. We follow that convention in this decision. Tr. 18:5–16.

D. The Instituted Grounds

We instituted a trial on the following grounds of unpatentability
(Dec. 39):

Reference	Basis	Claims Challenged
Guidash patent	§ 103(a)	10–12, 15, 17–19, and 22
Sakurai	§ 103(a)	10, 11, 15–18, and 22
Tanaka	§ 103(a)	10–15 and 17–22

E. The '493 Patent

The '493 patent describes metal-oxide semiconductor (“MOS”)-type² solid-state imaging devices to be used with equipment such as home video cameras, digital still cameras, and cameras incorporated in cellular phones. Ex. 1001, 1:15–19. Although the embodiments of the '493 patent include components typical in such solid-state imaging devices (e.g., photodiodes, floating diffusion layer sections, transfer gates, and reset, amplifier, and address transistors), as detailed in the patent’s Background of the Invention

² MOS-type transistors have three terminals: a “source,” “from which charge carrie[r]s flow into channel toward the drain”; a “drain,” “into which charge carriers flow from the source through the channel”; and a “gate,” which “controls the current between source and drain by a voltage applied to its terminal.” IEEE 100, *The Authoritative Dictionary of IEEE Standards Terms* 337, 476, 1074 (7th ed. 2000) (Ex. 3003); *see also* Ex. 1009, 103 (“**drain** In a *field-effect transistor* the connection to the *channel* which *majority carriers* enter on leaving the channel.”); 301 (“**source** Of a *field-effect transistor* the connection to the channel from which *majority carriers* enter the channel.”).

and shown in the prior art circuit diagram of Figure 9, the patent describes and claims particular physical layouts of those components. *Id.* at 1:20–3:12; Pet. 2–5; Prelim. Resp. 5–7. According to the '493 patent,

[i]n general, as the circuit size is smaller, yields of the circuit are improved more, thereby reducing the cost of the circuit. Therefore, laying out a circuit according to predetermined design rules is an important technical task in designing the semiconductor integrated circuit. However, as for a sensor in which photosensitive cells are each formed by three transistors, no specific layout of these photosensitive cells has been clearly known to public.

Ex. 1001, 3:15–23.

Figure 7, reproduced below, depicts one such layout:

FIG. 7

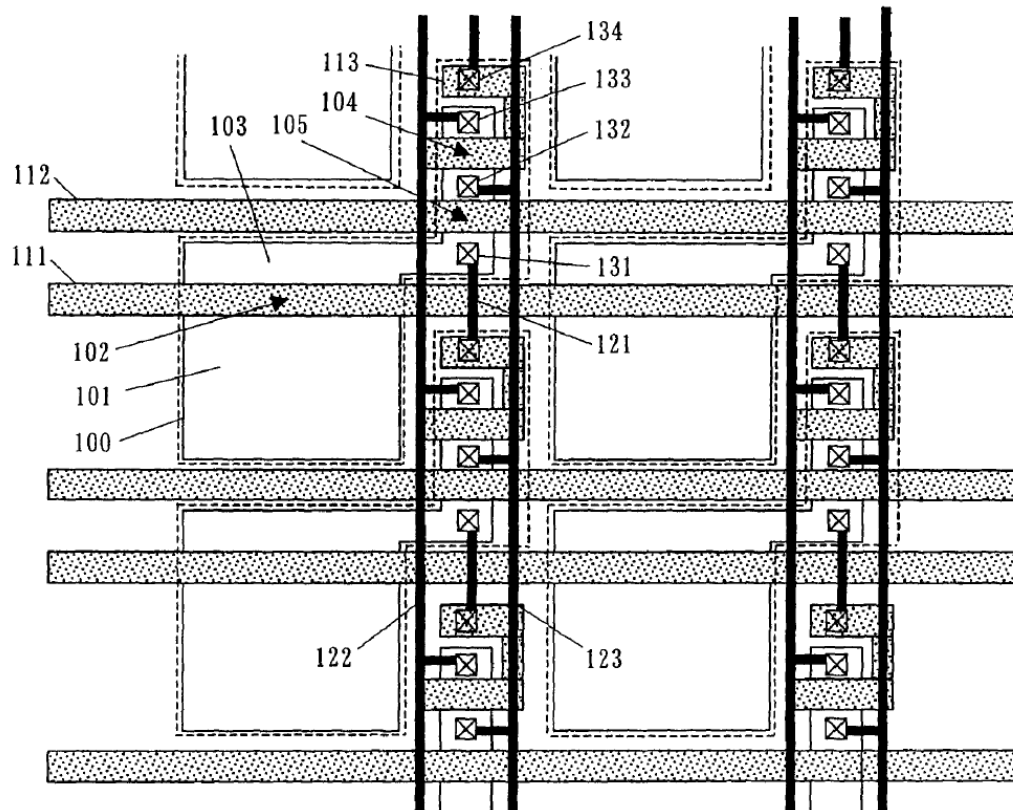


Figure 7 is a diagram illustrating two columns and two rows (out of many) of photosensitive cells of a layout pattern for a sensor. *Id.* at 5:37–38, 11:3–6; *see also id.* at 1:30–34 (“Note that, for the purpose of simplifying descriptions, it is assumed herein that the photosensitive cells are arranged in a 2×2 matrix. In practice, however, the photosensitive cells are arranged in a matrix with several tens to thousands of rows and columns.”). A particular cell includes active region 100. *Id.* at 11:5–6. At the three portions in which active region 100 and polysilicon wires 111, 112, and 113 overlap, transistors are formed. *Id.* at 11:6–9, 12–15. These include transfer gate 102 separating active region 100 into photodiode 101 and floating diffusion layer section 103. *Id.* at 11:19–25. Reset transistor 105 and amplifier transistor 104 also are included. *Id.* at 11:12–18.

In operation, the reset transistors are controlled by a vertical shift register to first reset the floating diffusion layer sections. *Id.* at 1:42–45. The amplifier transistors produce outputs on vertical signal lines. *Id.* at 1:45–49. The transfer gates are controlled by the vertical shift registers to transfer electric charges stored in the photodiodes to the floating diffusion layer sections, causing signal voltages corresponding to the electric charges to appear on the vertical signal lines. *Id.* at 1:52–59.

The components are further connected by metal wires 121–123 and contact holes 131–134. *Id.* at 12:33–36. Floating diffusion layer section 103 is connected to the gate of amplifier transistor 104 by contact hole 131 and metal wire 121. *Id.* at 12:36–39, 12:56–58. Contact hole 132 is provided on a common drain shared by amplifier transistor 104 and reset transistor 105, and connects the common drain to metal wire 123 (a power supply line). *Id.* at 12:39–42. Contact hole 133 connects the source of amplifier transistor

104 to metal wire 122 (a vertical signal line). *Id.* at 12:43–45. Contact hole 134 connects the gate of amplifier transistor 104 to the floating diffusion layer of the next cell in the up direction. *Id.* at 12:45–49. Inferring from the repetition in Figure 7, the unlabeled wire connected to contact hole 134 corresponds to a wire 121 of the cell immediately above and the unlabeled contact hole connected to wire 121 opposite that of contact hole 131 corresponds to a contact hole 134 connected to the gate of the amplifier transistor of the cell immediately below.

In the embodiment of Figure 7, contact holes 131–134 are aligned approximately in one straight line. *Id.* at 12:49–51. According to the '493 patent, “[t]his can reduce an area required for layout of these four contact holes. Therefore, it is possible to reduce the size of the laid-out photosensitive cells, thereby reducing the circuit size of the entire sensor.” *Id.* at 12:52–55.

Claims 10 and 17 are the only independent claims challenged in this proceeding. Claim 10, reproduced below, is illustrative of the claimed subject matter:

10. An imaging device formed in a semiconductor substrate, the imaging device comprising:
 - a plurality of photodiodes arranged in rows and columns, each photodiode for a given row of photodiodes formed in a corresponding active region of the semiconductor substrate;
 - a transfer gate disposed over the first active region so as to define an associated photodiode on one side of the transfer gate and an associated floating diffusion element on another side of the transfer gate;
 - an amplifier transistor;

- a reset transistor;
- a first wire electrically connecting the associated floating diffusion element to a gate electrode of the amplifier transistor;
- a first contact hole connected to a second wire disposed over the semiconductor substrate and being for receiving an output of a source of the amplifier transistor;
- a second contact hole connecting a drain of the reset transistor to a third wire disposed over the first semiconductor substrate; and
- a third contact hole connected to a source of the reset transistor,

wherein the first, second, and third contact holes are aligned substantially in a straight line.

Claim 17 is substantially similar to claim 10. The “first contact hole” and “second contact hole” limitations of claim 17 are phrased slightly differently than their counterparts in claim 10, but are not substantively different for purposes of this proceeding. Accordingly, we treat claim 10 as representative of the independent claims.

II. ANALYSIS

A. *Claim Construction*

We interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–45 (2016). In applying a broadest reasonable construction, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the

context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In the Institution Decision, we preliminarily construed the terms “active region,” appearing in independent claims 10 and 17, and “share a common drain,” appearing in dependent claims 15 and 22. Dec. 8–14. Patent Owner continues to contest both of these constructions, PO Resp. 15–37, while Petitioner contends that we should maintain them, Reply 7–20. We address the parties’ arguments as to “active region” below. Nevertheless, as to “share a common drain,” Patent Owner concedes that the Guidash patent teaches this limitation even under Patent Owner’s proposed construction. Tr. 32:18–33:3. Because we conclude that the Guidash patent teaches each limitation of claims 15 and 22, we do not reach whether Tanaka or Sakurai teach the limitations of claims 15 and 22. Accordingly, we need not revisit our construction of “share a common drain” to resolve the parties’ dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

As to “active region,” the dispute is whether an active region must have a boundary across which charges cannot flow. In our Institution Decision, we preliminarily construed “active region” to mean “a contiguous region of the substrate through which charges can flow and where components such as photodiodes, diffusion layers, and portions of transistors are formed.” Dec. 12. We rejected the construction Patent Owner proposed in the Preliminary Response, namely, “an area where active transistors, photodiodes, and/or diffusion layers are formed that is surrounded by a device insulation region.” *Id.* at 9 (quoting Prelim. Resp. 11). We reasoned

that the claims do not recite insulation as part of an active region and, indeed, the specification of the '493 patent describes an insulation region as a component separate from an active region. *Id.* at 10–11 (citing Ex. 1001, 3:64–4:1 (“In each photosensitive cell, the photodiode, the transfer transistor, the floating diffusion layer section, the amplifier transistor, and the reset transistor are formed in one active region surrounded by a device insulation region . . .”)). We concluded that reading an insulation region as part of the claimed active region would be importing an extraneous limitation into the claims improperly. *Id.* at 11 (citing *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988) (“By ‘extraneous,’ we mean a limitation read into a claim from the specification wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim. Where a specification does not require a limitation, that limitation should not be read from the specification into the claims.”)).

In its Response, Patent Owner argues that “active region” should be construed to mean “a contiguous region of the substrate through which charges can flow, having a boundary across which charges cannot flow, and where components such as photodiodes, diffusion layers, and portions of transistors are formed.” PO Resp. 37. Thus, Patent Owner would start with our construction and add to it “having a boundary across which charges cannot flow.” Based on Patent Owner’s response to questioning at the oral argument, it is unclear whether Patent Owner still contends that an active region includes an insulation region. Tr. 39:8–13 (“The insulation is the boundary of the active region, and which is reflected in the proposed construction, that it has a boundary. No, so, I wouldn’t say that the -- the

insulation region is part of the active region. It is certainly what forms the boundary of the active region.”), 39:18–21 (“[Y]ou don’t have to have an insulation region, necessarily, in those terms, but you need something that confines the charge because the active region is defined by the region in which the charge is confined.”), 40:5–8 (“We’re defining the ‘active region’ by what this attribute of an active region that is required for the charge to be confined. And within that, there has to be a boundary for the active region.”). As explained below, the only boundary Patent Owner considers sufficient is an insulation region.

In essence, Patent Owner argues that (1) the ’493 patent describes the active region of the invention as including an insulation region and (2) Dr. Afromowitz testifies that, to be usable, an active region must be maximally isolated from other regions and that, to achieve maximum isolation, an insulation region, in particular an oxide insulation, must be used.

Regarding the specification, the ’493 patent states in its Abstract that certain components “are formed in one active region surrounded by a *device isolation region*.” Ex. 1001, Abstract (emphasis added). In the Summary of the Invention section, the specification states that certain components “are formed in one active region surrounded by a *device insulation region*.” *Id.* at 3:64–4:1 (emphasis added). Later, in its Description of the Preferred Embodiment section, in describing the embodiment of Figure 4, the specification states that “active region 200 is surrounded by a *device isolation region* (not shown).” *Id.* at 8:56–57 (emphasis added). The remaining references to active regions in the specification do not mention either isolation or insulation.

Patent Owner argues that these references to “isolation” and “insulation” in the specification show that charge is confined in the active region. PO Resp. 27–28. Patent Owner argues that because the Summary of the Invention and the Abstract use “insulation” and “isolation” similarly, the patent uses those terms interchangeably. *Id.* at 28. Relying on the Afromowitz Declaration, Patent Owner contends that the specification uses both “insulation” and “isolation” to mean the more restrictive “insulation” rather than the broader “isolation”; in other words, “one having ordinary skill in the art would have understood from the specification that the claimed active regions are all isolated by an insulation region.” *Id.* at 29 (citing Ex. 2003 ¶ 33). Neither Patent Owner nor Dr. Afromowitz states why the more restrictive option is required.

In reply, Petitioner argues that the specification uses “active region” dozens of time and only once states that it is surrounded by a device insulation region. Reply 10. Petitioner further argues that the claims do not specify the character of the boundary of an active region and that the specification repeatedly refers to an active region without referring to what surrounds it. *Id.* As to the specific references to “insulation” and “isolation,” Petitioner argues that they reinforce our preliminary construction because they expressly describe insulation and isolation regions as being separate from the active regions. *Id.* at 10–11.

We agree with Petitioner. The challenged claims recite an “active region” without a recitation of an isolation region or an insulation region. Thus, the plain language of the claims does not require an insulation region serving as a border for an active region. As to the specification, it merely describes a device isolation region, specifically not shown, as an example

region surrounding an active region of the preferred embodiment, but does not indicate that an isolation region is a part of an active region or necessarily accompanies an isolation region. Ex. 1001, 8:56–58. We are not persuaded that the '493 patent's one reference to "insulation" redefines active region or narrows the term "isolation" used elsewhere in the specification. We maintain our conclusion (Dec. 11) that reading an insulation region as part of the claimed active region (or necessarily accompanying an active region) based on the disclosure in the specification would be importing an extraneous limitation into the claims improperly. *See E.I. du Pont de Nemours*, 849 F.2d at 1433.

As noted above, Patent Owner also relies on the testimony of Dr. Afromowitz to provide technical reasons why an active region must have a border, such as an insulation region, across which charge cannot flow. Patent Owner contends that "[i]n order to serve its function in the imaging device, the active region must be insulated/isolated from other regions of the chip." PO Resp. 30 (citing Ex. 2003 ¶ 35). Patent Owner again ties this to an insulation region, arguing that, "[i]n the context of MOS image sensor devices, this means that a dielectric, or non-conducting material or barrier is used to prevent the flow of an electric current under the influence of an electric field or a voltage difference." *Id.* (citing Ex. 2003 ¶ 34). In his testimony, Dr. Afromowitz relies on the American Heritage Dictionary to conclude that "isolation" implies being apart or separate, that "insulate" means to prevent the passage of electricity, and, therefore, "an active region as envisioned by the inventor is a region that, by its intrinsic nature, is maximally isolated from other regions and in addition prevents, to the greatest possible degree, electric current from entering or leaving contiguous

regions of the substrate.” Ex. 2003 ¶ 34 (citing Ex. 2012). Dr. Afromowitz does not explain how the dictionary definitions he relies upon support his conclusion with respect to the term “active region.” We find that the dictionary definitions do not adequately support Dr. Afromowitz’s testimony, that his conclusions do not logically follow from this evidence, and, therefore, that his testimony is not credible on this point.

Again relying on Dr. Afromowitz, and additionally on treatises, Patent Owner argues that it was known in the art that “the active region is usually physically defined by the isolation material surrounding it.” PO Resp. 30–32 (citing Ex. 2003 ¶ 36; Ex. 2009; Ming Bo Lin, *Introduction to VLSI Systems: A Logic, Circuit, and System Perspective*, 203–04 (2012) (not introduced as an exhibit)). According to Dr. Afromowitz,

a person of ordinary skill in the art understands that this term of art applies to specifically bounded regions of the device across whose boundary charges cannot flow. The boundary is physically exhibited, at least, as an area where charge is confined. If the construction permits charge flow across the boundary, then an essential feature of the active region is missing, and the construction would be in contradiction to the purpose of the active region.

Ex. 2003 ¶ 36. Dr. Afromowitz does not cite to or explain the bases for this testimony. We find this testimony to be conclusory and unpersuasive and, accordingly, give it little weight. See 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

As to the cited treatises, Patent Owner concedes that “[a] person of ordinary skill in this field would know that there are different methods that have been used to isolate active regions of a semiconductor device,” but

argues that only insulation, such as the use of dielectric materials or oxide described in Exhibit 2009, is consistent with the use of “active region” in the ’493 patent. PO Resp. 32–33 (citing Ex. 2003 ¶ 37). Patent Owner argues that other forms of isolation, such as p/n junction isolation (purportedly used in the prior art), are not consistent with the active regions of the patent, because they would result in charge being leaked away from the photodetectors, “making the device unusable for all practical purposes.” *Id.* at 33–34 (citing Ex. 2003 ¶¶ 37–39). Dr. Afromowitz repeats these arguments in his testimony, but, once again, does not state the bases for these opinions. Ex. 2003 ¶¶ 37–39. In particular, Dr. Afromowitz does not explain how Patent Owner’s cited treatises (Ex. 2009; Ex. 2010; Lin) support his conclusions. Moreover, as Petitioner points out (Reply 14), Dr. Afromowitz admitted on cross-examination that prior art active regions were isolated by p/n junctions and that he did not know whether, at the time of the invention, such p/n junction isolation was more or less common than the insulation his Declaration states was necessary to make a device that was not unusable. Ex. 1015, 57:2–58:17. In light of the lack of supporting factual bases for the conclusory opinion in his Declaration and his cross-examination testimony indicating a lack of knowledge in the subject matter area, we find Dr. Afromowitz’s testimony on this point to lack credibility. Accordingly, we give it little weight.

Moreover, we have reviewed Patent Owner’s extrinsic evidence and find that it does not support Patent Owner’s conclusion that isolation regions other than insulation regions (including p/n junction isolation) are inconsistent with the ’493 patent’s teachings or that such isolation would have rendered devices unusable. To the contrary, as Petitioner argues

(Reply 12–14), these extrinsic references show that it was known to use active regions with isolation regions other than dielectric and oxide insulation. This further undermines Dr. Afromowitz’s testimony that such isolation would have rendered devices unusable.

In sum, the claim language itself does not restrict “active region” to a region bounded by insulation, maximally isolated, or otherwise including a boundary across which charges cannot flow.³ Likewise, the ’493 patent’s reference to a device insulation region is, at best, a non-limiting example of a device isolation region described as part of the patent’s preferred embodiment. We see no indication that this reference is a lexicographic definition or statement of disavowal. We have considered Patent Owner’s extrinsic evidence but find it unpersuasive. Patent Owner’s treatises support Petitioner’s position that active regions were known in the art with or without insulation regions. Patent Owner’s expert declaration is contradicted by the language of the claims, the specification, Patent Owner’s treatises, and the witness’s own cross-examination testimony. Thus, it is entitled to little weight. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (en banc) (internal quotation marks and citation omitted) (“[C]onclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court. Similarly, a court should discount any expert testimony that is clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent.”).

³ We note that Patent Owner was unable to quantify the effectiveness of an insulation that provides maximal isolation. Tr. 45:1–19.

On the complete record, we maintain our construction of “active region,” namely, “a contiguous region of the substrate through which charges can flow and where components such as photodiodes, diffusion layers, and portions of transistors are formed.”

B. Alleged Obviousness of Claims 10–12, 15, 17–19, and 22 over the Guidash Patent

Petitioner contends that claims 10–12, 15, 17–19, and 22 would have been obvious over the Guidash patent. Pet. 30–38, 40–43.

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are “such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” We resolve the question of obviousness on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.⁴ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In an obviousness analysis, some reason must be shown as to why a person of ordinary skill would have combined or modified the prior art to achieve the patented invention. *See Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008). A reason to combine or modify the prior art may be found explicitly or implicitly in market forces; design incentives;

⁴ The record does not include arguments or evidence regarding objective indicia of nonobviousness.

the “interrelated teachings of multiple patents”; “any need or problem known in the field of endeavor at the time of invention and addressed by the patent”; and the background knowledge, creativity, and common sense of the person of ordinary skill. *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1328–29 (Fed. Cir. 2009) (quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–21 (2007)).

1. Level of Ordinary Skill

Petitioner does not state in the Petition its contention as to the level of ordinary skill in the art. Rather, Petitioner states that it is discussed in the Guidash Declaration. Pet. 11. Mr. Guidash testifies that a skilled artisan would have had “a Bachelor’s degree in electrical engineering, physics, or material science and approximately 3–5 years of industrial experience or equivalent research or teaching experience, or a Master’s degree in the same fields and 1–3 years of industrial experience or equivalent research or teaching experience in the field of semiconductor image sensor design and fabrication.” Ex. 1002 ¶ 45. Patent Owner argues that Petitioner did not reproduce Mr. Guidash’s opinion in the Petition. PO Resp. 58–59.

Nevertheless, Patent Owner does not provide a statement of the level of skill in the art and, when asked at the oral hearing, confirmed that it does not dispute Mr. Guidash’s opinion. Tr. 36:18–37:10. In any case, Mr. Guidash’s opinion as to the state of the art is consistent with the level of skill indicated by the prior art of record in this proceeding—namely the Guidash patent, Sakurai, and Tanaka. See *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Patent Owner makes several arguments to the effect that the art is unpredictable and that changing a circuit layout would have introduced undesirable and unpredictable consequences. PO Resp. 6–9. *See also id.* at 37 (“Analog integrated circuit design in general, and image sensor pixel circuit design and layout has always been regarded as something of a black art.”), 38 (“Because of the susceptibility of a circuit’s performance to small changes in the layout of that circuit and because the design rules are vast and complex, making any change to an analog circuit’s layout can have severe ramifications on the functioning of that circuit.”). Patent Owner argues that “[i]n many instances throughout the Petition, Petitioner’s expert opines that ‘it would have been obvious’ to move certain contact holes, wires, etc. in order arrive at some supposed benefit” and that “these arguments are disingenuous and misleading.” *Id.* at 38. Nevertheless, in this proceeding, Petitioner does not argue that a skilled artisan would have needed to move contact holes, wires, etc., to arrive at the challenged claims.⁵ Thus, we need not address Patent Owner’s contentions regarding the predictability of the art to resolve the parties’ dispute in this proceeding.

2. Scope and Content of the Prior Art - Overview of the Guidash Patent

The Guidash patent describes solid-state image sensors having a plurality of pixels arranged in a series of rows and columns. Ex. 1003, Abstract, 1:7–13. Figure 4, reproduced below, illustrates an example.

⁵ The parties do raise the issue of the predictability of moving contact holes and wires in the related proceeding, IPR2016-00938.

Fig.4

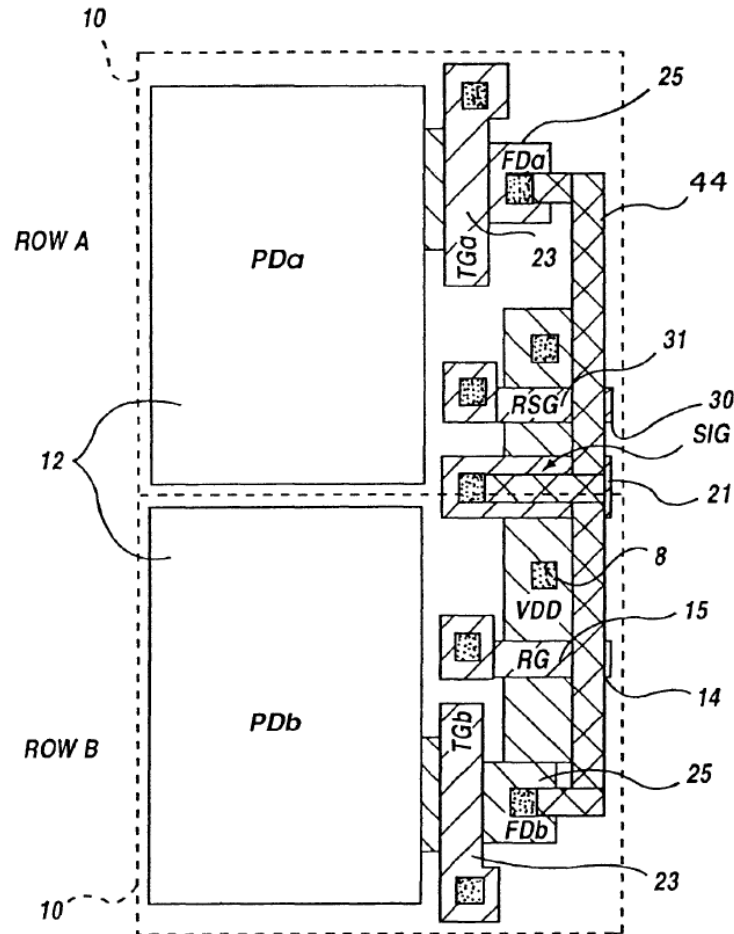


Figure 4 is a top view of two row-adjacent pixels, showing how the two physically separate floating diffusions in each pixel are interconnected to each other and to a source follower input transistor. *Id.* at 3:48–56.

Pixel 10 includes photodiode photodetectors 12 and floating diffusions 25 separated by transfer gates 23. *Id.* at 3:57–58. Floating diffusions 25 are physically and spatially isolated from each other and are electrically connected to one another, and to the gate of source follower input signal transistor 21, by conductive interconnect layer 44. *Id.* at 3:65–

4:4. Both source follower input transistor 21 and reset transistor 14 are connected to voltage supply 8 (“VDD”). *Id.* at 3:60–62.

3. *Comparison of the Guidash patent claims 10–12, 15, 17–19, and 22; differences between the challenged claims and the Guidash patent*

Petitioner contends that most of the limitations of the challenged claims are expressly disclosed in the Guidash patent. For those limitations not disclosed expressly, Petitioner relies on testimony from Mr. Guidash that a skilled artisan would have inferred those limitations based on the type of technology the artisan would have found most appropriate to use.

Regarding claim 10, Petitioner contends that the Guidash patent teaches an imaging device formed in a semiconductor substrate, comprising a plurality of photodiodes arranged in rows and columns, citing to the Abstract of the Guidash patent. Pet. 31 (citing Ex. 1003, Abstract (“An image sensor having a plurality of pixels arranged in a series of row and columns comprising a semiconductor substrate”)). Based on this evidence, we agree.

Petitioner contends that photodiode PDa and floating diffusion FDa (shown in Figure 4, reproduced above), together, constitute an “active region of the semiconductor substrate.” Pet. 31–32. Similarly, Petitioner contends that photodiode PDb and floating diffusion FDb, together, constitute another active region physically separated from the other active region by isolating regions. *Id.* at 32. We agree that the Guidash patent describes two contiguous regions over which charge can flow (PDa + FDa and PDb + FDb), each at least isolated from the other. For example, the Guidash patent explains that “[i]n FIG. 4 the floating diffusions 25, are physically and

spatially isolated from each other and are electrically connected to each other and the source follower input transistor 21 by means of a conductive interconnect layer 44.” Ex. 1003, 3:67–4:4; *see also id.* at 4:7–13 (“Floating diffusion 25, FDa, while on the same electrical node as floating diffusion FDb, is spatially isolated from floating diffusion 25 FDb. Therefore, floating diffusion 25 FDa while on the same electrical node as, floating diffusion 25 FDb, does not serve as the source 16 for the reset transistor 14, while floating diffusion FDb does serve as the source 16 of the reset transistor 14.”).

Patent Owner contends that the Guidash patent does not teach active regions because Petitioner has not shown anything in the Guidash patent that would indicate an active region having a boundary across which charges cannot flow. PO Resp. 45–46. Rather, Patent Owner argues, “Petitioner fails to identify an insulated active region, and fails to show the rational underpinning required to show obviousness.” *Id.* at 46. Patent Owner further contends that “Guidash 665 discloses that these regions are *spatially* separated” and that “[a] person having ordinary skill in the art would have understood that a spatial separation does not mean that charges cannot flow out of the boundary of the region.” *Id.* at 45–46 (citing Ex. 1003, 3:63–67, 4:7–9). Although the Guidash patent states that the two regions depicted in Figure 4 are “physically and spatially isolated from each other,” Ex. 1003, 4:1–2, we need not determine whether such physical separation in addition to spatial separation indicates an insulation region. Rather, as explained in Section II.A above, an “active region” is “a contiguous region of the substrate through which charges can flow and where components such as photodiodes, diffusion layers, and portions of transistors are formed,” and

need not (a) be maximally isolated, (b) include an insulation region, or (c) include a boundary over which charge cannot pass. Under our construction, we find that PDa and FDa, together, are an active region and that PDb and FDb, together, are another active region.

Petitioner further contends that transfer gate TGa is disposed over the active region of PDa and FDa and defines a photodiode (PDa) on one side and an associated floating diffusion element (FDa) on the other. Pet. 32–33. We agree that this is shown in Figure 4 of the Guidash patent, reproduced above. Thus, we find that the Guidash patent teaches “a transfer gate disposed over the first active region so as to define an associated photodiode on one side of the transfer gate and an associated floating diffusion element on another side of the transfer gate,” as recited in claim 10.

Petitioner identifies source follower transistor 21 and reset transistor 14, both formed on floating diffusion FDb, respectively as an “amplifier transistor” and “reset transistor,” as recited in claim 10. *Id.* at 33. Mr. Guidash testifies that source follower transistor 21 is an amplifier transistor. Ex. 1002 ¶ 80. We credit this testimony, which is undisputed. We find that the Guidash patent teaches “an amplifier transistor” and “a reset transistor,” as recited in claim 10.

As shown in Figure 4 of the Guidash patent, conductive interconnect layer 44 connects floating diffusion FDa to the gate electrode of source follower input signal transistor 21 (the amplifier transistor). Pet. 33–34. As noted above, the Guidash patent explains that “[i]n FIG. 4 the floating diffusions 25, are physically and spatially isolated from each other and are electrically connected to each other and the source follower input transistor 21 by means of a *conductive interconnect layer 44.*” Ex. 1003, 3:67–4:4

(emphasis added). We find that the conductive interconnect layer 44 of the Guidash patent is “a first wire electrically connecting the associated floating diffusion element to a gate electrode of the amplifier transistor,” as recited in claim 10.

Petitioner identifies, in Figure 4, the square contact above the designation “RSG” as “a first contact hole,” as recited in claim 10. Pet. 34–35. Mr. Guidash testifies that, when row select transistor 31 (labeled RSG) is on, and thus short-circuited, the identified contact hole is for “receiving an output of a source of the amplifier transistor,” as recited in claim 10.

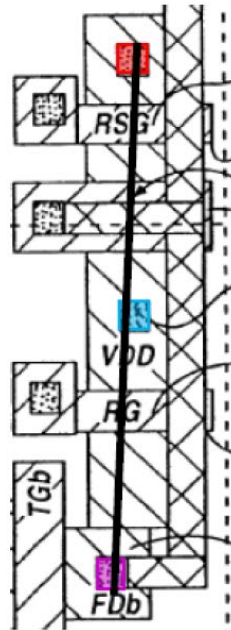
Ex. 1002 ¶ 228. Mr. Guidash also testifies that contact holes are used to connect between an active region and a layer above, that the source of amplifier transistor 21 is the output value of the pixel, and, therefore, it would have been obvious that the output of amplifier transistor 21, the first contact hole, would be connected to a wire so that that the output could be transferred and stored as part of a digital image. *Id.* ¶ 229. We credit this testimony, which is undisputed. Accordingly, we find that the Guidash patent teaches “a first contact hole connected to a second wire disposed over the semiconductor substrate and being for receiving an output of a source of the amplifier transistor,” as recited in claim 10.

Petitioner identifies, in Figure 4, the square contact labeled VDD (voltage supply 8) as a “second contact hole,” as recited in claim 10, connecting the drain of reset transistor 14 to a third wire disposed over the semiconductor substrate. Pet. 35–36. The Guidash patent does not specify whether the transistors of Figure 4 are NMOS or PMOS transistors. Nevertheless, relying on other examples in the Guidash patent, Mr. Guidash testifies that NMOS transistors would have been the obvious choice. *Id.* at

36 (citing Ex. 1002 ¶ 230). If NMOS technology is used, Petitioner argues, electrons in reset transistor 14 would flow toward VDD, making it the drain. *Id.* (citing Ex. 1002 ¶ 230). Mr. Guidash further testifies that it would have been obvious to deliver VDD using a conductor in the metal layer, which Petitioner argues would be a “third wire,” as recited in claim 10. *Id.* (citing Ex. 1002 ¶ 230). We credit Mr. Guidash’s testimony, which is undisputed. Accordingly, we find that the Guidash patent teaches “a second contact hole connecting a drain of the reset transistor to a third wire disposed over the first semiconductor substrate,” as recited in claim 10.

Petitioner identifies the dark square shown directly above the label FDb in Figure 4 as a “third contact hole,” as recited in claim 10. Pet. 36–37. Mr. Guidash testifies that the source of reset transistor 14 is at floating diffusion element FDb. Ex. 1002 ¶ 231. We credit this testimony, which is undisputed. Accordingly, we find that the Guidash patent teaches “a third contact hole connected to a source of the reset transistor,” as recited in claim 10.

Petitioner submits an annotation of Figure 4, reproduced below, showing the identified first, second, and third contact holes substantially in alignment. Pet. 37.



Petitioner's annotated Figure 4 shows the first contact hole in red, the second contact hole in blue, and the third contact hole in purple, along with a straight black line connecting the three contact holes. *Id.* We agree that these holes are substantially in alignment. Accordingly, we find that the Guidash patent teaches "wherein the first, second, and third contact holes are aligned substantially in a straight line," as recited in claim 10.

In sum, we find that the Guidash patent, in light of the knowledge of a skilled artisan as explained by Mr. Guidash, teaches each limitation of claim 10. We have considered Patent Owner's argument that the Guidash patent does not teach active regions, but find that argument unpersuasive for the reasons given above. Patent Owner does not contest that the Guidash patent teaches the other limitations of claim 10.

As explained above, claim 17 is substantially similar to claim 10 and we treat claim 10 as representative. Petitioner incorporates its argument and evidence for claim 10 as to its allegations for claim 17. Pet. 41–43. Patent Owner also argues claims 10 and 17 together. PO Resp. 44. For the reasons

given for claim 10, we find that the Guidash patent teaches each limitation of claim 17.

Claims 11 and 12 depend from claim 10 and claims 18 and 19 depend from claim 17. Claims 11 and 18 each recite that “the first wire includes a straight portion disposed in the column direction” and claims 12 and 19 each recite that “the first wire includes a portion disposed in a direction traversing column direction.” We find that Figure 4 of the Guidash patent shows such portions of conductive interconnect layer 44, the alleged “first wire,” with portions of conductive interconnect layer 44 running from left to right and a portion running up to down. Thus, we find that the Guidash patent teaches the additional limitations of claims 11, 12, 18, and 19.

Claim 15 depends from claim 10. Claim 22 depends from claim 17. Both claims 15 and 22 recite “wherein the amplifier transistor and the reset transistor share a common drain.” Petitioner argues that, as shown in Figure 4, both source follower input signal transistor 21 and reset transistor 14 share VDD as their drain. Pet. 40. Specifically, Petitioner argues that, because transistor 21 is described as a source-follower type, VDD 8 is the drain and the output side facing the row-select transistor RSG is the source. *Id.* We find that Figure 4 shows that VDD 8 is in a portion of the active region physically shared by both the reset transistor 14 and the source follower input signal transistor 21. Thus, we find that the reset transistor and amplifier transistor shown in Figure 4 share a common drain. Patent Owner concedes that the Guidash patent teaches the additional limitation of claims 15 and 22. Tr. 32:18–33:3.

4. Conclusion of Obviousness

As explained above, in light of the knowledge of a skilled artisan as explained by Mr. Guidash, the Guidash patent teaches each limitation of claims 10–12, 15, 17–19, and 22. Mr. Guidash has provided undisputed testimony that it would have been obvious to implement Figure 4 of the Guidash patent using NMOS technology and that, when such technology is used, any limitations not expressly disclosed by the Guidash patent would have been obvious. Patent Owner does not argue or introduce evidence of objective indicia of nonobviousness. Upon consideration of all the evidence, we conclude that Petitioner has proved by a preponderance of the evidence that claims 10–12, 15, 17–19, and 22 would have been obvious over the Guidash patent.

C. Alleged Obviousness of Claims 10 and 16 over Sakurai

Petitioner contends that claims 10, 11, 15–18, and 22 would have been obvious over Sakurai. Pet. 12–30. Nevertheless, because we conclude that claims 10, 11, 15, 17, 18, and 22 would have been obvious over the Guidash patent, we do not reach whether those claims also would have been obvious over Sakurai, other than to evaluate independent claim 10, from which claim 16 depends. We determine below that claims 10 and 16 would have been obvious over Sakurai.

1. Scope and Content of the Prior Art - Overview of Sakurai

Sakurai describes techniques, including specific layouts, for optimizing the layout of a pixel portion of a solid-state image pickup device.

Ex. 1008, Abstract. Sakurai provides an outline of the components of such a device:

As shown in Fig. 1, one pixel has a photodiode portion PD, a transfer switch MS11 for transferring signal charges from the photodiode portion PD, an amplifier means MS14 for amplifying the transferred signal and outputting it, a selection switch MS13 for selecting the pixel, and a reset switch MS12 for clearing the remaining signal charges and resetting them to a potential VR. Signals ϕ_{TX} , ϕ_{RES} , and ϕ_{SEL} are used to control the transfer switch MS11, reset switch MS12, and selection switch MS13, respectively.

Id. ¶ 5.

Figure 5, reproduced below, illustrates a specific layout:

FIG. 5

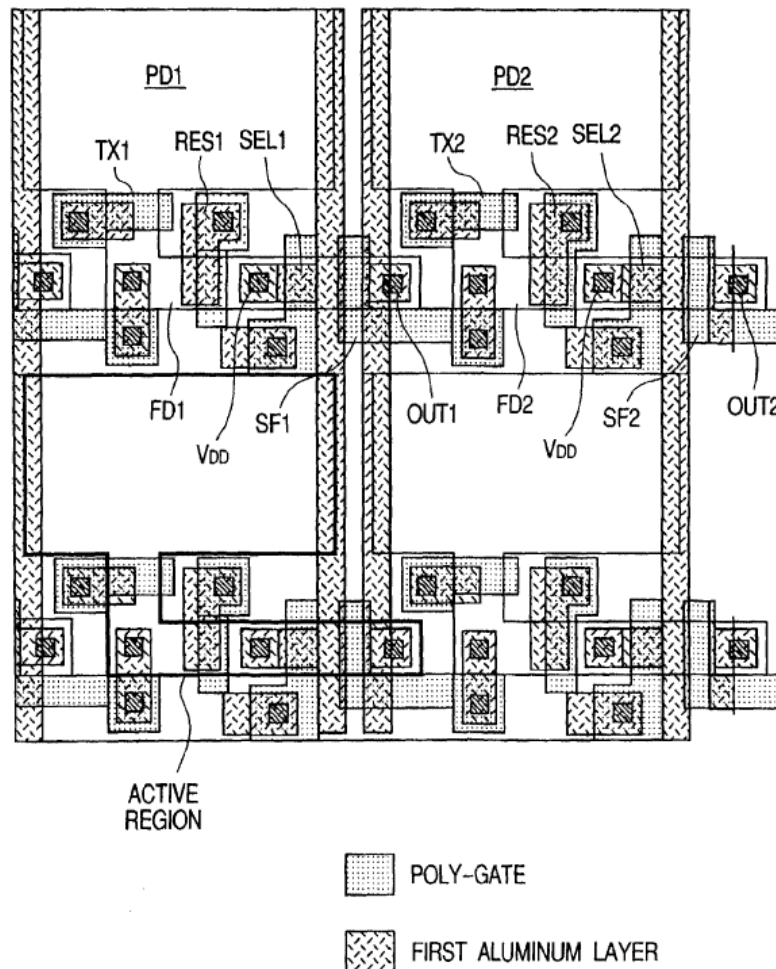


Figure 5 is a diagram of a layout of a solid-state image pickup device.

Id. ¶ 14 (col. 3, ll. 34–36).

Transfer switch TX2, floating diffusion FD2, reset switch RES2, selection switch SEL2, amplifier means SF2, and output portion OUT2 surround photodiode portion PD2. *Id.* ¶ 27. An active region for an unlabeled photodiode in the lower-left quadrant of Figure 5 is indicated by a bold line. *Id.* We note similar active regions for PD1, PD2, and the

unlabeled photodiode adjacent to the bolded active region in the lower-right quadrant of Figure 5. A signal from photodiode portion PD2 is output through amplifier means SF1 and output portion OUT1 arranged on the side of photodiode portion PD1. *Id.* ¶ 28. Floating diffusion FD2 and amplifier means SF1 are connected using a polysilicon layer and a first aluminum layer. *Id.* Amplifier means SF1 and output portion OUT1 are formed in the same active region as that of photodiode portion PD1. *Id.*

2. Comparison of Sakurai to claims 10 and 16; differences between claims 10 and 16 and Sakurai

Petitioner contends that most of the limitations of the challenged claims are expressly disclosed in Sakurai. For those limitations not disclosed expressly, Petitioner relies on testimony from Mr. Guidash that a skilled artisan would have inferred those limitations based on the type of technology the artisan would have found most appropriate to use.

Claim 16 depends from claim 10. Regarding claim 10, Petitioner contends that Figure 5 of Sakurai illustrates a plurality (four) of photodiodes (e.g., PD1 and PD2) arranged in rows and columns (two rows and two columns). Pet. 13. We agree, and find that Sakurai teaches “[a]n imaging device formed in a semiconductor substrate,” with “a plurality of photodiodes arranged in rows and columns,” as recited in claim 10.

Petitioner contends that each photodiode is formed in a corresponding active region, citing to Figure 5’s express description of an “ACTIVE REGION.” *Id.* at 14. Sakurai explains that “[a] region indicated by a bold line in Fig. 5 is an active region” and that “[t]he amplifier means SF1 and

output portion OUT1 are formed in the same active region as that of the photodiode portion PD1.” Ex. 1008 ¶¶ 27–28.

Patent Owner argues that Sakurai does not describe the characteristics of the regions it terms active regions and, thus, does not specify whether those regions confine charge. PO Resp. 51. Rather, Patent Owner argues, “Sakurai is simply silent as to what it is other than being identified as a bold line.” *Id.* at 51–52. We disagree. As explained in Section II.A above, an “active region” is “a contiguous region of the substrate through which charges can flow and where components such as photodiodes, diffusion layers, and portions of transistors are formed,” and need not be maximally isolated, include an insulation region, or include a boundary over which charge cannot pass. As shown in Figure 5, PD1 and FD1 together is a contiguous region of the substrate through which charges can flow and where a photodiode (PD1), a diffusion layer (FD1), and portions of transistors (TX1) are formed. Similarly, PD2 and FD2, together, is a contiguous region of the substrate through which charges can flow and where a photodiode (PD2), a diffusion layer (FD2), and portions of transistors (TX2) are formed. Accordingly, we find that Sakurai teaches “each photodiode for a given row of photodiodes formed in a corresponding active region of the semiconductor substrate,” as recited in claim 10.

Petitioner contends that Sakurai’s transfer switch TX2 is a transfer gate disposed over the active region of photodiode PD2 and floating diffusion FD2. Pet. 14–15. We agree, and find that Sakurai teaches “a transfer gate disposed over the first active region so as to define an associated photodiode on one side of the transfer gate and an associated

floating diffusion element on another side of the transfer gate,” as recited in claim 10.

Petitioner points to Sakurai’s amplifier means SF1 or SF2 and reset switch RES1 or RES2 as “an amplifier transistor” and “a reset transistor,” respectively, as recited in claim 10. Pet. 15–16. Relying on Mr. Guidash’s testimony, Petitioner contends that these components are transistors because they are formed by polysilicon gate material crossing an active region. *Id.* at 16 (citing Ex. 1002 ¶¶ 197–198). We credit this testimony, which is undisputed. We find that Sakurai teaches “an amplifier transistor” and “a reset transistor,” as recited in claim 10.

Sakurai states that “the floating diffusion FD2 on the photodiode portion PD2 side and the amplifier means SF1 on the photodiode portion PD1 side are connected using a polysilicon layer and a first aluminum layer.” Ex. 1008 ¶ 28. We agree with Petitioner (Pet. 16–17) that this teaches “a first wire electrically connecting the associated floating diffusion element to a gate electrode of the amplifier transistor,” as recited in claim 10.

Petitioner further contends that the square labeled OUT1 in Figure 5 is “a first contact hole” and that the vertical aluminum layer crossing it is “a second wire disposed over the semiconductor substrate” that receives an output of a source (OUT1) of the amplifier transistor (SF1). *Id.* at 17–19. Relying on the testimony of Mr. Guidash, Petitioner argues that it would have been obvious to implement Figure 5 using NMOS transistors and, in that instance, because amplifier transistor SF1 is configured in a source-follower arrangement, OUT1 is the source of the amplifier transistor and the opposite side of SF1, connected to V_{DD} , is the drain. *Id.* at 18 (citing

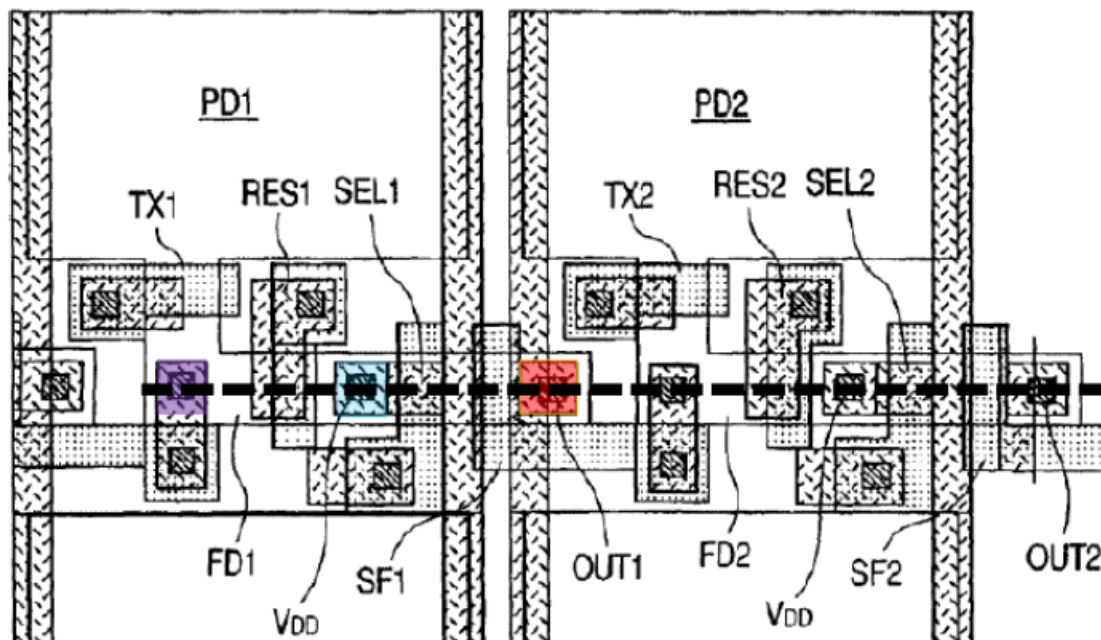
Ex. 1002 ¶ 201). Again relying on Mr. Guidash, Petitioner argues that, because the source of amplifier transistor SF1 is the output value of the pixel, and the output value would be connected to a wire to transfer and store the value as part of a digital image, the vertical aluminum wire overlapping OUT1 is obviously connected to a contact hole to receive the output of SF1. *Id.* at 18–19 (citing Ex. 1002 ¶ 202). We credit Mr. Guidash’s testimony, which is undisputed. Accordingly, we find that Sakurai teaches “a first contact hole connected to a second wire disposed over the semiconductor substrate and being for receiving an output of a source of the amplifier transistor,” as recited in claim 10.

Petitioner points to Sakurai’s square box labeled V_{DD} as “a second contact hole” connecting a drain of reset transistor RES1 to a portion of the aluminum layer, which Petitioner contends is “a third wire,” as recited in claim 10. *Id.* at 19–20. Relying on Mr. Guidash’s testimony, Petitioner argues that reset transistor RES1 is obviously an NMOS transistor and, because V_{DD} is a power supply, electrons flow out of reset transistor RES1 toward V_{DD}. *Id.* at 19 (citing Ex. 1002 ¶ 203). Thus, Petitioner argues, V_{DD} is the drain of reset transistor RES1. *Id.* at 19–20. We credit Mr. Guidash’s testimony, which is undisputed. Accordingly, we find that Sakurai teaches “a second contact hole connecting a drain of the reset transistor to a third wire disposed over the first semiconductor substrate,” as recited in claim 10.

Petitioner identifies the square box depicted directly under transfer switch TX1 in Figure 5 as “a third contact hole connected to a source of” reset transistor RS1, as recited in claim 10. *Id.* at 20. This contact hole is on the opposite side of reset transistor RS1 from V_{DD}, the drain (as explained above). Thus, it is the source. Accordingly, we find that Sakurai teaches “a

third contact hole connected to a source of the reset transistor,” as recited in claim 10.

Petitioner provides an annotation of a portion of Sakurai’s Figure 5 (reproduced below) to show the alignment of the first, second, and third contact holes. Pet. 20–21.



Petitioner’s annotated Figure 5 shows the first contact hole in red, the second contact hole in blue, and the third contact hole in purple, along with a straight black dotted line connecting the three contact holes. *Id.* We agree that these holes are substantially in alignment. Accordingly, we find that Sakurai teaches “wherein the first, second, and third contact holes are aligned substantially in a straight line,” as recited in claim 10.

Regarding claim 16, Petitioner notes that the identified “first wire” is a straight line. Pet. 22–23. Petitioner incorporates its argument for claim 11, in which Petitioner provides an annotated version of Figure 5 with a dotted line showing that the first wire is a straight vertical line between

floating diffusion FD2 and the gate electrode of amplifier transistor SF1. *Id.* at 11. We find that Sakurai teaches “the first wire is disposed in approximately a straight line between the associated floating diffusion element and the gate electrode of the amplifier transistor,” as recited in claim 16.

In sum, we find that Sakurai, in light of the knowledge of a skilled artisan as explained by Mr. Guidash, teaches each limitation of claims 10 and 16. We have considered Patent Owner’s argument that Sakurai does not teach active regions, but find that argument unpersuasive for the reasons given above. Patent Owner does not contest that Sakurai teaches the other limitations of claims 10 and 16.

3. Conclusion of Obviousness

As explained above, in light of the knowledge of a skilled artisan as explained by Mr. Guidash, Sakurai teaches each limitation of claims 10 and 16. Mr. Guidash has provided undisputed testimony that it would have been obvious to implement Figure 5 of Sakurai using NMOS technology and that, when such technology is used, any limitations not expressly disclosed by Sakurai would have been obvious. Patent Owner does not argue or introduce evidence of objective indicia of nonobviousness. Upon consideration of all the evidence, we conclude that Petitioner has proved by a preponderance of the evidence that claims 10 and 16 would have been obvious over Sakurai.

D. Alleged Obviousness of Claims 10, 13, 14, 17, 20, and 21 over Tanaka

Petitioner contends that claims 10–15 and 17–22 would have been obvious over Tanaka. Pet. 43–60. Nevertheless, because we conclude that claims 10, 11, 12, 15, 17, 18, 19, and 22 would have been obvious over the Guidash patent, we do not reach whether those claims also would have been obvious over Tanaka, other than to evaluate independent claims 10 and 17, from which claims 13, 14, 20, and 21 depend. We determine below that claims 10, 13, 14, 17, 20, and 21 would have been obvious over Tanaka.

1. Scope and Content of the Prior Art - Overview of Tanaka

Tanaka describes amplified solid-state imaging devices having a MOS transistor structure that enables simultaneous formation of plural MOS transistors each having a different threshold voltage. Ex. 1012 ¶ 1. Figure 1, reproduced below, illustrates an example:

gates are at the intersection of polysilicon wiring 13b and 13c and the surfaces between photodiodes 11a and 11b and accumulation diode 12. *Id.*

Reset transistor gate 18 is formed at the intersection of drain line diffusion layer 16a and polysilicon wiring 13a. *Id.* ¶ 22. Amplifying transistor gate 19 is formed at the intersection of drain line diffusion layer 16b and first polysilicon wiring 13e. *Id.* Selection transistor gate 20 is formed at the intersection of drain line diffusion layer 16b and polysilicon wiring 13d. *Id.*

2. *Comparison of Tanaka to claims 10, 13, 14, 17, 20, and 21; differences between claims 10, 13, 14, 17, 20, and 21 and Tanaka*

Petitioner contends that most of the limitations of the challenged claims are expressly disclosed in Tanaka. For those limitations not disclosed expressly, Petitioner relies on testimony from Mr. Guidash that a skilled artisan would have inferred those limitations based on the type of technology the artisan would have found most appropriate to use.

Petitioner acknowledges that Figure 1 of Tanaka illustrates a single pixel, rather than “a plurality of photodiodes arranged in rows and columns,” as recited in claim 10. Pet. 44. Nevertheless, Petitioner argues that a skilled artisan would have recognized that Figure 1 represents one pixel in an arrangement of rows and columns, connected, for example, via polysilicon wiring 13a, 13b, 13c, and 13d. *Id.* at 44–45 (citing Ex. 1002 ¶¶ 258–61). We agree that this is the straightforward reading of Tanaka.

Petitioner argues that photodiodes 11a and 11b, along with accumulation diode 12, as shown bounded by solid lines, are a contiguous diffusion region with transfer gates (14a and 14b) formed thereon. *Id.* at 45.

Thus, Petitioner argues, together they constitute an “active region of the semiconductor substrate,” as recited in claim 10. *Id.* at 45–46. Mr. Guidash testifies that “[t]his region is an active region because it is formed as a contiguous diffusion region in the substrate (having transfer gates therein), and because electrical charge can flow between the photodiodes and the floating diffusion region in the middle.” Ex. 1002 ¶ 262. According to Mr. Guidash, it is typical in the art to represent active regions in this manner. *Id.* Petitioner argues that it would have been obvious that this pixel configuration would have been repeated in rows and columns, forming corresponding active regions for each photodiode. Pet. 46.

Patent Owner argues that Petitioner has not identified an active region in Tanaka. PO Resp. 47–50. Patent Owner argues, “[a]s explained in the Claim Construction section above, an active region as envisioned by ’493 Patent is a region that is maximally isolated from other regions having a boundary that confines charges, and minimizing to the greatest possible degree, electric current from entering or leaving the boundary” and that “Tanaka, however, provides no disclosure of any charge boundary whatsoever.” PO Resp. 47. According to Patent Owner, “[n]othing in Tanaka would indicate it has an active region confining charges at a boundary.” *Id.* at 49. Patent Owner cited to the testimony of Dr. Afromowitz, which essentially repeats this argument. *Id.* at 47–49 (citing Ex. 2003 ¶¶ 88, 113).

We are not persuaded. As explained in Section II.A above, an “active region” is “a contiguous region of the substrate through which charges can flow and where components such as photodiodes, diffusion layers, and portions of transistors are formed,” and need not be maximally isolated,

include an insulation region, or include a boundary over which charge cannot pass. We credit Mr. Guidash's testimony that the region in Figure 1 bounded by solid lines, including photodiodes 11a and 11b and accumulation diode 12, is a contiguous region through which charges can flow. Accordingly, we find that Tanaka teaches "each photodiode for a given row of photodiodes formed in a corresponding active region of the semiconductor substrate," as recited in claim 10.

As to a "transfer gate," as recited in claim 10, Tanaka explains that "[t]he transfer transistor gates 14a and 14b for transferring the signal charge accumulated to the accumulation diode 12 are structured at the intersections with the first polysilicon wiring 13b and 13c between the accumulation diode 12 and the photodiodes 11a and 11b, respectively." Ex. 1012 ¶ 20. Petitioner contends that the transfer transistor gates 14a and 14b are examples of "a transfer gate disposed over the first active region so as to define an associated photodiode on one side of the transfer gate and an associated floating diffusion element on another side of the transfer gate," as recited in claim 10. Pet. 46–47. Specifically, Petitioner argues, transfer transistor gates 14a and 14b correspond to "a transfer gate disposed over the first active region," photodiodes 11a and 11b are "an associated photodiode on one side of the transfer gate," and accumulation diode 12 is "an associated floating diffusion element on another side of the transfer gate." *Id.* Mr. Guidash testifies that the identity of the floating diffusion element "is apparent because of its arrangement on the other side of the transfer gates 14a and 14b, as well as its connection over the first wire to the gate of the amplifier transistor." Ex. 1002 ¶ 262.

Patent Owner appears to argue that accumulation diode 12 is not a floating diffusion element. PO Resp. 49. Specifically, Patent Owner argues that “Petitioner makes no explanation as to why one having ordinary skill in the art would understand that an ‘accumulation diode’ as disclosed by Tanaka, would disclose the claimed ‘floating diffusion element’ much less indicate this is an ‘active region.’” *Id.* We disagree. As noted above, Mr. Guidash explains that the accumulation diode can be identified as a floating diffusion element based on its position in the circuit of Figure 1 and the components to which it is connected. Ex. 1002 ¶ 165. We credit this testimony. Patent Owner does not cite to evidence to support its argument. On this record, we find that Tanaka teaches “a transfer gate disposed over the first active region so as to define an associated photodiode on one side of the transfer gate and an associated floating diffusion element on another side of the transfer gate,” as recited in claim 10.

Petitioner further contends that Tanaka’s amplifying transistor gate 19 is “an amplifier transistor,” as recited in claim 10, and that Tanaka’s reset transistor gate 18 is “a reset transistor.” Pet. 47–48. We agree with Petitioner.

As to “a first wire,” as recited in claim 10, Tanaka explains:

In the direction perpendicular to the first polysilicon wiring 13 to 13e, a second polysilicon wiring 15 and a drain line diffusion layers 16a and 16b are disposed. At the intersections of the second polysilicon wiring 15, drain line diffusion layer 16a, the accumulation diode 12, and the first polysilicon wiring 13e, a first, second and third contact sections 17a, 17b, and 17c, respectively, are formed.

Ex. 1012 ¶ 21. Petitioner contends that second polysilicon wiring 15 is “a first wire” because it connects accumulation diode 12, the floating diffusion

element, with polysilicon wiring 13e, the gate electrode of amplifying transistor 19. Pet. 49–50. We agree with Petitioner and find that Tanaka teaches “a first wire electrically connecting the associated floating diffusion element to a gate electrode of the amplifier transistor,” as recited in claim 10.

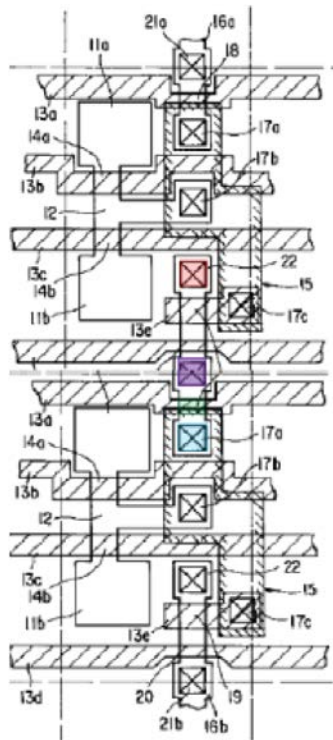
Petitioner identifies signal line contact section 22, directly above amplifier transistor gate 19, as a “first contact hole,” as recited in claim 10. *Id.* at 50–51. Relying on Mr. Guidash’s testimony, Petitioner argues that the signal line coupled to the signal line contact section obviously would be a wire, as it carries the electrical output of the pixel. *Id.* at 50 (citing Ex. 1002 ¶ 273). Mr. Guidash infers that signal line contact section 22 is connected to the source of amplifying transistor gate 19 because the contact at the other side of the gate is referred to as a “drain line contact section.” Ex. 1002 ¶ 275 (citing Ex. 1012 ¶ 23). Additionally, as above, Mr. Guidash testifies that it would have been obvious to use NMOS transistors in implementing Figure 1 of Tanaka, which additionally indicates that signal line contact section 22 is the source of amplifying transistor gate 19. *Id.* ¶ 276. We credit Mr. Guidash’s testimony, which is undisputed. Accordingly, we find that Tanaka teaches “a first contact hole connected to a second wire disposed over the semiconductor substrate and being for receiving an output of a source of the amplifier transistor,” as recited in claim 10.

Petitioner contends that drain line contact section 21b, immediately above reset transistor gate 18, is “a second contact hole,” as recited in claim 10. Pet. 52–53. Petitioner again relies on testimony of Mr. Guidash that it would have been obvious to use NMOS technology. *Id.* at 52 (citing Ex. 1002 ¶ 279). Mr. Guidash also testifies that the drain line coupled to the

drain line contact section obviously is a wire because it carries the electrical power supply Vdd. Ex. 1002 ¶ 280. We credit Mr. Guidash's testimony, which is undisputed. Accordingly, we find that Tanaka teaches "second contact hole connecting a drain of the reset transistor to a third wire disposed over the first semiconductor substrate," as recited in claim 10.

Petitioner further contends that Tanaka's first contact section 17 is "a third contact hole," as recited in claim 10. Pet. 53. Relying on Mr. Guidash, Petitioner argues that first contact section 17 is at the source of reset transistor gate 18 because the other side is the drain. *Id.* (citing Ex. 1002 ¶ 281). We credit Mr. Guidash's testimony, which is undisputed. Accordingly, we find that Tanaka teaches "a third contact hole connected to a source of the reset transistor," as recited in claim 10.

Petitioner provides a figure, reproduced below, showing the circuit of Tanaka's Figure 1 repeated once, in the column direction, and annotated to show the alignment of the first, second, and third contact holes. Pet. 53.



Petitioner's modified and annotated Figure 1 shows the first contact hole in red, the second contact hole in purple, and the third contact hole in blue. *Id.* We agree that these holes are substantially in alignment. Accordingly, we find that Tanaka teaches "wherein the first, second, and third contact holes are aligned substantially in a straight line," as recited in claim 10.

In sum, we find that Tanaka, in light of the knowledge of a skilled artisan as explained by Mr. Guidash, teaches each limitation of claim 10.

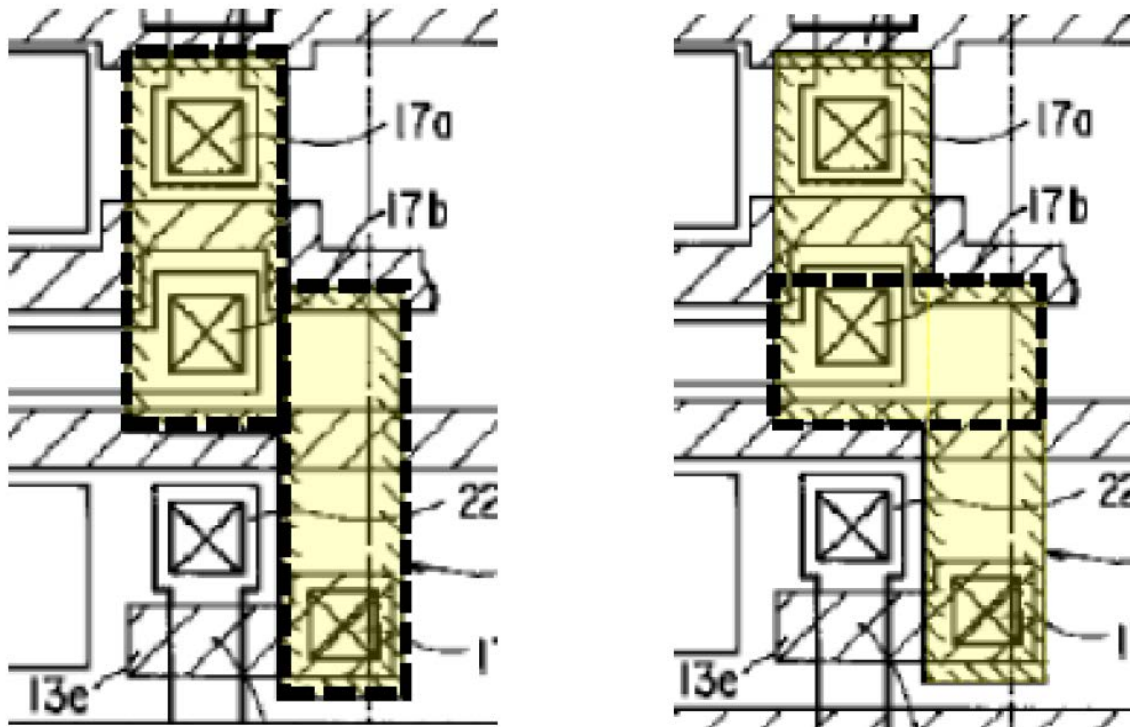
As explained above, claim 17 is substantially similar to claim 10 and we treat claim 10 as representative. Petitioner incorporates its argument and evidence for claim 10 as to its allegations for claim 17. Pet. 58–60. Patent Owner also argues claims 10 and 17 together. PO Resp. 47. For the reasons given for claim 10, we find that Tanaka teaches each limitation of claim 17.

Claim 13 depends from claim 10 and claim 20 depends from claim 17. Each of claims 13 and 20 recites:

the first wire includes a straight portion disposed in a first column direction and another portion disposed in a direction traversing column direction, and

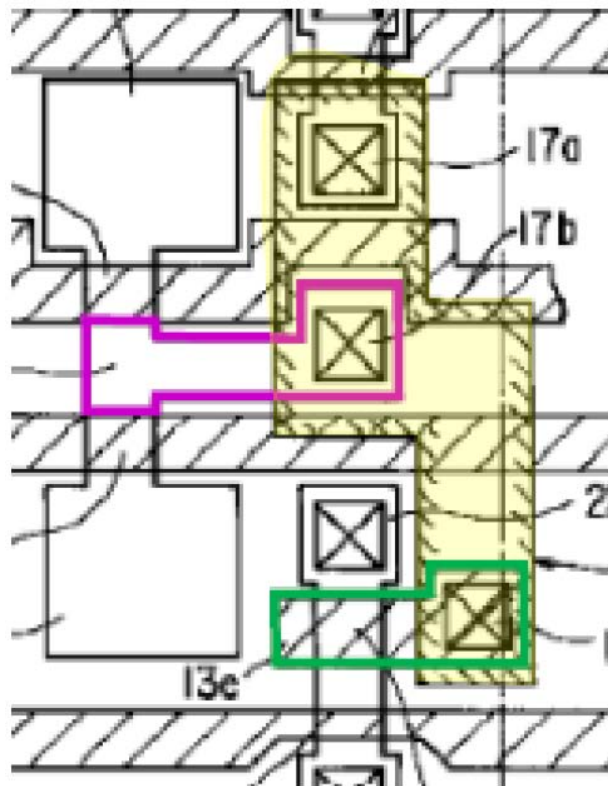
the straight portion is connected to the associated floating diffusion element.

Petitioner's identifications of straight and traversing portions of a first wire are shown in its annotations to Tanaka's Figure 1, reproduced below:



The above two figures are annotated versions of a portion of Tanaka's Figure 1 using yellow and dotted lines to identify two straight portions of wire 15, in a column direction (first annotated figure), and a portion disposed in a direction traversing the column direction (second annotated figure). Pet. 54.

Petitioner provides a third annotated figure (reproduced below) to show that the straight portion of wire 15 is connected to accumulation diode 12, the floating diffusion element:



The above figure is an annotated version of a portion of Tanaka's Figure 1 using yellow to show wire 15 and purple outline to show the floating diffusion element. Pet. 55.

The parties dispute whether the straight portion of wire 15 or the traversing portion is connected to the floating diffusion element. Petitioner contends that it is the straight portion. *Id.* As shown in the two annotated figures above, Petitioner identifies contact 17b as connected to both the straight and traversing portions of wire 15. Patent Owner contends that "[t]his makes it is ambiguous what exactly Petitioner is identifying in Tanaka that it claims meets the requirements for claim 13." PO Resp. 41.

Patent Owner further argues that Mr. Guidash conceded in deposition that the horizontal (traversing) portion of Tanaka's wire 15, and not the vertical (column) portion, is connected to the floating diffusion element.

Id. at 42–43 (citing Ex. 2011, 90:16–91:14). Mr. Guidash, however, testified that straight and traversing portions of the first wire of claim 13 are not mutually exclusive; thus, the floating diffusion element can be connected to both, as in the case of Tanaka’s wire 15. Ex. 2011, 89:22–90:14. Petitioner contends that the ’493 patent also shows a first wire as having overlapping straight and traversing portions at the corners. Reply 26–27 (citing Ex. 1001, Fig. 5 (metal wire 221)).

We agree with Petitioner. Tanaka’s floating diffusion element is connected to a corner of wire 15, at the point where a straight portion, in the column direction, transitions to a traversing portion. Thus, Tanaka’s floating diffusion element is connected to both the straight and traversing portions. Accordingly, we find that Tanaka teaches “the straight portion is connected to the associated floating diffusion element,” as recited in claims 13 and 20. In sum, we find that Tanaka teaches the additional limitations of claims 13 and 20.

Claim 14 depends from claim 10 and claim 21 depends from claim 17. Each of claims 14 and 21 recites “wherein transfer gates corresponding to adjacent photodiodes are formed by a continuous conducting material layer.” Petitioner contends that it would have been obvious to form adjacent photodiodes and transfer transistor gates with polysilicon wiring 13b and 13c formed as continuous strips of polysilicon. Pet. 55–56. As Petitioner points out, Tanaka shows polysilicon wiring 13b and 13c with curved lines at their ends, which we agree suggests that those wires continue to adjacent pixels. Pet. 56. Additionally, Mr. Guidash testifies that a skilled artisan would have known that the entire gate wiring for read-out transistors in all cells of a row could be energized at one time because the address transistors

determine which cell is active. Ex. 1002 ¶ 292. According to Mr. Guidash, using a continuous strip of polysilicon material advantageously would have saved space in a layout. *Id.* We credit Mr. Guidash's testimony, which is undisputed. Accordingly, we find that Tanaka teaches the additional limitation of claims 14 and 21.

3. Conclusion of Obviousness

As explained above, in light of the knowledge of a skilled artisan as explained by Mr. Guidash, Tanaka teaches each limitation of claims 10, 13, 14, 17, 20, and 21. Mr. Guidash has provided undisputed testimony that it would have been obvious to implement Figure 1 of Tanaka using NMOS technology and that, when such technology is used, any limitations not expressly disclosed by Tanaka would have been obvious. Patent Owner does not argue or introduce evidence of objective indicia of nonobviousness. Upon consideration of all the evidence, we conclude that Petitioner has proved by a preponderance of the evidence that claims 10, 13, 14, 17, 20, and 21 would have been obvious over Tanaka.

III. CONCLUSION

Petitioner has demonstrated, by a preponderance of the evidence, that claims 10–12, 15, 17–19, and 22 are unpatentable over the Guidash patent; claims 10 and 16 are unpatentable over Sakurai; and claims 10, 13, 14, 17, 20, and 21 are unpatentable over Tanaka.

IV. ORDER

For the reasons given, it is:

ORDERED, based on a preponderance of the evidence, that claims 10–22 of U.S. Patent No. 7,944,493 B2 are unpatentable; and

FURTHER ORDERED, because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 7,944,493 B2

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