

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION,
Petitioner,

v.

COLLABO INNOVATIONS, INC.,
Patent Owner.

Case IPR2016-00940
Patent 8,030,724 B2

Before DAVID C. McKONE, GREGG I. ANDERSON, and
JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–4 of U.S. Patent No. 8,030,724 B2 (Ex. 1001, “the ’724 patent”) are unpatentable.

A. Procedural History

Sony Corporation (“Petitioner”)¹ filed a Petition for *inter partes* review of claims 1–4 (“the challenged claims”) of the ’724 patent. Paper 2 (“Pet.”). Petitioner provided a Declaration of R. Michael Guidash (Ex. 1002) to support its positions. Collabo Innovations, Inc. (“Patent Owner”)² filed a Preliminary Response. Paper 6.

Pursuant to 35 U.S.C. § 314(a), on October 24, 2016, we instituted *inter partes* review to determine whether claims 1 and 2 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Asano³; and whether claims 3 and 4 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Asano and Shibayama.⁴ See Paper 7 (“Inst. Dec.”). Subsequent to

¹ Petitioner identifies Sony Corporation of America and Sony Electronics Inc. as additional real-parties-in-interest. Pet. 1.

² Patent Owner identifies Wi-LAN Technologies Inc. and Wi-LAN Inc. as additional real-parties-in-interest. Paper 5, 1.

³ WO2006/073085 A1, published July 13, 2006 (Ex. 1003). Citations throughout this Final Written Decision are to the certified translation of Asano (Ex. 1006).

⁴ JP Pat. App. Pub. No. P2004-165602A, published June 10, 2004 (Ex. 1004). Citations throughout this Final Written Decision are to the certified translation of Shibayama (Ex. 1005).

institution, Patent Owner filed a Patent Owner Response (Paper 12, “PO Resp.”), along with a Declaration of Martin Afromowitz, Ph.D. (Ex. 2002) to support its positions. Petitioner filed a Reply (Paper 15, “Pet. Reply”) to the Patent Owner Response. An oral hearing was held on July 11, 2017. A transcript of the hearing is included in the record. Paper 23.

B. Related Proceedings

The parties indicate that the ’724 patent has been asserted in *Collabo Innovations, Inc. v. Sony Corp.*, No. 1:15-cv-01094 (D. Del.). Pet. 1; Paper 5, 1.

C. The ’724 Patent

The ’724 patent relates to solid-state imaging devices, and methods for fabricating such devices. Ex. 1001, at [54]. According to the ’724 patent, the invention “provide[s] a solid-state imaging device having a structure that can suppress an increase in leakage current at the PN junction and an increase in dark current.” *Id.* at 2:60–64.

Figures 1A and 1B of the '724 patent, annotated by the panel, are reproduced below.

FIG. 1A

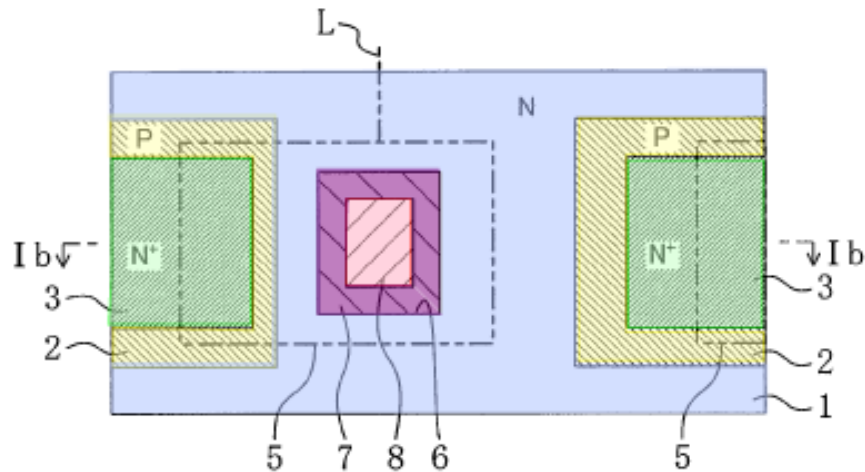


FIG. 1B

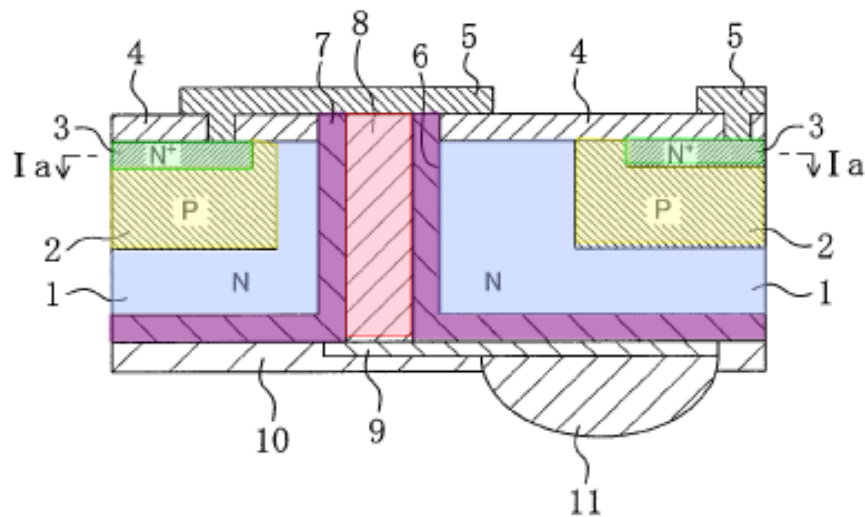


Figure 1A is plan view of a solid-state imaging device along line Ia-Ia of Figure 1B, and Figure 1B is a cross-sectional view of the solid-state imaging device along line Ib-Ib of Figure 1A. Ex. 1001, 4:24–28. As seen in Figures

1A and 1B, P-type semiconductor layer 2 (highlighted in yellow) is formed in semiconductor substrate 1 (highlighted in blue), which is formed of N-type silicon. *Id.* at 5:24–28. N⁺-type semiconductor layer 3 (highlighted in green) is formed in a surface portion of P-type semiconductor layer 2. *Id.* at 5:28–30. Insulating film 4 is formed on a surface of semiconductor substrate 1. *Id.* at 5:30–32.

Through-hole 6 is formed in insulating film 4 and semiconductor substrate 1. *Id.* at 6:8–9. Insulating film 7 (highlighted in purple, above) is formed on a sidewall portion of through-hole 6, as well as on a rear surface of semiconductor substrate 1. *Id.* at 6:11–13. Through-electrode 8 (highlighted in pink, above) is formed, filling the inside of insulating film 7. *Id.* at 6:13–14. Pad portion 5 is formed on a front side of semiconductor substrate 1 and is connected to N⁺-type semiconductor layer 3 and through-electrode 8 through openings in insulating film 4. *Id.* at 6:19–22. Rear surface electrode 9, insulating resin layer 10, and protruding electrode 11 are formed on a rear side of semiconductor substrate 1. *Id.* at 6:25–34.

According to the invention of the '724 patent, “a region in which the P-type semiconductor layer 2 is formed is reduced as compared to the conventional art” (*id.* at 6:43–45), which is shown in Figures 13A and 13B, annotated by the panel, and reproduced below.

FIG. 13A

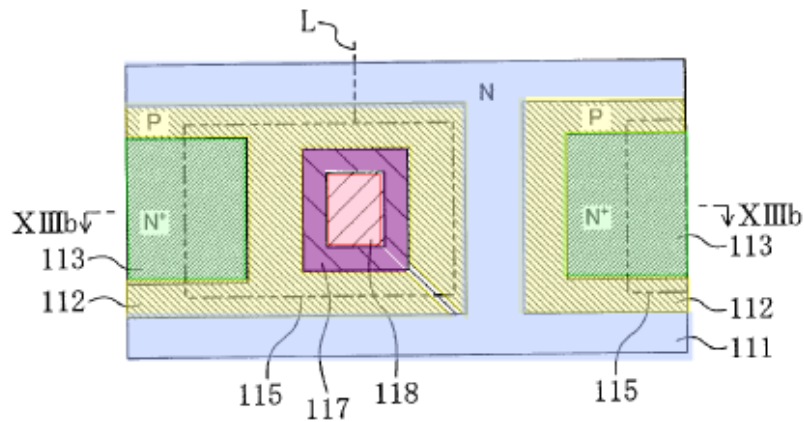


FIG. 13B

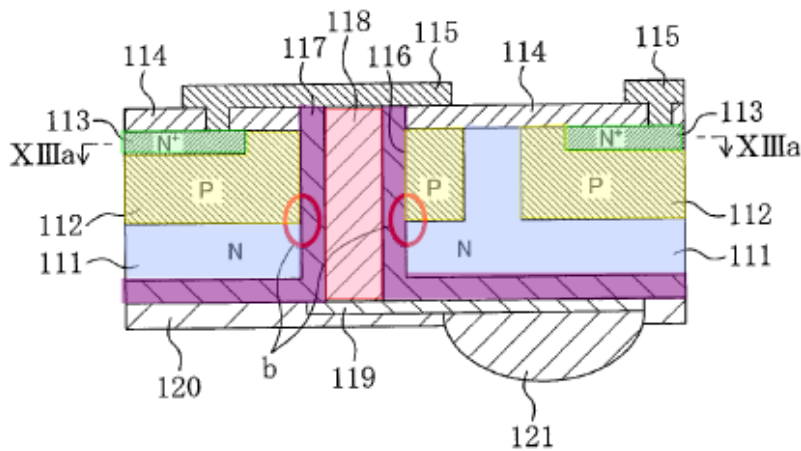


Figure 13A is a plan view of a conventional solid-state imaging device along line XIIIa-XIIIa of Figure 13B, and Figure 13B is a cross-sectional view of the conventional solid-state imaging device along line XIIIb-XIIIb of Figure 13A. Ex. 1001, 5:3–7. Similar features are highlighted in similar colors, as compared to the annotated versions of Figures 1A and 1B, reproduced above. As can be seen in a comparison of Figures 1A and 1B to Figures 13A and 13B, “through hole 6 [of the device of Figures 1A and 1B] does not penetrate through a PN junction region,” whereas through hole 116

in the device of Figures 13A and 13B *does* penetrate through a PN junction region (see points b, circled in red, above). *Id.* at 6:45–47; 2:30–34. In the embodiment shown in Figures 1A and 1B, through hole 6 “penetrates through a region having a single conductivity type, and the through electrode 8 is formed in the through hole 6.” *Id.* at 6:47–49. According to the ’724 patent, by this arrangement, “it is possible to reduce and suppress a leakage current at a PN junction caused by etching damage or the like occurring when a through hole penetrates through the PN junction region, and a dark current that becomes more significant during an operation at high temperature.” *Id.* at 6:50–54. These benefits “result[] in a solid-state imaging device having a high-sensitivity and a high [signal-to-noise (S/N)] ratio.” *Id.* at 6:54–57.

For both the preferred embodiments and the conventional solid-state imaging device according to the ’724 patent, the basic configuration of an internal circuit region and a peripheral circuit region of the imaging device is illustrated in Figure 12, reproduced below.

FIG. 12

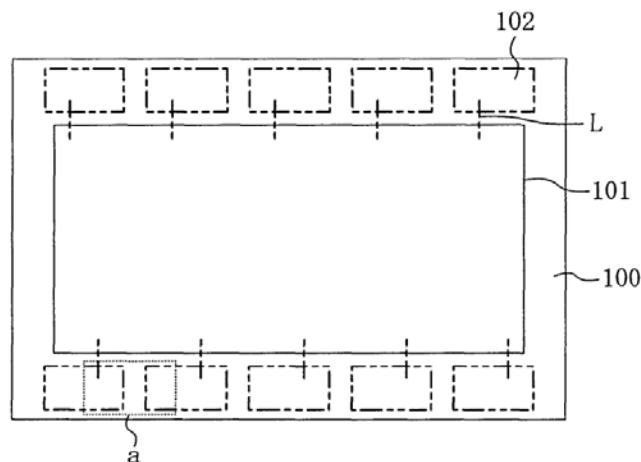


Figure 12 is a plan view showing a schematic structure of a conventional solid-state imaging device, according to the ’724 patent. Ex. 1001, 1:39–40.

The '724 patent describes internal circuit region 101 “provided at a middle portion of” semiconductor substrate 100, and peripheral circuit region 102 “provided at a peripheral portion” of semiconductor substrate 100. *Id.* at 1:41–46. The '724 patent further describes internal circuit region 101 as “having a light receiving portion and a drive circuit portion” and describes peripheral circuit region 102 as “having a pad portion and a protective circuit portion.” *Id.* In describing the preferred embodiments, the '724 patent also refers to Figure 12 to show the location of the peripheral circuit region and an internal circuit region, including light receiving portions. *Id.* at 5:36–65.

The configurations described above with respect to Figures 1A and 1B and Figures 13A and 13B, correspond to region “a” of Figure 12. *Id.* at 1:49–51, 5:17–20. The '724 patent describes that light receiving portions, each of which “is a photodiode made of the N⁺-type semiconductor layer . . . formed in the P-type semiconductor layer,” are provided in the P-type semiconductor layer, and “[t]he peripheral circuit, the protective circuit and the like are also formed in the P-type semiconductor layer.” *Id.* at 2:1–8.

D. Illustrative Claim

Of the challenged claims, claim 1 is independent. Claims 2–4 depend, directly or indirectly, from claim 1. Claim 1 of the '724 patent, reproduced below, is illustrative of the challenged claims:

1. A solid-state imaging device, comprising:

 a first conductivity type semiconductor substrate having the imaging region and the peripheral circuit region on a main surface thereof;

 an imaging region formed on a main surface of the semiconductor substrate and having a plurality of light receiving

portions arranged two-dimensionally and for generating signal electric charges by photoelectric conversion;

a peripheral circuit region formed on a main surface of the semiconductor substrate and formed in an outer peripheral portion of the imaging region;

a second conductivity type first semiconductor layer formed in the first conductivity type semiconductor substrate at a side of the main surface of the semiconductor substrate;

a first conductivity type second semiconductor layer formed in the first semiconductor layer;

a through electrode formed in a through hole penetrating through the semiconductor substrate in a thickness direction of the semiconductor substrate;

a pad portion formed on the main surface of the semiconductor substrate and connected to the through electrode; and

a side insulating film formed at a side surface of the through electrode.

Ex. 1001, 15:35–16:22.

II. ANALYSIS

A. *Principles of Law*

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to

each claim’’)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378–79 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burdens of persuasion and production in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁵ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In that regard, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech.*, 504 F.3d at 1259. The level of ordinary skill in the

⁵ Neither party directs our attention to specific objective evidence of nonobviousness.

art may be reflected by the prior art of record.⁶ *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

At this final written decision stage, we determine whether a preponderance of the evidence of the record shows that the challenged claims would have been obvious in view of the asserted prior art. We analyze the asserted grounds of unpatentability in accordance with those principles.

B. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). Pursuant to that standard, the claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. *See In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir. 2010). We generally give claim terms their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (“The ordinary and customary meaning ‘is the meaning that the term would have to a person of

⁶ Mr. Guidash testifies that a person of ordinary skill in the art would have had “a Bachelor’s degree in electrical engineering, physics, or material science and approximately 3–5 years of industrial experience or equivalent research or teaching experience, or a Master’s degree in the same fields and 1–3 years of industrial experience or equivalent research or teaching experience.” Ex. 1002 ¶ 53; Pet. 15. Patent Owner does not provide a statement of the level of skill in the art. Mr. Guidash’s opinion as to the level of ordinary skill is consistent with the level of skill indicated by the prior art of record in this proceeding.

ordinary skill in the art in question.” (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc))).

The claims, however, “should always be read in light of the specification and teachings in the underlying patent,” and “[e]ven under the broadest reasonable interpretation, the Board’s construction ‘cannot be divorced from the specification and the record evidence.’” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (quoting *In re NTP, Inc.*, 654 F.3d 1279, 1288 (Fed. Cir. 2011)). In other words, “[u]nder a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history.” *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016) (citing *Straight Path IP Grp., Inc. v. Sipnet EU S.R.O.*, 806 F.3d 1356, 1362 (Fed. Cir. 2015)). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. See *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). However, limitations are not to be read from the specification into the claims. See *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

In the Institution Decision, we preliminarily construed the phrase “peripheral circuit region . . . formed in an outer peripheral portion of the imaging region,” appearing in independent claim 1. Inst. Dec. 8–11. Specifically, we determined that a peripheral circuit region *formed in an outer peripheral portion of the imaging region* includes, at least, a peripheral circuit region *formed at or adjacent the outer edges of the imaging region*. See *id.*

Patent Owner indicates that “[f]or purposes of this proceeding, Patent Owner adopts the Board’s interpretation of the term in so far as it addresses

the relative location of the region with respect to the image sensor array, however, the Board does not address the substance of the circuit region itself, which requires further clarification.” PO Resp. 7 (citing Ex. 2002 ¶ 30). Patent Owner contends that a person of ordinary skill in the art would have understood that a peripheral circuit region is a region in which peripheral circuits are formed. *Id.* (citing Ex. 2002 ¶ 31). According to Patent Owner, “the issue remains as to what constitutes a peripheral circuit in light of the claims and specification of the ’724 Patent.” *Id.*

Citing to the Specification, Patent Owner argues that the peripheral circuit region contains “at least, transistors that have source/drains that are preferably formed in the same step as the regions of ‘higher impurity that that of the semiconductor substrate.’” *Id.* (citing Ex. 1001, 4:4–20, 9:42–51, 12:60–13:2, 14:62–15:3). Patent Owner points to further disclosure in the Specification of the ’724 patent that “[t]he P-type semiconductor layer 2 and the N⁺-type semiconductor layer 3 form a protective circuit in a peripheral circuit region (see 102 in FIG. 12).” *Id.* at 8–9 (quoting Ex. 1001, 5:36–38). Patent Owner contends, based on this disclosure, “a person having ordinary skill in the art would have understood that a peripheral circuit region contains a protective circuit, comprising a P-type semiconductor layer and an N⁺-type semiconductor layer.” *Id.* at 9 (citing Ex. 2002 ¶ 33). Ultimately, Patent Owner concludes that the term “peripheral circuit” means “a circuit formed in an outer peripheral portion of the imaging region including at least MOSFETs formed of a p-type and an n⁺-type semiconductor layer.” *Id.* (citing Ex. 2002 ¶ 34).

In its Reply, Petitioner argues not only that Patent Owner’s “extremely narrow construction of ‘peripheral circuit’ is not supported” by

Dr. Afromowitz⁷ or the '724 patent, but also that the term “peripheral circuit” is “found in the claims only as a part of ‘peripheral circuit region’, [and] needs no independent construction.” Pet. Reply 5. According to Petitioner, “[t]he claims merely require a ‘region’ in a particular location (peripheral), to be used for a particular purpose (circuits). However, the claims do not require specific *kinds* of circuits in the claimed region.” *Id.* at 6–7. Petitioner asserts that, although the Specification provides examples of what can be peripheral circuits (e.g., a pad portion or a protective circuit portion (Ex. 1001, 1:41–46)), these examples do not act to define peripheral circuit or support a narrow construction, such as that proposed by Patent Owner. Pet. Reply 9.

We agree with Petitioner, and determine that Patent Owner’s proposed construction⁸ attempts to improperly import limitations from the Specification into the claims. *See In re Van Geuns*, 988 F.2d at 1184; *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988) (“Where a specification does not require a limitation, that limitation should not be read from the specification into the claims.”). We determine that the portions of the Specification on which Patent Owner

⁷ Petitioner argues that Dr. Afromowitz’s proposed construction is inconsistent with the position taken in the Patent Owner Response. *See* Pet. Reply 5–6. Based on our adopted construction of “peripheral circuit region” (discussed *infra*), however, we need not address this question.

⁸ It is unclear from the record whether Patent Owner proposes that the peripheral circuit region requires “at least, transistors that have source/drains” (PO Resp. 7), “a protective circuit, comprising a P-type semiconductor layer and an N⁺-type semiconductor layer” (*id.* at 9), and/or “at least MOSFETs formed of a p-type and an n⁺-type semiconductor layer” (*id.*). Our analysis is the same, however, under any of these proposals.

relies (see PO Resp. 7) do not provide a lexicographic definition of “peripheral circuit region.” See *In re Paulsen*, 30 F.3d at 1480 (“‘Where an inventor chooses to be his own lexicographer and to give terms uncommon meanings, he must set out his uncommon definition in some manner within the patent disclosure’ so as to give one of ordinary skill in the art notice of the change.” (internal citations omitted)). For example, the Specification describes that

the step of forming a region having a higher impurity concentration than that of the semiconductor substrate and the step of forming the light receiving portion are preferably the same step, or the step of forming a region having a higher impurity concentration than that of the semiconductor substrate and the step of forming a source/drain region of an MOSFET in the peripheral circuit region are preferably the same step.

Ex. 1001, 4:4–12. The Specification also describes “the N⁺-type semiconductor layers can be formed at the same time when the source/drain diffusion region of the MOSFET is formed or the cathode of the diode is formed in the peripheral circuit region if the N⁺-type semiconductor layers are formed relatively shallow.” *Id.* at 9:42–46; see *id.* at 12:60–64, 14:62–66 (each including similar disclosure). These cited portions merely provide examples, according to preferred embodiments, rather than a definition of “peripheral circuit region.”

The Specification of the ’724 patent does not support Patent Owner’s assertion that the “peripheral circuit region” must “includ[e] at least MOSFETs formed of a p-type and an n⁺-type semiconductor layer” (PO Resp. 9). For example, the Specification describes that “a peripheral circuit region 102 [has] a pad portion and a protective circuit portion.” Ex. 1001, 1:43–45. The Specification also describes that “[t]he P-type semiconductor

layer 2 and the N⁺-type semiconductor layer 3 form a protective circuit in a peripheral circuit region (see 102 in FIG. 12).” *Id.* at 5:36–38. Neither of these citations mentions nor requires a MOSFET.

The language of claim 1 itself also is instructive. Claim 1 recites both an “imaging region” and a “peripheral circuit region.” Although claim 1 expressly recites that the “imaging region” has “a plurality of light receiving portions,”⁹ there is no corresponding express recitation of any structural element formed in the “peripheral circuit region.” We decline to require any specific structural element be formed in the peripheral circuit region, when no such structural element is recited in the claim. *See In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998) (“[T]he name of the game is the claim.”).

Instead, we maintain our previous construction, that a peripheral circuit region *formed in an outer peripheral portion of the imaging region* includes, at least, a peripheral circuit region *formed at or adjacent the outer edges of the imaging region*. In view of the parties’ dispute, we further determine that the claims do not require any particular specific type of circuit be formed in the peripheral circuit region, but that the claims merely

⁹ This configuration of the imaging region is described in the Specification in the paragraph immediately following the description that “[t]he P-type semiconductor layer 2 and the N⁺-type semiconductor layer 3 form a protective circuit in a peripheral circuit region (see 102 in FIG. 12)” (Ex. 1001, 5:36–38). *See id.* at 5:51–65 (“[I]n an internal circuit region (see 101 in FIG. 12), in the P-type semiconductor layer 2, an imaging region having a plurality of light receiving portions . . . [is] provided. Note that the light receiving portion in the internal circuit region, which is a photodiode made of the N⁺-type semiconductor layer 3 formed in the P-type semiconductor layer 2, accumulates electric charges, depending on the intensity of the received light.”).

require a peripheral region (i.e., a region formed at or adjacent the outer edges of the imaging region) that is used for circuits.

Except as discussed above, no other terms require express construction for purposes of this Final Written Decision. *See, e.g., Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

C. Obviousness in View of Asano

Petitioner asserts that claims 1 and 2 are unpatentable under 35 U.S.C. § 103 as obvious in view of Asano. Pet. 2, 34–46. Patent Owner argues that Asano does not teach all the features of the claims, and that one of skill in the art would not modify Asano in the manner asserted by Petitioner. PO Resp. 14–32. We have reviewed the entire record before us, including the parties’ contentions and supporting evidence presented during this trial. For the reasons explained below, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1 and 2 would have been obvious in view of Asano.

1. Scope and Content of the Prior Art – Overview of Asano

Asano relates to solid-state image pickup devices and methods for manufacturing the same. Ex. 1006 ¶ 1. Figure 1 of Asano is reproduced below.

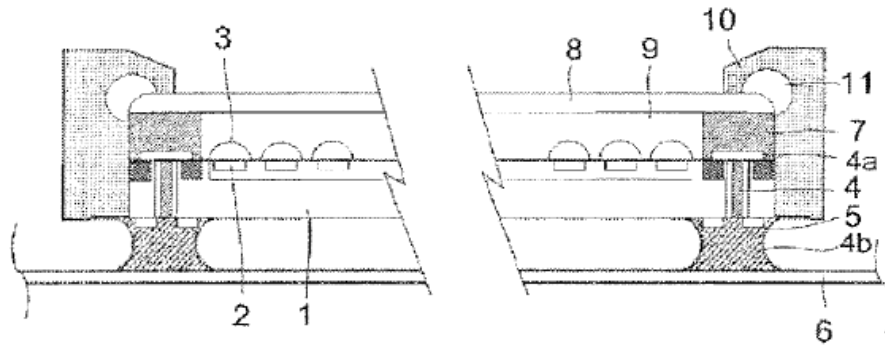


Figure 1 is a structural sectional view showing a basic construction of the image pickup device of Asano. *Id.* ¶ 19. The image pickup device shown in Figure 1 includes “a large number of photoreceiving sections 2, and microlenses 3 formed individually on the photoreceiving sections, disposed on the front face of the wafer 1.” *Id.* ¶ 20. “Penetrating electrodes 4 are provided at numerous locations in the peripheral section of the wafer 1, through which power is supplied to, and electrical signals are transmitted to and from, the photoreceiving sections 2.” *Id.* Electrodes 4 are connected to electrode pad 4a on one end and rear face electrode 5 on the other end. *Id.*

Figure 3 of Asano is reproduced below.

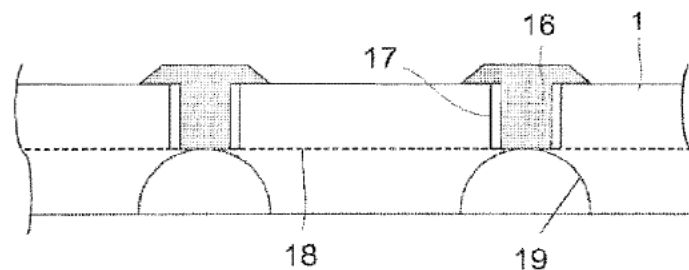


Figure 3 is a sectional view showing formation of penetrating electrodes 4, according to Asano. *Id.* ¶ 42. “[T]renches 16 are formed from the front face of the wafer 1 beforehand, localized oxide film 17 is formed, . . . [and] the

trenches are filled with an electrode material to form the wiring and then connected to the electrode pad.” *Id.* As described in Asano, by forming through electrodes using this method “the occurrences of dry etching damage and crystal defects can be considerably reduced.” *Id.* ¶ 43.

2. Comparison of Asano to Claims 1 and 2; Differences Between the Challenged Claims and Asano

Petitioner contends that most of the limitations of claims 1 and 2 are expressly disclosed in Asano. For those limitations not disclosed expressly, Petitioner relies on testimony from Mr. Guidash that a skilled artisan would have understood the other elements to be present in the imaging device of Asano.

Claim 1

solid-state imaging device

Regarding claim 1, Asano describes a solid-state image pickup device and methods for manufacturing the same. Ex. 1006, Title; see Pet. 35 (citing Ex. 1006, Title, ¶ 8). Based on this evidence, we agree that Asano teaches a solid-state imaging device.

a first conductivity type semiconductor substrate having the imaging region and the peripheral circuit region on a main surface thereof

Petitioner relies on wafer 1 of Asano, an “n-type wafer,” as teaching the claimed first conductivity type semiconductor substrate. Pet. 36 (citing Ex. 1006 ¶ 45; Ex. 1002 ¶¶ 206–207). Based on this evidence, we agree that Asano teaches a first conductivity type semiconductor substrate. The claimed imaging region and peripheral circuit region formed on the substrate are discussed in detail below.

an imaging region formed on a main surface of the semiconductor substrate and having a plurality of light receiving portions arranged two-dimensionally and for generating signal electric charges by photoelectric conversion

Petitioner asserts that photoreceiving regions 2, each with an optical element (microlenses 3) formed thereon, and disposed on the front face of wafer 1, teach the claimed “imaging region” formed on “a main surface” of the substrate. Pet. 36–37 (citing Ex. 1006, Abstract, ¶¶ 19–20, Fig 1; Ex. 1002 ¶¶ 208–209). Regarding the claimed “imaging region . . . having a plurality of light receiving portions [being] arranged two-dimensionally,” Petitioner notes that Asano does not expressly state that photoreceiving regions 2 and microlenses 3 (which Petitioner maps to the claimed “imaging region”) are arranged two-dimensionally. *Id.* at 35, 39. Petitioner, however, contends that this arrangement would have been obvious in view of the teachings of Asano. *Id.* at 38–39. In particular, Petitioner argues that one of skill in the art would have understood that imaging devices, such as the one taught in Asano, include two-dimensional arrays of photoreceiving sections in practice. *Id.* at 39–40 (citing Ex. 1006, Abstract, ¶ 65; Ex. 1002 ¶¶ 219–222, 224). Based on this evidence, we agree that Asano teaches an imaging region formed on a main surface of the semiconductor substrate and having a plurality of light receiving portions arranged two-dimensionally.

Regarding the claimed “imaging region” being “for generating signal electric charges by photoelectric conversion,” Petitioner points to Asano’s teaching that power is supplied to, and electrical signals are transmitted to and from, photoreceiving sections 2 via electrodes 4. *Id.* at 40 (citing Ex. 1006 ¶ 20). Petitioner also points to Mr. Guidash’s testimony that image pickup devices sense images using photoreceiving sections to generate such

signal electric charges by photoelectric conversion, as claimed. *Id.* (citing Ex. 1002 ¶¶ 29, 32, 223). Based on this evidence, we agree that Asano teaches an imaging region for generating signal electric charges by photoelectric conversion.

a peripheral circuit region formed on a main surface of the semiconductor substrate and formed in an outer peripheral portion of the imaging region

Petitioner relies on a “protection diode” of Asano as teaching the claimed “peripheral circuit region” formed on “a main surface” of the substrate.¹⁰ Pet. 37 (citing Ex. 1006 ¶¶ 19, 25; Ex. 1002 ¶ 210), 38 (citing Ex. 1006 ¶ 56, Fig. 1; Ex. 1002 ¶ 215). According to Petitioner, “the peripheral circuit region [of Asano], including . . . the protection diode immediately below the electrode pads, is formed near an outer region . . . of the imaging region,” thus, teaching that the peripheral circuit region is “formed in an outer peripheral portion of the imaging region,” as claimed. *Id.* at 40 (citing Ex. 1006, Fig. 1; Ex. 1002 ¶ 225).

Patent Owner argues that “Asano does not disclose a peripheral circuit region.” PO Resp. 15. Patent Owner’s arguments in this regard are premised on its assertion that the peripheral circuit region as claimed must include a specific protective circuit and/or MOSFETs. *See id.* at 16–18. As discussed above in Section II.B, we are not persuaded by Patent Owner’s claim construction arguments in this regard. Instead, as we have construed

¹⁰ Petitioner also argues that electrode pads 4a are “circuit elements in a circuit region” and that “it would have been obvious to include additional circuits in the peripheral circuit region [of Asano].” Pet. 37. Because we determine the disclosed protection diode of Asano teaches this limitation, we do not address Petitioner’s additional arguments, or Patent Owner’s opposition thereto.

the claims, the claimed peripheral circuit region does not require any particular specific type of circuit be formed therein, but instead the claims require only a peripheral region that is used for circuits. Patent Owner does not dispute that a protection diode is a circuit. *See* Pet. Reply 15.

Accordingly, Patent Owner's arguments in this regard are not persuasive. *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (stating that it is well established that limitations not appearing in the claims cannot be relied upon for patentability).

Patent Owner further argues that “even if the protection diode referenced by Asano were considered a ‘circuit element’ . . . Asano provides no description of where the protection diode would be located that would qualify it as part of a peripheral circuit region.” PO Resp. 19–20 (citing Ex. 2002 ¶ 47). Petitioner, however, relies on express disclosure of Asano that “[p]enetrating electrodes 4 are provided at numerous locations *in the peripheral section of the wafer 1*” and, in a CCD device, “the p-type region for the protection diodes *is provided immediately below or at the periphery of the electrode pad.*” Ex. 1006 ¶¶ 20, 45 (emphases added); Pet. 37–38; Ex. 1002 ¶¶ 210, 215–217; *see also* Pet. Reply 15 (“Asano therefore teaches protection diodes that are formed on a main surface of the semiconductor substrate and at or adjacent the outer edges of an imaging region, because those diodes are formed ‘immediately below or at the periphery of the pad electrode.’”). We, thus, are not persuaded by Patent Owner's argument that there is no teaching in Asano with respect to the location of the protection diode.

Patent Owner further contends that “Petitioner incorrectly imports into Asano's Figure 1 a feature from an embodiment specifically distinguished

by Asano from the embodiment of Figure 1.” PO Resp. 22. As Petitioner notes in its Reply, however, “paragraphs 0037–0055 [of Asano] are not a distinct embodiment from other Asano devices.” Pet. Reply 10; *id.* at 16–19 (Petitioner’s detailed arguments in this regard). We agree with Petitioner that these paragraphs “describe the manufacturing of *all* Asano devices.” *Id.* at 11. This is consistent with the disclosure of Asano. Figure 1 of Asano (i.e., the “First Embodiment”) is described as “Basic Configuration of the Image Pickup Device.” Ex. 1006 ¶ 19; *see* Pet. Reply 10. The so-called “Second Embodiment” of Asano is described as “Method for Manufacturing an Image Pickup Device” and teaches a method for forming “[t]he image pickup devices according to the present invention.” Ex. 1006 ¶ 37; *see* Pet. Reply. 10–11. In other words, the “First Embodiment” describes the structure of the device of Asano, and the “Second Embodiment” describes the method of manufacturing that device. Accordingly, we are not persuaded by Patent Owner’s arguments that the relied-upon embodiments of Asano cannot be considered together.

Patent Owner also argues that “Petitioner’s [m]otivation to modify Asano is [f]aulty.” PO Resp. 25–27. Specifically, Patent Owner argues that “[t]he peripheral region shown [in Asano] is small, just large enough for penetrating electrodes and pads, and has no n^+ -type layer there in which to build the sources and drains of MOSFETs.” *Id.* at 25–26 (citing Ex. 2002 ¶ 56). According to Patent Owner, “[a]dding those necessary elements to Asano would entail a complete redesign of Asano.” *Id.* (citing Ex. 2002 ¶ 56). First, as noted above, we determine there is no requirement that the peripheral circuit region includes MOSFETs. Second, Petitioner does not rely on a modification of Asano for teaching the claimed peripheral circuit

region; Petitioner's position, discussed above, is that Asano teaches a protection diode "provided immediately below or at the periphery of the electrode pad" (Ex. 1006 ¶ 45), which is "in the peripheral section of the wafer" (*id.* ¶ 20). Accordingly, Patent Owner's arguments in this regard also are unpersuasive.

For the reasons discussed, and based on the above evidence, we agree that Asano teaches a peripheral circuit region formed on a main surface of the semiconductor substrate and formed in an outer peripheral portion of the imaging region.

a second conductivity type first semiconductor layer formed in the first conductivity type semiconductor substrate at a side of the main surface of the semiconductor substrate

Petitioner points to Asano's "p-type well formed at the front face section of the n-type wafer" as teaching the claimed "second conductivity type first semiconductor layer formed in the first conductivity type semiconductor substrate." Pet. 40–41 (citing Ex. 1006 ¶ 45; Ex. 1002 ¶¶ 227–228). Petitioner's annotated version of Figure 1 (*id.* at 41) is reproduced below.

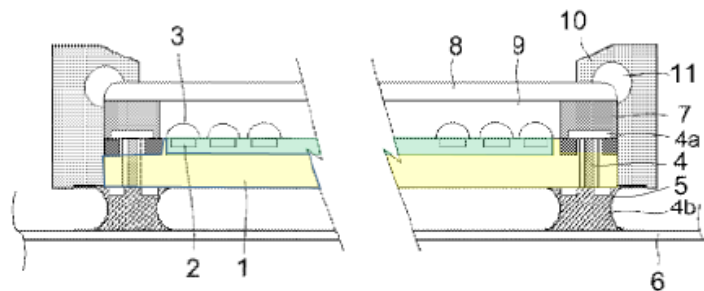


Figure 1 is a sectional view of the image pickup device of Asano. Ex. 1006 ¶ 19. As seen in annotated Figure 1, the p-type well (highlighted in green) is "formed . . . at a side of the main surface of the semiconductor substrate" (highlighted in yellow). Pet. 41.

Based on this evidence, we agree that Asano teaches a second conductivity type first semiconductor layer formed in the first conductivity type semiconductor substrate at a side of the main surface of the semiconductor substrate.

a first conductivity type second semiconductor layer formed in the first semiconductor layer

Petitioner notes that Asano does not expressly state that the photodiodes include n-type layers formed in the p-type well. Pet. 35. Petitioner provides uncontested testimony from Mr. Guidash, however, that one skilled in the art would understand that the sensor of Asano must include an n-type layer in the p-type well, thus forming a p-n junction, in order for the sensor to function properly.¹¹ *Id.* at 41–42 (citing Ex. 1002 ¶¶ 231–232). Petitioner relies on this n-type layer as teaching the claimed “first conductivity type second semiconductor layer formed in the first semiconductor layer.” *Id.* Petitioner’s annotated version of Figure 1 (*id.* at 42) is reproduced below.

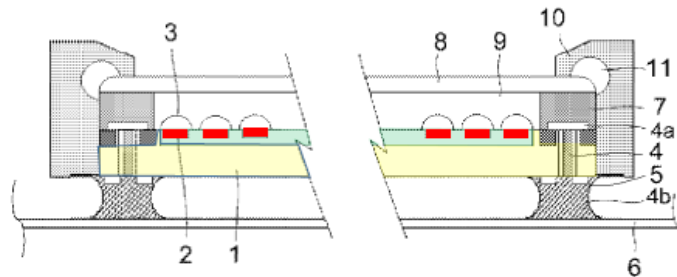


Figure 1 is a sectional view of the image pickup device of Asano, as annotated by Petitioner. Ex. 1006 ¶ 19. In the annotated Figure 1, the

¹¹ Dr. Afromowitz asserts that Asano does not include any “discussion of a PN junction” (Ex. 2002 ¶ 43), but does not dispute Mr. Guidash’s testimony that one of skill in the art would understand that there must, in fact, be such a PN junction in order for the device of Asano to operate as intended.

n-type layer Petitioner relies on as teaching the claimed “first conductivity type second semiconductor layer” is highlighted in red, with the p-type well (which Petitioner maps to the claimed “first semiconductor layer”) highlighted in green, and wafer 1 (which Petitioner maps to the claimed “substrate”) highlighted in yellow. Pet. 42.

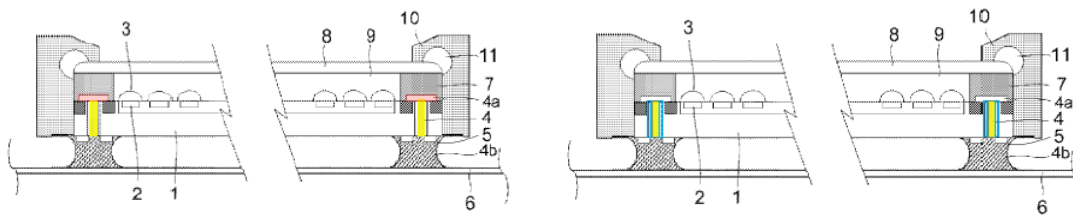
Based on this evidence, we agree that Asano teaches a first conductivity type second semiconductor layer formed in the first semiconductor layer.

a through electrode formed in a through hole penetrating through the semiconductor substrate in a thickness direction of the semiconductor substrate

a pad portion formed on the main surface of the semiconductor substrate and connected to the through electrode

a side insulating film formed at a side surface of the through electrode

Two additional annotated versions of Figure 1, provided by Petitioner (Pet. 42, 45) are reproduced below.



Each annotated version of Figure 1 is a sectional view of the image pickup device of Asano, as annotated by Petitioner. Ex. 1006 ¶ 19. The annotated versions of Figure 1 show electrodes 4 (highlighted in yellow), electrode pads 4a (highlighted in pink), and localized oxide film 17 (highlighted in blue), upon which Petitioner relies as teaching the claimed through electrode, pad portion, and side insulating film, respectively. Pet. 42 (citing

Ex. 1006 ¶ 20; Ex. 1002 ¶ 234), 43 (citing Ex. 1006 ¶ 20; Ex. 1002 ¶ 237), 44 (citing Ex. 1006 ¶ 42; Ex. 1002 ¶ 240).

As can be seen in the figures above, and as described in Asano, electrodes 4 are “formed in a through hole penetrating through the semiconductor substrate in a thickness direction of the semiconductor substrate,” as claimed. *Id.* at 42–43 (citing Ex. 1006 ¶¶ 38–39, 41, Figs. 2a, 2b; Ex. 1002 ¶¶ 235–236). As also can be seen in the figures above, electrode pads 4a are “formed on the main surface of the semiconductor substrate.” *Id.* at 43 (citing Ex. 1006 ¶ 20; Ex. 1002 ¶ 237). Asano also teaches that electrodes 4 are “connected to” electrode pads 4a. Ex. 2006 ¶ 20; *see* Pet. 43. The figures above also show localized oxide film 17 being “formed at a side surface of the through electrode,” as claimed. Pet. 45 (citing Ex. 1002 ¶¶ 242–243); *see* Ex. 1006 ¶ 42, Fig. 3; Ex. 1002 ¶¶ 239–241).

Based on this evidence, we agree that Asano teaches the claimed through electrode, pad portion, and side insulating film.

Claim 2

Regarding claim 2, which recites that “the through hole penetrates through only a first conductivity type area of the semiconductor substrate,” (Ex. 1001, 16:24–26), Petitioner relies on Figure 8 of Asano, which is similar to Figure 1, and “shows an embodiment where the through holes containing electrodes 4” “penetrat[e] only through the N-type substrate 1,” as teaching this claim feature. Pet. 45–46 (citing Ex. 1006 ¶¶ 20, 26, Fig. 8; Ex. 1002 ¶¶ 245–247).

Patent Owner argues that “Petitioner again relies on a nonobvious mixture of embodiments in Asano.” PO Resp. 27. According to Patent

Owner, Mr. Guidash “fails to even attempt to tie [the interline CCD discussion] of Asano to the embodiments of Figures 1 and 8.” *Id.* at 29. In particular, Patent Owner argues that in Petitioner’s proposed imaging device, the “p-type region of the protection diode would reside immediately below or at the periphery of the electrode pad 4a” and “thus, the electrode 4 would pass through both the p-type region and the n-type wafer as Petitioner has described the structure for purposes of . . . claim 1.” *Id.* at 30. According to Patent Owner, “for purposes of showing that the through hole of Figure 8 penetrates through only a first conductivity type area, Petitioner ignores the protection diode.” *Id.*

We disagree. As noted by Petitioner, Asano teaches “reshaping the p-type region into ‘an annular shape or plural divided regions’ so that the electrode can ‘be formed in the wafer region on the inside of the annular region or the plural divided regions where the region for the protection diode is absent.’” Pet. Reply 24 (quoting Ex. 1006 ¶¶ 45–47); see Ex. 1002 ¶ 247. Asano also recognizes advantages of “[f]orming [the penetrating electrodes] in the region having the same conductive type as that of the wafer,” such as “achieving highly precise and stable device characteristics.” Ex. 1006 ¶ 47; Pet. Reply 24. Thus, contrary to Patent Owner’s assertion, by reshaping the p-type region of the protection diode, “both the protection diode *and* the electrode can be formed immediately below the pad without penetrating through a PN-junction.” Pet. Reply 25 (citing Ex. 1006 ¶ 46).

Based on this evidence, we agree that Asano teaches the through hole penetrating through only a first conductivity type area of the semiconductor substrate.

3. Conclusion of Obviousness

Upon consideration of all the evidence, we conclude that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1 and 2 would have been obvious over Asano.

D. Obviousness in View of Asano and Shibayama

Petitioner asserts that claims 3 and 4 are unpatentable under 35 U.S.C. § 103 as obvious in view of Asano in combination with Shibayama. Pet. 2, 46–49. Patent Owner argues that the cited combination does not disclose all features of the claims and that one of skill in the art would not have combined the references in the manner asserted by Petitioner. PO Resp. 32–34. We have reviewed the entire record before us, including the parties’ contentions and supporting evidence presented during this trial. For the reasons explained below, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 3 and 4 would have been obvious in view of the asserted references.

1. Scope and Content of the Prior Art – Overview of Shibayama

Shibayama relates to a semiconductor device and process for producing the same. Ex. 1005, Abstract. Figure 17 of Shibayama is reproduced below.

FIG. 17

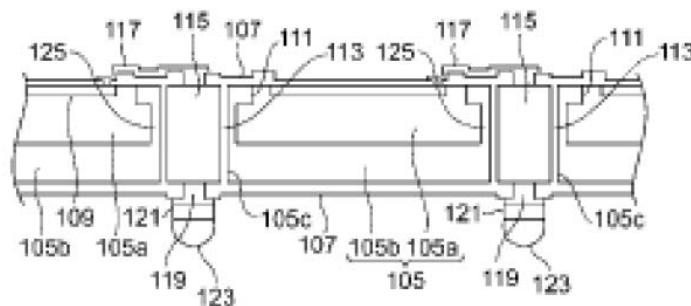


Figure 17 is a sectional view of the photodiode array of Shibayama.

Id. ¶ 54. As seen in Figure 17, the device of Shibayama includes through holes 105c with through-wiring 115 (i.e., a through electrode) disposed therein. *Id.* ¶¶ 61, 63. Through-wiring 115 is surrounded by oxidized film 113. *Id.* ¶¶ 61–63. During formation of through holes 105c, holes 141 are etched into substrate 105. *Id.* ¶¶ 83–84, Fig. 20(c). Shibayama describes that forming holes 141 can result in damage at the wall faces, resulting in unnecessary carriers, which can in turn cause dark current and/or noise. *Id.* ¶ 98.

The faces of the through holes are doped to create high concentration N-type regions 125 surrounding the through hole. *Id.* ¶ 85, Fig. 21(a). Shibayama notes that “the n-type high impurity concentration regions 125 formed along the wall faces defining the through holes can trap the unnecessarily generated carriers thereby preventing them from affecting the photodiodes.” *Id.* ¶ 76. The walls of holes 141 are then covered with oxidized film 113, and polysilicon (which serves as through-wiring 115) is deposited. *Id.* ¶¶ 85–87, Fig. 21(b).

2. Comparison of Asano and Shibayama to Claims 3 and 4;
Differences Between the Challenged Claims and the
Asano/Shibayama Combination

Claim 3 depends from claim 1, and recites “a first conductivity type third semiconductor layer formed in the semiconductor substrate around the through electrode.” Ex. 1001, 16:27–31. Claim 4 depends from claim 3, and recites “the third semiconductor layer is formed from the main surface of the semiconductor substrate to another surface of the semiconductor substrate opposite to the main surface of the semiconductor substrate.” *Id.* at

16:32–36. Petitioner relies on Shibayama as teaching these claim features. Pet. 46–49.

According to Petitioner, both Asano and Shibayama recognize that damage may result from forming through holes. Pet. 47 (citing Ex. 1006 ¶ 43; Ex. 1002 ¶¶ 75, 253); *see* Ex. 1005 ¶¶ 23, 76. Asano further recognizes that such damage can reduce sensor performance, and that imaging sensors are “extremely sensitive to damage and defects.” Ex. 1006 ¶ 43; *see* Pet. 47. Petitioner notes that “[t]o alleviate such damage, Shibayama proposes forming N-type regions 125 and/or the N⁺-type layers 25 along the wall faces of the through holes.” Pet. 47 (citing Ex. 1002 ¶ 75); *see* Ex. 1005 ¶¶ 23, 50–51, 76.

Petitioner contends that “[i]t would also have been obvious to form a semiconductor layer, such as the N-type high impurity concentration regions 125 or N⁺-type layers 25 of Shibayama, around the wall surfaces of the through holes disclosed in Asano.” Pet. 46–47. According to Petitioner, “[t]his would have reduced performance degradation caused by issues such as leakage or dark currents.” *Id.* at 47 (citing Ex. 1002 ¶ 255). It also would “trap undesirable carriers.” *Id.* (citing Ex. 1002 ¶¶ 255–256).

Petitioner argues that Asano, as modified, would include the claimed “first conductivity type third semiconductor layer formed in the semiconductor substrate around the through electrode,” as recited in claim 3. Pet. 48. Petitioner further argues that “it would have also been obvious to form the layers from the main surface of the substrate to an opposite surface as disclosed by Shibayama,” and as required by claim 4. *Id.* at 48–49 (citing Ex. 1002 ¶¶ 259, 261).

Patent Owner argues that “[t]here is no discussion in Asano of the conductivity of any substrate or layer in the Figure 1 embodiment.” PO Resp. 32 (citing Ex. 2002 ¶ 43). Thus, according to Patent Owner, “no matter the disclosure of Shibayama, it would not have been obvious to modify the Figure 1 embodiment of Asano to include ‘a first conductivity type third semiconductor layer formed in the semiconductor substrate around the through electrode,’ because there is no discussion at all regarding any conductivity within the Figure 1 embodiment.” *Id.* (citing Ex. 2002 ¶ 43). Contrary to Patent Owner’s assertion, Asano discloses that the conductivity type of the substrate is n-type. Ex. 1006 ¶ 45; see Pet. Reply 25. Shibayama also discloses an n-type substrate and teaches using “n-type high impurity concentration regions 125 formed along the wall faces defining the through holes” in the substrate, to trap “unnecessary carriers.” Ex. 1005 ¶ 76; see Pet. Reply 25–26. Thus, Patent Owner’s argument is not persuasive.

Patent Owner also argues that Petitioner’s analysis regarding the combination of references is deficient. PO Resp. 33–34. As noted above, Mr. Guidash testifies that both Asano and Shibayama recognize that damage may result from forming through holes in a substrate. Ex. 1005 ¶¶ 23, 75, 76, 253. Mr. Guidash further testifies that “[w]hile Asano discloses . . . forming through holes that penetrate an area of the substrate with only one conductivity type (N-type), leakage or dark current may nonetheless result from, for example, mechanical damage from etching, as described in Shibayama.” *Id.* ¶ 255 (citing *id.* ¶¶ 245–247); see also Ex. 1013, 17:23–18:8 (Dr. Afromowitz testifying that dark current cannot be eliminated, only reduced.). According to Mr. Guidash, “[m]odifying Asano by forming an N-type semiconductor layer, such as layers 25 or 125 disclosed by

Shibayama, on the wall faces of the through holes and around the through electrodes would have been well within ordinary skill and would have produced no unpredictable results.” Ex. 1002 ¶ 256. Mr. Guidash further testifies that methods familiar to one of ordinary skill in the art, such as diffusion or ion implantation, could be used to form such layers. *Id.* ¶¶ 186, 257. Dr. Afromowitz does not provide testimony specifically rebutting the testimony of Mr. Guidash on these points, and we credit Mr. Guidash’s testimony in this regard.

Based on the above evidence, we are persuaded that Petitioner’s proposed modification is the “combination of a known imaging device (Asano Fig. 1) with a known solution (forming an N-type semiconductor layer or region around through electrodes) to address an issue (reduce the impact of common issues such as leakage current and dark current) well-understood by those with ordinary skill in the art.” Pet. 48. We further are persuaded that the modification was well within the ordinary skill in the art to implement and would have yielded predictable results. *KSR*, 550 U.S. at 416; see Pet. 48 (citing Ex. 1005 ¶¶ 43, 85; Ex. 1006 ¶ 48; Ex. 1002 ¶ 257; Ex. 1001, 14:35–37), 49 (citing Ex. 1005 ¶ 23; Ex. 1002 ¶¶ 261–262).

Based on this evidence, we agree that the combination of Asano and Shibayama teaches the limitations of claims 3 and 4.

3. Conclusion of Obviousness

Upon consideration of all the evidence, we conclude that Petitioner has demonstrated, by a preponderance of the evidence, that claims 3 and 4 would have been obvious over Asano and Shibayama.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1 and 2 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Asano. We also determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 3 and 4 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Asano and Shibayama.

IV. ORDER

Accordingly, it is:

ORDERED, based on a preponderance of the evidence, that claims 1–4 of U.S. Patent 8,030,724 B2 are *unpatentable*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2016-00940
Patent 8,030,724 B2

PETITIONER:

Matthew A. Smith
Andrew S. Baluch
SMITH BALUCH LLP
smith@smithbaluch.com
baluch@smithbaluch.com

Zhuanjia Gu
TURNER BOYD LLP
gu@turnerboyd.com

PATENT OWNER:

Terry Saad
Nicholas Kliewer
BRAGALONE CONROY PC
tsaad@bcpc-law.com
nkliewer@bcpc-law.com