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Paper 10
Entered: January 3, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
and GLOBALFOUNDRIES U.S. INC.,
Petitioners,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01246[1]
Patent 7,126,174 B2

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a)

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[1] Case IPR2016-01247 has been consolidated with this proceeding. GlobalFoundries U.S. Inc.'s motions for joinder in Cases IPR2017-00925 and IPR2017-00926 were granted.

I. BACKGROUND

Petitioner Taiwan Semiconductor Manufacturing Company, Ltd. filed two Petitions requesting *inter partes* review of claims 1–12 and 14–18 of U.S. Patent No. 7,126,174 B2 (Ex. 1001, "the '174 patent") pursuant to 35 U.S.C. § 311(a), as listed in the following chart.

Case Number	Challenged Claims	Petition
IPR2016-01246	1–3, 5–7, 9–12, and 14–18	Paper 2 ("Pet.")
IPR2016-01247	1, 4, 5, 8–12, 14, and 16	Paper 2 ("-1247 Pet.")

On January 4, 2017, we instituted an *inter partes* review of claims 1–12 and 14–18 on four grounds of unpatentability and consolidated Case IPR2016-01247 with Case IPR2016-01246 (Paper 8, "Dec. on Inst.").[2] Patent Owner Godo Kaisha IP Bridge 1 filed a Patent Owner Response (Paper 14, "PO Resp."), Petitioner filed a Reply (Paper 21, "Reply"), and Patent Owner filed a Sur-Reply (Paper 37, "Sur-Reply"), pursuant to our authorization (Paper 28). Petitioner filed a Motion to Exclude (Paper 29, "Pet. Mot.") certain evidence submitted by Patent Owner. Patent Owner filed an Opposition (Paper 39, "PO Mot. Opp.") and Petitioner filed a Reply (Paper 42, "Pet. Mot. Reply"). Patent Owner filed a Motion to Exclude (Paper 32, "PO Mot.") certain evidence submitted by Petitioner. Petitioner

[2] On June 9, 2017, we granted motions for joinder filed by GlobalFoundries U.S. Inc. ("GlobalFoundries") in Cases IPR2017-00925 and IPR2017-00926, and authorized GlobalFoundries to participate in this proceeding only on a limited basis. *See* Paper 20; IPR2017-00925, Paper 13; IPR2017-00926, Paper 12. Although the papers referenced herein were filed by Taiwan Semiconductor Manufacturing Company, Ltd., we refer to both entities as "Petitioner" throughout this Decision.

filed an Opposition (Paper 40, "Pet. Mot. Opp.") and Patent Owner filed a Reply (Paper 41, "PO Mot. Reply"). An oral hearing was held on August 7, 2017, and a transcript of the hearing is included in the record (Paper 46, "Tr.").[3]

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–12 and 14–18 are unpatentable.

A. The '174 Patent

The '174 patent discloses a "semiconductor device including transistors and connection[s] between the transistors for constituting [a large-scale integration (LSI) integrated circuit (IC)] with high integration and a decreased area." Ex. 1001, col. 1, ll. 13–16. At the time of the '174 patent, various improvements had been made in semiconductor manufacturing due to "increasing demands for more refinement of the semiconductor device." *Id.* at col. 1, ll. 17–22. The '174 patent describes one known method of forming an isolation structure (for shielding devices from each other on a substrate) known as Local Oxidation of Silicon (LOCOS), which was "conventionally adopted in view of its simpleness and low cost." *Id.* at col. 1, ll. 22–25. The LOCOS isolation method involves selective oxidation of a silicon substrate, but has a disadvantage in that it results in a "bird's beak" overhanging area of silicon dioxide. *Id.* at col. 1, ll. 29–31. "As a result, the dimension of a transistor is changed because an

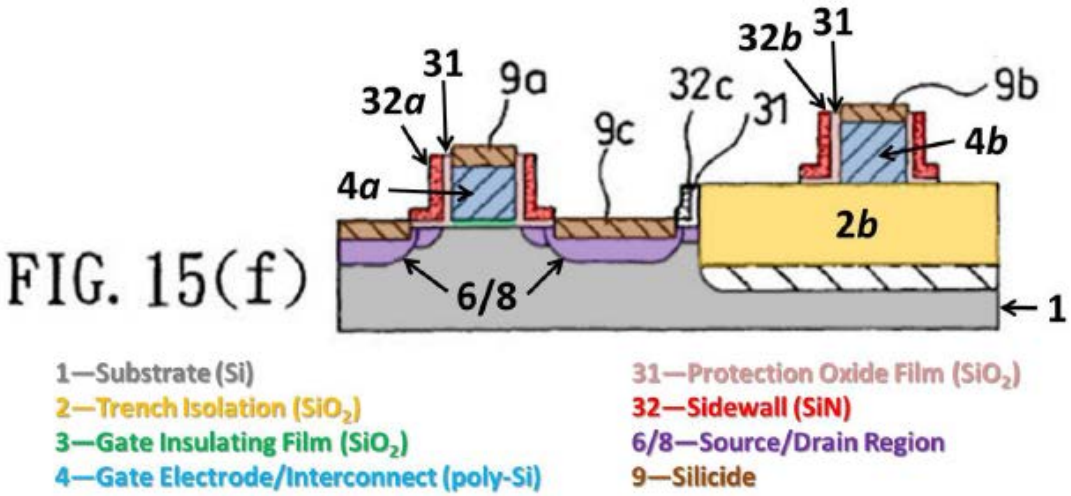
[3] Pursuant to our authorization provided to the parties by email, the parties filed a joint errata to the hearing transcript (Paper 47).

insulating film of the isolation invades [the] transistor region against the actually designed mask dimension." *Id.* at col. 1, ll. 31–34. According to the '174 patent, compared to LOCOS, "trench buried type isolation" (or "trench isolation") was determined to be "more advantageous for manufacturing a refined semiconductor device." *Id.* at col. 1, ll. 25–28.

The '174 patent describes a "conventional semiconductor device" with a trench isolation structure "whose top surface is flattened so as to be at the same level as the top surface of the silicon substrate" (as shown in Figure 17) or whose top surface is higher than the surface of the silicon substrate (as shown in Figure 20(e)). *Id.* at col. 1, l. 52–col. 2, l. 6 (structure 2b), col. 4, l. 16–col. 5, l. 11 (trench isolation 105a). By using the "conventional trench isolation" structure, "the dimensional change of the source/drain region can be suppressed because the bird's beak" created using LOCOS is avoided. *Id.* at col. 4, ll. 16–19, col. 5, ll. 12–17. According to the '174 patent, using the trench isolation method caused various problems of its own due to the etching required. *Id.* at col. 5, ll. 21–58.

The '174 patent describes various embodiments of semiconductor devices and methods of manufacturing the same. The manufacturing process for Embodiment 10 is depicted in the sequence of Figures 12, 13(a)–(e), and 15(a)–(f). *Id.* at col. 21, ll. 33–34, col. 26, ll. 36–45 (referring to the previously described process of Embodiment 8).

Petitioner provides on page 13 of the Petition a colored and annotated version of Figure 15(f) of the ’174 patent, reproduced below, which is consistent with the ’174 patent’s disclosure.



The figure above depicts a device including isolation 2b, which is the result of forming a trench in silicon substrate 1 and filling it with insulating material. *Id.* at col. 21, ll. 39–50, col. 22, ll. 34–44. “[E]lectrode sidewalls 32a, interconnection sidewalls 32b and a step sidewall 32c each having an L-shape remain on the sides of the gate electrode 4a, the gate interconnection 4b and the step portion, respectively.” *Id.* at col. 27, ll. 4–8. The ’174 patent describes various advantages of forming “L-shaped sidewalls” in the manner disclosed. *Id.* at col. 27, ll. 34–47.

B. Illustrative Claim

Claim 1 of the ’174 patent recites:

> 1. A semiconductor device, comprising:
>
> a trench isolation surrounding an active area of a semiconductor substrate;
>
> a gate insulating film formed over the active area;
>
> a gate electrode formed over the gate insulating film;

first L-shaped sidewalls formed over the side surfaces of the gate electrode;

first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area

an interconnection formed on the trench isolation; and

second L-shaped sidewalls formed over the side surfaces of the interconnection.

C. Prior Art

The pending grounds of unpatentability in the instant *inter partes* review are based on the following prior art:

U.S. Patent No. 4,506,434, issued Mar. 26, 1985 (Ex. 1010, "Ogawa");

U.S. Patent No. 5,021,353, issued June 4, 1991 (Ex. 1017, "Lowrey");

U.S. Patent No. 5,153,145, issued Oct. 6, 1992 (Ex. 1002, "Lee"); and

U.S. Patent No. 5,539,229, filed Dec. 28, 1994, issued July 23, 1996 (Ex. 1015, "Noble").

D. Pending Grounds of Unpatentability

The instant *inter partes* review involves the following grounds of unpatentability:

References	Basis	Claims
Lee and Noble	35 U.S.C. § 103(a)[4]	1–3, 5–7, 9–12, and 14–18

[4] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Because the challenged claims of the '174 patent have an effective filing date before the

References	Basis	Claims
Lee and Ogawa	35 U.S.C. § 103(a)	1–3, 5–7, 9–12, and 14–18
Lowrey and Noble	35 U.S.C. § 103(a)	1, 4, 5, 8–12, 14, and 16
Lowrey and Ogawa	35 U.S.C. § 103(a)	1, 4, 5, 8–12, 14, and 16

II. ANALYSIS

A. Claim Interpretation

The ’174 patent expired on July 24, 2016 (after the filing of the Petitions). We previously granted Patent Owner’s motions requesting a district court-type claim interpretation approach under 37 C.F.R. § 42.100(b). Dec. on Inst. 6, 28. In district court, claim terms are given their plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Patent Owner proposes various interpretations that were adopted by the district court in a related case where Patent Owner asserted the ’174 patent against another party. PO Resp. 41–43; *see* Ex. 3001, 7–11,

effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103.

App'x A. Patent Owner, however, does not base any of its arguments in its Response on those interpretations or explain how they impact the analysis of the challenged claims. As in the Decision on Institution, we conclude that no claim terms require explicit interpretation. *See* Dec. on Inst. 7. Nevertheless, we have reviewed the district court's interpretations and conclude that they are both reflective of the plain and ordinary meaning of the terms and consistent with our analysis of the prior art herein.

B. Principles of Law

To prevail in challenging claims 1–12 and 14–18 of the '174 patent, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). The question of obviousness is resolved on the basis of underlying factual determinations, including "the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved."[5] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

[5] Additionally, secondary considerations, such as "commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418 (for an obviousness analysis, "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does").

A motivation to combine the teachings of two references can be "found explicitly or implicitly in market forces; design incentives; the 'interrelated teachings of multiple patents'; 'any need or problem known in the field of endeavor at the time of invention and addressed by the patent'; and the background knowledge, creativity, and common sense of the person of ordinary skill." *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013) (citation omitted). Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'" (citation omitted)).

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may have relevancy." *Graham*, 383 U.S. at 17–18. The record, however, lacks any such evidence.

C. Level of Ordinary Skill in the Art

Petitioner argues[6] that a person of ordinary skill in the art at the time of the '174 patent would have had "(1) the equivalent of a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, or the equivalent; (2) a working knowledge of semiconductor processing technologies for integrated circuits; and (3) at least two years of experience in related semiconductor processing analysis, design, and development." Pet. 16 (citing Ex. 1004 ¶ 72).[7] Patent Owner argues that a person of ordinary skill in the art would have had "at least a Bachelor's degree in Electrical, Materials, Mechanical, or Chemical Engineering, or a related degree, and at least two years of experience working in semiconductor processing and fabrication, semiconductor equipment manufacturing, or semiconductor materials." PO Resp. 23 (citing Ex. 2012 ¶ 29). Patent Owner disputes Petitioner's proposed definition as not requiring any experience with "semiconductor processing and fabrication." *Id.* at 24. According to Patent Owner, "[d]esign is different from fabrication" and "actual fabrication experience is an important component to a [person of ordinary skill in the art's] understanding of what can practically, rather than theoretically be fabricated." *Id.*

[6] Petitioner makes a number of similar arguments in both of its Petitions. As to these arguments, we refer only to the papers filed in Case IPR2016-01246 for ease of reference.

[7] We previously authorized the parties to file corrected versions of three declarations and expunged the original versions. *See* Dec. on Inst. 7 n.4; Paper 18. Accordingly, we refer herein to the versions of Exhibit 1004 filed by Petitioner on September 13, 2016 (now numbered as Exhibits 1004 and 1024), and the version of Exhibit 2012 filed by Patent Owner on June 8, 2017.

Based on the record developed during trial, including our review of the '174 patent and the types of problems and solutions described in the '174 patent and cited prior art, we agree with Petitioner's assessment of the level of ordinary skill in the art and apply it for purposes of this Decision. Patent Owner's proposed definition is overly broad. For example, it requires experience with semiconductor processing and fabrication, equipment manufacturing, "or" materials. *Id.* Thus, an individual having only general experience with semiconductor materials would meet the requirement.

Petitioner's definition, on the other hand, is more specifically directed to the technology described in the '174 patent, requiring both knowledge of "semiconductor processing technologies *for integrated circuits*" and "experience in *related* semiconductor processing analysis, design, and development." Pet. 16 (emphases added); *see* Ex. 1001, col. 1, l. 13–col. 11, l. 9 (disclosing that "[t]he present invention relates to a semiconductor device including transistors and connection between the transistors" and describing previous designs of semiconductor devices with high integration and high performance, issues with previous designs, and potential solutions); Ex. 1004 ¶¶ 41–63 (testifying as to the state of the art of metal-oxide-semiconductor field-effect transistors (MOSFETs) and isolation structures, including the industry's movement from LOCOS isolation to shallow trench isolation (STI), by the time of the '174 patent). It also requires practical experience ("working knowledge" of processing technologies and experience in "related" analysis, design, and development), contrary to Patent Owner's argument. *See* PO Resp. 24. Finally, given the disclosures in the '174 patent and cited prior art, we agree with Petitioner that a Master of Science degree (or equivalent) in the relevant area better reflects the level

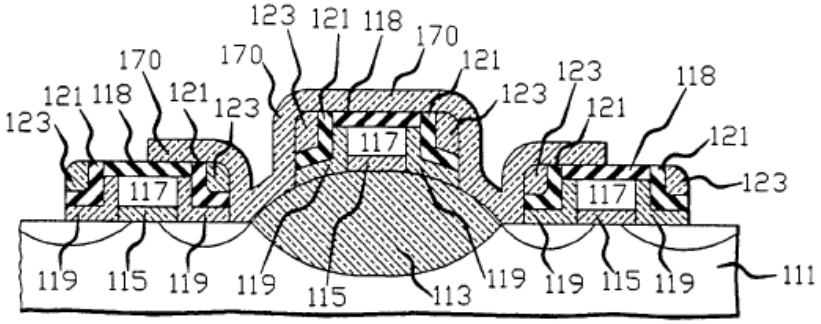
of education and training that an ordinarily skilled artisan would have possessed at the time than a Bachelor's degree, as Patent Owner contends.

D. Obviousness Ground Based on Lee and Noble (Claims 1–3, 5–7, 9–12, and 14–18)

1. Lee

Lee describes a "field effect transistor with a gate stack formed upon a semiconductor substrate." Ex. 1002, col. 1, ll. 57–59. "During fabrication, three material layers are formed over the gate stack and upon the substrate. At least the outer two material layers are sequentially anisotropically etched, creating two spacers adjacent the gate stack (and gate runners)." *Id.* at col. 1, ll. 59–63. Lee describes a fabrication process depicted in Figures 11–15. Figure 15 of Lee is reproduced below.

FIG. 15



The device shown above includes, *inter alia,* field oxide 113 formed on substrate 111, and spacer layer 121 of silicon nitride or silicon oxynitride. *Id.* at col. 6, ll. 47–51, col. 7, ll. 6–16.

2. Noble

Noble describes "shallow trench isolation (STI) in which the insulating material is raised above the surface of the semiconductor."

Ex. 1015, col. 1, ll. 8–10. Noble describes a fabrication process depicted in Figures 9–13. Figure 13 of Noble is reproduced below.

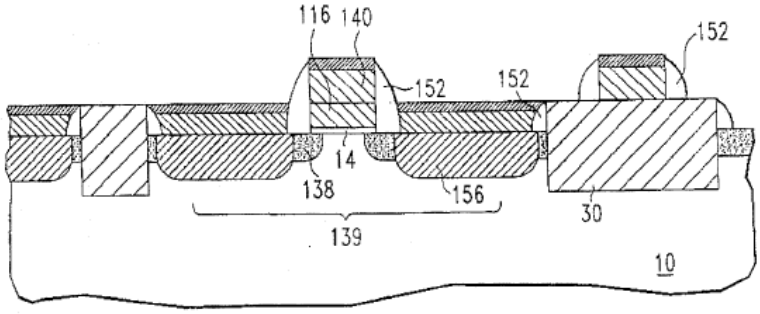


FIG. 13

The device shown above includes, *inter alia*, raised STI 30, created by etching to form a trench that is filled with insulating material. *Id.* at col. 4, ll. 40–46, Figs. 3–4.

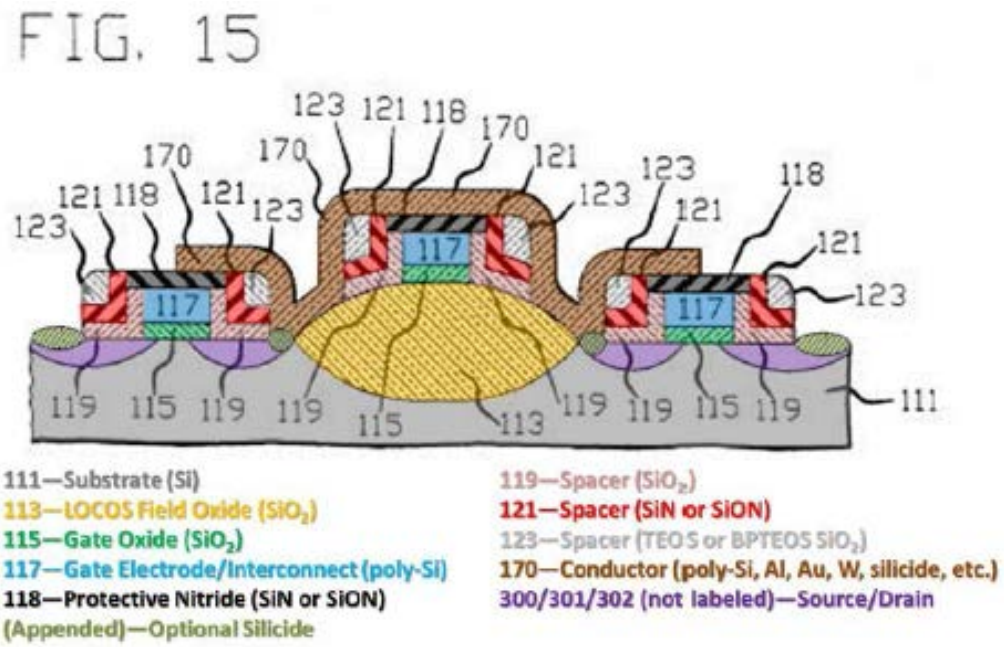
3. Claim 1

a. Whether Lee and Noble Collectively Teach All of the Limitations of Claim 1

Petitioner explains in detail how Lee[8] and Noble collectively teach every limitation of claim 1, relying on the testimony of Sanjay Kumar Banerjee, Ph.D., as support. Pet. 21, 30–44 (citing Ex. 1004 ¶¶ 98–126). Specifically, Petitioner relies on Lee as teaching all of the limitations other than a "trench isolation." *Id.* Petitioner argues that Lee's disclosed device has an isolation (i.e., field oxide 113) surrounding an active area of a semiconductor substrate (i.e., substrate 111), a "gate insulating film" (i.e., gate oxide 115) formed over the active area, a "gate electrode" (i.e., layer 117 above the source and drain) formed over gate oxide 115, "first L-shaped

[8] Lee was not considered during prosecution of the '174 patent. *See* Ex. 1001, (56).

sidewalls" (i.e., layer 121) formed over the side surfaces of layer 117, "first silicide layers" (described in Lee but not shown explicitly in Figure 15) formed on the sides of the first L-shaped sidewalls within the active area, an "interconnection" (i.e., layer 117 above field oxide 113), and "second L-shaped sidewalls" (i.e., layer 121) formed over the side surfaces of the interconnection. *Id.* (citing Ex. 1002, col. 3, ll. 9–11, col. 7, ll. 5–16 (disclosing that "spacers 19 and 21 (which are nested beneath spacer 23) have a generally 'L-shaped' appearance (in cross-section)," and layer 121 is formed "in a manner analogous to that depicted" in the figures depicting spacers 19 and 21)). Petitioner provides on page 18 of the Petition the following colored and annotated version of Figure 15 of Lee, which we find is consistent with Lee's disclosure.



The figure above depicts Lee's device including field oxide 113, which is formed using LOCOS rather than trench isolation. *Id.* at 32–33.

Petitioner relies on Noble as teaching a "trench isolation," citing Noble's description of STI 30. *Id.* at 32. Petitioner provides on page 19 of

the Petition the following colored and annotated version of Figure 13 of Noble, which we find is consistent with Noble's disclosure.

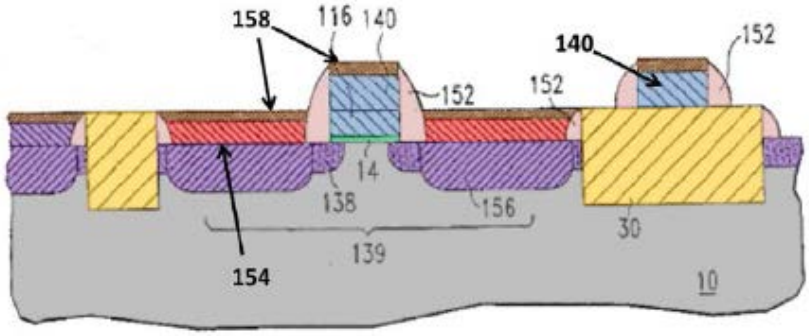


FIG. 13

10—Substrate (Si)
30—Raised STI
14—Gate Dielectric
116/140—Gate Electrode
154—Raised Source/Drain
152—Dielectric Spacers
138/156—Substrate Source/Drain
158—Silicide Regions (silicide)
140—Interconnection

The figure above depicts Noble's STI 30, as well as various components that are very similar to those of Lee, such as the gate electrode, interconnection, gate dielectric, source, drain, and silicide regions. *Id.* at 26–28 (describing the similar structures of Lee and Noble), 32–33.

As to the combined teachings of the references, Petitioner's position is that a person of ordinary skill in the art would have been motivated to replace Lee's LOCOS isolation with Noble's STI. *Id.* at 21 (arguing that a person of ordinary skill in the art "would have understood that *Noble*'s STI was a known substitute for *Lee*'s LOCOS isolation," and "[t]he combined teachings discussed in [the Petition] refer to the teachings of *Lee*, with its LOCOS isolation replaced by *Noble*'s STI"), 31–33 (relying on Noble for the "trench isolation" limitation), 40–42 (arguing that Lee teaches an "interconnection" that would be on the "trench isolation" as taught by Noble). Although the references have numerous features in common, Petitioner's obviousness ground is premised on only one change needing to

be made to Lee to render the claim obvious—replacing the LOCOS isolation in Lee's device (field oxide 113) with the trench isolation of Noble (STI 30). *See id.* Petitioner's arguments as to how Lee and Noble collectively teach every limitation of claim 1 are supported by the testimony of Dr. Banerjee and are persuasive. *See* Pet. 30–44; Ex. 1004 ¶¶ 98–126.

Patent Owner makes four arguments regarding the combined teachings of the references. First, Patent Owner argues that the combined device based on the teachings of Lee and Noble would not have "second L-shaped sidewalls," as recited in claim 1. PO Resp. 70–72. Patent Owner contends that the purpose of the alleged second sidewalls in Lee (layer 121 shown in red in the figure above) is to insulate the "gate runner" (layer 117)[9]

[9] Lee refers to the portion of layers 115, 117, and 118 above field oxide 113 as "gate level runner 203" or "runner 203":

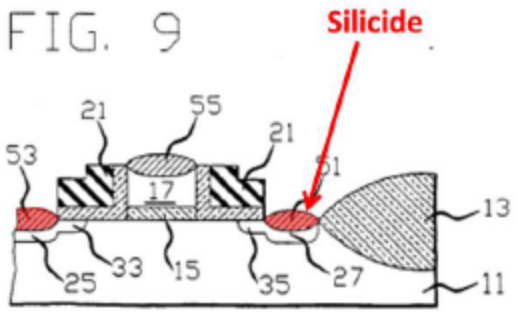
> Turning to FIG. 12, it may be noted that layers 118, 117, and 115 have been patterned to produce gates 201 and 205 together with runner 203 which extends over field oxide 113. Thus, it will be noted that FIGS. 12–15 depict the formation of two adjacent transistors separated by field oxide 113. Furthermore, gate level runner 203 extends along field oxide 113. Gate level runner 203 may be connected (although not shown in the particular cross-section of FIG. 12) to gate 201 or 205 or to the gate, source, or drain of some other transistor (not shown).

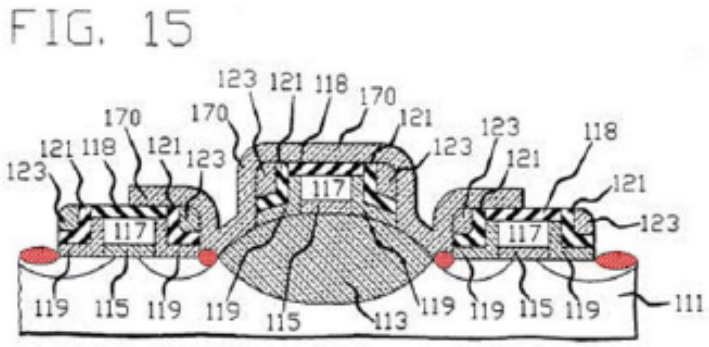
Ex. 1002, col. 6, l. 62–col. 7, l. 4; *see also id.* at col. 7, l. 40–col. 8, l. 5 ("The presence of protective nitride layer 118 together with nitride layer 121 which flanks runner 203 prevents electrical contact between patterned layer 170 and the conductive polysilicon heart 117' of runner 203. . . . Thus, the inventive structure has facilitated the formation of a sub-gate level interconnection between junction regions of different transistors (i.e., a connection formed prior to passivation dielectric deposition and contact window opening) without the possibility of shorting to a gate runner.").

so that conductive layer 170 can go over it without shorting, but "if the trench isolation of *Noble* is substituted for the LOCOS isolation of *Lee*, the necessary result is that there will be no gate runner on the trench isolation, and therefore no need for the second sidewalls on top of the trench isolation." *Id.* (emphasis omitted). We are not persuaded. Petitioner relies on Lee, which discloses an "interconnection" (i.e., layer 117) and "second L-shaped sidewalls" (i.e., layer 121), not Noble. Pet. 21, 40–44. Regardless of whether there would be a "need" for the sidewalls, Lee discloses them. Patent Owner and Dr. Schubert also do not explain sufficiently why it would be "necessary" to remove layer 117 on top of the isolation if Lee's LOCOS isolation were replaced with Noble's STI. *See* PO Resp. 72; Ex. 2012 ¶¶ 215–222.

Second, and similar to the preceding argument, Patent Owner asserts that any sidewalls on the side surfaces of the interconnection would not be "L-shaped" because Noble's gate stack and interconnection stack have different heights, and fabricating "second L-shaped sidewalls" (i.e., "sidewalls that substantially resemble a capital 'L' or its mirror image") is "highly problematic and would require re-engineering of *Lee*'s sidewall fabrication module." PO Resp. 73–78. Patent Owner contends that Lee's sidewalls would not be L-shaped "[g]iven the necessarily shorter height of the interconnect on top of the trench isolation." *Id.* at 78. Again, Petitioner relies on Lee, not Noble, for the "interconnection" and "second L-shaped sidewalls" limitations of claim 1. Pet. 40–44. Substituting Noble's STI in place of Lee's LOCOS isolation merely modifies what is below Lee's interconnection.

Third, Patent Owner argues that Lee in combination with Noble does not teach "first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area," as recited in claim 1. PO Resp. 79–81. Petitioner relies on Lee for this limitation. Pet. 38–40. Lee teaches "forming silicide regions 51 [and] 53, . . . respectively, above junctions 25 and 27," shown in Figures 7–10, then states in connection with its second disclosed process that "[s]hould salicidation be desired over source/drain regions 300, 301, and 302 it may also be performed in a manner analogous to that depicted in FIG. 9." Ex. 1002, col. 4, ll. 44–51, col. 7, ll. 22–25. Petitioner provides the following annotated versions of Figures 9 and 15 (Pet. 39–40) showing the relevant silicide layers.





The annotated figures above depict silicide layers in red formed on the sides of the L-shaped sidewalls. Patent Owner acknowledges that Figure 9 has the recited silicide layers, but notes that it has no interconnection, and Figure 15

has an interconnection but no silicide layers. PO Resp. 79. According to Patent Owner, it is unclear where the silicide layers would be in Figures 14 and 15 because Lee states that they are formed "over source/drain regions 300, 301, and 302" but does not label those areas. *Id.* at 79–80. Patent Owner argues that

> because the exposed portions of the source/drain regions closest to the LOCOS isolation in Fig. 14 are much smaller than the exposed portions of the source/drain region farthest from the LOCOS isolation in Fig. 14, the inventors of Lee might have meant that only those two regions are intended to have silicide on them. In other words, a silicide layer would be formed on only *one* side of the gate electrode, and *not* on both sides of the gate electrode, while the claim requires silicide layers formed on *both* sides of the L-shaped sidewalls.

Id. at 80–81 (citing Ex. 2012 ¶¶ 234–236). Patent Owner further argues that "it is impossible to know what the dimensions of the device proposed by Petitioner would be to determine where silicide layers would be appropriate without knowing exactly how the trench isolation of *Noble* would be inserted" in place of the LOCOS isolation of Lee. *Id.* at 81 (citing Ex. 2012 ¶ 237).

We are not persuaded of any ambiguity in Lee. Figure 9 of Lee shows silicide layers 51 and 53 on the sides of L-shaped sidewalls (i.e., layer 21). Figure 15 need not depict such layers, as the textual description that they may be created "in a manner analogous to that depicted in FIG. 9" is sufficient. *See* Ex. 1002, col. 7, ll. 22–25; *Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1380 (Fed. Cir. 2005) (finding that a figure is not necessary because "disclosing the embodiment in textual form is enough"). Formed in an "analogous" manner, the silicide layers would be located on the sides of the L-shaped sidewalls (i.e., layer 121) above the source and

drain regions (shown as semicircles[10] but not labeled) in Figure 15, just as they are located on the sides of the L-shaped sidewalls (i.e., layer 21) above junctions 25 and 27 in Figure 9. Further, we agree with Petitioner's explanation that the dimensions of the combined device based on Lee and Noble would not impact where the silicide layers are located, as "the openings used to define the source/drain ion implant regions also define where the source/drain silicide forms" in a normal self-aligned silicide process. *See* Reply 44; Ex. 1057 ¶ 150 (citing Ex. 1045, 398).

Fourth, pointing to Petitioner's annotated version of Figure 15 above, Patent Owner argues that the figure "shows red-colored pinpoint spots of indeterminate size or dimension," which "would run in a line (wire or cylinder) along the width of the device." PO Resp. 81–82. According to Patent Owner, "[a] line is not a 'layer.'" *Id.* at 82. We are not persuaded. Patent Owner does not explain in any detail what level of thickness would differentiate a "line" from a "layer." Moreover, Lee does not describe components 51 and 53 in Figure 9 as "lines," but rather "silicide regions," and states that salicidation may be performed in an "analogous" manner in Figures 14 and 15. Ex. 1002, col. 4, ll. 44–51, col. 7, ll. 22–25; *see* PO Resp. 85 (agreeing that Figure 9 "shows a silicide *layer*"). We find that this is a sufficient disclosure of silicide "layers" as recited in claim 1.

Thus, we are persuaded that Lee and Noble collectively teach every limitation of claim 1.

[10] An annotated version of Figure 15 showing the source/drain regions in Figure 15 appears on page 49 of the Petition.

b. Whether a Person of Ordinary Skill in the Art Would Have Been Motivated to Combine Lee and Noble and Would Have Had a Reasonable Expectation of Success in Doing So

Petitioner provides ample explanation as to why a person of ordinary skill in the art would have been motivated to replace Lee's LOCOS isolation with a trench isolation, based on the teachings of Noble. Pet. 21–30. Petitioner's assertions are supported by the references themselves, the state of the art at the time of the '174 patent, and the testimony of Dr. Banerjee. *See id.* (citing Ex. 1004 ¶¶ 82–97).

First, Petitioner explains the history of the art, where LOCOS was "cheaper and simpler" and the bird's beak problem "was not a major detriment to device density yet" in October 1989 at the time that Lee was filed, but by the mid-1990s, the industry had begun moving away from LOCOS and toward trench isolation. *Id.* at 22; *see* Ex. 1004 ¶¶ 48–55 (Dr. Banerjee describing the history of both types of isolation structures and testifying that the industry faced a choice in the 1990s—"increase device density and add expense (trench isolation), or maintain device density and costs (LOCOS)"—and "decided in favor of scaling," as it typically did), 83–85; Ex. 1015, (22) (Noble filed on December 28, 1994). Indeed, the '174 patent itself states that for "mass-production techniques," the "isolation forming method ha[d] started to be changed to the trench isolation method in which the dimensional change is very small." Ex. 1001, col. 1, ll. 36–43 (citing a specific example where IBM "introduced the trench isolation structure as a 0.5 μm CMOS [(complementary metal-oxide-semiconductor)] process"). The '174 patent describes "conventional" semiconductor devices of the time that had a trench isolation, either even with the top of the semiconductor substrate (shown in "Prior Art" Figure 17) or raised above

the surface of the semiconductor substrate (shown in "Prior Art" Figure 20(e)). *Id.* at col. 1, l. 44–col. 2, l. 6, col. 3, l. 53–col. 4, l. 19 (describing a "conventional trench isolation"); *see* Pet. 10–11, 23.

Other evidence demonstrates the industry trend toward trench isolation as well. Exhibit 1009 ("Schuegraf"), filed in October 1995, explains that LOCOS had been "[t]he most widely used technology" due to its "inherent simplicity in MOS process integration, cost effectiveness and adaptability," but "[i]n spite of its success, several limitations of LOCOS technology," including the bird's beak problem and lack of surface planarity, drove "the development of alternative isolation structures." *Id.* at col. 1, ll. 31–59.[11] Trench isolation technology was developed to overcome those limitations, and had become a recognized "alternative" to LOCOS. *Id.* at col. 1, l. 60–col. 2, l. 24; *see* Pet. 24; Ex. 1004 ¶¶ 52, 87–88. Ogawa similarly states that trench isolation was developed to overcome LOCOS's

[11] Petitioner cites a number of references, such as Schuegraf, as well as the "Background of the Invention" section of the '174 patent describing prior art semiconductor devices, that appropriately show the background knowledge that a person of ordinary skill in the art would have had in reading Lee and Noble, and that support Petitioner's arguments as to why a person of ordinary skill in the art would have been motivated to make the asserted combination and had a reasonable expectation of success. *See Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015) ("Art can legitimately serve to document the knowledge that skilled artisans would bring to bear in reading the prior art identified as producing obviousness."); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362–63 (Fed. Cir. 2013) (requiring consideration of "background information that could easily explain why an ordinarily skilled artisan would have been motivated to combine or modify the cited references to arrive at the claimed inventions"). We also address certain evidentiary arguments regarding one of the references, Exhibit 1014 ("Ueda"), below. *See infra* Section II.H.2.a.

drawbacks, such as the bird's beak problem, because LOCOS was "not necessarily satisfactory for the production of a semiconductor device having minute patterns." Ex. 1010, col. 1, ll. 17–66. Patent Owner's declarant, E. Fred Schubert, Ph.D., also acknowledged that there were "concerns that LOCOS isolation uses up too much space" and "[t]rench isolation was considered at that time, and was one of the candidates" to replace LOCOS. Ex. 1056, 75:6–77:2. Thus, the evidence shows that both LOCOS and trench isolation were known at the time of the '174 patent and that the industry trend was to use the latter rather than the former. *See KSR*, 550 U.S. at 418 (to determine whether there would have been a reason to combine teachings, it is often necessary to look to "the effects of demands known to the design community or present in the marketplace").

Second, Petitioner provides evidence that persons of ordinary skill in the art recognized LOCOS and trench isolation as substitutes, "interchangeable" with each other and "functionally equivalent." Pet. 5–6, 24–26. Schuegraf states that "Shallow Trench Isolation (STI) is used primarily for isolating devices of the same type and is often considered an alternative to LOCOS isolation." Ex. 1009, col. 2, ll. 20–22. Four other references cited by Petitioner state that either method may be used for their respective devices. Pet. 24–25; *see* Ex. 1011, col. 4, ll. 10–16; Ex. 1012, col. 3, ll. 8–10; Ex. 1013, col. 5, ll. 56–67; Ex. 1014, col. 22, ll. 49–52; Ex. 1004 ¶¶ 89–90. Dr. Banerjee also testifies that "LOCOS and STI are both methods for forming insulating materials in the same locations of the substrate to perform the same function," and "[t]hey are both performed near the very beginning in device processing." Ex. 1004 ¶ 82. This evidence demonstrates that a person of ordinary skill in the art reading Lee, for

example, would have viewed a trench isolation, such as the one disclosed in Noble, as a potential substitute for Lee's LOCOS isolation, which performs the same isolation function. Thus, the only difference between the semiconductor device of claim 1 and the prior art device described in Lee is a feature that was well-known in the prior art and known to be substitutable.

Third, Petitioner provides evidence that a person of ordinary skill in the art would have recognized specific advantages to using a trench isolation rather than LOCOS. Pet. 28–30. Primarily, using a trench isolation, as in Noble, permits greater device density as a result of eliminating the bird's beak problem that occurs with LOCOS. *Id.* at 4–7, 29–30 (citing Ex. 1004 ¶¶ 50–55, 95). Indeed, Patent Owner acknowledges that trench isolation "has a smaller spatial extent than LOCOS," allowing for a reduction in device size, "continued miniaturization, and higher transistor packing density." PO Resp. 17; *see also* Ex. 2012 ¶ 105 (same); Sur-Reply 8 (acknowledging that a "reason to substitute STI was the reduction in node size that it provided"); Ex. 1001, col. 1, ll. 17–28 (the '174 patent noting that trench isolation was considered "more advantageous" than LOCOS); Tr. 39:14–15 ("There is no question here that people wanted to use trench [isolation]."), 52:12–53:5 (acknowledging that it would have been "desirable to put a trench into – to substitute a trench for LOCOS," but arguing that it would not have been "desirable to put a trench into Lee"). Using a raised STI, as in Noble, also "helps localize source/drain regions by providing a barrier during the ion implantation or diffusion processes used to make them," mitigating a "wrap-around problem" that occurs when "the top of the isolation structure is level with the substrate surface." Pet. 6–7, 29 (citing Ex. 1015, col. 4, ll. 59–65, col. 5, ll. 5–9, Fig. 6). For these reasons, we

agree with Petitioner and Dr. Banerjee that an ordinarily skilled artisan would have viewed Noble's STI as an improvement to Lee's LOCOS isolation. *See id.* at 30; Ex. 1004 ¶ 96; *KSR*, 550 U.S. at 417 ("if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill").

Fourth, Petitioner provides evidence that a person of ordinary skill in the art would have known how, and been able, to fabricate a device with a LOCOS isolation as well as a device with a trench isolation. Lee describes the process for creating its device with a LOCOS isolation (field oxide 113) and Noble describes the process for creating its device with a trench isolation (STI 30). *See* Ex. 1002, col. 6, l. 46–col. 7, l. 52, Figs. 11–15; Ex. 1015, col. 3, l. 35–col. 6, l. 31 (also incorporating by reference U.S. Patent No. 5,173,439 (Ex. 1058), which describes "STI and processes for forming STI"), Figs. 1–13; Pet. 32–33. Ueda discloses fabrication processes using both isolation types. *See* Ex. 1014, col. 8, l. 13–col. 9, l. 33, col. 13, ll. 12–63, Figs. 1(a)–1(f), 12(a)–12(f); Pet. 25–26. The '174 patent acknowledges that both types were known at the time and describes prior art processes for creating a device with a trench isolation. *See* Ex. 1001, col. 1, l. 17–col. 5, l. 51. This evidence demonstrates that it was well-known at the time of the '174 patent how to fabricate a device with either a LOCOS isolation or a trench isolation. Also, other than their different isolation types, the Lee and Noble devices have numerous structural similarities, as shown in the colored figures reproduced above. *See supra* Section II.D.3.a; Pet. 26–28. As such, the evidence of record supports Petitioner's contention

that a person of ordinary skill in the art would have been able to combine the teachings of Lee and Noble to achieve a semiconductor device with all of the components recited in claim 1 and would have had a reasonable expectation of success in doing so.

Patent Owner makes a number of arguments challenging the asserted combination of Lee and Noble, which we now address. As an initial matter, many of Patent Owner's arguments are premised on its position that to prove the obviousness of claim 1, Petitioner was required to describe the particular sequence of steps by which a device based on the combined teachings of Lee and Noble would be made.[12] *See, e.g.*, PO Resp. 1–2 ("Petitioner has the burden of establishing how the identified components could be assembled by [a person of ordinary skill in the art] to arrive at the claimed invention"), 5 ("[w]hen combining semiconductor device features from two distinct devices, the fabricated features are inseparable from *how* the features are formed during the fabrication process"), 14 (arguing that the asserted prior art and the '174 patent "provide[] an extensive sequence of detailed fabrication process steps including relevant engineering details" and "[i]t is

[12] Dr. Schubert's testimony reflects this understanding as well. *See, e.g.*, Ex. 2012 ¶¶ 92 n.10 ("I understand that it would have been the burden of Petitioner to show that a fabrication process that follows from the various combinations of *Lee*, *Lowrey*, *Noble* and *Ogawa* would have obviated the '174 patent."), 230 ("Petitioner has failed to provide the actual process sequence it is contemplating. To properly establish obviousness, disclosure of the fabrication sequence is necessary."), 412 ("Petitioner has failed to provide the actual process sequence it is contemplating, i.e. Petitioner provided neither [a] pictorial nor [a] narrative process sequence. To properly establish obviousness, disclosure of the sequence is necessary.").

precisely this type of information which would be needed to establish obviousness" of the challenged claims).

Patent Owner does not cite any direct authority for this proposition, in semiconductor-related cases or otherwise, and we are aware of none. Patent Owner primarily relies on two cases. *See id.* at 2–5. In *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017), the Court held that brief explanations may suffice to demonstrate obviousness if "the technology is simple and familiar and the prior art is clear in its language and easily understood," but "complexity or obscurity of the technology or prior-art descriptions may well make more detailed explanations necessary." The Court found the Board's analysis deficient as to a motivation to combine and reasonable expectation of success because "the Board nowhere clearly explained, or cited evidence showing, *how* the combination of the two references was supposed to work." *Id.* at 993–94. Similarly, in *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368–69 (Fed. Cir. 2012), the Court stated that one must "be careful not to allow hindsight reconstruction of references to reach the claimed invention without any explanation as to how or why the references would be combined to produce the claimed invention," and found the record "devoid of any reason someone would combine [the cited] references" (citation omitted). *See also* Sur-Reply 6–7, 9 (citing *Rovalma, S.A. v. Bohler-Edelstahl GmbH & Co. KG*, 856 F.3d 1019, 1025 (Fed. Cir. 2017) ("the amount of explanation needed varies from case to case, depending on the complexity of the matter and the issues raised in the record")); Tr. 48:2–50:22 (discussing *Ariosa*, 805 F.3d at 1365–66, cited in the portion of *Personal Web* quoted above, and *Kinetic Concepts*).

We do not see how the complexity of semiconductor manufacturing in general requires a more detailed explanation regarding fabrication of the claimed "semiconductor device," particularly when Petitioner has presented ample evidence that both isolation techniques (LOCOS and trench isolation) were well-known in the art and recognized as alternatives, and that a person of ordinary skill in the art would have known how to fabricate a device with either type. At the very least, even if certain aspects of the recited semiconductor device may be complex, it does not appear that the substitution of trench isolation for LOCOS (which is the essential issue here) would have been considered unduly complex to a person of ordinary skill in the art, given all of the evidence discussed above.

To the extent Patent Owner's argument is that Petitioner needed to explain "how" Lee and Noble are being combined or "how" the combined device would work, *see, e.g.*, PO Resp. 4–5, 43–44, 49, Petitioner did so. Again, Petitioner's position is that an ordinarily skilled artisan would have substituted Noble's STI in place of Lee's LOCOS isolation. *See supra* Section II.D.3.a; Pet. 21, 31–33; PO Resp. 13, 43–44, 49, 63–65 (acknowledging that Petitioner's asserted combination is based on the substitution of trench isolation for LOCOS). There is no difference in how the device would work using either LOCOS or trench isolation, as both structures perform the same isolation function. *See* Ex. 1056, 78:9–17, 79:17–81:1 (Dr. Schubert acknowledging that both are "isolation structures").

Moreover, claim 1 is an apparatus claim, not a method claim. *Cf. Personal Web*, 848 F.3d at 989 (challenged patent claimed "methods" and "devices for carrying out the methods"); *Kinetic Concepts*, 688 F.3d at 1346

(challenged patents included method claims and apparatus claims with means-plus-function limitations). Claim 1 recites a "semiconductor device" comprising various physical components, one of which is a "trench isolation," but does not recite anything about how those components are formed. Thus, we do not read any process limitations into the claim, and do not require the relied upon prior art to disclose any particular fabrication process. *See Baldwin Graphics Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1344 (Fed. Cir. 2008); *Vanguard Prods. Corp. v. Parker Hannifin Corp.*, 234 F.3d 1370, 1372–73 (Fed. Cir. 2000) ("The method of manufacture, even when cited as advantageous, does not of itself convert product claims into claims limited to a particular process."); *cf. In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985) ("The patentability of a product does not depend on its method of production."). In sum, we are not persuaded, under the particular factual circumstances of this case, that the Petition is deficient for failing to set forth the precise sequence of steps by which a device based on the combined teachings of Lee and Noble would be fabricated. Petitioner's focus in the Petition appropriately is on how the cited prior art teaches every component of the claimed device and why a person of ordinary skill in the art would have been motivated to combine the references' teachings and would have had a reasonable expectation of success in doing so. *See* Pet. 21–44.

We now turn to Patent Owner's arguments to determine whether the fabrication processes of Lee and Noble are so different or incompatible that they would have discouraged a person of ordinary skill in the art from making the asserted combination or would not have produced a reasonable expectation of success in achieving the claimed device.

Patent Owner argues that Lee and Noble "are not combinable because they are based on completely contrasting designs, and any combination is pure hindsight," citing the testimony of Dr. Schubert. PO Resp. 43–48, 50–59 (citing Ex. 2012 ¶¶ 175–182, 186–214, 238–274). Specifically, Lee's LOCOS isolation is formed *before* gate dielectric and gate conductor formation, whereas Noble's trench isolation is formed *after* gate dielectric and gate conductor formation. *Id.* Figures 11 and 12 of Lee are reproduced below.

FIG. 11

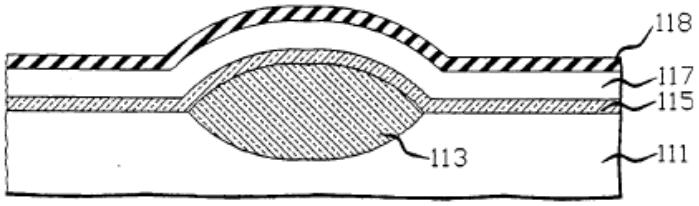


FIG. 12

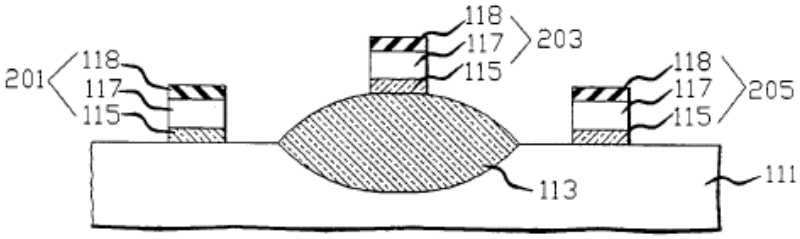


Figure 11 depicts field oxide 113, which is formed before forming the gate dielectric (layer 115), gate conductor (layer 117), and insulator (layer 118); Figure 12 depicts the layers after they are patterned to form "gate[]" stacks 201 and 205 and "runner" 203. Ex. 1002, col. 6, l. 47–col. 7, l. 4. Patent Owner asserts that the gate conductor (layer 117) in Lee "serve[s] a dual purpose—it forms the gate electrodes over the active areas, and it extends directly as a 'gate runner' or simply 'runner' to form the interconnect on top

of the isolation," "thereby inherently connecting gate stacks with interconnections." PO Resp. 51–53 (citing Ex. 2012 ¶¶ 126, 129).

Noble's process operates in the reverse order, where STI 30 is formed (by etching and filling a trench) after deposition of gate dielectric 14 and gate conductor 116, as shown in Figure 9 below.

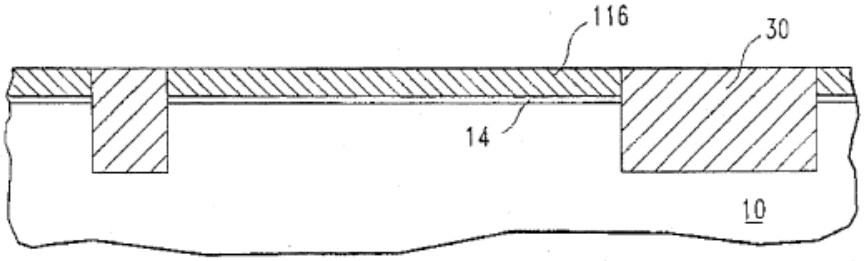


FIG. 9

Figure 9 above shows that gate conductor 116 is bounded on either side in the gate width direction by raised STI 30. Ex. 1015, col. 4, ll. 40–65. Unlike Lee, which has a gate conductor on top of the LOCOS isolation that acts as an interconnection, Noble uses conductive wiring level 140, which "extends over STI 30 to interconnect transistors or cells." *See id.* at col. 5, l. 49–col. 6, l. 6, Fig. 11. Patent Owner contends that Noble's sequence is thus designed to "prevent the gate conductor from wrapping around the trench corner," "avoid gate dielectric thinning adjacent the corner," and "avoid sharpening of the corner." PO Resp. 58–59 (quoting Ex. 1015, col. 2, ll. 30–35) (emphases omitted). According to Patent Owner and Dr. Schubert, a person of ordinary skill in the art would not have combined Lee and Noble due to these differences in process sequence. *See id.*; Ex. 2012 ¶ 150.

Patent Owner also points to various other ways in which the allegedly "contradictory" processes in Lee and Noble would cause a person of ordinary skill in the art not to combine their teachings. *See* PO Resp. 63–70;

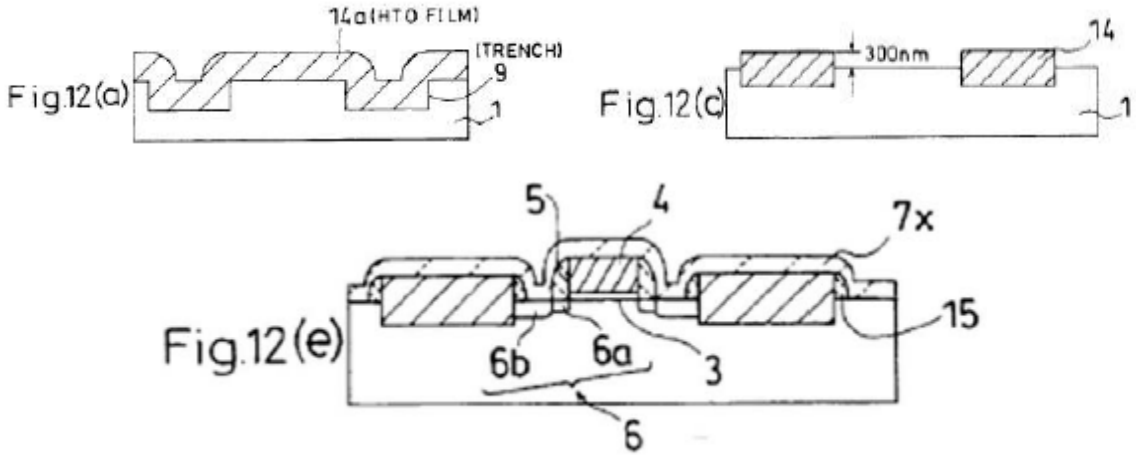
Sur-Reply 8–23. For instance, Patent Owner argues that "it is not possible to simply start with *Noble*'s . . . trench isolation without first forming the gate dielectric and gate conductor" because Noble's process "depends on" that order. PO Resp. 64–65 (citing Ex. 2012 ¶ 201). Patent Owner further contends that Noble uses different elements for its gate conductor and interconnect conductor and exhibits a "distinct height difference" between them (due to the raised STI), whereas Lee uses the same elements for both, such that they have the same height. *Id.* at 65–68. According to Patent Owner, "[u]sing different structures contradicts the teaching of *Lee* and thus a [person of ordinary skill in the art] would not look to *Noble*'s shallow trench isolation." *Id.* at 67–68 (citing Ex. 2012 ¶ 204).

We agree with Patent Owner that the layering sequence in the two references is different (LOCOS isolation formed before the gate stack components in Lee, and STI formed after the gate stack components in Noble). We are not persuaded, though, that such difference means a person of ordinary skill in the art would not have combined their teachings or would not reasonably have been expected to succeed. Importantly, Petitioner only relies on Noble for a teaching of a "trench isolation" as recited in claim 1. Petitioner relies on Lee for all other limitations, such as the "gate electrode," "interconnection," and "first L-shaped sidewalls" on the sides of the gate electrode. Patent Owner's arguments pertaining to Noble's gate stack and interconnection, therefore, are directed to a combination that Petitioner has not proposed; Petitioner does not rely on Noble as teaching those components. *See* PO Resp. 43 (arguing that Noble and Ogawa "necessarily include pre-existing structures (gate electrodes) which they bring along with them into any structure, such as" the device of Lee); Reply 45–47.

Patent Owner's position would require, in effect, that a person of ordinary skill in the art incorporate an STI into Lee's device in a manner that preserves the gate stack and interconnection of Noble's preferred embodiment. There is no need to do so, however. The devices of Lee and Noble need not be "physically combinable to render obvious" the device recited in claim 1. *See In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983). "It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements. . . . Rather, the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art." *In re Mouttet*, 686 F.3d 1322, 1332–33 (Fed. Cir. 2012); *see also MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015) ("[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference" (citation omitted)), *cert. denied*, 137 S. Ct. 292 (2016); *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (finding that "assertions that [one reference] cannot be incorporated in [another reference] are basically irrelevant, the criterion being not whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole"). Also, Noble "must be considered for everything that it teaches, not simply the . . . preferred embodiment" that forms the STI in a particular order with respect to other components. *See In re Applied Materials, Inc.*, 692 F.3d 1289, 1298 (Fed. Cir. 2012).

Moreover, the evidence of record indicates that it would have been within the skill of an ordinarily skilled artisan to form a raised STI before

forming the gate stack (i.e., the order in Lee, where the isolation structure is formed first). Ueda, for example, discloses multiple structures using LOCOS, notes that "[t]he present invention is also applicable to an isolation of trench structure," and discloses how to form a device with a raised trench isolation. *See* Pet. 25–26 (quoting Ex. 1014, col. 22, ll. 49–52). Petitioner and Dr. Banerjee point to Figures 12(a)–12(f) of Ueda, which depict, *inter alia*, the creation of a trench isolation prior to forming the gate stack. *Id.*; *see* Ex. 1004 ¶¶ 89–90. Figures 12(a), 12(c), and 12(e) of Ueda are reproduced below.



The above figures show trench 9 created via photolithography and dry-etching, oxide film 14 raised above substrate 1, and gate oxide film 3 and gate electrode 5 created after formation of the trench isolation. Ex. 1014, col. 13, ll. 12–63. Petitioner also cites the '174 patent's discussion of a prior art fabrication process and Exhibit 1016 to show what a person of ordinary skill in the art would have known regarding trench isolation. *See* Pet. 6, 22–23. We agree that these are examples of known processes for making a trench isolation before making any gate layers as well. *See* Reply 10–11; Ex. 1001, col. 4, l. 16–col. 5, l. 3, Figs. 20(a)–20(e); Ex. 1016, col. 3, l. 55–col. 4, l. 22, Figs. 1a–1e.

Petitioner has presented persuasive evidence that a person of ordinary skill in the art would have known multiple ways to form a raised STI before forming the gate stack and that the result of those processes would be a raised STI with the same structure as Noble. *See* Reply 15–16. Thus, regardless of the particular order of steps in Noble, Petitioner's reliance on Noble as teaching a trench isolation is proper and we find that an ordinarily skilled artisan would have been able and motivated to substitute it for Lee's LOCOS isolation, without changing Lee's order.[13]

[13] Patent Owner also argues in its Sur-Reply that because Lee utilizes "an unusual heavily-doped/lightly-doped process sequence," which "requires that dopants diffuse over a larger distance," a person of ordinary skill in the art "would not have been motivated to insert an STI into *Lee* to reduce node size." Sur-Reply 11–23. Patent Owner also attacks Dr. Banerjee's testimony based on various admitted misstatements regarding Lee's doping sequence during cross-examination. *Id.* at 18–23. These arguments do not appear to be directly responsive to any of the new exhibits filed by Petitioner with the Reply, which was the basis for authorizing the Sur-Reply. *See* Papers 27, 28 (Patent Owner arguing that a lengthy Sur-Reply was necessary to respond to "the lengthy arguments made by Petitioner in its Reply and numerous exhibits submitted with the Reply"). Regardless, as explained above, in assessing obviousness, we do not require an actual, physical substitution of Noble's STI into Lee's device. *See MCM Portfolio*, 812 F.3d at 1294; *Mouttet*, 686 F.3d at 1332–33; *Etter*, 756 F.2d at 859 (finding assertions that one reference could not be incorporated into another reference to be "basically irrelevant"); *Sneed*, 710 F.2d at 1550. Further, Patent Owner's arguments appear to be directed to purported problems or deficiencies with Lee itself, rather than issues arising *from the combination* that may have discouraged a person of ordinary skill in the art from combining Lee's teachings with those of Noble. In other words, any problems with Lee's sequence of doping (as in Lee's device using LOCOS) would also exist in the combined device (using trench isolation). The combined device, though, has the required structure (i.e., all of the components recited in claim 1) as Petitioner alleges and operates the same as Lee (using a trench isolation rather than LOCOS for isolation), and

Finally, Patent Owner argues that the fact that two of the inventors named on Lee "were aware that it was advantageous to use trench isolation" but chose to use LOCOS instead indicates that it would not have been obvious to substitute trench isolation for LOCOS. PO Resp. 72–73 (citing Ex. 2021). We disagree. Obviousness is "assessed from the perspective of the hypothetical person of ordinary skill in the art," not the inventor named on a prior art reference. *See Life Techs., Inc. v. Clontech Labs., Inc.*, 224 F.3d 1320, 1325 (Fed. Cir. 2000). Lee's use of LOCOS also is logical, given Petitioner's explanation that it was the primary technique in 1989 at the time Lee was filed, but the industry had begun moving to trench isolation by the mid-1990s. *See* Pet. 22–23; Reply 38; Ex. 1004 ¶¶ 52–55. We have reviewed all of Patent Owner's arguments and supporting evidence, and do not find them persuasive for the reasons set forth above.

c. Petitioner's Reply

Patent Owner argues in its Sur-Reply that Petitioner's Reply and evidence filed with the Reply should not be considered because Petitioner improperly described for the first time in the Reply "how" Petitioner was combining the relied upon prior art. Sur-Reply 2–6; *see also* Papers 27, 28 (discussing the parties' arguments leading to the Sur-Reply). Patent Owner contends that Petitioner "shift[ed] its arguments" from relying on embodiments from Noble (and Ogawa) that have an STI "embedded" within a gate electrode to instead "rely on other references alleged to teach isolations not-embedded within a gate electrode." *See* Sur-Reply 6.

Petitioner's asserted motivations for why a person of ordinary skill in the art would have made the combination would still apply.

As an initial matter, we need only evaluate the propriety of the portions of the Reply and accompanying evidence on which we rely herein, and we determine that those portions were appropriate. Petitioner explained in the Petition "how" Lee and Noble are being combined, namely that a person of ordinary skill in the art would have substituted Noble's STI in place of Lee's LOCOS isolation. *See supra* Section II.D.3.b. This is the basis for Petitioner's obviousness combination, both in the Petition and in the Reply. Petitioner's discussion of other references mentioned herein, such as Ueda, properly responded to Patent Owner's arguments as to why a person of ordinary skill in the art would not have been motivated to combine the references or would not have had a reasonable expectation of success due to their differences in fabrication processes, as well as Patent Owner's arguments regarding portions of Noble other than the STI (e.g., gate electrode and interconnection). *See* 37 C.F.R. § 42.23(b) ("A reply may only respond to arguments raised in the corresponding . . . patent owner response."); *Idemitsu Kosan Co., Ltd. v. SFC Co. Ltd.*, 870 F.3d 1376, 1380–81 (Fed. Cir. 2017) (permitting rebuttal argument from a petitioner in response to a patent owner's argument that a reference taught away from a particular combination, as such argument was "simply the by-product of one party necessarily getting the last word"). The other references mentioned herein also appropriately show the background knowledge of a person of ordinary skill in the art. *See supra* n.11; *Genzyme Therapeutic Prods. Ltd. P'ship v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1367–69 (Fed. Cir. 2016) (permitting "references [that] were not among the combinations of references on which the Board granted review" to be used to show a reasonable expectation of success, and stating that "the Board may consider

a prior art reference to show the state of the art at the time of the invention, regardless of whether that reference was cited in the Board's institution decision"). Petitioner does not rely on them as teaching the "trench isolation" limitation of claim 1. Thus, we are persuaded that the Reply arguments and evidence referenced herein were proper.

d. Conclusion

For the reasons set forth by Petitioner and explained above, we are persuaded that Lee and Noble collectively teach all of the limitations of claim 1, and that a person of ordinary skill in the art would have had reason to combine those teachings to achieve the semiconductor device of claim 1 and would have had a reasonable expectation of success in doing so. Petitioner has proven, by a preponderance of the evidence, that claim 1 would have been obvious based on Lee and Noble under 35 U.S.C. § 103(a).

4. Claims 2 and 6

Claims 2 and 6 recite that the first and second L-shaped sidewalls, respectively, are "made of a silicon nitride film." Lee discloses that layer 121 may be "silicon nitride." Ex. 1002, col. 7, l. 7. Patent Owner relies on its arguments regarding parent claim 1. PO Resp. 84. For the reasons stated by Petitioner, we are persuaded, by a preponderance of the evidence, that claims 2 and 6 would have been obvious based on Lee and Noble under 35 U.S.C. § 103(a). *See* Pet. 44–46, 49–50.

5. Claims 3, 7, 15, 17, and 18

Claim 3 recites "first protection oxide films formed between the gate electrode and the first L-shaped sidewalls," and claim 15 recites that "the first protection oxide film is a CVD oxide film." Claims 7, 17, and 18 recite similar limitations regarding "second protection oxide films formed between the interconnection and the second L-shaped sidewalls." To meet these limitations, Petitioner relies on layer 119 shown in Figure 15 of Lee. Pet. 46–47, 51–52, 61–63, 67–69. Patent Owner acknowledges that Lee teaches "silicon dioxide in between the gate electrode and the first L-shaped sidewalls in Fig[ure] 15," but contends that if Lee's LOCOS isolation is replaced with a trench isolation based on Noble, "there is no way of knowing whether the resulting second sidewalls (on the trench isolation) would be L-shaped" and "there would not be an interconnection having second L-shaped sidewalls," relying on its previous arguments to that effect. PO Resp. 84–86. We are not persuaded, as explained above. *See supra* Section II.D.3.a. For the reasons stated by Petitioner, we are persuaded, by a preponderance of the evidence, that claims 3, 7, 15, 17, and 18 would have been obvious based on Lee and Noble under 35 U.S.C. § 103(a). *See* Pet. 46–47, 51–52, 61–63, 67–69.

6. Claims 5 and 16

Claims 5 and 16 recite various limitations pertaining to the "first silicide layers" and "source/drain regions" on the sides of the gate electrode. Petitioner explains in detail, with annotated figures, how the limitations are taught by Lee. Pet. 38–40, 47–49, 63–67. Patent Owner again argues that the red circles in Petitioner's annotated Figure 15 above "are not layers but

lines (cylinders) or wires." PO Resp. 85. We are not persuaded, as explained above. *See supra* Section II.D.3.a. For the reasons stated by Petitioner, we are persuaded, by a preponderance of the evidence, that claims 5 and 16 would have been obvious based on Lee and Noble under 35 U.S.C. § 103(a). *See* Pet. 38–40, 47–49, 63–67.

7. Claims 9 and 10

Claim 9 recites that "the trench isolation has an upper surface higher than the surface of the active area." Claim 10 recites that "a lower portion of the interconnection provided on the upper surface of the trench isolation is located higher than the surface of the active area." Petitioner provides the following annotated versions of Figures 12 and 13 of Noble (Pet. 53, 56).

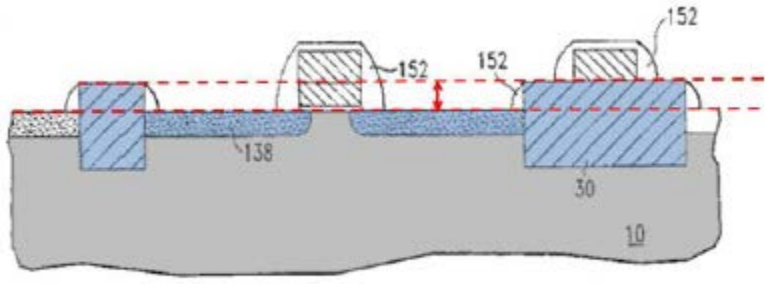


FIG. 12

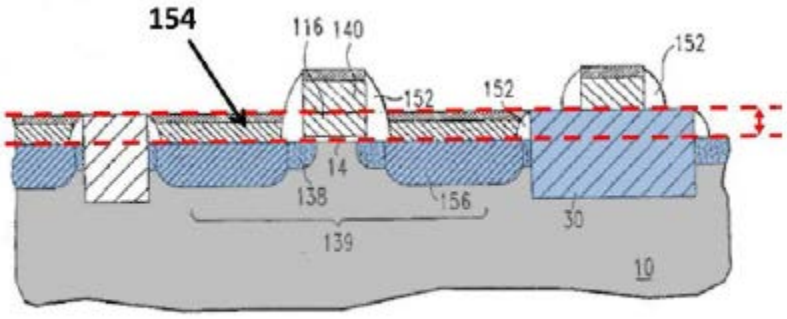


FIG. 13

The annotated figures above depict STI 30 with an upper surface (adjacent to an interconnection) that is higher than the surface of the active area of

substrate 10, by a distance shown with red arrows. *See id.* at 52–57. Patent Owner argues that Noble has silicide layers next to STI 30, so if Lee's LOCOS isolation is replaced with a trench isolation based on Noble, a person of ordinary skill in the art "would also use the raised source/drain regions disclosed in *Noble*," resulting in an upper surface that is even with the upper surface of STI 30. PO Resp. 86–88. We disagree. Petitioner's asserted combination incorporates Noble's teaching of a trench isolation (STI 30), but not other structures from Noble. Moreover, as Petitioner points out, "the active area" in claims 9 and 10 refers to "an active area of a semiconductor substrate" in parent claim 1. The surface of the active area of the substrate is at the lower dotted red line in the annotated figures above; the upper surface of raised source/drain 154 is not a surface of the substrate's active area. *See* Reply 49–50; Ex. 1015, col. 4, ll. 17–19 ("The term 'raised trench' refers to the fact that the trench extends beyond the surface of substrate 10 to the top of the gate stack."), col. 6, ll. 17–22 ("Dopant for the raised source/drain is implanted at low energy so as to avoid damage to the single crystal silicon below."); Ex. 1056, 123:15–21 (Dr. Schubert acknowledging that "the filling [of the trench in Noble] goes above the surface of the silicon"). For the reasons stated by Petitioner, we are persuaded, by a preponderance of the evidence, that claims 9 and 10 would have been obvious based on Lee and Noble under 35 U.S.C. § 103(a). *See* Pet. 52–57.

8. Claims 11, 12, and 14

Claims 11, 12, and 14 recite limitations pertaining to the material used for certain recited components. Claim 11 recites that "the interconnection is

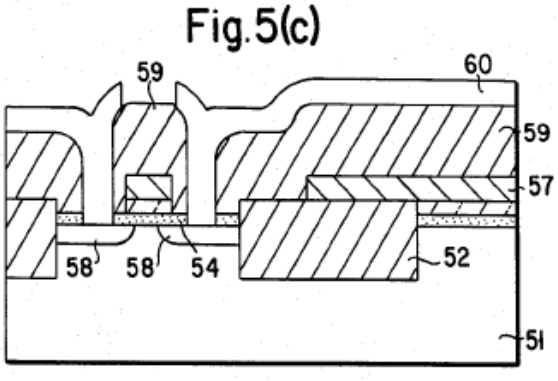
composed of the same material as the gate electrode," and claim 12 recites that "the gate electrode and the interconnection has at least a polysilicon film." Petitioner relies on the same component (i.e., layer 117), which Lee discloses is made of "polysilicon," used to form both structures in Figure 15 of Lee. Pet. 57–60 (citing Ex. 1002, col. 6, ll. 52–53). Claim 14 recites that "the first and second L-shaped sidewalls are made of the same insulating film." Petitioner relies on the same component (i.e., layer 121) used to form both sidewalls in Figure 15 of Lee. *Id.* at 60–61.

With respect to claims 11 and 12, Patent Owner argues that if Lee's LOCOS isolation is replaced with a trench isolation based on Noble, "the conductive wiring layer[] of *Noble* . . . would not be 'composed of the same material' and not have 'at least a polysilicon film.'" PO Resp. 89–90. Similarly, with respect to claim 14, Patent Owner argues that Noble does not teach sidewalls shaped like an L, it would be unclear whether the combined device would have second L-shaped sidewalls "[g]iven that the combined device would not have the gate conductor on top of the trench isolation," and even "if there were" second sidewalls, they would be different from the first L-shaped sidewalls. *Id.* at 90–91. We are not persuaded. As explained above, Petitioner relies on Lee as teaching the recited "gate electrode," "interconnection," and "first and second L-shaped sidewalls," and relies on Noble *only* as teaching a "trench isolation." *See supra* Section II.D.3.a. For the reasons stated by Petitioner, we are persuaded, by a preponderance of the evidence, that claims 11, 12, and 14 would have been obvious based on Lee and Noble under 35 U.S.C. § 103(a). *See* Pet. 57–61.

E. Obviousness Ground Based on Lee and Ogawa
(Claims 1–3, 5–7, 9–12, and 14–18)

1. Ogawa

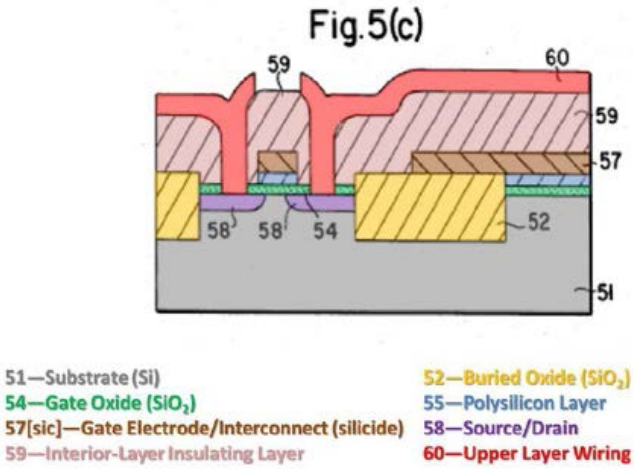
Ogawa describes "methods for production of buried insulating layers each of which surrounds a portion of a semiconductor substrate in which elements are fabricated, the buried insulating layers functioning to isolate from one another." Ex. 1010, col. 1, ll. 8–15. Ogawa describes LOCOS and its associated "bird's beak" problem. *Id.* at col. 1, ll. 17–60. According to Ogawa, LOCOS "is not necessarily satisfactory for the production of a semiconductor device having minute patterns," and other methods, such as where "each element is isolated from one another by buried insulating layers which are grown to fill grooves produced along the surface of a silicon (Si) substrate to surround each element," were developed to overcome the drawbacks of LOCOS. *Id.* at col. 1, ll. 58–68. Ogawa describes a fabrication process depicted in Figures 4(a)–(c) and 5(a)–(c). Figure 5(c) of Ogawa is reproduced below.



The figure above shows a device including, *inter alia*, portion 52, created by etching to form a groove that is filled with silicon dioxide. *Id.* at col. 6, ll. 16–59, col. 7, ll. 40–47, Figs. 4(b)–(c) (silicon dioxide layer 47 in groove 45).

2. Claim 1

As with the combination of Lee and Noble, Petitioner explains in detail how Lee and Ogawa[14] collectively teach every limitation of claim 1, relying on the testimony of Dr. Banerjee as support. Pet. 30–44, 70, 76–79 (citing Ex. 1004 ¶¶ 211–221). Petitioner relies on Lee as teaching all of the limitations other than a "trench isolation," referring to its previous analysis in the Petition, and relies on portion 52 in Ogawa as teaching a "trench isolation." *Id.*; *see CRFD Research, Inc. v. Matal*, 876 F.3d 1330, 1345–46 (Fed. Cir. 2017) (agreeing with the petitioner that it "incorporated [an] argument into other grounds of unpatentability . . . by direct citation to [the] argument in the petition"). Petitioner provides on page 21 of the Petition the following colored and annotated version of Figure 5(c) of Ogawa, which we find is consistent with Ogawa's disclosure.[15]



[14] Ogawa was not considered during prosecution of the '174 patent. *See* Ex. 1001, (56).

[15] The parties agree that label "57" is incorrect in Figure 5(c), and instead should be "56" (shown also in Figure 5(b)). *See* Pet. 20 n.4; PO Resp. 62 n.11; Ex. 1010, col. 7, ll. 49–56 (describing how molybdenum silicide layer 56 is "produced on the patterned polycrystalline silicon (Si) layer 55 and the remaining portion of the silicon dioxide (SiO_2) layer 54").

The figure above shows Ogawa's device with portion 52 of silicon dioxide, as well as various components that are very similar to those of Lee, such as the gate electrode, interconnection, gate dielectric, source, drain, and silicide regions. Pet. 71–73 (describing the similar structures of Lee and Ogawa), 76–77.

As to the combined teachings of the references, Petitioner's position again is that a person of ordinary skill in the art would have been motivated to replace the LOCOS isolation in Lee's device (field oxide 113) with the trench isolation of Ogawa (portion 52). *Id.* at 70 (arguing that a person of ordinary skill in the art "would have understood that *Ogawa*'s trench isolation was a known substitute for *Lee*'s LOCOS isolation," and "[t]he combined teachings discussed in [the Petition] refer to the teachings of *Lee*, with its LOCOS isolation replaced by *Ogawa*'s trench isolation"), 76–79. Petitioner's arguments as to how Lee and Ogawa collectively teach every limitation of claim 1 are supported by the testimony of Dr. Banerjee and are persuasive. *See* Pet. 30–44, 76–79; Ex. 1004 ¶¶ 211–221.

Petitioner's arguments regarding motivation to combine and reasonable expectation of success are similar to those presented with respect to Lee and Noble, and reference much of Petitioner's previous analysis regarding the history of LOCOS versus trench isolation and background knowledge of a person of ordinary skill in the art. *See* Pet. 70–76 (citing *id.* at 22–26); Ex. 1004 ¶¶ 198–209; *CRFD Research*, 876 F.3d at 1345–46. Notably, as Petitioner points out, Ogawa expressly states that trench isolation already was viewed as an improvement over LOCOS because, for example, it eliminated the bird's beak problem, allowing for increased device density. *See* Pet. 74–75. Ogawa discloses:

> There is now a tendency in which the dimensions of each element is decreased in order to satisfy requirements for a larger quantity of elements fabricated in a chip and also for a larger quantity of elements fabricated in the unit area of a chip. Such requirements are included in the requirements effective to satisfy the ultimate purposes for development of LSI's and further of VLSI's. Insofar as the processes for isolating each element fabricated in one chip from one another are concerned, a process which is called local oxidation of silicon is available, and it is well known that this process has various advantages in the aspects of easy production of durable wiring which is free from potential discontinuation thereof and the potential employment of self-alignment and the like. However, this local oxidation process has drawbacks. The first is the problem of bird's beak.

Ex. 1010, col. 1, ll. 17–34. Figure 1 of Ogawa is reproduced below.

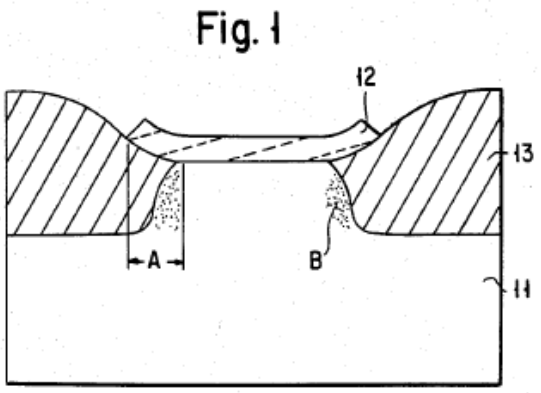


Figure 1 shows how silicon dioxide layer 13 grows laterally using LOCOS, creating a "bird's beak shape" under silicon nitride layer 12, where lateral length A of the bird's beak "causes a degradation of dimensional accuracy" and portion B causes undesirable strain. *Id.* at col. 1, ll. 34–50. Ogawa states that this LOCOS process was "not necessarily satisfactory for the production of a semiconductor device having minute patterns," and trench isolation "has been developed and is presently being used" "[t]o overcome the foregoing drawbacks." *Id.* at col. 1, ll. 58–66. Ogawa discloses a fabrication process for its device, including the creation of a trench isolation.

Id. at col. 3, ll. 49–58, col. 5, l. 39–col. 8, l. 24. The disclosure of Ogawa strongly supports Petitioner's contention that a person of ordinary skill in the art would have been motivated to improve Lee's device by replacing its LOCOS isolation with a trench isolation, as taught by Ogawa, and would have had a reasonable expectation of success in doing so.

Many of Patent Owner's arguments are made with respect to both the asserted ground based on Lee and Noble and the asserted ground based on Lee and Ogawa. *See, e.g.*, PO Resp. 43–53, 63–78, 81–83. These arguments are not persuasive for reasons similar to those set forth above. *See supra* Section II.D. Patent Owner's arguments largely pertain to other components of Ogawa, such as its gate stack and interconnection, on which Petitioner does not rely. Similar to its ground based on Lee and Noble, Petitioner relies on Ogawa *only* for a teaching of a "trench isolation."

With respect to the combination of Lee and Ogawa in particular, Patent Owner argues that a person of ordinary skill in the art would not have combined the references because Ogawa utilizes "an early, primitive and unreliable trench isolation formation process." PO Resp. 59–63 (citing Ex. 2012 ¶¶ 166–167). Specifically, Ogawa performs planarization to create its trench isolation by "attempting to dry etch photoresist and silicon dioxide (SiO_2) at an equal etch rate," which is "very difficult to attain because the substances being etched in *Ogawa* are so different." *Id.* at 59–60. We are not persuaded. Regardless of its fabrication method, Ogawa teaches the structure on which Petitioner relies, i.e., a "trench isolation." Further, as Petitioner points out, the '174 patent discloses using "etch-back through dry-etching" (as well as chemical mechanical polishing (CMP)) to form a trench isolation. Ex. 1001, col. 12, ll. 43–47, col. 22, ll. 45–48, col. 25,

ll. 22–25; *see* Reply 39. Thus, we are not persuaded that a person of ordinary skill in the art would have been discouraged from replacing Lee's LOCOS isolation with a trench isolation due to Ogawa's etch-back process.

For the reasons set forth by Petitioner and explained above, we are persuaded that Lee and Ogawa collectively teach all of the limitations of claim 1, and that a person of ordinary skill in the art would have had reason to combine those teachings to achieve the semiconductor device of claim 1 and would have had a reasonable expectation of success in doing so. Petitioner has proven, by a preponderance of the evidence, that claim 1 would have been obvious based on Lee and Ogawa under 35 U.S.C. § 103(a).

3. Dependent Claims 2, 3, 5–7, 9–12, and 14–18

We have reviewed and agree with Petitioner's contentions regarding dependent claims 2, 3, 5–7, 9–12, and 14–18, which are supported by the testimony of Dr. Banerjee. *See* Pet. 79–85; Ex. 1004 ¶¶ 222–255. In its Response, Patent Owner argues the asserted ground based on Lee and Noble and the asserted ground based on Lee and Ogawa together as to the dependent claims. PO Resp. 84–91. Patent Owner's arguments are not persuasive for the reasons set forth above. *See supra* Section II.D. Petitioner has proven, by a preponderance of the evidence, that claims 2, 3, 5–7, 9–12, and 14–18 would have been obvious based on Lee and Ogawa under 35 U.S.C. § 103(a).

F. Obviousness Ground Based on Lowrey and Noble (Claims 1, 4, 5, 8–12, 14, and 16)

1. Lowrey

Lowrey describes "[a]n improved CMOS fabrication process which uses separate masking steps to pattern N-channel and P-channel transistor gates from a single layer of conductively-doped polycrystalline silicon (poly) and incorporates self-aligned salicidation of conductive regions." Ex. 1017, Abstract. Lowrey describes a fabrication process depicted in Figures 1–12. Figure 12 of Lowrey is reproduced below.

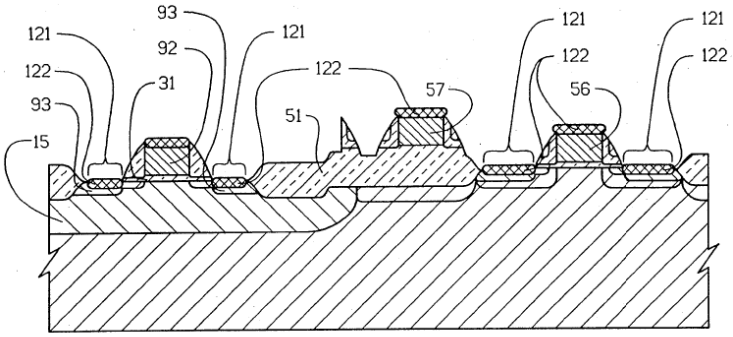


FIG. 12

The device shown above includes, *inter alia*, field oxide region 51 created "using the conventional LOCOS oxidation process," and mini-spacer oxide layers, formed into the shape shown in Figure 12 via etching. *Id.* at col. 8, ll. 31–35, col. 8, l. 58–col. 9, l. 18.

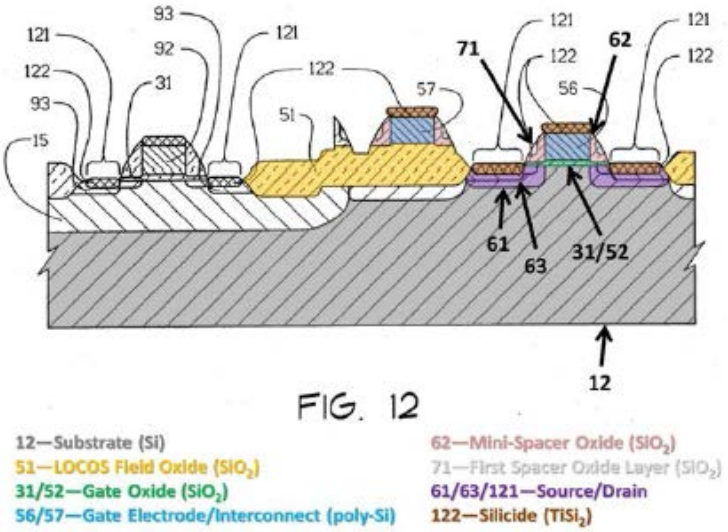
2. Claim 1

a. Whether Lowrey and Noble Collectively Teach All of the Limitations of Claim 1

Petitioner explains in detail how Lowrey[16] and Noble collectively teach every limitation of claim 1, relying on the testimony of Dr. Banerjee as support. -1247 Pet. 21, 30–44 (citing Ex. 1024 ¶¶ 96–119). Specifically, Petitioner relies on Lowrey as teaching all of the limitations other than a "trench isolation." *Id.* Petitioner argues that Lowrey's disclosed device has an isolation (i.e., field oxide region 51) surrounding an active area of a semiconductor substrate (i.e., silicon substrate 12), a "gate insulating film" (i.e., gate oxide layer 31/52) formed over the active area, a "gate electrode" (i.e., transistor gate 56) formed over gate oxide layer 31/52, "first L-shaped sidewalls" (i.e., etched mini-spacer oxide layer 62) formed over the side surfaces of transistor gate 56, "first silicide layers" (i.e., titanium silicide 122) formed on the sides of the first L-shaped sidewalls within the active area, an "interconnection" (i.e., N-channel interconnect 57), and "second L-shaped sidewalls" (i.e., etched mini-spacer oxide layer 62) formed over the side surfaces of the interconnection. *Id.*

[16] Lowrey was not considered during prosecution of the '174 patent. *See* Ex. 1001, (56).

Petitioner provides on page 18 of the -1247 Petition a colored and annotated version of Figure 12 of Lowrey, which we find is consistent with Lowrey's disclosure.



As shown above, Lowrey's device includes field oxide region 51, which is formed using LOCOS rather than trench isolation. *Id.* at 32.

Similar to its asserted ground based on Lee and Noble, Petitioner again relies on Noble as teaching a "trench isolation," citing Noble's description of STI 30, and notes the numerous similar structures in the devices disclosed in the two references, such as the gate electrode, interconnection, gate dielectric, source, drain, and silicide regions. *Id.* at 26–27 (describing the similar structures of Lowrey and Noble), 30–32.

As to the combined teachings of the references, Petitioner's position again is that a person of ordinary skill in the art would have been motivated to replace the LOCOS isolation in Lowrey's device (field oxide region 51) with a trench isolation as taught by Noble (STI 30). *Id.* at 21 (arguing that a person of ordinary skill in the art "would have understood that *Noble*'s trench isolation was a known substitute for *Lowrey*'s LOCOS isolation," and

"[t]he combined teachings discussed in [the -1247 Petition] refer to the teachings of *Lowrey*, with its LOCOS isolation replaced by *Noble*'s STI"), 30–32. Petitioner's arguments as to how Lowrey and Noble collectively teach every limitation of claim 1 are supported by the testimony of Dr. Banerjee and are persuasive. *See id.* at 30–44; Ex. 1024 ¶¶ 96–119.

Patent Owner makes two arguments regarding the combined teachings of the references. First, Patent Owner argues that Lowrey does not teach first and second "L-shaped sidewalls," as recited in claim 1. PO Resp. 102–04, 117; Sur-Reply 40–42. Petitioner identifies Lowrey's mini-spacer oxide layer 62 (shown in pink in the annotated Figure 12 above) on the sides of transistor gate 56 and N-channel interconnect 57, which is shaped like an L after etching. *See* -1247 Pet. 35–38, 42–44. Patent Owner acknowledges that "the figures in *Lowrey* show sidewalls with an L-shaped component and a *separate* section that fills in the L," but asserts that Lowrey's "final sidewalls" do not have any "distinct" component shaped like an L. PO Resp. 103 (second emphasis added). Patent Owner argues the following:

> The shape of the mini spacer oxide layer 62 may have an L-shape when it is initially deposited, but since both layers 62 and 71 are made of the same oxide material, they will ultimately be indistinguishable once layer 62 is applied. That is, a commonly used microscopic assessment technique such as scanning electron microscopy (SEM) of the sidewall structure in 1995 would show the two layers as an indistinguishable entity so that layer 62, which Dr. Banerjee contends would be L-shaped, would not substantially resemble the appearance of a capital letter L (or its mirror image). This is because the two components of the sidewall, layers 62 and 71, cannot be contrasted or distinguished (both are made from "oxide") and after they are deposited and etched, the patent no longer identifies them as separate layers, instead referring to them collectively only as layer 81.

> A necessary condition for a sidewall to appear L-shaped is that it is distinguishable from other components of the sidewall. Given that layer 62 is chemically indistinguishable from layer 71, its physical appearance is indistinguishable from layer 71 as well, and so the sidewall does not substantially resemble an L-shaped component.

Id. at 103–04 (citations omitted).

As Petitioner points out, however, mini-spacer oxide layer 62 and first spacer oxide layer 71 "are different layers, formed at different times, with intervening steps between their formation, and the drawings show them as separate layers throughout." Reply 40; *see* Ex. 1017, col. 8, l. 53–col. 9, l. 5 (describing the formation of both layers as shown in Figs. 6–7). Petitioner provides on page 37 of the -1247 Petition the following colored and annotated versions of Figures 7 and 12 of Lowrey.

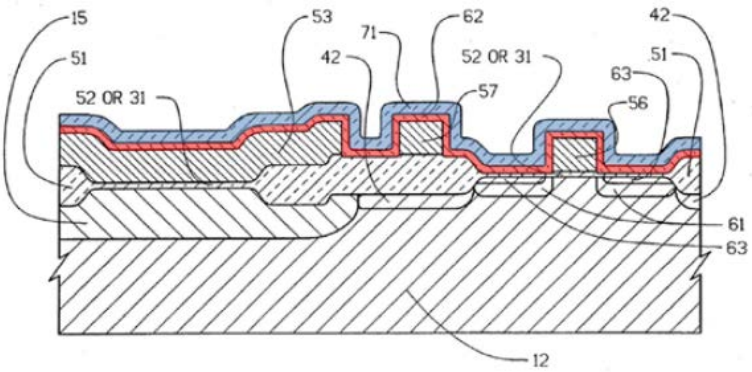


FIG. 7

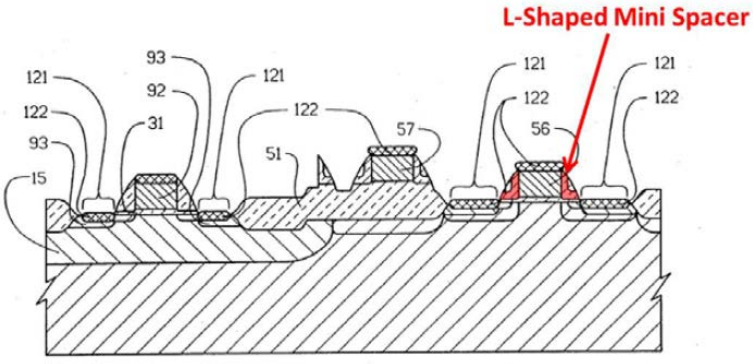


FIG. 12

The figures above depict mini-spacer oxide layer 62 in red and first spacer oxide layer 71 in blue, with Figure 12 showing mini-spacer oxide layer 62 on the sides of transistor gate 56 after etching. Lowrey discloses, in connection with Figure 8, that the two layers "are etched with a first anisotrophic etch, then optionally etched once again with a first isotropic etch to form a first set of sidewall spacers 81." Ex. 1017, col. 9, ll. 6–12. The fact that Lowrey eventually refers to "sidewall spacers 81" does not mean that they are not two layers (i.e., an L-shaped portion of mini-spacer oxide layer 62 and a wedge-shaped portion of first spacer oxide layer 71), particularly given that they remain shown as such in the figures. We also agree with Petitioner that the two layers are at least chemically different, as mini-spacer oxide layer 62 contains phosphorus but first spacer oxide layer 71 does not. *See* Reply 41; Ex. 1057 ¶ 147; Ex. 1017, col. 8, l. 53–col. 9, l. 5.

Second, Patent Owner argues that even if Lowrey teaches "second L-shaped sidewalls," there is nothing to suggest that they would be "formed over the side surfaces of the interconnection," as recited in claim 1, in the combined device. PO Resp. 118–119. According to Patent Owner, "the process of importing the trench isolation of *Noble* . . . inherently requires that the gate insulation and gate conductor be applied first, and then have a portion removed where the trench isolation will be inserted. As such, there would be no gate conductor electrode on top of the trench isolation." *Id.* at 118 (emphasis omitted). Further, if there were no gate electrode, when mini-spacer oxide layer 62 and first spacer oxide layer 71 are etched, "there would likely be insufficient height to the conductive wiring layer on the STI for an L-shape to form." *Id.* at 118–119. Patent Owner made a similar

argument with respect to the asserted combination of Lee and Noble, and we are not persuaded. *See supra* Section II.D.3. Petitioner relies on Lowrey for all components recited in claim 1 other than the "trench isolation." Thus, we do not look to other components in Noble as part of the combination. Petitioner's explanation regarding the L-shaped mini-spacer oxide layer 62 in the figures of Lowrey is sufficient. *See* -1247 Pet. 42–44.

Thus, we are persuaded that Lowrey and Noble collectively teach every limitation of claim 1.

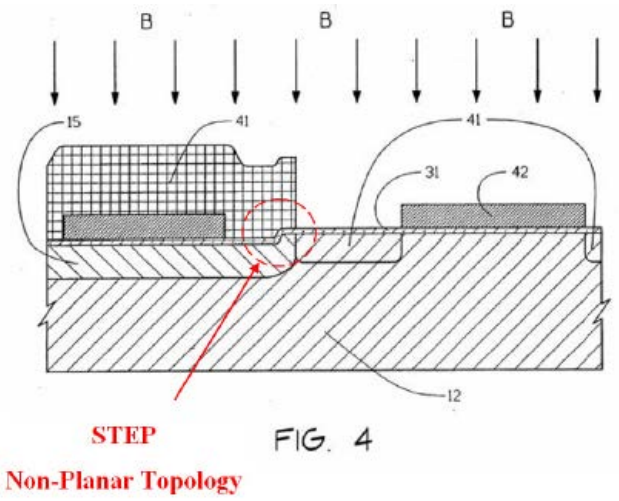
b. Whether a Person of Ordinary Skill in the Art Would Have Been Motivated to Combine Lowrey and Noble and Would Have Had a Reasonable Expectation of Success in Doing So

Petitioner's arguments regarding motivation to combine and reasonable expectation of success are very similar to those presented with respect to Lee and Noble, and repeat much of Petitioner's analysis regarding the history of LOCOS versus trench isolation and background knowledge of a person of ordinary skill in the art. *Compare* -1247 Pet. 21–30, *with* Pet. 21–30. Again, Petitioner's arguments are supported by the references themselves, the state of the art at the time of the '174 patent, and the testimony of Dr. Banerjee, and we find them persuasive. *See* -1247 Pet. 21–30; Ex. 1024 ¶¶ 80–94.

Patent Owner's arguments likewise are very similar to those made with respect to the asserted ground based on Lee and Noble, and we are not persuaded for similar reasons. *See, e.g.*, PO Resp. 63–69, 72–73, 110–17; *supra* Section II.D.3.b. With respect to the ground based on Lowrey and Noble in particular, Patent Owner argues that a person of ordinary skill in the art would not have used a trench isolation in Lowrey because "standard

planarization of the *Lowrey* device would ruin the *Lowrey* device." *See* PO Resp. 99–102 (citing Ex. 2012 ¶¶ 337–349). Patent Owner argues that creation of the trench isolation in Lowrey requires "(i) trench etching; (ii) refilling the trench (and coating the entire wafer) with an insulator (typically by chemical vapor deposition of SiO_2), and (iii) planarization of the wafer (e.g., by chemical mechanical planarization/polishing)" to flatten the wafer by removing excess silicon dioxide. *Id.* at 99.

Patent Owner provides the following annotated version of Figure 4 of Lowrey (*id.* at 100).



The figure above shows the "non-planar modulated surface topology" at this stage of Lowrey, where there is a "step in the Si active area surface" according to Patent Owner. *Id.* In the next step, shown in Figure 5, third photomask 41 is removed and field oxide region 51 is grown using LOCOS. Ex. 1017, col. 8, ll. 31–35. Patent Owner asserts that

> [t]he wafer surface area on which the trench isolation would have been etched is non-planar. As a result, the bottom of the trench would be non-planar. This in turn would have resulted in a non-uniformity of the trench causing non-uniformities of the electric field in the Si under the STI which is undesirable. For

> example, non-uniformities in the electric field can result in the enhancement of leakage currents.

PO Resp. 101; *see* Sur-Reply 23–40. Further, according to Patent Owner, forming a trench on an uneven surface like the one in Lowrey would result in "an uneven trench," either leaving unwanted material or removing wanted material, neither of which would have been acceptable to an ordinarily skilled artisan. PO Resp. 101–102.

Similar to the issues with Lee's doping sequence discussed above, Patent Owner's arguments regarding the step in Lowrey appear to be directed to an alleged problem with Lowrey itself, rather than a problem that would arise *from the combination* that may have discouraged a person of ordinary skill in the art from combining Lowrey's teachings with those of Noble. *See supra* n.13. Dr. Banerjee testifies that he

> do[es] not agree with Dr. Schubert that non-uniformity at the bottom of the trench would enhance leakage currents. *Lowrey* itself discloses a non-planar LOCOS isolation with non-uniformity at the bottom of the isolation region. Using STI with non-uniformity at the bottom of the trench would be no different and would not have deterred a person of ordinary skill in the art from this solution.

Ex. 1057 ¶ 107 n.11; *see id.* ¶¶ 104–111, 131–143. Dr. Banerjee also explains why the height difference in the combined device based on Lowrey's non-planar embodiment is immaterial in his view:

> In all of the[] processes [Dr. Banerjee discusses that substitute a trench isolation in place of Lowrey's LOCOS isolation], the structure is the same at the time the *Lowrey* MOS device is fabricated. The only exception is that in the illustrated embodiment of *Lowrey*, the surface of the substrate in the N-well regions are slightly lower than the surface of the substrate in the P-well regions. As a person of ordinary skill in the art would have recognized, that difference is not meaningful as it relates to

> the completion of the *Lowrey* device. For example, this level difference is present in *Lowrey* itself but does not adversely affect the device. For simplicity, the illustrations [provided by Dr. Banerjee] show level N-well and P-well regions. In the example where the N-well and P-well regions have slightly different heights, the illustrations would differ only in that the left-hand side of the STI structure in each figure would be slightly lower. The difference is immaterial to the process or device. For example, *Lowrey*'s illustrated embodiment already has a level difference, which does not prevent successful device formation. Eliminating that height difference also would not prevent successful device formation, because the height difference is immaterial to the subsequent processing steps for making the BiCMOS device structures. Whether there is or is not a level difference between the N-well and P-well regions is simply not relevant to whether a person of ordinary skill in the art would be able to complete the device according to the remaining descriptions in *Lowrey*. During contact formation, an interlevel dielectric (e.g., layer 131 in *Lowrey*) is deposited and planarized, so any level differences that could potentially affect the contacts (e.g., *Lowrey*'s metal layer 132) are eliminated.

Id. ¶ 132; *see* Reply 24 n.12. The combined device has the required structure (i.e., all of the components recited in claim 1) as Petitioner alleges and operates the same as Lowrey (using a trench isolation rather than LOCOS for isolation), and Petitioner's asserted motivations for why a person of ordinary skill in the art would have made the combination would still apply. We find Dr. Banerjee's explanation regarding the step in Lowrey persuasive and, given all of Petitioner's cited evidence, are persuaded that a person of ordinary skill in the art would have been motivated to combine Lowrey and Noble and would have had a reasonable expectation of success.

c. Conclusion

For the reasons set forth by Petitioner and explained above, we are persuaded that Lowrey and Noble collectively teach all of the limitations of claim 1, and that a person of ordinary skill in the art would have had reason to combine those teachings to achieve the semiconductor device of claim 1 and would have had a reasonable expectation of success in doing so. Petitioner has proven, by a preponderance of the evidence, that claim 1 would have been obvious based on Lowrey and Noble under 35 U.S.C. § 103(a).

3. Claims 4, 5, 8–10, and 16

We have reviewed and agree with Petitioner's contentions regarding dependent claims 4, 5, 8–10, and 16. *See* -1247 Pet. 44–55, 59–62. Patent Owner relies on its arguments regarding parent claim 1. PO Resp. 122. For the reasons stated by Petitioner, we are persuaded, by a preponderance of the evidence, that claims 4, 5, 8–10, and 16 would have been obvious based on Lowrey and Noble under 35 U.S.C. § 103(a). *See* -1247 Pet. 44–55, 59–62.

4. Claims 11, 12, and 14

Claims 11, 12, and 14 recite limitations pertaining to the material used for certain recited components. Claim 11 recites that "the interconnection is composed of the same material as the gate electrode," and claim 12 recites that "the gate electrode and the interconnection has at least a polysilicon film." To meet these limitations, Petitioner relies on the same "polysilicon layer" deposition used to form both transistor gate 56 and N-channel interconnect 57 in Figure 12 of Lowrey. -1247 Pet. 55–57 (citing Ex. 1017,

col. 7, ll. 14–20). Claim 14 recites that "the first and second L-shaped sidewalls are made of the same insulating film." To meet this limitation, Petitioner relies on the same component (i.e., mini-spacer oxide layer 62) used to form both sidewalls in Figure 12 of Lowrey. *Id.* at 58–59.

With respect to claims 11 and 12, Patent Owner argues that if Lowrey's LOCOS isolation is replaced with a trench isolation based on Noble, "the conductive wiring layer[] of *Noble* . . . would not be 'composed of the same material' and not have 'at least a polysilicon film.'" PO Resp. 122–123. Similarly, with respect to claim 14, Patent Owner argues that neither Lowrey nor Noble teaches sidewalls shaped like an L. *Id.* at 124–125. We are not persuaded. As explained above, Petitioner relies on Lowrey as teaching the recited "gate electrode," "interconnection," and "first and second L-shaped sidewalls," and relies on Noble *only* as teaching a "trench isolation." *See supra* Section II.F.2.a. We also agree with Petitioner that Lowrey teaches "first and second L-shaped sidewalls." *See id.* For the reasons stated by Petitioner, we are persuaded, by a preponderance of the evidence, that claims 11, 12, and 14 would have been obvious based on Lowrey and Noble under 35 U.S.C. § 103(a). *See* -1247 Pet. 55–59.

G. Obviousness Ground Based on Lowrey and Ogawa (Claims 1, 4, 5, 8–12, 14, and 16)

1. Claim 1

As with the other asserted combinations, Petitioner explains in detail how Lowrey and Ogawa collectively teach every limitation of claim 1, relying on the testimony of Dr. Banerjee as support. -1247 Pet. 30–44, 62, 68–71 (citing Ex. 1024 ¶¶ 175–185). Petitioner relies on Lowrey as teaching

all of the limitations other than a "trench isolation," referring to its previous analysis in the -1247 Petition, and relies on portion 52 in Ogawa as teaching a "trench isolation." *Id.*; *see CRFD Research*, 876 F.3d at 1345–46. As to the combined teachings of the references, Petitioner's position again is that a person of ordinary skill in the art would have been motivated to replace the LOCOS isolation in Lowrey's device (field oxide region 51) with the trench isolation of Ogawa (portion 52). -1247 Pet. 62 (arguing that a person of ordinary skill in the art "would have understood that *Ogawa*'s trench isolation was a known substitute for *Lowrey*'s LOCOS isolation," and "[t]he combined teachings discussed in [the -1247 Petition] refer to the teachings of *Lowrey*, with its LOCOS isolation replaced by *Ogawa*'s trench isolation"), 68–69. Petitioner's arguments as to how Lowrey and Ogawa collectively teach every limitation of claim 1 are supported by the testimony of Dr. Banerjee and are persuasive. *See id.* at 30–44, 68–71; Ex. 1024 ¶¶ 175–185.

Petitioner's arguments regarding motivation to combine and reasonable expectation of success are similar to those presented with respect to Lowrey and Noble (and Lee and Ogawa), reference much of Petitioner's previous analysis regarding the history of LOCOS versus trench isolation and background knowledge of a person of ordinary skill in the art, and discuss Ogawa's express teaching that trench isolation was viewed in the art as an improvement over LOCOS. *See* -1247 Pet. 62–68 (citing *id.* at 21–26); Ex. 1024 ¶¶ 163–174; *CRFD Research*, 876 F.3d at 1345–46. We are persuaded by Petitioner's analysis for similar reasons to those explained above regarding the other combinations. *See supra* Sections II.D.3.b, II.E.2.

Patent Owner argues the asserted ground based on Lowrey and Noble and the asserted ground based on Lowrey and Ogawa together. *See, e.g.*, PO Resp. 94–104, 110–127. These arguments are not persuasive for reasons similar to those set forth above. *See supra* Section II.F. For the reasons set forth by Petitioner and explained above, we are persuaded that Lowrey and Ogawa collectively teach all of the limitations of claim 1, and that a person of ordinary skill in the art would have had reason to combine those teachings to achieve the semiconductor device of claim 1 and would have had a reasonable expectation of success in doing so. Petitioner has proven, by a preponderance of the evidence, that claim 1 would have been obvious based on Lowrey and Ogawa under 35 U.S.C. § 103(a).

2. Dependent Claims 4, 5, 8–12, 14, and 16

We have reviewed and agree with Petitioner's contentions regarding dependent claims 4, 5, 8–12, 14, and 16, which are supported by the testimony of Dr. Banerjee. *See* -1247 Pet. 71–76; Ex. 1024 ¶¶ 186–209. In its Response, Patent Owner argues the asserted ground based on Lowrey and Noble and the asserted ground based on Lowrey and Ogawa together as to the dependent claims. PO Resp. 121–125. Patent Owner's arguments are not persuasive for the reasons set forth above. *See supra* Section II.F. Petitioner has proven, by a preponderance of the evidence, that claims 4, 5, 8–12, 14, and 16 would have been obvious based on Lowrey and Ogawa under 35 U.S.C. § 103(a).

H. Motions to Exclude

The party moving to exclude evidence bears the burden of proof to establish that it is entitled to the relief requested—namely, that the material sought to be excluded is inadmissible under the Federal Rules of Evidence. *See* 37 C.F.R. §§ 42.20(c), 42.62(a). For the reasons discussed below, the parties' Motions to Exclude are denied-in-part and dismissed-in-part.

1. Petitioner's Motion to Exclude

a. Dr. Schubert's Declarations (Exhibits 2001, 2011, and 2012)

Petitioner moves to exclude paragraphs 33–159 of Exhibit 2001, paragraphs 33–149 of Exhibit 2011, and paragraphs 4–10 and 35–458 of Exhibit 2012 under Federal Rule of Evidence 702. Pet. Mot. 3–6. Federal Rule of Evidence 702 provides:

> A witness who is qualified as an expert by knowledge, skill, experience, training, or education may testify in the form of an opinion or otherwise if:
>
> (a) the expert's scientific, technical, or other specialized knowledge will help the trier of fact to understand the evidence or to determine a fact in issue;
>
> (b) the testimony is based on sufficient facts or data;
>
> (c) the testimony is the product of reliable principles and methods; and
>
> (d) the expert has reliably applied the principles and methods to the facts of the case.

Petitioner argues that "Dr. Schubert is not qualified to opine on shallow trench isolation in silicon MOSFET devices." Pet. Mot. 3. For instance, Petitioner contends that "[a]lthough he has experience with III-V compound semiconductors and light-emitting devices (e.g., LEDs and laser diodes), those devices are very different from the Si MOSFET structures at issue in

these proceedings, and they do not involve LOCOS isolation or STI." *Id.* at 4. We have reviewed Dr. Schubert's testimony and are not persuaded that it would warrant the extreme remedy of exclusion. Petitioner's arguments regarding Dr. Schubert's alleged lack of specific experience with LOCOS isolation or STI indicate a mere disagreement with his testimony and pertain to the weight to be given to that testimony, which we are able to assess without excluding it. Petitioner's Motion to Exclude is denied as to Exhibits 2001, 2011, and 2012.

b. Other Exhibits

Petitioner moves to exclude Exhibits 2002–2010, 2013–2019, 2026–2030, 2032, and 2033 as "irrelevant and non-probative" under Federal Rules of Evidence 401, 402, and 403, and Exhibits 2003, 2004, and 2026 as hearsay under Federal Rules of Evidence 801 and 802. Pet. Mot. 6–13. Petitioner's Motion to Exclude is dismissed as moot with respect to these exhibits, as we do not rely on them in a manner adverse to Petitioner.[17]

2. Patent Owner's Motion to Exclude

a. Ueda (Ex. 1014)

Patent Owner moves to exclude Ueda on the basis that it is not prior art to the challenged claims. PO Mot. 1–6. Pre-AIA 35 U.S.C. § 103(c)(1) provided:

> Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under

[17] Indeed, Patent Owner does not mention any of Exhibits 2002, 2003, or 2005–2010 in its Response or Sur-Reply. *See* Pet. Mot. 6–9.

> this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person.

According to Patent Owner, Ueda and the application that issued as the '174 patent were commonly owned by Matsushita Electric Industrial Co., Ltd. PO Mot. 1, 3–4 (citing newly filed Exs. 2061–2076 as support).[18]

Petitioner's asserted grounds of unpatentability are based on combinations of Lee, Lowrey, Noble, and Ogawa. Petitioner relies on these references for every structural component recited in the challenged claims. Ueda is relied upon as support for Petitioner's contentions as to why a person of ordinary skill in the art would have been motivated to replace a LOCOS isolation (of Lee or Lowrey) with a trench isolation (of Noble or Ogawa) and to show the background knowledge that such a person would have had when considering the cited prior art. *See supra* Section II.D.3.b. Further, as explained above, Ueda (as well as other references and the testimony of Dr. Banerjee) show that it was within the knowledge of a person of ordinary skill in the art to make a trench isolation before making

[18] We stated in the Decision on Institution that we agreed with Petitioner, based on the record available at the time, that the '174 patent is not entitled to the July 27, 1995 filing date of Japanese Patent Application No. 7-192181, such that the earliest potential effective filing date of the '174 patent would be December 19, 1995. Dec. on Inst. 13 n.5. The parties did not address the effective filing date issue further during trial, and we do not perceive any reason or evidence that compels any deviation from our preliminary determination. Patent Owner also states that the '174 patent's "effective U.S. filing date is July 24, 1996." PO Mot. 2. Ueda was filed on December 12, 1995, and thus would constitute prior art under pre-AIA 35 U.S.C. § 102(e) (absent any potential application of 35 U.S.C. § 103(c)).

the gate stack, which is the order of steps in which Lee and Lowrey make their LOCOS isolations. *See id.*

That usage is proper, regardless of whether Ueda is disqualified as prior art under 35 U.S.C. § 103(c). *See Cross Med. Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1320–22 (Fed. Cir. 2005) (holding that "[e]vidence of a motivation to combine references need not be in the form of prior art," and finding certain materials prepared by clinical investigators, although not prior art to the patent at issue, to be sufficient to establish "a genuine issue of material fact . . . with respect to motivation to combine"); *National Steel Car, Ltd. v. Canadian Pacific Ry., Ltd.*, 357 F.3d 1319, 1337–38 (Fed. Cir. 2004) (holding that "[i]t has long been the law that the motivation to combine need not be found in prior art references, but equally can be found 'in the knowledge generally available to one of ordinary skill in the art,'" and "[t]he motivation to combine can be located either in a prior art reference, *or* it can be implicit in the knowledge of one of ordinary skill in the art," and finding that two documents "pre-dating the application for the [patent at issue]," although not prior art printed publications, showed a motivation to combine (citations omitted)); *Thomas & Betts Corp. v. Litton Sys., Inc.*, 720 F.2d 1572, 1580–81 (Fed. Cir. 1983) (holding that "unpublished internal criteria," "though not technically prior art, were, in effect, properly used as indicators of the level of ordinary skill in the art to which the invention pertained," where the district court had cited the criteria "as evidence of the fact that accomplishing a pitch change by means of offsetting paired apertures would have been within the knowledge of one of ordinary skill in the art"); *Lockheed Aircraft Corp. v. United States*, 553 F.2d 69, 78 (1977) ("It is clear that these reports . . . are not prior art

within the meaning of 35 U.S.C. §§ 102 or 103. . . . Nevertheless, such classified reports are indicative of the general level of skill in the art.").

Contrary to Patent Owner's arguments, Petitioner does *not* rely on Ueda for the "trench isolation" limitation of claim 1 (i.e., Petitioner does not argue that a person of ordinary skill in the art would have been motivated to replace Lee's or Lowrey's LOCOS isolation with the particular STI structure of Ueda). *See* PO Mot. Reply 1. Petitioner relies on Noble and Ogawa each as teaching the "trench isolation" limitation. *See supra* Section II.D.3.b. Moreover, even if Ueda and the application that issued as the '174 patent were commonly owned, the substance of Ueda's disclosure is not the inventors' disclosure. Ueda is probative of what a person of ordinary skill in the art would have been motivated to do and what would have been within that individual's skill level to do. Petitioner's reliance on Ueda is proper,[19] and Patent Owner's Motion to Exclude the exhibit is denied.

b. Exhibits 1003, 1005–1009, 1011–1014, 1016, 1018, 1025–1055, 1057, and 1058

Patent Owner moves to exclude Exhibits 1032, 1034, 1035, 1042, 1043, 1055, 1057, and 1058 as duplicative of other evidence submitted by Petitioner and, therefore, "not relevant, and . . . likely to cause unfair prejudice, confusing the issues, wasting time, and/or needlessly presenting cumulative evidence" under Federal Rules of Evidence 401, 402, and 403. PO Mot. 6–7 (citing Reply 17). Similarly, Patent Owner moves to exclude

[19] Given this conclusion, we need not determine whether Patent Owner's objection to Ueda, which did not mention 35 U.S.C. § 103(c), was sufficiently specific under 37 C.F.R. § 42.64(b)(1). *See* Pet. Mot. Opp. 3–4; Paper 12, 4.

Exhibits 1003, 1005–1008, 1011–1013, 1016, 1018, 1025–1055, 1057, and 1058 under the same rules as irrelevant because "(1) they contain little or no discussion regarding their relevance, (2) no effort was made to specifically link any of these exhibits to the unpatentability assertions, and (3) these exhibits are not part of any of the grounds for which trial was instituted, *i.e.*, none of these exhibits are referred to or cited by the Board in the Decision on Institution." PO Mot. 7–8. Finally, Patent Owner moves to exclude Exhibits 1003, 1005–1009, 1011–1014, 1016, 1018, 1025–1055, and 1058 under Rules 401 and 402 because "they are not alleged to be invalidating prior art and thus are irrelevant." PO Mot. 8–9.

We have considered all of the cited exhibits and rely on certain ones in this Decision. We also addressed above Petitioner's use of certain exhibits to show, for example, the background knowledge of a person of ordinary skill in the art. *See supra* n.11. Evidence is not irrelevant simply because it is not asserted as part of one of Petitioner's unpatentability grounds or was not cited in our Decision on Institution. *See id.*; *Genzyme*, 825 F.3d at 1367–69 (holding that "the Board may consider a prior art reference to show the state of the art at the time of the invention, regardless of whether that reference was cited in the Board's institution decision," and rejecting the argument that references could not be used to show a reasonable expectation of success because they "were not among the combinations of references on which the Board granted review"). Upon review of these exhibits, we find them relevant under Rule 401 and find that their probative value is not substantially outweighed by any of the factors listed in Rule 403.

Patent Owner further moves to exclude Exhibits 1025–1055, 1057, and 1058 as improperly submitted with Petitioner's Reply. PO Mot. 9–13. We addressed the propriety of Petitioner's Reply evidence above, and deny the Motion to Exclude as to the cited exhibits. *See supra* Section II.D.3.c.

c. Exhibits 1049 and 1051

Patent Owner moves to exclude Exhibits 1049 and 1051 under Federal Rules of Evidence 401–403 on the basis that they are not prior art to the challenged claims. PO Mot. 9. As we do not rely on them for our Decision, Patent Owner' Motion to Exclude is dismissed as moot with respect to these exhibits.

III. ORDER

Petitioner has demonstrated, by a preponderance of the evidence, under 35 U.S.C. § 103(a), that

(1) claims 1–3, 5–7, 9–12, and 14–18 are unpatentable over Lee and Noble;

(2) claims 1–3, 5–7, 9–12, and 14–18 are unpatentable over Lee and Ogawa;

(3) claims 1, 4, 5, 8–12, 14, and 16 are unpatentable over Lowrey and Noble; and

(4) claims 1, 4, 5, 8–12, 14, and 16 are unpatentable over Lowrey and Ogawa.

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–12 and 14–18 of the '174 patent have been shown to be unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude (Paper 29) is *denied-in-part* and *dismissed-in-part*; and

FURTHER ORDERED that Patent Owner's Motion to Exclude (Paper 32) is *denied-in-part* and *dismissed-in-part*.

This is a final decision. Parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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