Trials@uspto.gov
571-272-7822

Paper No. 46
Entered: January 17, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
and GLOBALFOUNDRIES U.S. INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01377[1]
Patent 6,197,696 B1

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

---

[1] GlobalFoundries U.S. Inc.'s motion for joinder in Case IPR2017-00922 was granted.

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 10–12 ("the challenged claims") of U.S. Patent No. 6,197,696 B1 (Ex. 1001, "the '696 patent") are unpatentable.

A. Procedural History

Taiwan Semiconductor Manufacturing Company, Ltd. ("Petitioner")[2] filed a Petition for *inter partes* review of claims 10–12 of the '696 patent. Paper 2 ("Pet."). Petitioner provided a Declaration of Bruce W. Smith, Ph.D., (Ex. 1002) to support its positions. Godo Kaisha IP Bridge 1 ("Patent Owner") filed a Preliminary Response to the Petition. Paper 6 ("Prelim. Resp."). Pursuant to our authorization (Paper 7), Petitioner filed a Reply to the Preliminary Response (Paper 9) and Patent Owner filed a Sur-Reply (Paper 10).

Pursuant to 35 U.S.C. § 314(a), on January 18, 2017, we instituted *inter partes* review to determine whether claims 10–12 are unpatentable

[2] On August 8, 2017, we granted a motion for joinder filed by GlobalFoundries U.S. Inc. ("GlobalFoundries") in IPR2017-00922, and authorized GlobalFoundries to participate in this proceeding only on a limited basis. *See* Paper 29; Ex. 3003 (IPR2017-00922, Paper 10). Although the papers referenced herein were filed by Taiwan Semiconductor Manufacturing Company, Ltd., we refer to both entities as "Petitioner" throughout this Decision.

under 35 U.S.C. § 103(a) as obvious in view of Grill[3] and Aoyama.[4] *See* Paper 11 ("Inst. Dec."). Subsequent to institution, Patent Owner filed a Patent Owner Response (Paper 19, "PO Resp."), along with a Declaration of Alexander Glew, Ph.D., (Ex. 2009) to support its positions. Petitioner filed a Reply (Paper 26, "Reply") to the Patent Owner Response, along with a second Declaration of Dr. Smith (Ex. 1050) in support thereof.

Petitioner filed a Motion to Exclude (Paper 30, "Pet. Mot.") certain evidence submitted by Patent Owner. Patent Owner filed an Opposition (Paper 37), and Petitioner filed a Reply (Paper 41). Patent Owner filed Observations on the cross-examination of Dr. Smith (Paper 34), and Petitioner filed a Response thereto (Paper 35). Pursuant to our authorization, Patent Owner also filed a listing of portions of Petitioner's Reply that allegedly exceed the proper scope of a reply (Paper 36).

A combined oral hearing for IPR2016-01376, IPR2016-01377, IPR2016-01378, and IPR2016-01379 was held on September 12, 2017. A transcript of the hearing is included in the record. Paper 45 ("Tr.").

B. Related Proceedings

The parties indicate that the '696 patent has been asserted in *Godo Kaisha IP Bridge 1 v. Broadcom Ltd.*, No. 2-16-cv-00134 (E.D. Tex. 2016). Paper 4, 2; Pet. 84. Three additional *inter partes* reviews challenge claims of the '696 patent. *See* Case IPR2016-01376; Case IPR2016-01378; Case IPR2016-01379; Pet. 82–83; Paper 4, 2–3.

---

[3] U.S. Patent No. 6,140,226, filed July 30, 1998, issued Oct. 31, 2000 (Ex. 1005).

[4] U.S. Patent No. 5,592,024, issued Jan. 7, 1997 (Ex. 1018).

C. The '696 Patent

The '696 patent relates to a "method for forming an interconnection structure in a semiconductor integrated circuit." Ex. 1001, 1:5–7. According to the '696 patent, "[a]n object of the present invention is providing a method for forming an interconnection structure in which an insulating film with a low dielectric constant can be formed by an ordinary resist application process." *Id.* at 3:2–5.

The '696 patent describes various embodiments of methods of forming an interconnection structure. *Id.* at [57]. The manufacturing process for a modified example of the fifth embodiment is depicted in Figures 24(a)–(c), 25(a)–(c), and 26(a)–(d). *Id.* at 24:52–27:60.

Figure 24(a) of the '696 patent is reproduced below.

Fig. 24(a)

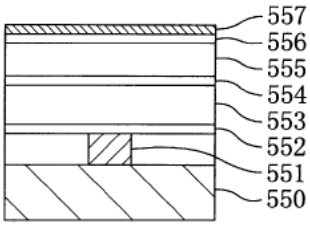


Figure 24(a), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. Ex. 1001, 9:28–31. As seen in Figure 24(a), silicon nitride film 552 is formed over first metal interconnects 551 (only one shown in Figure 24(a)), which are formed on semiconductor substrate 550. *Id.* at 24:60–62. First organic film 553, first silicon dioxide film 554, second organic film 555, second silicon dioxide film 556, and titanium nitride film 557 are deposited sequentially. *Id.* at 24:65–25:11.

Figure 24(b) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 24(b)

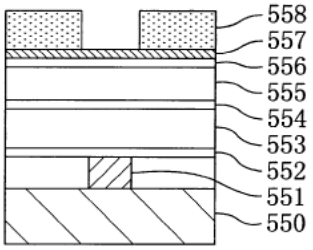


Figure 24(b), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. *Id.* at 9:28–31. In this step, first resist pattern 558 is formed on titanium nitride film 557. *Id.* at 25:19–21. First resist pattern 558 includes openings for forming wiring grooves of the interconnection structure. *Id.*

Figure 24(c) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 24(c)

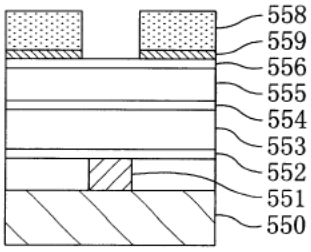


Figure 24(c), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. Ex. 1001, 9:28–31. In this step, titanium nitride film 557 is dry-etched using first resist pattern 558 as a mask, thereby forming mask pattern 559. *Id.* at 25:21–23.

Figure 25(a) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 25(a)

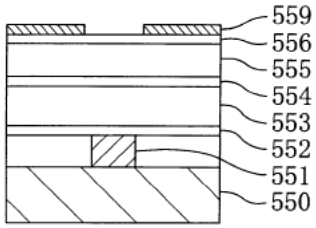


Figure 25(a), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. *Id.* at 9:32–35. In this step, first resist pattern 558 is removed. *Id.* at 25:26–27.

Figure 25(b) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 25(b)

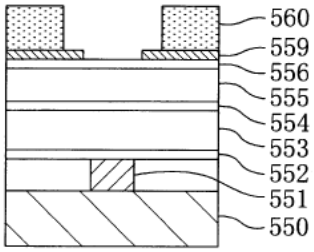


Figure 25(b), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. Ex. 1001, 9:32–35. In this step, second resist pattern 560 is formed on mask pattern 559. *Id.* at 25:27–29. Second resist pattern 560 includes openings for forming contact holes of the interconnection structure. *Id.* In this embodiment, the openings in second resist pattern 560 are larger than the designed size of the contact holes “in respective directions vertical and parallel to [the] wiring grooves.” *Id.* at 25:29–34.

Figure 25(c) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 25(c)

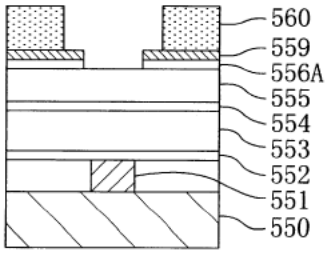


Figure 25(c), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. *Id.* at 9:32–35. In this step, second silicon dioxide film 556 is dry-etched using both second resist pattern 560 and mask pattern 559 as a mask, thereby forming patterned second silicon dioxide film 556A. *Id.* at 25:36–39.

A three-dimensional depiction of etching using both second resist pattern 560 and mask pattern 559 as a mask is provided in Figure 27(b) of the ’696 patent, which is reproduced below.

Fig. 27(b)

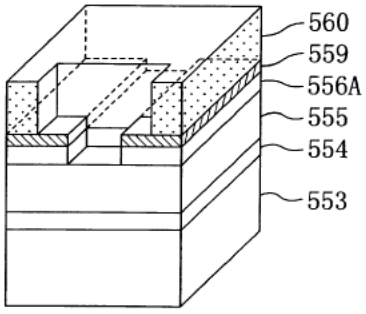


Figure 27(b), reproduced above, is a perspective view of the partially formed interconnection structure of Figure 25(c). Ex. 1001, 9:40–42. As can be seen in Figure 27(b), patterned second silicon dioxide film 556A is etched only where the openings in the second resist pattern 560 and mask pattern 559 overlap.

According to the ’696 patent, using larger openings in second resist pattern 560 allows “openings of the patterned second silicon dioxide film 556A for forming contact holes [such that they are] self-aligned with the openings of the mask pattern 559 for forming wiring grooves,” “even if the openings of the second resist pattern 560 for forming contact holes have misaligned with the openings of the mask pattern 559 for forming wiring grooves.” *Id.* at 25:46–52. This self-alignment occurs “because the openings of the patterned second silicon dioxide film 556A for forming contact holes are formed in respective regions where the openings of the second resist pattern 560 for forming contact holes overlap with corresponding openings of the mask pattern 559 for forming wiring grooves.” *Id.* at 25:53–57.

Figure 26(a) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 26(a)

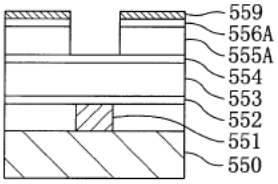


Figure 26(a), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. *Id.* at 9:36–39. In this step, second organic film 555 is dry-etched using patterned second silicon dioxide film 556A as a mask, thereby forming patterned second organic film 555A. *Id.* at 25:66–26:1; *see also id.* at Fig. 28(a) (showing a perspective view of this process step).

Figure 26(b) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 26(b)

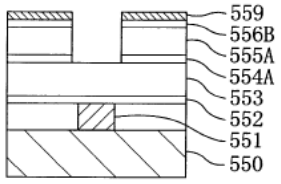


Figure 26(b), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. *Id.* at 9:36–39. In this step, patterned second silicon dioxide film 556A (Fig. 26(a)) is dry-etched using mask pattern 559 as a mask, and first silicon dioxide film 554 (Fig. 26(a)) is dry-etched using patterned second organic film 555A as a mask. *Id.* at 26:15–18; *see also id.* at Fig. 28(b) (showing a perspective view of this process step).

Figure 26(c) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 26(c)

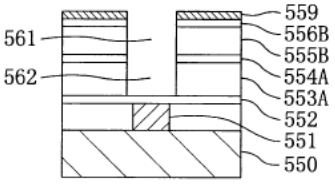


Figure 26(c), reproduced above, is a cross-sectional view of a partially formed interconnection structure during a process step for forming the same. Ex. 1001, 9:36–39. In this step, patterned second organic film 555A (Fig. 26(b)) is dry-etched using mask pattern 559 and patterned second silicon dioxide film 556B as a mask, and first organic film 553 (Fig. 26(b)) is dry-etched using patterned silicon dioxide film 554A as a mask. *Id.* at 26:22–26; *see also id.* at Fig. 29(a) (showing a perspective view of this process step). This etching forms patterned second organic film 555B

having wiring grooves 561 and patterned first organic film 553A having contact holes 562. *Id.* at 26:26–29.

Figure 26(d) of the ’696 patent, illustrating a subsequent step in the method of this embodiment, is reproduced below.

Fig. 26(d)

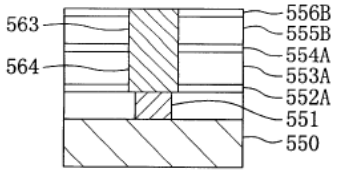


Figure 26(d), reproduced above, is a cross-sectional view of an interconnection structure formed by the method of the modified fifth embodiment. *Id.* at 9:36–39. In this step, silicon nitride film 552 is dry-etched using patterned first silicon dioxide film 554A as a mask. *Id.* at 26:30–31. This etching forms patterned silicon nitride film 552A having contact holes, and also exposes first metal interconnects 551 within contact holes 562. *Id.* at 26:32–34. Then, a metal film is deposited over the surface of the substrate to fill in contact holes 562 and wiring grooves 561, thus forming second metal interconnects 563 and contacts 564. *Id.* at 26:38–47.

D. Illustrative Claim

Of the challenged claims, claim 10 is independent, and claims 11 and 12 depend therefrom. Claim 10 of the ’696 patent, reproduced below, is illustrative of the challenged claims:

> 10. A method for forming an interconnection structure, comprising the steps of:
>
> a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film;

e) forming a thin film over the fourth insulating film;

f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes;

j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes;

> l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and
>
> m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

Ex. 1001, 34:1–49.

II. ANALYSIS

A. Principles of Law

To prevail in its challenges to the patentability of the claims, Petitioner must demonstrate by a preponderance of the evidence that the challenged claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378–79 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burdens of persuasion and production in *inter partes* review).

A claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would

have been obvious at the time the invention was made." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). The question of obviousness is resolved on the basis of underlying factual determinations, including "the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved."[5] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418 (for an obviousness analysis, "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does"). A motivation to combine the teachings of two references can be "found explicitly or implicitly in market forces; design incentives; the 'interrelated teachings of multiple patents'; 'any need or problem known in the field of endeavor at the

[5] Additionally, secondary considerations, such as "commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy." *Graham*, 383 U.S. at 17–18. The record, however, lacks any such evidence.

time of invention and addressed by the patent'; and the background knowledge, creativity, and common sense of the person of ordinary skill." *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013) (citation omitted). Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'" (citation omitted)).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have possessed "(1) the equivalent of a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, or the equivalent; (2) a working knowledge of semiconductor processing technologies for integrated circuits; and (3) at least two years of experience in related semiconductor processing analysis, design, and development. Additional graduate education could substitute for professional experience, and significant work experience could substitute for formal education." Pet. 30 (citing Ex. 1002 ¶ 167) (internal citations omitted). Dr. Glew testifies that "a person of ordinary skill in the art would have had a Bachelor's of Science degree in materials science engineering, electrical engineering, mechanical engineering, chemical engineering, or an equivalent degree, and at least two years of experience in semiconductor processing or equipment." Ex. 2009 ¶ 22.

We note the parties' proposals differ in the specific degree required (i.e., Master of Science vs. Bachelor's of Science); however, neither party argues this distinction makes a difference in analyzing the asserted ground or other issues in this proceeding. For clarity of the record, we adopt Petitioner's proposal regarding the level of ordinary skill in the art, as it is more specifically directed to the technology described in the '696 patent. In addition, given the disclosures in the '696 patent and cited prior art, we agree with Petitioner that a Master of Science degree (or equivalent) in the relevant area better reflects the level of education and training that an ordinarily skilled artisan would have possessed at the time than a Bachelor's degree, as Patent Owner contends. Our findings and conclusions, however, would be the same under either party's proposed level of ordinary skill in the art. The level of ordinary skill in the art in this case further is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). Pursuant to that standard, the claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. *See In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir. 2010). We generally give claim terms their ordinary and customary meaning. *See In re Translogic*

Tech., Inc., 504 F.3d 1249, 1257 (Fed. Cir. 2007) ("The ordinary and customary meaning 'is the meaning that the term would have to a person of ordinary skill in the art in question.'" (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc))).

The claims, however, "should always be read in light of the specification and teachings in the underlying patent," and "[e]ven under the broadest reasonable interpretation, the Board's construction 'cannot be divorced from the specification and the record evidence.'" *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (quoting *In re NTP, Inc.*, 654 F.3d 1279, 1288 (Fed. Cir. 2011)). In other words, "[u]nder a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history." *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016) (citing *Straight Path IP Grp., Inc. v. Sipnet EU S.R.O.*, 806 F.3d 1356, 1362 (Fed. Cir. 2015)). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). However, limitations are not to be read from the specification into the claims. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

1. Construction of "using the [designated layer] as a mask"

In the Institution Decision, we preliminarily construed the phrase "using the [designated layer] as a mask"[6] as "using the [designated layer] to

[6] Claim 10 recites several steps of etching "using" various layers—for example, the first resist pattern [step g]/second resist pattern and the mask pattern [step i]/patterned fourth insulating film [step j]—"as a mask." As shorthand, we refer to the various layers as "the designated layer."

define areas for etching."[7] Inst. Dec. 11–15. We further determined that "to meet the limitation 'using the [designated layer] for etching,' the designated layer 'must actually be *used* to *define areas for etching*.'" *Id.* at 15 (quoting Prelim. Resp. 6 (emphasis Patent Owner's)). Patent Owner agrees with this construction—namely, that "'using' something 'as a mask' during etching means *using it to define areas for etching*." PO Resp. 8–9. Petitioner also applied this construction in this proceeding. *See* Tr. 6:7–18; *see also id.* at 19:10–16 (Petitioner's counsel: "No, no, we did not present a construction and we did not contest the Board's construction."). The parties do not dispute that "using the [designated layer] as a mask" means "using the [designated layer] to define areas for etching," and we discern no reason from the evidence presented to change this construction. We, therefore, maintain our preliminary construction for purposes of this Final Written Decision.

2. Application of the Construction of "using the [designated layer] as a mask"

In the Institution Decision, we also provided additional guidance as to what "using the [designated layer] to define areas for etching" encompasses. *See* Inst. Dec. 15–19. In this regard, we provided the following non-exhaustive examples:

> [W]e do not consider a mask pattern that is entirely within a surrounding resist layer to be "used as a mask" within the meaning of claim 10.

Id. at 15–16.

[7] The district court construed the phrase in the same manner in an Order dated November 9, 2016. Ex. 3002, 20–22.

> We . . . are not persuaded that a layer, positioned between an overlying layer and the layer being etched and having an edge in line and flush with an edge of the overlying layer, is "used as a mask" within the meaning of claim 10. Instead, to be "used as a mask," the between layer would need to define an additional portion of the layer being etched that is to be shielded from etching.

Id. at 18 (citing Figures 25(c) and 27(b) of the '696 patent as an example of "defin[ing] an additional portion . . . to be shielded from etching").

> Our construction does not preclude, for example, a layer positioned between an overlying layer and the layer being etched from acting as a mask, within the meaning of claim 10, in an instance where the overlying layer also is removed during the etching, and thus, the between layer acts to shield the layer being etched during etching.

Id. at 18 n.7.

Patent Owner argues, pointing to this discussion, that "the Board . . . incorrectly added an ***additional negative limitation*** that 'a layer, positioned between an overlying layer and the layer being etched and having an edge in line and flush with an edge of the overlying layer' is **not** '"used as a mask" within the meaning of claim 10.'" PO Resp. 9–10 (quoting Inst. Dec. 18) (emphasis Patent Owner's); *see also id.* at 10–18. Patent Owner presents several arguments regarding this allegedly improper "additional negative limitation."[8] Because the parties' arguments regarding the priority claim of

[8] The Institution Decision does not add any negative limitations to the claim construction. Our construction of "using the [designated layer] as a mask" was simply "using the [designated layer] to define areas for etching." *See* Inst. Dec. 11–15. Patent Owner refers to our discussion of what the claim construction encompasses as an "additional negative limitation." For convenience, we mirror Patent Owner's language in discussing Patent Owner's arguments. However, as noted, we do not view the discussion

the '696 patent (*see infra* Section II.D.1) turn on the application of our claim construction, we address Patent Owner's arguments here for convenience.

> *Whether the "additional negative limitation impermissibly excludes preferred embodiments" of the '696 Patent (PO Resp. 10)*
>
> Patent Owner argues:
>
> > The additional negative limitation improperly excludes three preferred embodiments (*i.e.*, the third embodiment, a modified version of the third embodiment, and a modified version of a fifth embodiment) because they each require using an overlying layer and an intermediate layer together as a mask, where the intermediate layer has an edge that is ***in line and flush with*** an edge of the overlying layer.

PO Resp. 10–11 (citing Ex. 1001, 10:19–20, 16:39–48, 18:59–20:49, 24:52–27:60; Ex. 2009 ¶¶ 50–62).

While we agree with Patent Owner that a construction that "exclud[es] a preferred embodiment . . . 'is rarely, if ever, correct'" (PO Resp. 10 (citing *On–Line Techs. v. Bodenseewerk Perkin–Elmer GmbH*, 386 F.3d 1133, 1138 (Fed. Cir. 2004))), we note also that *every* claim need not cover *every* preferred embodiment (*see, e.g.*, *Cybersettle, Inc. v. Nat'l Arbitration Forum, Inc.*, 243 F. App'x 603, 608 (Fed. Cir. 2007) (nonprecedential) ("Although Cybersettle's characterization of the specification is accurate, its argument based on the specification is flawed. That is because our

---

found at pages 15 to 19 of the Institution Decision as adding a negative limitation, but rather as examples of factual circumstances in which a particular layer is or is not used to define areas for etching. In other words, the discussion to which Patent Owner refers as an "additional negative limitation," was merely additional guidance provided to the parties as to what "using the [designated layer] to define areas for etching" encompasses. *See id.* at 15–19.

interpretation of claim 1 does not exclude the discussed embodiments from the scope of the claimed invention, but only excludes those embodiments from the scope of that claim. Although claim 1 does not capture the discussed embodiments, other claims do.")). Further, there is no requirement that every feature disclosed in the specification be recited in the claims. *See Ventana Med. Sys., Inc. v. Biogenex Labs., Inc.*, 473 F.3d 1173, 1181–82 (Fed. Cir. 2006) ("Although the preferred embodiments also contain a 'direct dispensing' feature, the inventors were not required to claim this feature in the '861 patent and, indeed, did not do so.").

In any event, we disagree that our construction, or our application thereof with which Patent Owner disagrees, excludes the features of the embodiments identified by Patent Owner. Regarding the modified fifth embodiment, for example, claim 10 covers this embodiment. A chart comparing the modified fifth embodiment to claim 10 is provided below.[9] *See* Ex. 1001, 24:53–26:47.

Claim 10	**Figures Illustrating Modified Fifth Embodiment**
A method for forming an interconnection structure, comprising the steps of:	
a) forming a first insulating film [553] over lower-level metal interconnects [551];	Fig. 24(a)

[9] The bracketed numbers within the claim language identify the elements of the corresponding figures, as recited in the claims. They correspond to the identifications made in the description of the modified fifth embodiment, correlating the specific elements in the figures to the claim language. *See, e.g.*, Ex. 1001, 24:65–66 ("a first organic film 553 (first insulating film)").

Claim 10	**Figures Illustrating Modified Fifth Embodiment**
b) forming a second insulating film [554], having a different composition than that of the first insulating film, over the first insulating film [557];	
c) forming a third insulating film [555], having a different composition than that of the second insulating film, over the second insulating film [554];	
d) forming a fourth insulating film [556], having a different composition than that of the third insulating film, over the third insulating film [555];	
e) forming a thin film [557] over the fourth insulating film [556];	
f) forming a first resist pattern [558] on the thin film [557], the first resist pattern [558] having openings for forming wiring grooves;	Fig. 24(b)
g) etching the thin film [557] using the first resist pattern [558] as a mask, thereby forming a mask pattern [559] out of the thin film to have the openings for forming wiring grooves;	Fig. 24(c)
h) removing the first resist pattern [558] and then forming a second resist pattern [560] on the fourth insulating film [556] and the mask pattern [559], the second resist pattern [560] having openings for forming contact holes;	Fig. 25(a), Fig. 27(a) Fig. 25(b), (seen in Fig. 27(b), after the etching of step (i))
i) dry-etching the fourth insulating film [556] using the second resist pattern [560] and the mask pattern [559] as a mask, thereby patterning the fourth insulating film [556A] to have the openings for forming contact holes;	Fig. 25(c), Fig. 27(b)
j) dry-etching the third insulating film [555] using the patterned fourth insulating film [556A] as a mask, thereby patterning the third insulating film [555A] to have the openings for forming contact holes;	Fig. 26(a); Fig. 28(a)

Claim 10	**Figures Illustrating Modified Fifth Embodiment**
k) dry-etching the patterned fourth insulating film [556A] and the second insulating film [554] using the mask pattern [559] and the patterned third insulating film [555A] as respective masks, thereby forming wiring grooves in the patterned fourth insulating film [556B] and patterning the second insulating film to have the openings for forming contact holes [554A];	Fig. 26(b); Fig. 28(b)
l) dry-etching the patterned third insulating film [555A] and the first insulating film [553] using the mask pattern [559] and the patterned second insulating film [554A] as respective masks, thereby forming the wiring grooves [561] and the contact holes [562] in the patterned third insulating film and the first insulating film, respectively; and	Fig. 26(c); Fig. 29(a)
m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects [563] and contacts [564] connecting the lower- and upper-level metal interconnects together.	Fig. 26(d); Fig. 29(b)

Patent Owner points to Figures 28(b) and 29(a) of the '696 patent, and provides annotated versions, reproduced below (PO Resp. 14[10]).

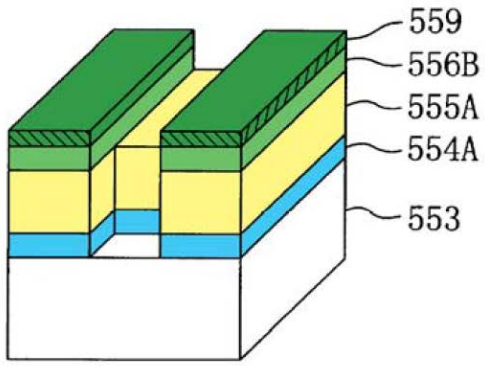


Fig. 28(b)

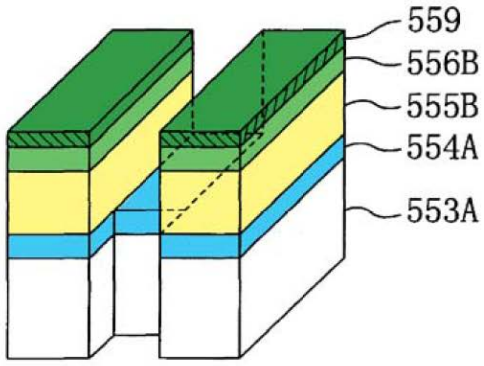


Fig. 29(a)

Figures 28(b) and 29(a), above, are perspective views of a partially formed interconnection structure. Ex. 1001, 9:43–48. As noted by Patent Owner, the Specification describes that, after the step shown in Figure 28(b),

> the *patterned second organic film 555A is dry-etched using the mask pattern 559 and the patterned second silicon dioxide film 556B as a mask*, and the first organic film 553 is dry-etched using the patterned first silicon dioxide film 554A as a mask, thereby forming a patterned second organic film 555B having wiring grooves 561 and a patterned first organic film 553A having contact holes 562 as shown in FIGS. 26(c) and 29(a).

Ex. 1001, 26:22–29 (emphasis added); PO Resp. 13. Patent Owner argues that patterned second silicon dioxide film 556B (i.e., the claimed patterned fourth insulating layer with the wiring grooves formed therein) is not used as a mask, under our application of the construction, despite being described as

[10] Patent Owner indicates that "[a]s illustrated [in the Patent Owner Response] layers being used as a mask for a certain step are indicated in green, [and] layers to be or having been etched for a certain step are indicated in yellow." PO Resp. 7 n.5 (citing Ex. 2009 ¶ 43 n.2).

such in the Specification. PO Resp. 13–14. The claim, however, does not recite this step in this manner. As noted in the chart above, in this embodiment, step (k) of claim 10 results in the structure shown in Figure 28(b). The step describing the etching of patterned second organic film 555A corresponds to step (l) of claim 10, and recites only "dry-etching the patterned third insulating film [555A] . . . using the mask pattern [559] . . . as [a] mask[]." The claim does not recite using the patterned fourth insulating layer with the wiring grooves formed therein (i.e., patterned second silicon dioxide film 556B) as a mask for etching the patterned third insulating film (i.e., patterned second organic film 555A). Thus, contrary to Patent Owner's assertion, our application of the construction does not exclude this embodiment.

Similarly, regarding the third embodiment and the modified third embodiment, the portions of the Specification that Patent Owner asserts are excluded from the claims under our application of the construction are not actually recited in any claim.

Regarding the modified third embodiment, Patent Owner points to Figures 16(c) and 16(d) of the '696 patent, and provides annotated versions, reproduced below (PO Resp. 12).

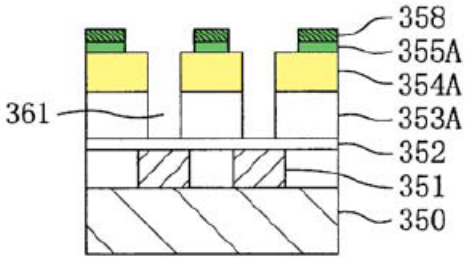


Fig. 16(c)

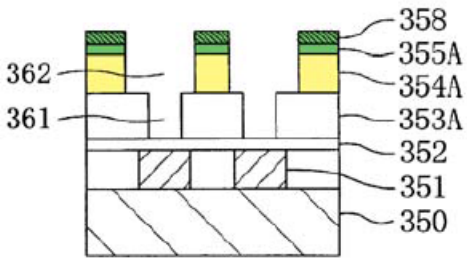


Fig. 16(d)

Figures 16(c) and 16(d), above, are cross-sectional views of a partially formed interconnection structure. Ex. 1001, 9:1–4. As noted by Patent Owner, the Specification describes that, after the step shown in Figure 16(c)

> the *patterned organic film 354A is dry-etched using the mask pattern 358 and the patterned second silicon dioxide film 355A having the openings for forming wiring grooves as a mask*, thereby forming the wiring grooves 362.

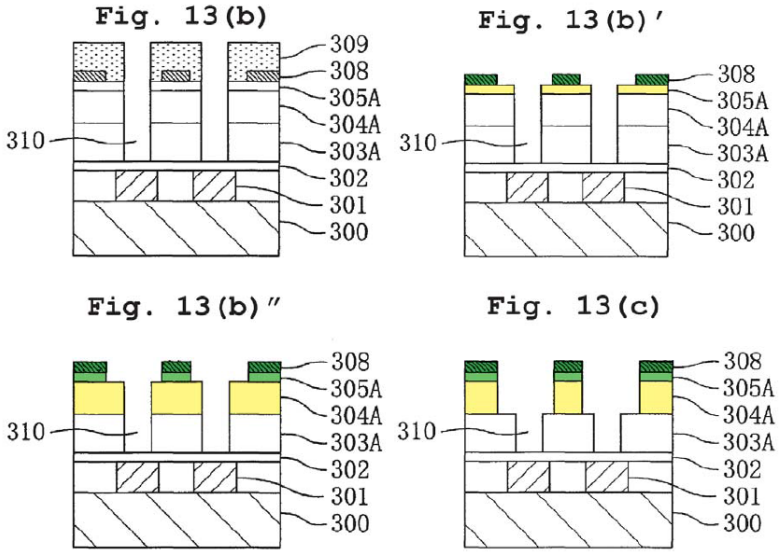
Ex. 1001, 19:50–54 (emphasis added); PO Resp. 11–12. Mapping the modified third embodiment to claim 10,[11] this description corresponds to claim step (l), which recites "dry-etching the patterned third insulating film [354A] . . . using the mask pattern [358] . . . as [a] mask[]." Notably, the claim does not recite using the patterned fourth insulating film (i.e., patterned second silicon dioxide film 355A) as a mask in this recited step. Mapping the modified third embodiment to claim 13, this description corresponds to an unclaimed step between claim steps (j) and (k). Thus, again contrary to Patent Owner's assertion, our application of the construction, on this point, does not exclude the third modified embodiment.[12]

---

[11] We note that for purposes of this discussion, we focus on the portions of the embodiment identified by Patent Owner as being excluded from the claim. By "mapping" this embodiment to the claims, we are not indicating an agreement with respect to Patent Owner's other arguments regarding priority, discussed below—namely that the modified third embodiment provides written description support for step (i) of claim 10.

[12] Claims 1–9 each include steps requiring the presence of both the first resist pattern and second resist pattern in a single step (*see, e.g.*, claim 1, step (h), claim 8, step (h)). Because the modified third embodiment requires removal of the first resist pattern before formation of the second resist pattern (*see* Ex. 1001, 19:30–32), these claims cannot cover this embodiment.

Regarding the third embodiment, Patent Owner points to Figures 13(b) and 13(c) of the ’696 patent, and provides annotated versions (including intermediate steps not depicted in the ’696 patent), reproduced below (PO Resp. 13).



Figures 13(b), 13(b)’, 13(b)’’, and 13(c), above, are cross-sectional views of a partially formed interconnection structure. Ex. 1001, 8:58–60. As noted by Patent Owner, the Specification describes that, after the step shown in Figure 13(b)

> the *patterned low-dielectric-constant SOG film 304A is dry-etched using the mask pattern 308 and the patterned second organic-containing silicon dioxide film 305A having the openings for wiring grooves as a mask*, thereby forming the wiring grooves 311.

Ex. 1001, 17:34–40 (emphasis added); PO Resp. 12–13. Mapping the third embodiment to claim 10, this description corresponds to claim step (l), which recites “dry-etching the patterned third insulating film [304A] . . . using the mask pattern [308] . . . as [a] mask[].” Notably, the claim does not recite using the patterned fourth insulating film (i.e., patterned second silicon

dioxide film 305A) as a mask in this recited step. Mapping the third embodiment to claim 13, this description corresponds to an unclaimed step between claim steps (j) and (k). Thus, again contrary to Patent Owner's assertion, our application of the construction, on this point, does not exclude the third embodiment.[13]

Finally, we note that our determination in the Institution Decision that a layer that is shown in the drawings as "in line and flush with an edge of" an overlying layer does not necessarily act as a mask (*see* Inst. Dec. 17–18) is not inconsistent with the disclosure in the '696 patent. For example, with respect to Figures 16(c) and 16(d) of the modified third embodiment, the '696 patent *expressly states* that both layers identified by Patent Owner (i.e., layers 355A and 358) are used as a mask. *See* Ex. 1001, 19:50–54. Thus, the teaching in the '696 patent that layer 355A is used as a mask, in addition to layer 358, in etching layer 354A is not determined from the teachings of Figures 16(c) and 16(d) alone. *See* Tr. 30:23–31:3 (Patent Owner's counsel noting that "the '696 specification expressly says 509 is a mask. It *doesn't depict how* 509 is a mask, but we know . . . that there are three-dimensional aspects of some of these objects . . . ." (emphasis added)). Similarly, throughout the Specification, whether or not a particular layer is used as a mask is not determined from the figures alone. Instead, in some instances, the Specification indicates *in the text* that certain between layers

[13] Claims 1–9 each include steps requiring the presence of both the first resist pattern and second resist pattern in a single step (*see, e.g.*, claim 1, step (h), claim 8, step (h)). Because the third embodiment requires removal of the first resist pattern before formation of the second resist pattern (*see* Ex. 1001, 17:17–18), these claims cannot cover this embodiment.

are used as a mask, whereas in other instances, it does not.[14] The Specification of the '696 patent does not include any express definition of a "mask" that is inconsistent with our application of the claim construction.

Whether the "additional negative limitation is impermissibly narrower than the Phillips *Standard" (PO Resp. 14)*

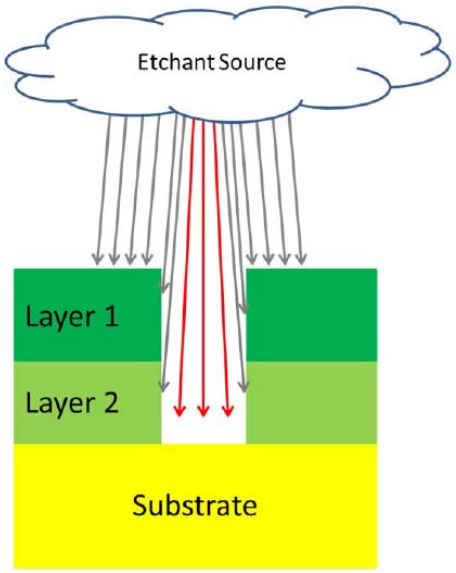
Patent Owner argues that the "[broadest reasonable interpretation] 'cannot be narrower' than the construction under *Phillips*." PO Resp. 14 (citing *Facebook v. Pragmatus AV*, 582 F. App'x 864, 868–69 (Fed. Cir. 2014) (nonprecedential)). However, our construction is, in fact, identical to

[14] Patent Owner also points, for example, to the description of Figures 6(a) to 6(b) as allegedly inconsistent with our application of the construction, arguing that layer 104A is identified in the Specification as a mask, and it is "flush with the sidewall on the right" in Figures 6(a) and 6(b). *See* Tr. 38:10–40:6. Patent Owner contends further that the Specification does not identify top layer 108 as a mask. *Id.* For the etch illustrated in these figures, the Specification describes that patterned organic-containing silicon dioxide film 104A has the openings for the contact holes (Ex. 1001, 13:25–27), and mask pattern 108 has the openings for the wiring grooves (*id.* at 12:66–13:4). The etch of silicon nitride film 102, depicted in Figures 6(a) and 6(b), forms the contact holes in that layer. *Id.* at 13:37–41. The description in the Specification that patterned organic-containing silicon dioxide film 104A is used as a mask for this etch is consistent with our application of the construction—in other words, layer 104A is expressly described as defining areas for etching (to create the contact holes). This is yet another instance in which the Specification expressly describes a between layer (i.e., layer 104A) as a mask; the discussion does not, however, preclude layer 108 from also acting as a mask. *See also* Tr. 65:25–66:21 (Petitioner's counsel discussing the "context" of the description in the Specification). We also note that this discussion relates to "problems caused by the misalignment of the second resist pattern 109 with the first resist pattern 107." Ex. 1001, 12:44–46. In the non-misaligned embodiment (*see id.* at Figs. 2(c), 3(a)), layer 104A is not a flush middle layer during the etch of layer 102A.

that of the district court. *Compare* Ex. 3002, 22 (construing "using the [first resist pattern/second resist pattern and the mask pattern/patterned third insulating film] as a mask" to mean "using the [first resist pattern/second resist pattern and the mask pattern/patterned third insulating film] to define areas for etching"), *with* Inst. Dec. 15 (construing "using the [designated layer] as a mask" to mean "using the [designated layer] to define areas for etching"); *see* PO Resp. 14–15. Petitioner notes that the district court never applied the construction, as we must do in this proceeding, and, thus, Patent Owner has no basis to assert the district court would have applied the construction any differently. Reply 9. We agree.

Whether the "additional negative limitation is inconsistent with the plain and ordinary meaning, understanding of a person of ordinary skill in the art[, and Dr. Smith's] prior publication" (PO Resp. 15)

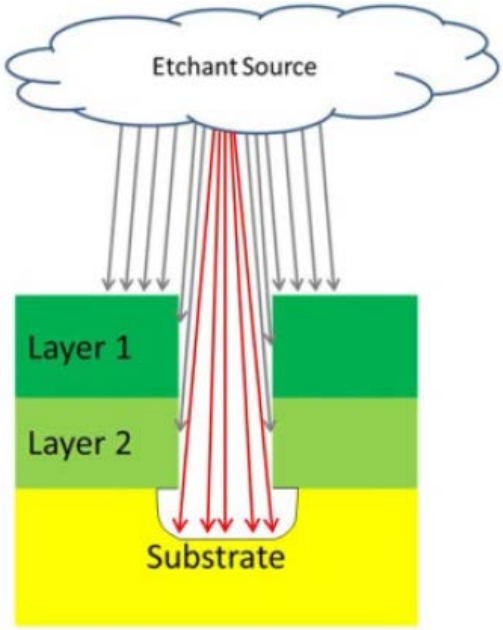
Finally, Patent Owner argues "the Board has taken a narrow view that considers only top surfaces of a layer and excludes sidewalls of a layer from defining areas for etching that is inconsistent with the term's plain and ordinary meaning." PO Resp. 15 (citing Inst. Dec. 15; Ex. 2009 ¶¶ 63–65). Patent Owner provides an illustration of a "multi-layer mask (composed of an intermediate layer having edges in line and flush with edges of a top layer)," reproduced below (*id.* at 15–16).



The figure, above, is an illustration provided by Patent Owner of a "multi-layer mask." *Id.* According to Patent Owner, "although top surfaces of the top layer mask vertical flow of etchant, sidewalls of the top layer and the intermediate layer also mask horizontal flow of etchant, thereby collimating the flow of etchant to define areas of etching a substrate." *Id.* at 16 (citing Ex. 2009 ¶ 66). Patent Owner continues "[m]oreover, it is undisputed that Layer 1's bottom portion bordering the hole is part of the mask, and there is no meaningful difference between the function of the material bordering the hole at the top of Layer 2 from the material bordering the hole at the very bottom of Layer 1." *Id.* (citing Ex. 2009 ¶¶ 67–68); *see also* Tr. 36:15–37:10 (Patent Owner's counsel arguing that, although only two layers are shown in the figure above, any number of flush sidewalls would act as a mask as long as the layer "comes in contact with the etchant, however minute").

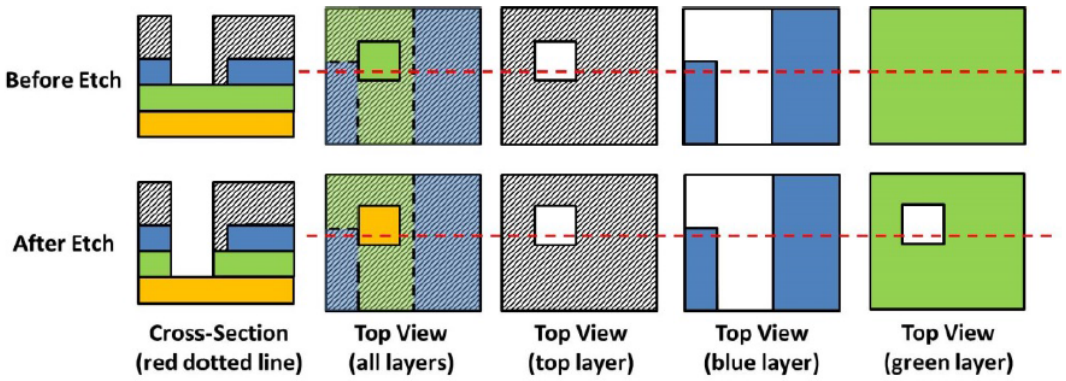
In its Reply, Petitioner argues that the etching process at issue (i.e., reactive ion etching) is "highly directional with negligible lateral deviation."

Reply 4–5 (citing Ex. 1031, 25, 39, 41; Ex. 1032, 56; Ex. 1050 ¶ 11). According to Petitioner, Patent Owner's representation above is inaccurate. Petitioner notes that if non-vertical trajectories were included, the layer being etched would be undercut, as shown in Petitioner's revised representation reproduced below (Reply 5 (citing Ex. 1050 ¶ 12)).



The figure, above, is an illustration provided by Petitioner, showing a revision of Patent Owner's illustration of a "multi-layer mask." *Id.* According to Petitioner, undercutting does not occur during reactive ion etching in practice (*id.* (citing Ex. 1050 ¶ 12)), but instead reactive ion etching "result[s] in directional, anisotropic etching" (*id.* (quoting Ex. 1031, 41)). *See id.* at 5–6 (citing Ex. 1031, 40–41; Ex. 1050 ¶¶ 13–15). Thus, according to Petitioner, Patent Owner's "speculat[ion]" that "a buried layer blocks laterally traveling particles" during etching (*see* PO Resp. 16) is incorrect. Reply 4. According to Petitioner, such a buried layer "has nothing to do with the etch" and does not define an area for etching. *Id.*

Petitioner provides an illustrative example, reproduced below (Reply 4; Ex. 1050 ¶ 29).



The figures above are an illustration of a mask, provided by Petitioner. As shown in these figures, the striped layer contains a via pattern, which is transferred into the green layer by the illustrated etch. *See* Reply 4 (citing Ex. 1050 ¶ 29). The blue layer, which under Patent Owner's argument would comprise a mask in the illustrated etch, contains a wiring pattern, and according to Petitioner "plays no role [in] defining the square-shaped via pattern, which is what a mask does." *Id.* (citing Ex. 1050 ¶ 29). In this example, the shape of the via etched into the green layer is defined by the opening in the striped (top) layer, and is not defined by the blue (buried) layer. Ex. 1050 ¶ 29.

We credit Dr. Smith's testimony regarding the anisotropic characteristics of reactive ion etching, finding it more consistent with the evidence of record. Ex. 1050 ¶¶ 11–15. While we recognize that no anisotropic etch will be perfectly vertical (*see* Tr. 33:6–34:10), Dr. Smith testifies that one of skill in the art would recognize that such an etch is vertical "[w]ithin the capability of measurement or within the requirements of manufacturing." Ex. 2040, 22:6–10; *see also id.* at 22:11–12 (further

noting "the word 'perfectly' [vertical] would have to be defined in that context"); Ex. 1031, 626–27 ("In ion-enhanced etching, both chemical and physical components are acting, but the profiles are not just a linear combination of isotropic chemical etching and anisotropic physical etching . . . . Instead, the profile for ion-enhanced etching is much more like the case for physical etching acting alone . . . . If the chemical component in the etch system is increased, the vertical etching is increased but not the lateral etching, which is not what would be expected from chemical etching. . . . Whatever the exact mechanism for ion-enhanced etching, . . . directional enhancement will result in directional, anisotropic etching."); Reply 4–5. Further, Dr. Glew's testimony as to how a person of ordinary skill in the art would have read the claim language is not supported by evidence of record. *See* Ex. 2009 ¶¶ 63–68 (citing only the '696 patent and the generic dictionary definition of "mask" (Ex. 3001) referenced in the Institution Decision); 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

Patent Owner also points to a prior publication of Dr. Smith discussing a "trilayer resist" that is allegedly inconsistent with his testimony in this proceeding. *See* PO Resp. 17 (citing, e.g., Ex. 2018, 642–43, 657). We find Petitioner's explanation of the "tri-layer resist process" more accurately reflects the understanding of one of skill in the art. Petitioner cites to several contemporary references in explaining that a "tri-layer resist process . . . begins with an intermediate hard mask layer (e.g., SiO2) sandwiched between a top photoresist layer and a bottom planarization/primary layer. The top resist layer is the mask for patterning

the intermediate layer, and afterward, the intermediate layer acts as the mask for etching the bottom layer. The intermediate layer is not a mask because of its sidewalls; it becomes a mask after eliminating the top resist layer . . . ." Reply 6–7 (internal citations omitted) (citing Ex. 1032, 41–42, 70, Fig. 17; Ex. 1033, 14, Fig. 11; Ex. 1034, Abstract, 2:28–35, 3:20–41; Ex. 1045, 4–6; Ex. 1046, 3; Ex. 1047, 2–3; Ex. 2010, 60:22–63:2; Ex. 2015, 8; Ex. 1050 ¶ 18); *see also* Ex. 1050 ¶¶ 16–19. We are not persuaded Dr. Smith's prior publication is inconsistent with his testimony on this point in this proceeding or with our application of the claim construction.

3. Conclusion as to Claim Construction

For all of the reasons set forth herein and in the Institution Decision, we construe "using the [designated layer] as a mask" to mean "using the [designated layer] to define areas for etching," and are not persuaded that a layer, depicted as being positioned between an overlying layer and the layer being etched and having an edge in line and flush with an edge of the overlying layer, is used as a mask within the meaning of claim 10, absent textual discussion describing the layer as such.

D. Whether Grill Qualifies as Prior Art

Each of the asserted grounds relies, at least in part, on Grill. *See* Pet. 42–82. Patent Owner argues that "Grill is not prior art." *See* PO Resp. 18–50. We, thus, at the outset determine the prior art status of Grill as to claims 10–12 of the '696 patent.

The application that issued as the '696 patent was filed on March 23, 1999. Ex. 1001, at [22]. The '696 patent claims priority to Japanese

Application No. 10-079371, filed on March 26, 1998 ("the Japanese priority application"[15]). *Id.* at [30].

Grill was filed on July 30, 1998 and issued on October 31, 2000. Ex. 1005, at [22], [45]. Grill also claims priority to U.S. Provisional Application No. 60/071,628, filed January 16, 1998 ("Grill provisional application"). *Id.* at [60].

Petitioner asserts that "[d]ue to its filing date, *Grill* is prior art to the '696 patent under [35 U.S.C.] § 102(e)" (Pet. 31), because as Petitioner argues, the challenged claims are not entitled to the filing date of the Japanese priority application. *Id.* at 22–30. Petitioner additionally asserts that "*Grill* is prior art . . . under §102(e) even if the challenged claims were entitled" to the filing date of the Japanese priority application, because Grill itself is entitled to the earlier filing date of the Grill provisional application. *Id.* at 31.

Patent Owner argues that claims 10 and 11 are entitled to the '696 patent's claimed priority date of March 26, 1998 (PO Resp. 20–34), and that Petitioner has not shown that Grill is entitled to the priority date of the Grill provisional application (*id.* at 34–50).

1. The '696 Patent's Claim to the Japanese Priority Application

"Under [35 U.S.C.] section 119, the claims set forth in a United States application are entitled to the benefit of a foreign priority date if the corresponding foreign application supports the claims in the manner required by section 112, ¶ 1." *In re Gosteli*, 872 F.2d 1008, 1010 (Fed. Cir. 1989); *see also K & K Jump Start/Chargers, Inc. v. Schumacher Elec. Corp.*,

[15] Petitioner provided a certified translation of the Japanese priority application. Ex. 1014.

13 F. App'x 982, 983 (Fed. Cir. 2001) (nonprecedential) ("The later filed [U.S.] patent . . . is entitled to the filing date of the earlier filed [foreign] patent . . . if the earlier filed patent meets the written description test of 35 U.S.C. § 112, first paragraph.").

Petitioner points to several features of independent claim 10 that it contends are not supported in the Japanese priority application. Pet. 23–30. In particular, Petitioner asserts that the embodiments described in the Japanese priority application do not disclose steps (h), (i), (j), or (l) of claim 10. *See id.* Patent Owner argues that the variant of the third embodiment described in the Japanese priority application fully supports claims 10 and 11 under 35 U.S.C. § 112, first paragraph. PO Resp. 20–34. In our Institution Decision, we preliminarily determined that the variant of the third embodiment described in the Japanese priority application did not provide sufficient support for step (i) of claim 10. *See* Inst. Dec. 22–25. The parties' dispute focuses on this limitation. Thus, we focus our discussion on step (i) of claim 10.

Claim 10, step (i)

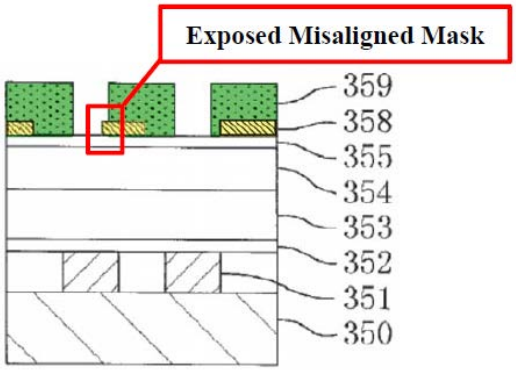
Claim 10, step (i) recites "dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes."

Petitioner argues that the third, variant of the third, and fourth embodiments of the Japanese priority application do not disclose step (i) of claim 10. Pet. 25–26. Because Patent Owner's arguments focus on the variant of the third embodiment, we limit our discussion to this embodiment.

Patent Owner's argument that this claim step is disclosed in the Japanese priority application is as follows:

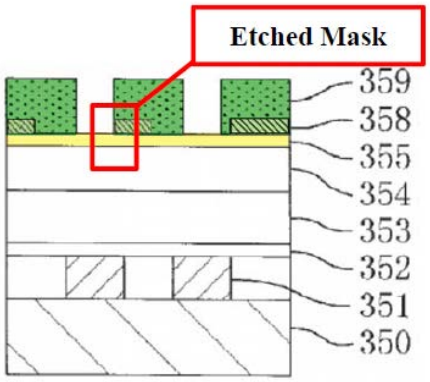
> For example, [the Japanese priority application] discloses that the second resist pattern 359 may be misaligned during fabrication. To address this misalignment, [the Japanese priority application] describes etching the underlying mask pattern 358 "using the second resist pattern 359 as a mask." As a result, edges of the second resist pattern 359 become ***in line and flush with*** the edges of the mask pattern 358. Accordingly, when the underlying fourth insulating film is subsequently patterned, both the second resist pattern and the mask pattern together define areas for the patterning and are both "used . . . as a mask," as recited in claim 10.

PO Resp. 25 (internal citations omitted) (citing Ex. 1014 ¶¶ 93, 96; Ex. 2009 ¶ 89). Patent Owner provides a series of illustrations to support this point. *Id.* at 25–27. First, Patent Owner includes a modified version of Figure 16(a) of the Japanese priority application, reproduced below (*id.* at 26 (citing Ex. 1014 ¶ 96; Ex. 2009 ¶ 90)).



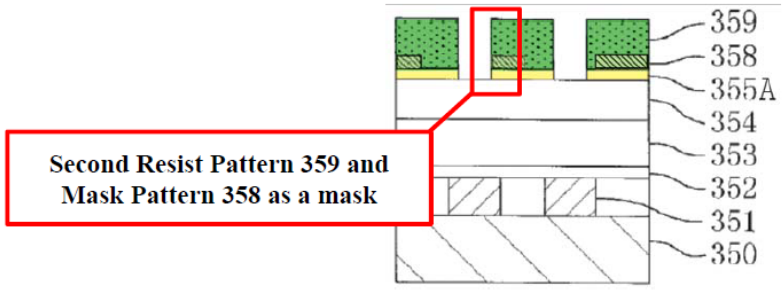
According to Patent Owner, the above figure illustrates Figure 16(a) in the case where "the mask pattern 358 is exposed to the openings of the second resist pattern 359 for the formation of contact holes because of the misalignment." *Id.* at 25 (citing Ex. 1014 ¶ 96; Ex. 2009 ¶ 90). Patent

Owner then provides another modified version of Figure 16(a) of the Japanese priority application, reproduced below (*id.* at 26 (citing Ex. 1014 ¶ 96; Ex. 2009 ¶ 91)).



According to Patent Owner, the above figure illustrates Figure 16(a) "[a]fter 'the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask,' [such that] edges of mask pattern 358 are ***in line and flush with*** edges of second resist pattern 359." *Id.* (citing Ex. 1014 ¶ 96; Ex. 2009 ¶ 91).

Patent Owner further includes another modified version of Figure 16(a) of the Japanese priority application, reproduced below (*id.* at 27 (citing Ex. 1014 ¶¶ 93, 96; Ex. 2009 ¶ 92)).



According to Patent Owner, the above figure illustrates Figure 16(a) after "[e]tching of the 'fourth insulating film [355]' is . . . done 'using the second resist pattern [359] and the mask pattern [358] as a mask,' using the edges

that are in line and flush." *Id.* at 26 (citing Ex. 1014 ¶¶ 93, 96; Ex. 2009 ¶ 92).

Patent Owner's arguments in this regard are premised on its assertion that "using the [designated layer] as a mask" encompasses a situation in which the modified mask pattern 358, having "edges that are in line and flush" with second resist pattern 359, is therefore used as a mask. For the reasons discussed above, we do not agree with Patent Owner that "us[ed] . . . as a mask" necessarily encompasses such a situation. *See supra* Section II.C.2.

We note that the application of our construction would not *preclude* layer 358 as shown in Patent Owner's modified Figure 16(a) from ever being a mask when etching layer 355, if it were in fact *described* as such. However, there is no such description in the Japanese priority application; instead, the corresponding discussion identifies *only* second resist pattern 359 as a mask for this etching step. *See* Ex. 1014 ¶ 96 ("If there is a concern that the second resist pattern 359 has been misaligned with the first resist pattern 357, then the mask pattern 358 should be dry-etched using the second resist pattern 359 as a mask before the second silicon dioxide film 355 is dry-etched *using the second resist pattern 359 as a mask*." (emphasis added)). Further, as noted by Petitioner (Reply 10–11), the corresponding discussion is, at best, ambiguous as to whether mask pattern 358 is "used as a mask" for etching layer 355. Ex. 1014 ¶ 96 ("That is to say, if the mask pattern 358 is exposed to the openings of the second resist pattern 359 for the formation of contact holes because of the misalignment of the second resist pattern 359 with the first resist pattern 357, then the mask pattern 358 is dry-etched using the second resist pattern 359 as a mask. In this manner,

the openings of the mask pattern 358 are expanded to include the openings for the formation of wiring grooves and contact holes." (emphasis added)). This disclosure is not sufficient to provide support under 35 U.S.C. § 112, first paragraph, for step (i) of claim 10. *See Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998) ("For a claim in a later-filed application to be entitled to the filing date of an earlier application under 35 U.S.C. § 120 (1994), the earlier application must comply with the written description requirement of 35 U.S.C. § 112, ¶ 1 (1994). . . . A disclosure in a parent application that merely renders the later-claimed invention obvious is not sufficient to meet the written description requirement; the disclosure must describe the claimed invention with all its limitations." (citing *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1571–72 (Fed. Cir. 1997))); *see also K & K Jump Start*, 13 F. App'x at 984 ("In order for claim 1 of the [U.S.] patent to be entitled to the priority date of the [foreign] application, the test set forth in [*Tronzo*, 156 F.3d at 1158] must be satisfied.").

2. Conclusion as to Whether Grill Qualifies as Prior Art

Having considered the evidence in this record, we determine that, at least, step (i) of claim 10 is not supported by the Japanese priority application.[16] Accordingly, the effective filing date of the challenged claims is March 23, 1999, and Grill is available as prior art as to claims 10–12 of the '696 patent under 35 U.S.C. § 102(e).

[16] Because we find that claim 10 is not supported by the Japanese priority application, we need not discuss the parties' arguments and evidence regarding whether or not Grill is entitled to the priority date of the Grill provisional application. Nor must we decide whether Petitioner's corresponding arguments and evidence submitted in the Reply are proper.

E. Obviousness in View of Grill and Aoyama

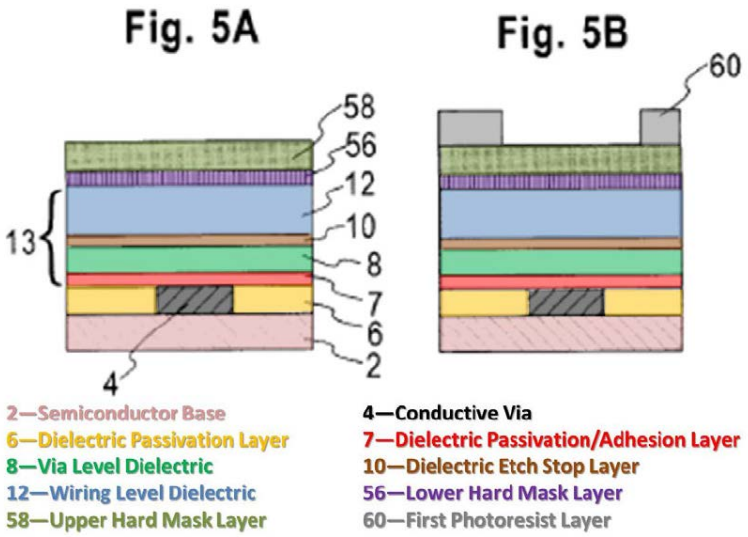
Petitioner asserts that claims 10–12 are unpatentable under 35 U.S.C. § 103 as obvious in view of the combination of Grill and Aoyama. Pet. 59–77. Patent Owner argues that one of ordinary skill in the art would not have combined the references in the manner asserted by Petitioner. PO Resp. 50–77. For the reasons explained below, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 10–12 would have been obvious in view of Grill and Aoyama.

1. Scope and Content of the Prior Art

Overview of Grill

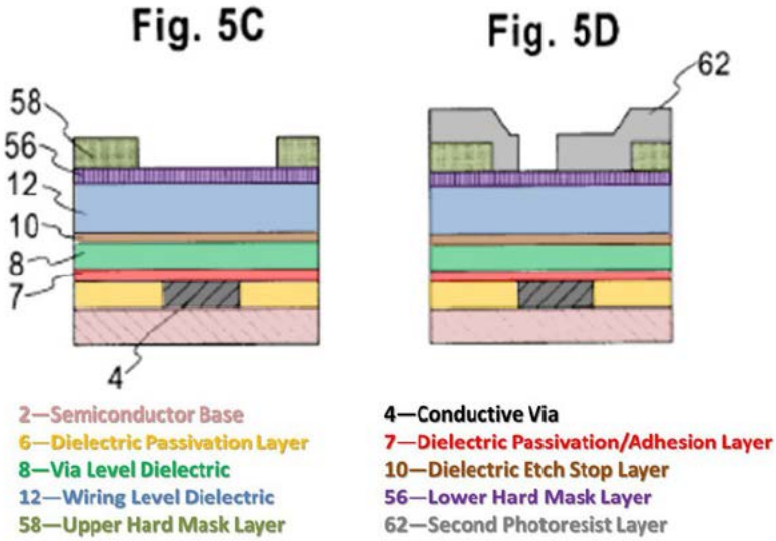
Grill relates to "lithographic methods for forming a dual relief pattern in a substrate, and the application of such methods to fabricating multilevel interconnect structures in semiconductor chips by a Dual Damascene process." Ex. 1005, at [57].

Grill describes various embodiments; one exemplary embodiment is depicted in Figures 5A–5H and 1J–1L. Petitioner provides annotated and colored versions of Figures 5A and 5B of Grill (Pet. 33), reproduced below.



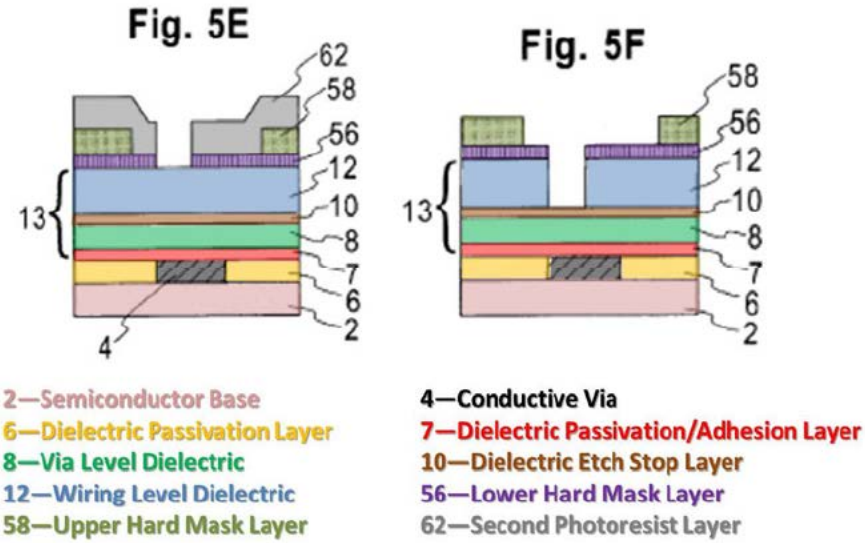
Petitioner's annotated versions of Figures 5A and 5B of Grill, reproduced above, show cross-sectional views of partially formed structures during process steps in the method of an embodiment of Grill. Ex. 1005, 3:45–47. The structure of Figure 5A is formed, and then first photoresist layer 60 is formed and patterned, as shown in Figure 5B. *Id.* at 7:30–44.

Petitioner provides annotated and colored versions of Figures 5C and 5D of Grill (Pet. 33), which illustrate subsequent steps in the method of this embodiment and are reproduced below.



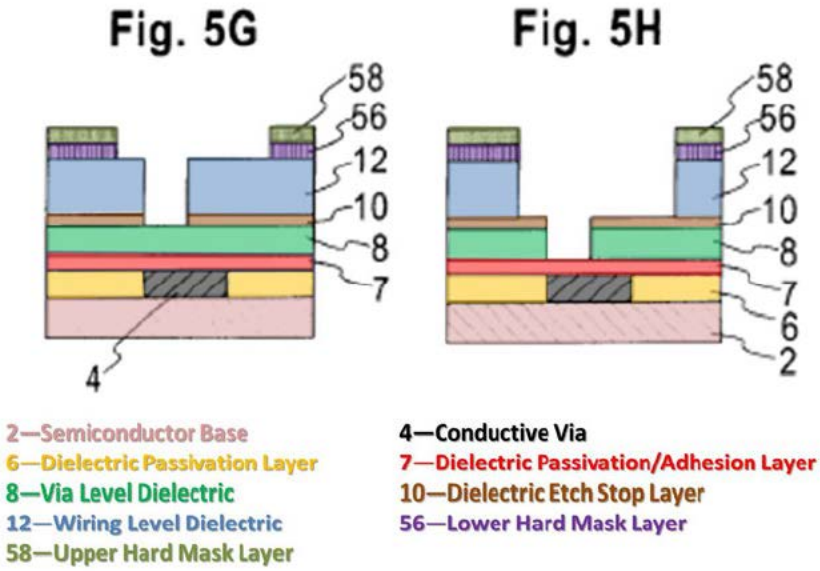
Petitioner's annotated versions of Figures 5C and 5D of Grill, reproduced above, show cross-sectional views of partially formed structures during process steps in the method of an embodiment of Grill. Ex. 1005, 3:45–47. The pattern of photoresist pattern 60 is transferred into upper hard mask layer 58, as shown in Figure 5C. *Id.* at 7:45–50. Pattern 60 is removed and second photoresist layer 62 is formed and patterned, as shown in Figure 5D. *Id.* at 7:51–55.

Petitioner provides annotated and colored versions of Figures 5E and 5F of Grill (Pet. 34), which illustrate subsequent steps in the method of this embodiment and are reproduced below.



Petitioner's annotated versions of Figures 5E and 5F of Grill, reproduced above, show cross-sectional views of partially formed structures during process steps in the method of an embodiment of Grill. Ex. 1005, 3:45–47. The pattern of photoresist pattern 62 is transferred into lower hard mask layer 56, as shown in Figure 5E. *Id.* at 7:57–61. The pattern is further transferred to wiring level dielectric layer 12, by an etch that also removes second photoresist layer 62, as shown in Figure 5F. *Id.* at 7:62–66.

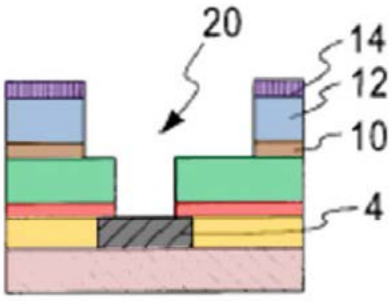
Petitioner provides annotated and colored versions of Figures 5G and 5H of Grill (Pet. 35), which illustrate subsequent steps in the method of this embodiment and are reproduced below.



Petitioner's annotated versions of Figures 5G and 5H of Grill, reproduced above, show cross-sectional views of partially formed structures during process steps in the method of an embodiment of Grill. Ex. 1005, 3:45–47. Exposed portions of lower hard mask layer 56 and etch stop layer 10 are removed by etching, as shown in Figure 5G. *Id.* at 7:67–8:2. A further etch removes exposed portions of dielectric layers 8 and 12, as shown in Figure 5H. *Id.* at 8:2–5.

As noted in Grill, after completion of the step shown in Figure 5H, the structure may be completed as shown in Figures 1J through 1L. *See id.* at 8:5–8. A final etch removes the exposed portions of optional dielectric layer 7, which also removes the exposed portions of etch stop 10, as shown in Figure 1J, an annotated and colored version of which is reproduced below (Pet. 35). Ex. 1005, 4:61–64, 8:5–8; Ex. 1002 ¶ 148.

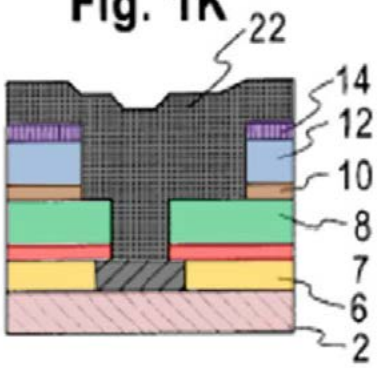
Fig. 1J



2—Semiconductor Base
6—Dielectric Passivation Layer
8—Via Level Dielectric
12—Wiring Level Dielectric
58—Upper Hard Mask Layer
4—Conductive Via
7—Dielectric Passivation/Adhesion Layer
10—Dielectric Etch Stop Layer
56—Lower Hard Mask Layer

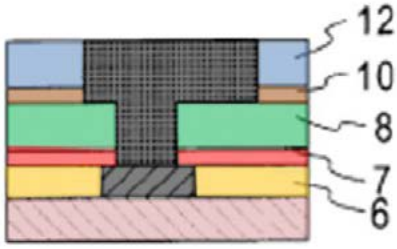
Petitioner's annotated version of Figure 1J, reproduced above, shows a cross-sectional view of a partially formed structure during one step in a dual damascene process flow. Ex. 1005, 3:33–36. Petitioner provides annotated and colored versions of Figures 1K and 1L of Grill (Pet. 36), which illustrate subsequent steps in the method of this embodiment and are reproduced below.

Fig. 1K



2—Semiconductor Base
6—Dielectric Passivation Layer
8—Via Level Dielectric
12—Wiring Level Dielectric
22—Wiring Level

Fig. 1L

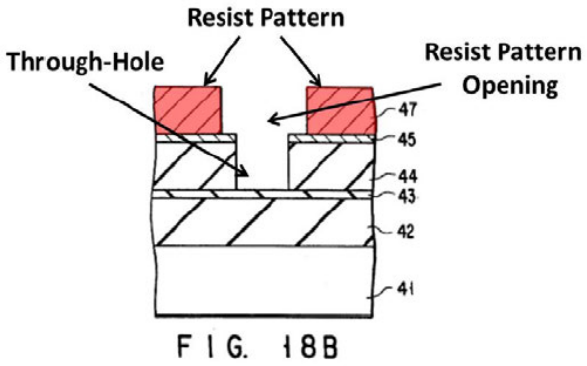


4—Conductive Via
7—Dielectric Passivation/Adhesion Layer
10—Dielectric Etch Stop Layer
14/56—Hard Mask Layer

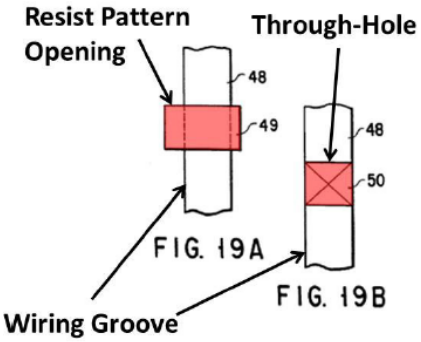
Petitioner's annotated versions of Figures 1K and 1L, reproduced above, show cross-sectional views of partially formed structures during process steps in a dual damascene process flow. Ex. 1005, 3:33–36. As seen in Figure 1K, cavity 20 (Fig. 1J) is filled with conductive material 22, which is then planarized by a chemical-mechanical polishing process, as shown in Figure 1L. *Id.* at 4:64–5:8, 8:5–8.

Overview of Aoyama

Aoyama teaches a dual damascene process in which the opening in a via resist pattern is wider than the wiring groove. Ex. 1018, 15:48–51, 16:3–5, Figs. 18A–18C, 19A–19B. Petitioner's annotated versions of Figures 18B, 19A, and 19B of Aoyama (Pet. 38) are reproduced below.



Side View



Top View

Figure 18B is a cross-sectional view of an intermediate structure formed at a process step for forming a through-hole according to an embodiment of Aoyama. Ex. 1018, 8:42–45. Figures 19A and 19B are plan views of the embodiment of Figure 18B. *Id.* at 8:46–48. As is highlighted in Petitioner's annotated figures, opening 49 in resist pattern 47 for forming through-hole 50 is wider than the wiring groove 48. *Id.* at 16:3–8, Figs. 18B, 19A.

According to Aoyama, this allows the through-hole to be formed having the same width as the wiring groove, even if resist pattern 47 is misaligned. *Id.* at 16:14–16, Fig. 19B.

2. Whether the Grill/Aoyama Combination Teaches all Limitations of the Challenged Claims

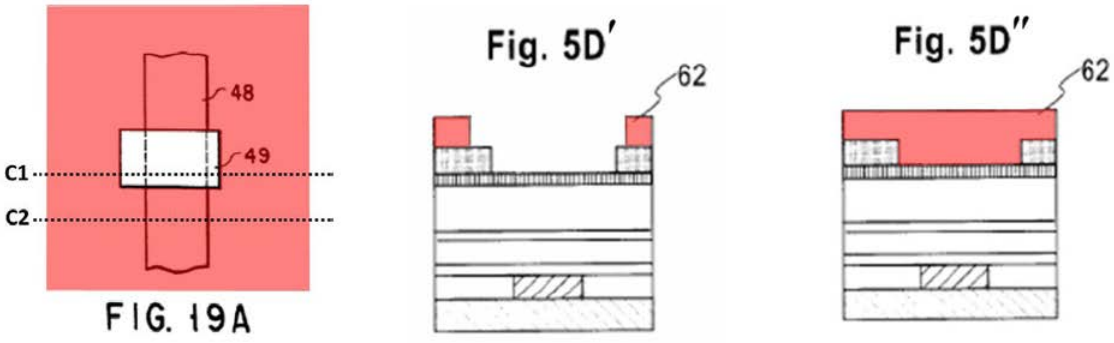
Claim 10 recites a "method for forming an interconnection structure." Grill is titled "Dual Damascene Processing for Semiconductor Chip Interconnects," and discloses "methods to fabricat[e] multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels." Pet. 43 (citing Ex. 1005, at [54], [57]); *id.* at 60. The following table provides a basic summary of Petitioner's mapping of the combination of Grill and Aoyama to the physical elements of claim 10.

Claim 10	**Grill & Aoyama**
lower-level interconnects	conductive via 4 of Grill
first insulating film	via dielectric 8 of Grill
second insulating film	dielectric etch stop layer 10 of Grill
third insulating film	wiring level dielectric 12 of Grill
fourth insulating film	lower hard mask layer 56 of Grill
thin film	upper hard mask layer 58 of Grill
mask pattern	patterned upper hard layer 58 of Grill
first resist pattern	patterned first resist layer 60 of Grill
second resist pattern	patterned second resist layer 62 of Grill, as modified by Aoyama's teachings

Claim 10	Grill & Aoyama
contact holes	cavity 20 of Grill (holes in etch stop 10 and via level dielectric 8), as modified by Aoyama's teachings
wiring grooves	cavity 20 of Grill (holes in lower hard mask 56 and wiring level dielectric 12), as modified by Aoyama's teachings
upper-level metal interconnects	conductive wiring material 22 of Grill
contacts	conductive wiring material 22 of Grill

See Pet. 43–50, 52–53, 60–73 (citing Ex. 1005, 1:25–27, 3:60–4:13, 4:64–5:8, 7:30–55, 7:57–8:5, 8:29–31, Figs. 1K, 1L, 5A–5H; Ex. 1018, 16:18–21, Fig. 19A; Ex. 1002 ¶¶ 195–219, 225–26, 250–55, 257–83, 286–87). Petitioner cites to evidence in the record that the combination of Grill and Aoyama teaches each of the method steps recited in claim 10. *See id.*

Further, Petitioner describes exactly how a person of ordinary skill in the art would have modified Grill based on the teachings of Aoyama. *See* Pet. 62–73. Petitioner's annotated version of Figure 19A of Aoyama and modified and annotated versions of Figure 5D of Grill (*id.* at 63) are reproduced below.



Petitioner's annotated version of Figure 19A of Aoyama, reproduced above, shows the shape of Aoyama's through-hole, viewed from above. *Id.* Petitioner's annotated and modified versions of Figure 5D of Grill, reproduced above, are cross-sectional views of a partially formed interconnection structure at a step in a method of forming the same, according to one embodiment of Grill, as modified by Aoyama, along line C1 of Figure 19A (Fig. 5D') and along line C2 of Figure 19A (Fig. 5D''). *Id.* (citing Ex. 1002 ¶ 259).

In Petitioner's proposed modification, second resist layer 62 of Grill is modified to have a through-hole shaped as taught by Aoyama. *Id.* (citing Ex. 1002 ¶¶ 258–59; Ex. 1018, 16:18–21). According to Petitioner, when lower hard mask layer 56 of Grill is etched, in the Grill-Aoyama combination, a person of ordinary skill would have understood that second resist pattern 62 and mask pattern 58 are used as masks, thus meeting the limitations recited in step (i) of claim 10. *Id.* at 65 (citing Ex. 1002 ¶¶ 264–65). As illustration, Petitioner provides an annotated version of Figure 19A of Aoyama and modified and annotated versions of Figure 5E of Grill (*id.*), which are reproduced below.

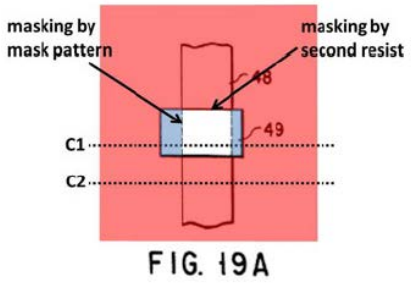
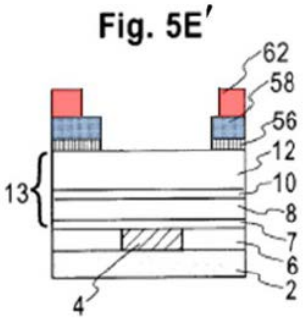
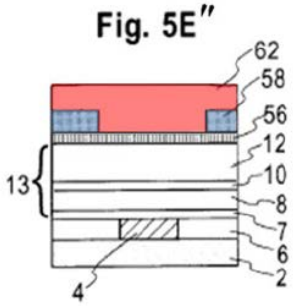


FIG. 19A





Petitioner's annotated version of Figure 19A of Aoyama, reproduced above, shows the shape of Aoyama's through-hole, viewed from above, with red

areas indicating photoresist (i.e., second resist pattern 62) and blue areas indicating a layer corresponding to mask pattern 58 of Grill. Pet. 65. Petitioner's modified and annotated versions of Figure 5E of Grill, reproduced above, are cross-sectional views of a partially formed interconnection structure at a step in a method of forming the same, according to one embodiment of Grill, as modified by Aoyama, along line C1 of Figure 19A (Fig. 5E') and along line C2 of Figure 19A (Fig. 5E''). *Id.* (citing Ex. 1002 ¶ 265).

Patent Owner does not present arguments regarding any of the individual claim elements or steps. *See generally* PO Resp. Based on the evidence presented, we find that Petitioner's proposed combination of Grill and Aoyama teaches using both patterned second resist layer 62 of Grill as modified by the teachings of Aoyama (i.e., the claimed second resist pattern) and patterned upper hard layer 58 (i.e., the claimed mask pattern) as a mask for etching lower hard mask layer 56 (i.e., the claimed fourth insulating film), as required by claim 10, step (i). We also find that Petitioner has shown sufficiently that all of the other recited method steps of claim 10 are taught by the combination of Grill and Aoyama. *See* Pet. 43–50, 52–53, 60–73. We address in more detail, below, Petitioner's reasons for combining the references, and Patent Owner's arguments presented in the Patent Owner Response.

Claim 11 depends from claim 10 and further recites that "at least one of the first and third insulating films is mainly composed of an organic component." Ex. 1001, 34:50–52. Petitioner relies on Grill as disclosing this limitation. *See* Pet. 59, 73–74. In particular, Petitioner asserts that Grill discloses that "dielectrics 8 and 12 [(which Petitioner maps to the claimed

first and third insulating films)] might be carbon-based materials such as . . . organic or inorganic polymer dielectrics." *Id.* at 59 (citing Ex. 1005, 4:1–13; Ex. 1002 ¶¶ 243–47). Claim 12 depends from claim 10 and further recites that "a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend." Ex. 1001, 34:53–57. Petitioner relies on Aoyama as disclosing this limitation. *See* Pet. 76–78. In particular, Petitioner asserts that Aoyama teaches that problems caused by misalignment of the photomask during through-hole (via) formation may be solved by using a resist pattern with a through-hole wider than the wiring groove. *Id.* (citing Ex. 1018, 3:6–38, 6:7–14, 15:48–16:30, Figs. 5B, 5D, 18B, 19A, 19B; Ex. 1002 ¶¶ 294–300). Patent Owner does not substantively discuss dependent claims 11 and 12, apart from its discussion of independent claim 10. We determine that Petitioner has shown that the combination of Grill and Aoyama teaches all limitations of claims 11 and 12, for the reasons stated by Petitioner.

3. Whether a Person of Ordinary Skill in the Art Would Have Had Reason to Combine Grill and Aoyama and Would Have Had a Reasonable Expectation of Success in Doing So

Petitioner asserts a person of ordinary skill would have found it obvious to combine certain teachings of Grill and Aoyama. *See* Pet. 39–42. Patent Owner disagrees. *See* PO Resp. 50–77.

Petitioner's Arguments and Evidence

Petitioner argues that both Grill and Aoyama relate to problems involving misalignment of masks during interconnect formation. *See* Pet. 39–42.

According to Petitioner, Grill addresses the problem of "lithographic rework" required when misalignment between the via pattern and the wiring pattern occurs. *Id.* at 39 (citing Ex. 1005, 2:26–38). Such rework can cause damage to the underlying dielectric. *Id.* (citing Ex. 1005, 2:26–32). Grill addresses this problem using two hard masks on top of the wiring-level dielectric, which allows lithographic alignment for both via and wiring levels to be completed and the patterns transferred before the underlying inter-level dielectrics are exposed. *Id.* at 39–40 (citing Ex. 1005, 2:64–3:6, Fig. 5A).

Further, according to Petitioner, "*Aoyama* explains that misalignment of the photomask during via formation can cause the via dimensions to be too small and the wiring dimensions to be too large," which is undesired. *Id.* at 40 (citing Ex. 1018, 3:18–21, 3:29–38, 6:7–14, Figs. 5B, 5D). Aoyama addresses this problem by using "a resist pattern with a via opening wider than the wiring groove." *Id.* (citing Ex. 1018, 16:3–5, Figs. 18B, 19A). Using this wider resist pattern "increases misalignment tolerance." *Id.* (citing Ex. 1018, 16:14–16).

Petitioner argues that a person of ordinary skill in the art "would have appreciated that *Grill*'s and *Aoyama*'s solutions complement one another." *Id.* at 41 (citing Ex. 1002 ¶ 188). Specifically, Petitioner asserts that "[w]hen misalignment occurs [in a semiconductor damascene process], *Grill*'s structure permits lithographic rework without damaging the underlying dielectrics" (*id.* (citing Ex. 1005, 2:26–38; Ex. 1002 ¶ 188)), while "*Aoyama*'s wider via pattern reduces instances of misalignment, preventing the time-consuming, inefficient, and costly process of photolithographic rework" (*id.* (citing Ex. 1002 ¶ 188)).

Petitioner provides testimony of Dr. Smith that a person of ordinary skill in the art "would have found it obvious that combining *Grill*'s two hard masks with *Aoyama*'s widened via pattern would not require modification of the *Grill* process" (Ex. 1002 ¶ 189) and "would have understood that the combination of *Aoyama* and *Grill* predictably reduces instances of misalignment and permits lithographic rework when misalignment does occur" (Ex. 1002 ¶ 190). *See* Pet. 41–42. Petitioner's explanation as to why a person of ordinary skill in the art would have had reason to combine the teachings of Grill and Aoyama and would have had a reasonable expectation of success are supported by the testimony of Dr. Smith and are persuasive.

Patent Owner's Arguments and Evidence and Our Analysis

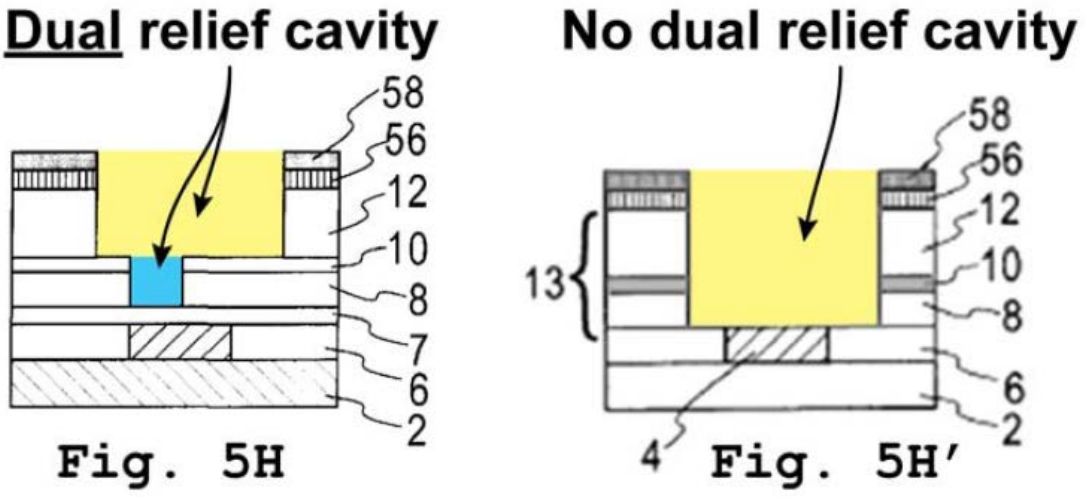
Patent Owner argues that Petitioner has not demonstrated that it would have been obvious to combine Grill and Aoyama. PO Resp. 50–77. Patent Owner makes several arguments in this regard, which we address in turn.

Whether the Modification Renders Grill Unsatisfactory for its Intended Purpose

Patent Owner argues that Petitioner's modification of Grill would render Grill unsatisfactory for its intended purpose. PO Resp. 53–57. According to Patent Owner, "Grill repeatedly emphasizes throughout its specification that its 'present invention' is directed to forming a dual relief pattern and using said dual relief pattern to form a dual relief cavity in a substrate." *Id.* at 53 (citing Ex. 1005, at [57], 1:12–15, 2:41–50, 7:16–19; Ex. 2009 ¶ 148). Patent Owner asserts that the "dual-relief patterns of Grill include a larger wiring pattern over a smaller via pattern that are used to form a dual relief cavity that includes a wiring trench and via hole, respectively." *Id.* at 54 (citing Ex. 1005, 1:48–49, 7:25–29). Patent Owner

further argues that "Grill's dual-relief patterns are intended to enable precise placement of vias within a wire trench's width—not length." *Id.* at 57 n.22 (citing Ex. 1005, 2:64–3:1, 4:34–35, 4:51–52, 5:18–22, 5:24–33, 7:16–29; Ex. 2010, 13:7–14:20, 18:8–20, 19:14–20:7; Ex. 2009 ¶¶ 150–55).

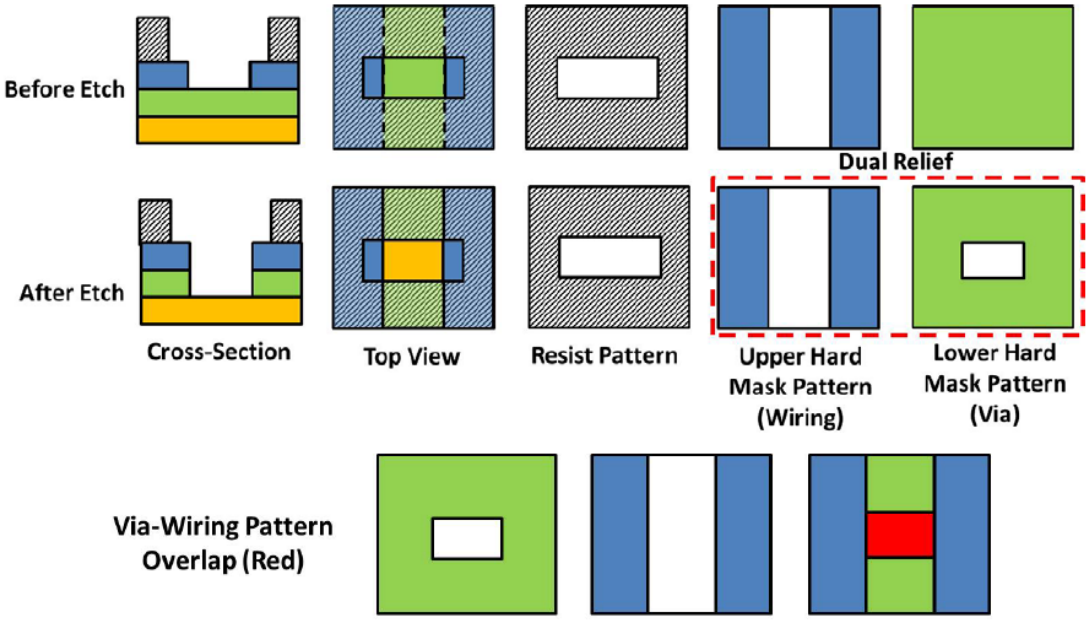
Patent Owner argues that, in Petitioner's proposed modification, the dual-relief pattern of Grill is eliminated. Patent Owner provides an illustration, reproduced below (PO Resp. 56).



The figures above show versions of Figure 5H of Grill, as annotated by Patent Owner. *Id.* Patent Owner asserts that "[t]his elimination of the dual-relief pattern eliminates Grill's ability to control placement of the via over the underlying wire." *Id.* (citing Ex. 2009 ¶ 154).

In its Reply, Petitioner argues that "dual relief pattern," as discussed in Grill, "refers to dual damascene technology: making wiring and via levels in the same processing module." Reply 23 (citing Ex. 1005, at [57]). According to Petitioner, "[n]othing prohibits the wiring and via levels in a dual-relief pattern from having the same width." *Id.* (citing Ex. 1050 ¶¶ 56–

57). By way of explanation, Petitioner provides an illustration, reproduced below (Reply 24; Ex. 1050 ¶ 57).



The figures above show an illustration provided by Petitioner of a dual-relief pattern with wiring and via levels having the same width. Dr. Smith testifies that, in this example, "[t]he dual relief pattern collectively refers to the openings in the blue layer (a wiring pattern) and the green layer (a via pattern)." Ex. 1050 ¶ 57. We agree with Petitioner that this example is consistent with the disclosure in Grill that "all features of a smaller area (via) pattern substantially overlap with the features of a larger area (wiring) pattern" (Ex. 1005, 7:27–29). *See* Reply 24.[17]

[17] To the extent Patent Owner asserts that this argument is "an improper new argument never before presented by Petitioner" (PO Resp. 57 n.22), we determine that Petitioner's discussion properly responds to Patent Owner's arguments that Petitioner's modification would have rendered Grill unsatisfactory for its intended purpose. *See* 37 C.F.R. § 42.23(b) ("A reply may only respond to arguments raised in the corresponding . . . patent owner response."); *Idemitsu Kosan Co., Ltd. v. SFC Co. Ltd.*, 870 F.3d 1376, 1380–

Although the figures of Grill illustrate that, in the preferred embodiments, the dual relief patterns include a via pattern that is more narrow than the wiring pattern, we do not agree with Patent Owner that one of ordinary skill in the art would view the teachings of Grill to be so limited. In fact, Grill expressly states "this combination of via and wiring level patterns should be viewed as a special case of the general category of dual relief patterns." Ex. 1005, 7:27–29; Reply 23; Ex. 1050 ¶¶ 56–57. Petitioner's proposed modification maintains a dual relief pattern, as discussed above, which meets the intended purpose of Grill described by Patent Owner. Accordingly, we are not persuaded that Petitioner's proposed modification would render Grill unsatisfactory for its intended purpose.

Whether the Modification Changes Grill's Principle of Operation

Patent Owner argues that Petitioner's modification of Grill would change Grill's principle of operation. PO Resp. 57–68. Patent Owner asserts that Petitioner's combination "ignore[s] detrimental effects of Aoyama's wider via hole pattern on Grill's dual-mask system that would undermine Grill's principle of operation of critical dimension control." *Id.* at 58 (citing Ex. 2009 ¶ 159). Patent Owner's arguments in this regard are premised on an assertion that, in Petitioner's proposed modification of Grill, Grill's upper hard mask 58 is exposed prematurely to etching steps, which "degrades Grill's upper hard mask 58, causing loss of control over the dimension of the wire trench over the via hole." *Id.* at 58–61; Ex. 2009

81 (Fed. Cir. 2017) (permitting rebuttal argument from a petitioner in response to a patent owner's argument that a reference taught away from a particular combination, as such argument was "simply the by-product of one party necessarily getting the last word").

¶¶ 161–63. Patent Owner argues that, in Petitioner's proposed modification, there are five steps during which hard mask layer 58 "must persist"—namely "(1) etching through layer 56, (2) etching through layer 12, (3) etching through layer 10 and layer 56, (4) etching through layer 8, and (5) etching through layer 7." PO Resp. 59 (citing Ex. 2009 ¶ 161).

We note that, in Grill, hard mask layer 58 already is exposed to the etchant after the step of etching through layer 12. *See* Ex. 1005, Figs. 5E, 5F; *see also id.* at 7:64–66 ("Patterned second resist layer 62 is absent from FIG. 5F because it is typically removed by the etching process used to pattern dielectric 12."). Thus, hard mask layer 58 is "prematurely" exposed to etchant, in Petitioner's proposed combination, only during the steps of (1) etching through lower hard mask layer 56 and (2) etching through dielectric layer 12. Further, contrary to Patent Owner's assertion (PO Resp. 62–63), Grill does not describe "protecting" upper hard mask layer 58 with resist 62 while etching lower hard mask layer 56. Rather, Grill merely discloses the "pattern of resist layer 62 is then transferred into lower hard mask layer 56" (Ex. 1005, 7:57–58), with no mention of "protecting" lower hard mask layer 58. Notably, Grill does use the word "protect" with respect to "lower hard mask layer 56 [being] still in place to *protect* dielectric 12" in the instance that resist layer 62 must be reworked due to misalignment. *See* Ex. 1005, 7:55–58 (emphasis added).

As noted by Petitioner (Reply 25), Grill expressly teaches "[h]ard mask layers 56 and 58 . . . have different etch properties from each other and from the dielectric underlayers 12 and 8." Ex. 1005, 7:31–35. Petitioner argues that "[b]ecause layer 58 has different etch properties from layers 56 and 12, a [person of ordinary skill in the art] would not have been concerned

about 'premature' exposure of layer 58 while etching layers 56 and 12, because layer 58 resists those etches." Reply 25 (citing Ex. 1050 ¶¶ 58–65). For example, according to Dr. Smith, a "person of ordinary skill in the art would have known many processes for selectively etching silicon nitride [(i.e., the specific exemplary material disclosed in Grill for lower hard mask 56)] relative to silicon dioxide [(i.e., the specific exemplary material disclosed in Grill for upper hard mask 58)]." Ex. 1050 ¶ 60; Ex. 1005, 7:35–38.

Having considered the evidence of record, we do not find that Petitioner's proposed combination would have resulted in upper hard mask 58 of Grill being "prematurely degrade[d]" as Patent Owner argues. *See* PO Resp. 58–67. Instead, we find that a person of ordinary skill in the art would have understood from the teachings of Grill that layer 58 of Petitioner's proposed modification would resist the etches used for etching layers 56 and 12. *See* Reply 25 (citing Ex. 1050 ¶¶ 58–65). Thus, we are not persuaded by Patent Owner's argument that Petitioner's proposed modification would change Grill's principle of operation.

Whether Grill Teaches Away from the Combination

Patent Owner argues that Grill teaches away from a combination with Aoyama. PO Resp. 68–77.

First, Patent Owner argues that the "Grill teaches away from the combination with Aoyama because its rework problem would result in damage to Aoyama's carbon-based etch stop layer." *Id.* at 69. According to Patent Owner, "Petitioner improperly ignores that part of Aoyama's misalignment solution is its use of carbon etch stopper film 45." *Id.* Patent Owner's arguments focus on problems that allegedly would occur if the

carbon etch stopper film 45 is removed from Aoyama or is added to Grill. *See id.* at 69–74. This is not the combination proposed by Petitioner, however. Petitioner's position is that one of ordinary skill in the art would have used Aoyama's teaching of using a wider via hole pattern in the process disclosed in Grill, in order to avoid misalignment. *See* Reply 27.

According to Patent Owner, a person of ordinary skill in the art "would have understood that it would not be possible to modify Grill by combining it with Aoyama's wider via hole pattern (and certainly would not have had a reasonable expectation of success) without also including Aoyama's carbon etch stopper film 45." PO Resp. 71 (citing Ex. 2009 ¶ 184). Petitioner, in its Reply, presents evidence that "[v]ia patterns wider than the wiring groove were well-known and did not require carbon etch-stops." Reply 27–28 (citing Ex. 1040, 2:64–3:45, Figs. 1–4; Ex. 1041, 3:39–45, Figs. 5–6; Ex. 1050 ¶¶ 66–68).[18] Further, in Aoyama, carbon etch stopper film 45 acts to prevent etching of second insulating film 44 during formation of through-hole 50, thereby avoiding undesired widening of the wiring groove. Ex. 1018, 16:12–16, Figs. 18B, 18C. As discussed above, we find that a person of ordinary skill in the art would have understood from the teachings of Grill that layer 58 of Petitioner's proposed modification would resist the etches used for etching layers 56 and 12 (*see* Reply 25 (citing Ex. 1050 ¶¶ 58–65)). Thus, in Petitioner's proposed combination,

[18] To the extent Patent Owner asserts that this argument is an improper new argument (Paper 36), we determine that Petitioner's discussion properly responds to Patent Owner's arguments that one of ordinary skill in the art would not have had a reasonable expectation of success of modifying Grill using Aoyama's wider hole pattern. *See* 37 C.F.R. § 42.23(b); *Idemitsu*, 870 F.3d at 1380–81.

hard mask layer 58 of Grill performs the relevant necessary functions of Aoyama's carbon etch stopper film 45. Any problems pointed out by Patent Owner that allegedly are caused due to the removal of carbon etch stopper film 45 in Aoyama or the addition of such a film in Grill are irrelevant.

Second, Patent Owner argues that "Grill warns against layers of resist that are thicker over certain areas, which would be required by Aoyama's approach." PO Resp. 75 (citing Ex. 1005, 5:29–35; Ex. 2009 ¶ 190). However, the discussion in Grill to which Patent Owner cites relates to a problem that Grill describes with respect to the prior art process upon which Grill purports to improve. *See* Ex. 1005, 3:33–39, 5:9–33; Reply 28–29. The embodiment of Grill upon which Petitioner relies in its combination purports to solve the problems described in Figure 2A by the use of hard mask layers 56 and 58. *See* Ex. 1005, 7:16–61 (discussing that resist rework "presents no problem" due to hard mask layers 56 and 58).

Accordingly, we are not persuaded the references teach away from Petitioner's proposed combination.

Conclusion

For the reasons discussed, we determine that Petitioner has shown that a person of ordinary skill in the art would have combined Grill and Aoyama in the manner asserted. In particular, we are persuaded that a person of ordinary skill in the art would have had reason to use the wider via hole pattern disclosed in Aoyama in the dual damascene process disclosed in Grill, with a reasonable expectation of success.

4. Conclusion of Obviousness

Upon consideration of all the evidence, we conclude that Petitioner has demonstrated, by a preponderance of the evidence, that claims 10–12 would have been obvious over Grill and Aoyama.

F. Petitioner's Motion to Exclude

Petitioner moves to exclude Exhibits 2015, 2018, and 2019 as "irrelevant and non-probative" under Federal Rules of Evidence 401, 402, and 403. Pet. Mot. 1–2. Petitioner's Motion to Exclude is dismissed as moot, as we do not rely on any of these exhibits in a manner adverse to Petitioner.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 10–12 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Grill and Aoyama.

IV. ORDER

Accordingly, it is:

ORDERED, based on a preponderance of the evidence, that claims 10–12 of U.S. Patent No. 6,197,696 B1 are *unpatentable*; and

FURTHER ORDERED that Petitioner's Motion to Exclude is *dismissed*.

Because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Darren M. Jiron
E. Robert Yoches
J. Preston Long
Joshua L. Goldberg
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, LLP
darren.jiron@finnegan.com
bob.yoches@finnegan.com
j.preston.long@finnegan.com
joshua.goldberg@finnegan.com

PATENT OWNER:

James L. Davis, Jr.
Andrew N. Thomases
Jordan M. Rossen
ROPES & GRAY LLP
james.l.davis@ropesgray.com
andrew.thomases@ropesgray.com
jordan.rossen@ropesgray.com

J. Steven Baughman
PAUL, WEISS, RIFKIND, WHARTON & GARRISON LLP
sbaughman@paulweiss.com