

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION, GLOBALFOUNDRIES U.S., INC.,
MICRON TECHNOLOGY, INC. and
SAMSUNG ELECTRONICS COMPANY, LTD.¹,
Petitioner,

v.

DANIEL L. FLAMM,
Patent Owner.

Case IPR2017-00281
Patent RE40,264 E

Before CHRISTOPHER L. CRUMBLEY, JO-ANNE M. KOKOSKI, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Samsung Electronics Company, Ltd. was joined as a party to this proceeding via a Motion for Joinder in IPR2017-01750.

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Intel Corporation, GLOBALFOUNDRIES U.S., Inc., Micron Technology, Inc. and Samsung Electronics Company, Ltd., (collectively “Petitioner”) challenge the patentability of claims 37–50 and 67 of U.S. Patent No. RE40,264 (Ex. 1001, “the ’264 patent”), owned by Daniel L. Flamm. (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during trial. For the reasons discussed below, we determine that Petitioner has shown by a preponderance of the evidence that claims 37–50 and 67 of the ’264 patent are unpatentable.

A. Procedural History

On December 2, 2016, Intel Corporation, GLOBALFOUNDRIES U.S., Inc., and Micron Technology, Inc. (collectively, “Initial Petitioners”) filed a Petition requesting an *inter partes* review of claims 37–50 and 67 of the ’264 patent. Paper 2 (“Pet.”). Patent Owner filed a Preliminary Response. Paper 8. On June 13, 2017, we instituted an *inter partes* review of the challenged claims. Paper 10 (“Decision on Institution” or “Dec. on Inst.”) Subsequent to institution, Samsung Electronics Company, Ltd. (“Samsung”) filed a petition and motion for joinder with the instant proceeding. *Samsung Electronics Company, Ltd. v. Daniel L. Flamm*, Case IPR2017-01751, Papers 1, 3. On September 15, 2017, we granted Samsung’s petition and motion for joinder, joining Samsung as a petitioner in this *inter partes* review. Paper 14, 7.

Thereafter, Patent Owner filed a Patent Owner Response (Paper 13, “PO Resp.”) and Petitioner filed a Reply (Paper 15, “Reply”). The Petition is supported by the Declaration of Dr. John Bravman (Ex. 1006, “the Bravman Declaration”) and the Reply is supported by the Reply Declaration of Dr. John Bravman (Ex. 1024, “the Bravman Reply Declaration”). Patent Owner’s Response is supported by the Declaration of Dr. Daniel L. Flamm² (Ex. 2001, “the Flamm Declaration”).

Oral hearing was requested by both parties. Papers 16, 17. A consolidated oral hearing for this proceeding and Cases IPR2017-00279, IPR2017-00280, and IPR2017-000282, involving the same parties and the ’264 patent, and Cases IPR2017-00391, IPR2017-00392, and IPR2017-00406, involving the same parties and unrelated patents, was held on March 7, 2018. A transcript of the consolidated hearing has been entered into the record. Paper 29 (“Tr.”).

B. Related Proceedings

Petitioner reports that the Patent Owner has asserted the ’264 patent in five proceedings in the Northern District of California (Case Nos. 5:16-cv-01578-BLF, 5:16-cv-1579-BLF, 5:16-cv-1580-BLF, 5:16-cv-1581-BLF, and 5:16-cv-02252-BLF) and that Lam Research Corporation has filed a declaratory judgment action against Patent Owner on the ’264 patent, also in the Northern District of California (Case No. 5:15-cv-01277-BLF). Pet. 2.

² Daniel L. Flamm is both the Patent Owner and Patent Owner’s declarant in this proceeding.

Petitioner also challenges certain claims of the '264 patent in IPR2017-00279, IPR2017-00280, and IPR2017-00282, which were filed concurrently with the Petition in this proceeding. The parties also identified nine other IPR petitions for review of the '264 patent, filed by Lam Research Corporation or Samsung, none of which are currently pending. *See* Pet. 2; Prelim. Resp. 1 (identifying IPR2015-01759 (institution denied); IPR2015-01764 (terminated-settled); IPR2015-01766 (institution denied); IPR2015-01768 (terminated-settled); IPR2016-00468 (institution denied); IPR2016-00469 (institution denied); and IPR2016-00470 (institution denied); IPR2016-01510 (institution denied) and; IPR2016-01512 (Final Written Decision – challenged claims unpatentable)).

C. The '264 Patent

The '264 patent, titled “Multi-Temperature Processing,” relates generally to methods and systems for controlling the heating and cooling time of a substrate (e.g., wafer) during plasma processing in a single processing chamber. *See, e.g.*, Ex. 1001, 1:18–21. A “plasma etching apparatus according to the present invention” is shown in Figure 1 of the '264 patent, reproduced below. *Id.* at 2:66–67.

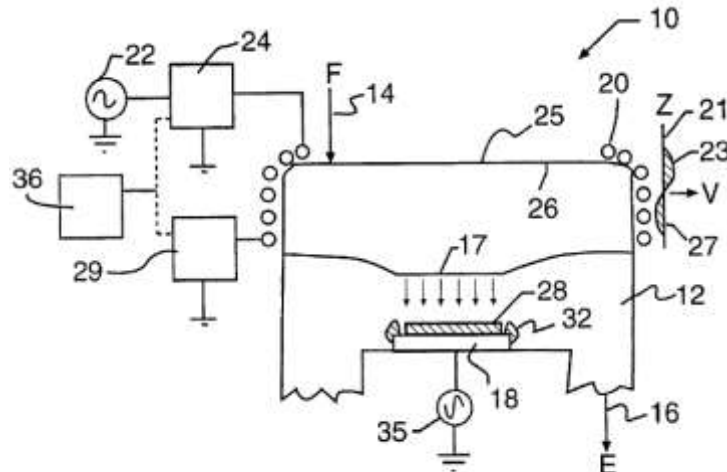


FIG. 1

Figure 1 above illustrates a plasma etching apparatus having chamber 12 and a substrate holder (product support chuck or pedestal 18) for holding a substrate (product 28, such as a wafer to be etched). *Id.* at 3:24–25, 3:32–33, 3:40–42. The substrate holder, which is thermally coupled to the substrate, “can rapidly change its temperature.” *Id.* at 3:51–55.

One embodiment of a temperature control system according to the invention is shown in Figure 7 below. *Id.* at 3:11–13, 15:65–67.

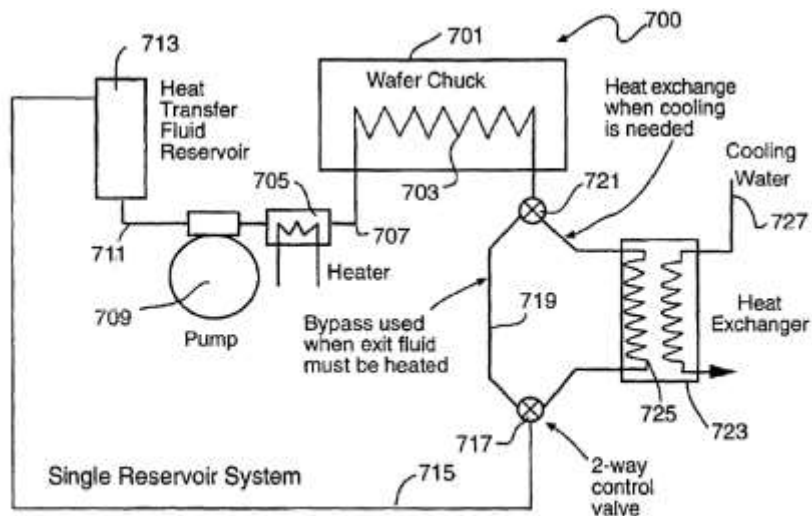


Fig. 7

Figure 7, shown above, depicts a temperature control system having substrate holder (also called “wafer chuck” or “wafer holder”) 701, heater 705, heat transfer fluid reservoir 713, and heat exchanger 723. *Id.* at 15:65–16:8. Fluid is “pumped from the reservoir through the heating unit, which selectively sets the temperature of the fluid.” *Id.* at 16:9–11. The fluid “transfers energy in the form of heat to the wafer holder to a desirable temperature.” *Id.* at 16:14–16. In another embodiment, the fluid can also be cooled using heat exchanger 723. *Id.* at 16:20–21. In a specific embodiment, “system 700 operates in a manner to program a process temperature of the substrate holder.” *Id.* at 16:28–30. An electrical heater heats the fluid to a desired temperature, which is “determined by comparing the desired wafer or wafer chuck set point temperature to a measured wafer or wafer chuck temperature.” *Id.* at 16:36–41.

A microprocessor-based system can be used to control the temperature of the substrate holder by selectively turning elements of the system (e.g., heater, fluid reservoir) on or off. *Id.* at 17:1–9. For example, if the measured temperature of the wafer or chuck is below the desired temperature “a suitable control algorithm such as a proportional controller or a proportional-integral-derivative (i.e., ‘PID’) controller algorithm increases the temperature by supplying more power to the heater.” *Id.* at 16:41–46. “The heat exchanger, fluid flow rate, coolant-side fluid temperature, heater power, chuck, etc., should be designed using conventional means to permit the heater to bring the fluid to a setpoint temperature and bring the temperature of the chuck and wafer to predetermined temperatures within

specified time intervals and within specified uniformity limits.” *Id.* at 16:60–67.

The ’264 patent states that conventional processing of resist layers, which is performed at low temperatures in order to help prevent rupturing of cross-linked layers and contaminative particulate matter, requires excessive time and lower throughput. *Id.* at 2:17–26. The ’264 patent states that the present invention overcomes these disadvantages by removing the ion implanted layer at a lower temperature followed by rapidly removing a majority of resist at a higher temperature. *See id.* at 2:26–30. For example, a “sequence of temperature changes” may be employed to avoid “various types of processing damage to the device and material layers.” *Id.* at 2:34–37. Figure 10, shown below, illustrates a simplified process according to the invention. *Id.* at 18:58–59.

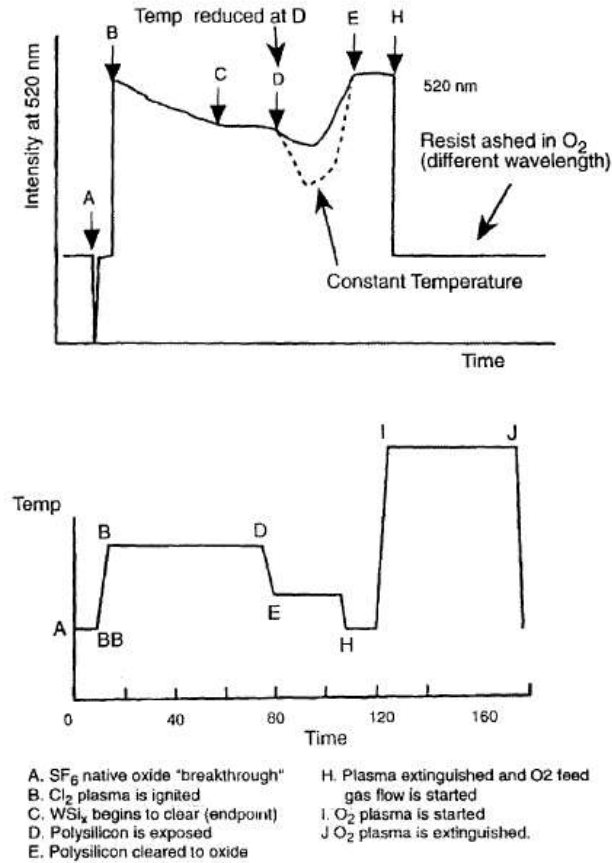


Fig. 10

The process shown in Figure 10, above, plots changes in temperature against processing time. *See id.*, Fig. 10; *see also id.* at 18:58–19:64 (providing details of the process shown in Figure 10). For example, during the isotropic breakthrough step (time A through BB), an SF₆ plasma is used to remove native oxide at a low temperature, such as room temperature. *Id.* at 18:63–66, Fig. 10. At the end of this step, at time BB, the control program increases within several seconds to a higher steady state value at time B. *Id.* at 19:8–10. The tungsten silicide layer is then etched at a constant temperature until the layer is breached. *Id.* at 19:10–15. At point D, the

wafer temperature is gradually reduced in order to achieve a slower and more anisotropic polysilicon etching step. *Id.* at 19:36–28.

D. Illustrative Claims

Of the claims challenged by Petitioner, only claim 37 is independent. Claim 37, with bracketed material and formatting added for clarity, is reproduced below:

37. A method of processing a substrate during the manufacture of a device, the method comprising:

[a] placing a substrate having a film thereon on a substrate holder within a chamber of a plasma discharge apparatus,

[b] the plasma discharge apparatus comprising:

a substrate temperature control system comprising a substrate temperature sensor and a substrate temperature control circuit operable to adjust the substrate temperature to a predetermined substrate temperature value with a first heat transfer process; and a substrate holder temperature control system comprising a substrate holder temperature sensor and a substrate holder temperature control circuit operable to adjust the substrate holder temperature to a predetermined substrate holder temperature value with a second heat transfer process;

[c] performing a first film treatment of a first portion of the film at a selected first substrate temperature;

[d] with the substrate temperature control circuit, changing from the selected first substrate temperature to a selected second substrate temperature, the selected second substrate temperature being different from the selected first substrate temperature; and

[e] performing a second film treatment of a second portion of the film at the selected second substrate temperature;

[f] wherein the substrate holder is heated above room temperature during at least one of the first or the second film treatments, and the substrate temperature control circuit is operable to change the substrate temperature from the selected first substrate temperature to the selected second substrate temperature within a preselected time period to process the film.

E. Instituted Grounds

We instituted an *inter partes* review of claims 37–50 and 67 on the following grounds of unpatentability:

(1) Whether claims 37–46 are unpatentable under § 103(a) over the combination of Kadomura³ and Matsumura;⁴

(2) Whether claims 40, 42, 45, 49, and 67 are unpatentable under § 103(a) over the combination of Kadomura, Matsumura, and Muller;⁵

(3) Whether claim 50 is unpatentable under § 103(a) over the combination of Kadomura, Matsumura, and Kikuchi;⁶

(4) Whether claims 37–46, 50, and 67 are unpatentable are unpatentable under § 103(a) over the combination of Kikuchi and Matsumura;

³ U.S. Patent No. 6,063,710, filed Feb. 21, 1997, issued May 16, 2000 (Ex. 1005, “Kadomura”).

⁴ U.S. Patent No. 5,151,871, filed Jun. 15, 1990, issued Sept. 29, 1992 (Ex. 1003, “Matsumura”).

⁵ U.S. Patent No. 5,605,600, filed Mar. 13, 1995, issued Feb. 25, 1997 (Ex. 1002, “Muller”).

⁶ U.S. Patent No. 5,226,056, filed Jan. 9, 1990, issued July 6, 1993 (Ex. 1004, “Kikuchi”).

(5) Whether claims 41 and 49 are unpatentable under § 103(a) over the combination of Kikuchi, Matsumura, and Muller, and

(6) Whether claims 37, 47, and 48 are unpatentable under § 103(a) as having been obvious over the combination of Moslehi '824,⁷ Oka,⁸ and Matsumura. Dec. on Inst. 40.

II. DISCUSSION

A. Principles of Law

To prevail on its challenges, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.⁹ See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

⁷ U.S. Patent No. 5,466,824, filed May 17, 1993, issued Aug. 29, 1995 (Ex. 1010, “Moslehi”)

⁸ U.S. Patent No. 6,235,563 B1, filed Nov. 7, 1991, issued May 22, 2001 (Ex. 1011, “Oka”).

⁹ The record does not contain evidence or argument of objective evidence of non-obviousness.

The level of ordinary skill in the art may be reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. Level of Ordinary Skill in the Art

Citing its declarant, Petitioner contends that a person of ordinary skill in the art at the relevant time (“POSITA”) would have had (i) a Bachelor’s degree in chemical engineering, materials science engineering, electrical engineering, physics, chemistry, or a similar field, and three or four years of work experience in semiconductor manufacturing or related fields; or (ii) a Master’s degree in chemical engineering, materials science engineering, electrical engineering, physics, chemistry, or a similar field, and two or three years of work experience in semiconductor manufacturing or related fields; or (iii) a Ph.D. in chemical engineering, materials science engineering, electrical engineering, physics, chemistry, or a similar field.

Pet. 24 (citing Ex. 1006 ¶¶ 19–21).

Patent Owner does not contest Petitioner’s description of the level of ordinary skill in its Response. Based on our review of the ’264 patent, the cited prior art, and the testimony of the parties’ declarants, we agree with Petitioner’s assessment of the level of ordinary skill in the art, and apply it for purposes of this Decision. *See Okajima*, 261 F.3d at 1355 (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown”).

C. Claim Construction

The '264 patent is expired.¹⁰ For claims of an expired patent, the Board's claim interpretation is similar to that of a district court. *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). Claim terms are given their ordinary and customary meaning as would be understood by a person of ordinary skill in the art at the time of the invention, and in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

For purposes of our Decision on Institution, we determined that none of the claims terms requires an explicit construction. Dec. on Inst. 10. During the instituted trial, neither party disagreed with this assessment, and we again see no need to provide an express construction for any of the terms in the challenged claims.

¹⁰ Neither party disputes that the '264 patent has expired. The earliest patent application referenced for the benefit of priority under 35 U.S.C. § 120 for the '264 patent was filed on December 4, 1995, and the patent has no term extensions. The term of the '264 patent, therefore, expired no later than December 4, 2015. *See* 35 U.S.C. § 154(a)(2) (2012 & Supp. III 2015) (stating that the term of a patent grant ends twenty (20) years from the date on which the application for the patent was filed in the United States, "or, if the application contains a specific reference to an earlier filed application or applications under section 120, 121, 365(c), or 386(c), from the date on which the earliest such application was filed").

D. Priority Date for the Challenged Claims of the '264 Patent

The '264 patent is a reissue of U.S. Patent No. 6,231,776 B1 (“the '776 patent”), which issued from U.S. Patent Application No. 09/151,163 (“the '163 application”) filed September 10, 1998. Ex. 1001, [64]. The '163 application claims priority to both (1) U.S. Provisional Application No. 60/058,650 (“the '650 provisional application”), filed on September 11, 1997, and (2) U.S. Patent Application No. 08/567,224 (“the '224 application”), filed on December 4, 1995. *Id.* at [64], [60], [63], 1:11–15.

Petitioner contends that the challenged claims of the '264 patent are not entitled to claim priority to a filing date any earlier than the September 11, 1997, filing date of the '650 provisional application, and, therefore, each of the asserted references qualifies as prior art to the challenged claims. *See* Pet. 9–12, 16, 18. Specifically, Petitioner contends that the '264 patent is not entitled to claim priority to the earlier filed '224 application because the '224 application fails to disclose, *inter alia*, changing the temperature of a substrate from “the selected first substrate temperature to the selected second substrate temperature within a preselected time period” as required by independent claim 37. *Id.* at 9–10 (citing Ex. 1006 ¶¶ 30–31).

Patent Owner has not introduced any evidence or argument that the '224 application provides written description support for the independent claim. *See generally* PO Resp. Nor does Patent Owner contend that any of the asserted references are not prior art to the '264 patent. Evaluating Petitioner’s unchallenged arguments, we determine that the challenged claims of the '264 patent are not entitled to claim priority to the December 4,

1995, filing date of the '224 application. As a consequence, we find that Kadomura, which was filed on February 21, 1997, Oka, which was filed on November 7, 1991, and the remaining asserted references, each of which issued before the September 11, 1997, filing date of the '650 provisional application, qualify as prior art to the challenged claims of the '264 patent. *See Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008) (stating that the patent owner has the burden of production to make a claim of priority that the challenged claims are entitled to a filing date prior to the date of the alleged prior art).

E. Asserted Art

1. Kadomura

Kadomura, titled “Method and Apparatus for Dry Etching with Temperature Control,” discloses, *inter alia*, a multi-temperature process for etching portions of a semiconductor wafer. Ex. 1005 at [54], [57]. The etching tool of Kadomura shown in Figure 4 has a wafer stage for holding the wafer/substrate during processing, thermometer for measuring wafer temperature, and a control device, having a PID controller, for controlling the temperature of wafer based on temperature measurements from the thermometer. *See id.* at 11:36–59, 12:37–48, Fig. 4. Kadomura adjusts the wafer temperature by adjusting the temperature of wafer stage 12, using a heater or chiller 17. *See id.* at 10:7–10 (stating the change in temperature of specimen W is controlled by “the cooling means and the heater disposed to the stage 12”); *see also id.* at 12:37–38 (the “cooling degree for the specimen [] is controlled by the flow rate of the coolant supplied from the chiller”). The temperature sensed by thermometer 18 is detected by a

feedback control device (feedback control means) 25 comprising a PID controller. *Id.* at 12:39–43. Kadomura explains that feedback control device 25 controls the cryogenic valve “to obtain a gas coolant flow rate previously determined by experiment or calculation based on the difference between the detected temperature and the predetermined temperature for the specimen.” *Id.* at 12:43–49.

Kadomura discloses several examples of multi-temperature etch processes. For example, one process includes a first step of etching silicide and polysilicon at room temperature (20°C) and a second step of etching polysilicon at a lower temperature (-30°C). *Id.* at 6:18–7:7; Figs. 1A–1C. In between these etching steps, gases remaining in the diffusion chamber are exhausted and the etching gas used in the second step is introduced; the gas is stabilized and the inside of the diffusion chamber is controlled to a constant pressure. *Id.* at 6:36–44. During “a series of such operations, that is directly after the completion of the etching of the first step,” gas coolant at -140°C from the chiller is supplied to the wafer stage to rapidly cool the wafer. *Id.* at 6:44–51. The temperature of the wafer reaches -30°C “within a short period of time of about 30 sec by such rapid cooling.” *Id.* at 6:52–55.

After completing these two steps, a heater within substrate holder stage 12 returns the wafer specimen temperature back up to 20°C. *Id.* at 7:31–47. The tool then repeats the same two-temperature etch process. *Id.* at 6:63–7:7, 7:31–47.

In another embodiment, the first etching step occurs at a low temperature (i.e., -30°C) and the second etching step is applied at a much higher temperature (i.e., 50°C). *Id.* at 9:54–10:27. A control mechanism for

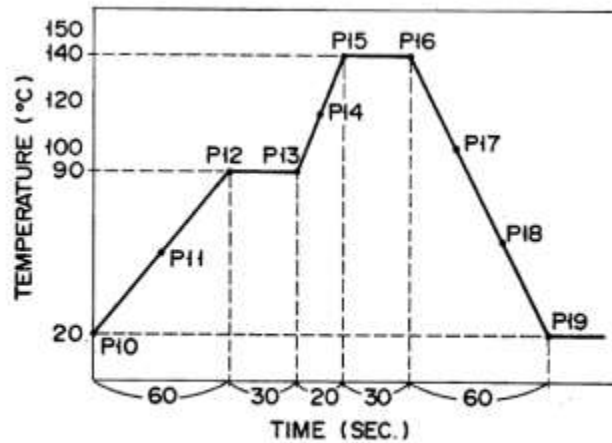
the cooling means and the heater disposed to the wafer stage are controlled to rapidly heat the specimen W between the etching steps. *See id.* at 10:7–10. The temperature of the wafer reaches 50°C “within a short period of time of about fifty (50) seconds.” *Id.* at 10:11–27.

2. Matsumura

Matsumura generally relates to heat-processing semiconductor wafers and, in particular, to controlling the temperature of a semiconductor wafer during processing. *See Ex. 1003, 1:8–13; see also id.* at 2:60–65 (stating one objective is to provide a “simpler method of heat-processing semiconductor devices whereby temperatures of the semiconductor devices can be controlled at devices-heating and -cooling times so as to accurately control their thermal history curve”).

Matsumura’s temperature control system uses a central processing unit (“CPU”) having a PID controller that stores “as a predetermined recipe, information showing a time-temperature relationship and applicable for either heating [a wafer] to a predetermined temperature for a predetermined period of time or cooling the [wafer] from a predetermined temperature over a predetermined period of time.” *See id.* at 3:1–7, 5:64–6:6, 8:56–62; *see also id.* at [57] (stating a “control system controls either the heating of the wafer or the cooling thereof, or both, in accordance with the detected temperature signal and the [stored] information”).

An example of a predetermined recipe is shown in Figure 9 below. *See id.* at 8:56–57.



F I G. 9

Figure 9, shown above, is a diagram showing a “recipe relating to a thermal history curve of a wafer-stage,” showing temperature as a function of time. *See id.* at 4:42–43; *see also id.* at 8:56–68 (stating “Points P 10 to P 19 shown in figure 9 are set in the recipe to surely reproduce the thermal history curve of the wafer”). The information “relating to temperatures and times at these points P 10 to P 19 is inputted as a command temperature table to the CPU.” *Id.* at 8:59–62.

Figure 5A, reproduced below, is a schematic diagram of an adhesion unit included in a resist processing system of Matsumura that includes wafer stage 12 for heating and cooling wafer W in accordance with recipes inputted into a CPU. *See id.* at 4:28–29, 5:13–17, 6:6–9.

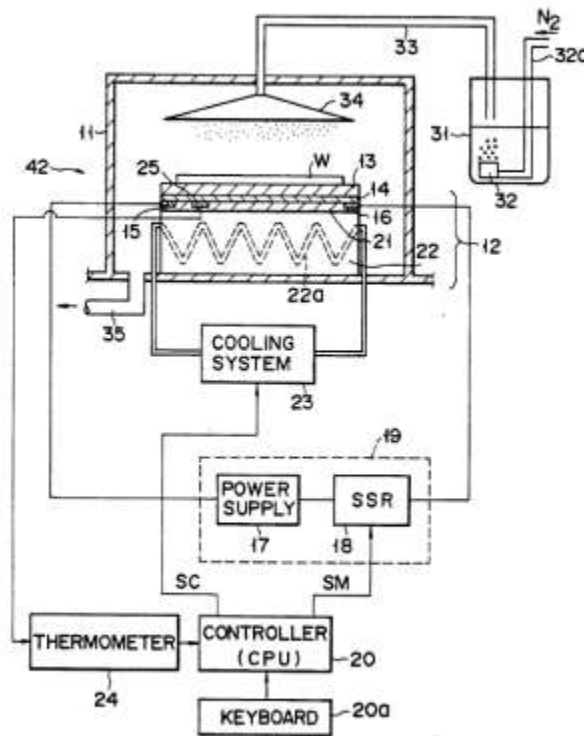


FIG. 5A

Figure 5A, reproduced above, depicts adhesion unit 42 having wafer-stage 12 that can heat and cool the semiconductor wafers (e.g., wafer W). *Id.* at 5:14–16. Recipes, including heating and other conditions, are inputted to the CPU by keyboard 20a. *Id.* at 6:6–9. Thermometer 24, which has thermal sensor attached to thin film 14, is attached to a control system 20. *See id.* at 5:57–6:4. Based on the recipe and temperature detecting signal, control system 20 controls the amount of coolant supplied from the cooling system to cooling jacket 22 under stage 12 and the current applied to conductive thin film 14 to raise the temperature of the wafer. *Id.* at 5:64–6:61.

Matsumura states that, although “the present invention has been applied to the adhesion and baking processes for semiconductor wafers in the above-described embodiments . . . , it can also be applied to any of the

ion implantation, [chemical vapor deposition (“CVD”)], etching and ashing processes.” *Id.* at 10:3–7.

3. Muller

Muller is directed to methods of shaping etch profiles by controlling wafer temperature using an electrostatic chuck and coolant circulating through a cathode and by changing the pressure of the gas filled in the gaps between the wafer and the cathode. Ex. 1002 at [54], Abstract, 1:7–12, 1:44–64, 4:51–5:25. Figure 4 of Muller, which depicts an example of an apparatus used to accomplish the multi-temperature etching methods, is reproduced below.

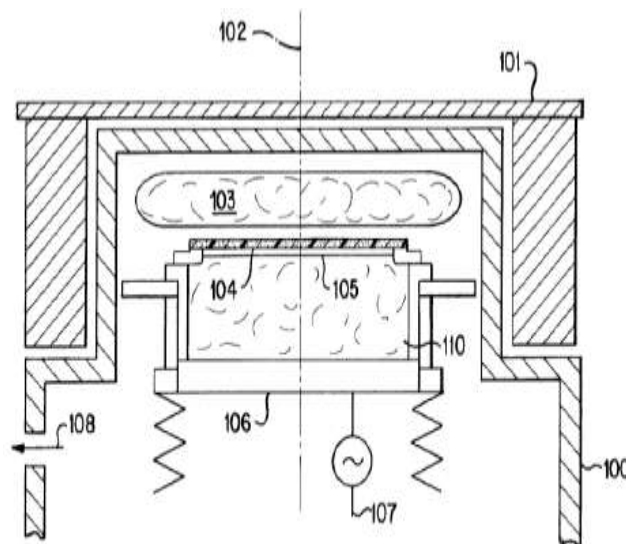


FIG. 4

Figure 4 depicts wafer 104, electrostatic chuck 105, cathode 106, and gas filled gap 110 between cathode 106 and wafer 104. *Id.* at 4:33–54.

Muller teaches that the change in taper angle of etched trenches correlates with increasing wafer temperature during the etching processes. Ex. 1002,

3:33–66, Figs. 1, 2. Muller explains that changing pressure of the gas filled in the gaps between the wafer and cathode, which can be accomplished in a very short period of time, results in an immediate effect on wafer temperature. *Id.* For example, wafer temperature can be increased by approximately 50°C over a time of “several seconds” during etching. *Id.* at 4:64–5:25, 5:41–48.

In one example, Muller teaches performing an initial etch at either 125°C or 145°C. *Id.* at 3:45–52, 3:56–66. The two etching temperature examples correspond to two different coolant temperatures. For example, use of a cathode coolant at 10°C results in a wafer temperature of approximately 125°C, while use of a cathode coolant at 30°C results in a wafer temperature of approximately 145°C. *Id.* at 3:45–52. Figure 3 below shows the wafer temperature at the two cathode coolant temperatures as a function of time.

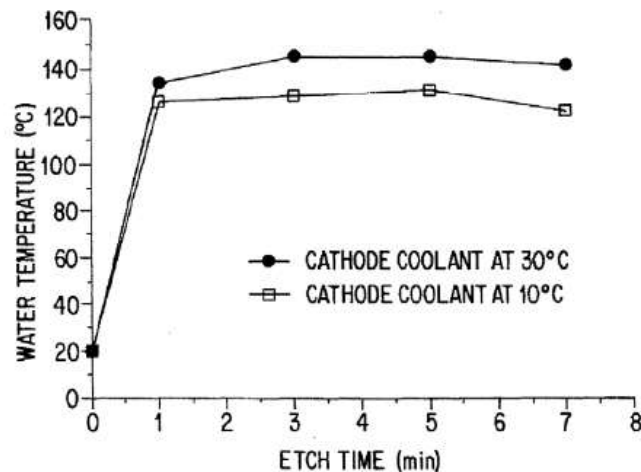


Figure 3 depicts a graph illustrating the change in wafer temperature for various coolant temperatures as a function of etch time.

In another example of an etching process, the gas-filled gap is pressurized for a first time period and then the pressure in the gap is rapidly changed to a second pressure for a second period of time. *Id.* at 4:64–5:3. Then, the gas pressure underneath the chuck is changed to increase wafer temperature by 50°C in “several seconds” during etching. *Id.* at 4:64-5:25, 5:41–48. In this example, using a 30°C coolant, the initial pressure is maintained for 70 seconds, after which the gap pressure is decreased for the remaining 6 minutes of etch time. *Id.* at 5:26–33.

4. Kikuchi

Kikuchi is directed to methods for plasma ashing a resist film by initially controlling the temperature of the substrate below that at which explosion of the resist film occurs until after a surface portion of a resist film has been removed. Ex. 1004, Abstract. Kikuchi describes ashing a wafer's photoresist film at two sequential temperatures using either infrared heat lamp 5 or hot plate 7 to raise the temperature, and thermometers 10, 66 to measure the wafer and hot plate temperatures. *See, e.g., id.* at 1:56–2:3, 7:20–34, 7:62–68, 8:8–14, 11:6–9, Figs. 12, 13. Figure 1 of Kikuchi is reproduced below.

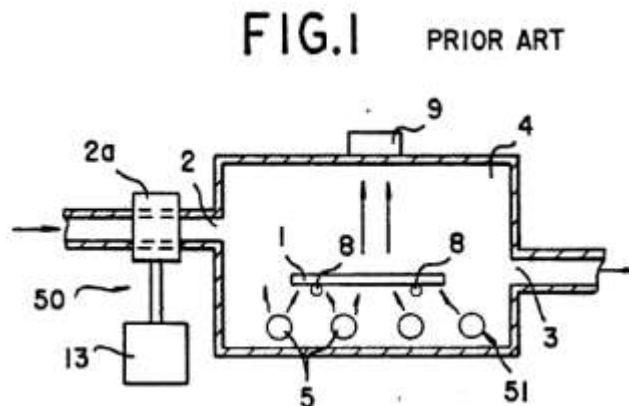


Figure 1 depicts a “conventional ashing method” in which a substrate is placed on rack 8 and is heated by infrared lamps 5 to a predetermined temperature in about 5 seconds (as shown by curve A in Figure 3). *Id.* at 1:56–60. The temperature of the substrate is controlled by infrared thermometer 9. *Id.* at 1:56–65, 4:62–63. Kikuchi explains that in this embodiment, it is difficult to coat the resist film 11 on only the front surface of substrate 1 as film will also be deposited on the rear surface of substrate 1. *Id.* at 2:47–61. Kikuchi states that if the substrate 1 is heated in contact with hot plate 7 to remove the resist film by ashing, hot plate 7 prevents the reactive radicals from working on that resist film and the resist film may remain on the rear surface of substrate 1. *Id.* at 2:61–67; Figs. 8, 9. Figure 11, shown below, depicts a sectional side view of an embodiment of the invention of Kikuchi.

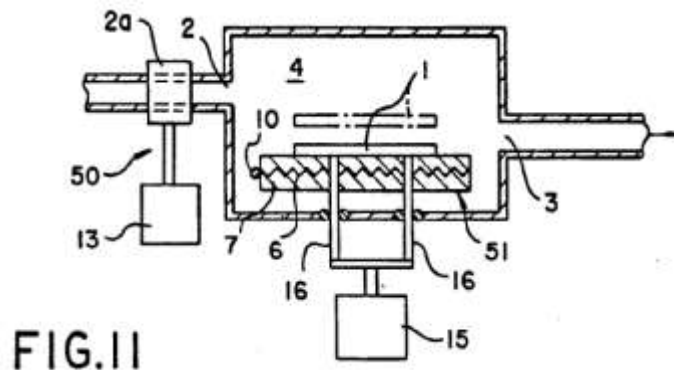


Figure 11 depicts a semiconductor substrate (wafer) 1, thermometer 10, pins 16, and heating means 51 having hot plate 7, inside of vacuum treatment chamber 4. *Id.* at 7:19–33. Kikuchi describes using the pins to suspend the substrate being ashed above the hot plate to remove a surface layer of photoresist, lowering pins 16 to place the substrate on the hot plate,

and then raising the temperature to ash the remaining portion of the photoresist at a high temperature. *Id.* at 8:1–14; *see also* Ex. 1006 ¶ 86.

Kikuchi describes etching a photoresist over a range of temperatures, with an initial step of 70°C–160°C and a rapid increase to 200°C over a time period of 5 to 10 seconds. *See, e.g.*, Ex. 1004, 2:37–46, 3:33–44, 5:46–54, Figs. 12, 13.

5. Moslehi '824

Moslehi '824 is directed to a lamp-heated chuck for uniform semiconductor wafer processing in lamp-heated and radio-frequency plasma device processing applications, over a wide range of temperatures that may reach as high as 1100°C. *See* Ex. 1010, [54], 1:9–15, 1:60–65, 5:16–21.

Moslehi '824 states that its chuck can be used to uniformly heat a semiconductor wafer from its back side and avoid the edge non-uniformity or cooling problems typical of known single wafer rapid thermal processing (RTP) based semiconductor device fabrication equipment. *See id.* at 4:16–21. Moslehi '824 also states that its chuck “may serve as a source of RF frequency for local RF plasma generation from activated species for plasma-enhanced deposition and etching or cleaning processes.” *Id.* at 10:34–39.

Figure 3 of Moslehi '824, reproduced below, illustrates a single-wafer semiconductor fabrication reactor. *Id.* at 6:10–13.

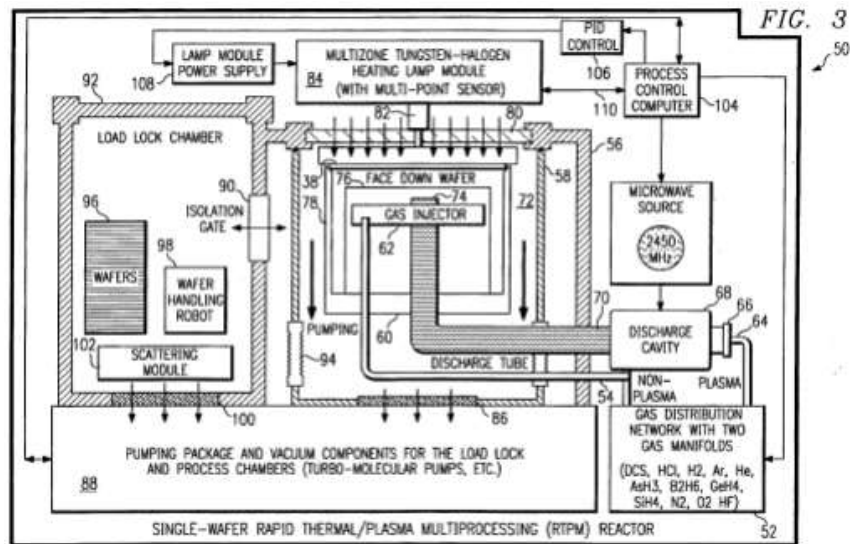


Figure 3 depicts single-wafer semiconductor fabrication reactor 50 having process chamber 72, semiconductor wafer 38, chuck assembly 82, heating lamp module 84, control computer 104, and PID computer 106. *See id.* at 6:10–33. Heating lamp module 84 has a multi-point temperature sensor. *See id.* at Fig. 3, 4:40–45, 6:44–50. Process control computer 104 provides multiple temperature control signals to PID controller 106 in response to temperature readings of the multi-point sensors. *See id.* at 7:3–16. The PID controller receives measured multi-point temperature sensor outputs as well as the desired wafer temperature set point (from process control computer 104) and delivers suitable power set points to lamp power supply module 108. *Id.* at 7:7–12. Signal lines 110 between process control computer 104 and multi-zone illuminator 84 include “signals from multi-point temperature sensors for real-time semiconductor wafer 38 temperature measurements and lamp power readings.” *Id.* at 7:12–16. As different semiconductor wafers are placed on the chuck surface, the temperature of chuck 82 and wafer 38 may be determined to vary by known amounts. *See id.* at 10:1–9. 2.

6. Oka

Oka is directed to methods of manufacturing a semiconductor device. Ex. 1011, 1:8–14. Oka discloses forming silicon film 602 on insulation support 601 by plasma CVD at a temperature of about 400°C to 800°C (*id.* at 20:25–34, Fig. 6A) followed by forming second silicon film 603 by plasma CVD at a temperature of about 150°C to about 300°C (*id.* at 20:52–56, Fig. 6B). After formation of silicon films 602 and 603, polycrystalline silicon layer 604 is formed by performing a “thermal treatment” for several hours at 550°C–650°C to obtain crystal growth via solid phase recrystallization. *Id.* at 20:66–21:10.

F. Asserted Obviousness of Claims 37–46 over Kadomura and Matsumura

1. Independent Claim 37

Claim 37 is directed to a method of processing a substrate during the manufacturing of a device. In general, the claim requires [a]¹¹ placing a substrate on a substrate holder, [c] performing a first film treatment of a first portion of the film at a selected first substrate temperature, [d] changing the selected first substrate temperature to a selected second substrate temperature, and [e] performing a second film treatment of a second portion of the film at a selected second substrate temperature. Claim 37 also requires [b] that the plasma discharge apparatus has a substrate temperature control system that has a substrate temperature sensor and a substrate temperature control circuit operable to adjust the substrate temperature. The plasma

¹¹ For clarity and consistency, the bracketed letters refer to claim elements as identified in Section I.D.

discharge apparatus also has a substrate holder temperature control system that has a substrate holder temperature sensor and a substrate holder temperature control circuit operable to adjust the substrate holder temperature. In addition, claim 37 requires [f] that the substrate holder be heated to above room temperature during the first or second film treatment and that the substrate temperature control circuit is operable to change the substrate temperature from the first to the second substrate temperature “within a preselected time period” to process the film.

Petitioner explains how the combination of Kadomura and Matsumura teaches each of the limitations of claim 37 and has articulated reasons why a skilled artisan would have combined the teachings of the asserted references. *See* Pet. 25–49. Patent Owner opposes. *See* PO Resp. 6–16.

Claim elements 37[a]–[e]

We have reviewed Petitioner’s undisputed contentions and evidence that the cited art teaches or suggests the preamble and limitations [a]–[e] of claim 37. *See* Pet. 25–34. We agree with and adopt Petitioner’s analysis as to these claim elements. *See id.*

For example, we agree with Petitioner’s contention that Kadomura teaches placing a substrate having a film (e.g., wafer specimen W having layers, including silicon dioxide film 31) on a substrate holder (wafer stage 12) in a chamber of a plasma discharge apparatus (processing chamber 2) as required by claim element 37[a]. *Id.* at 25 (citing Ex. 1005, 6:5–16, 11:8–13, 11:36–42, Fig. 1A; Ex. 1006 ¶ 136).

We also agree that Kadomura teaches a plasma discharging device including a substrate (wafer) temperature control system with a substrate

temperature sensor (thermometer 18) and a substrate temperature control circuit (control device 25 with a PID controller) to set the wafer to a predetermined temperature using a first heat transfer process, as recited in claim element 37[b]. *See id.* at 26 (citing Ex. 1005, Fig. 4). Kadomura's control device 25 determines wafer temperature with thermometer 18 and adjusts the measured temperature to match a "predetermined temperature," such as 20°C, -30°C, or 50°C. *Id.* (citing Ex. 1005, 6:29, 7:7, 9:62, 10:27, 12:38–48). Kadomura's tool adjusts the wafer's temperature to a predetermined temperature by transferring heat between substrate holder stage 12 and the wafer. *See* Ex. 1005, 3:24–49; Pet. 26.

We also agree with Petitioner that the combination of Kadomura and Matsumura teaches a substrate holder temperature control system with a control circuit and a substrate holder temperature sensor to set the substrate holder to a predetermined temperature using a second heat transfer process, as recited in claim element 37[b]. *See* Pet. 27–31. Matsumura teaches using sensor 25 and thermometer 24 to measure the temperature of stage 12 at conductive thin film 14 built into stage 12. *See* Ex. 1003, Fig. 5. Matsumura's control system 20 uses a control circuit (central processing unit (CPU) 201 with PID controller 203) to respond to wafer temperature detection signals. *See* Ex. 1003, 5:58–6:2, 6:28–32, 8:18–22, 8:29–31, Figs. 8, 9. Matsumura's control system 20 is programmed with "predetermined recipes" for heating or cooling the stage to set the wafer "to a predetermined temperature." *See* Ex. 1003, 3:1–7; *see also* Pet. 27–28. We agree with Petitioner's argument, supported by the unrebutted testimony of Dr. Bravman, that it would have been obvious to one of ordinary skill in the

art to include Matsumura's temperature sensor in the Kadomura-Matsumura system to measure the substrate holder temperature in order to confirm that the desired temperature was achieved, to set the substrate holder temperature to the desired value, and to directly gauge how well heat was transferred between the holder and the wafer (and vice versa) in order to adjust recipes and improve processing efficiencies. *Id.* at 30–31 (citing Ex. 1003, 5:42–45, 6:2–4, 7:20–22; Ex. 1005, 3:19–22, 5:18–26, 11:48–51; Ex. 1006 ¶¶ 75, 141–142).

We also agree with Petitioner's undisputed contention that Kadomura teaches performing a film treatment (etching) of a first portion of film (e.g., silicide layer 33 and part of polysilicon layer 32) at a selected first substrate temperature (e.g., 20°C or -30°C), as required by claim element 37[c], and performing a second film treatment (etching) of a second portion of the film (e.g., polysilicon layer 32) at a selected different second substrate temperature (e.g., -30°C or 50°C), as required by claim element 37[e]. *See* Pet. 34 (citing Ex. 1005, 6:63–7:7, 10:17–27; Ex. 1006 ¶ 53). We also agree with Petitioner's contention that Kadomura teaches the limitations of claim element 37[d] by etching a polysilicon layer in a first step at -30°C and etching a polysilicon layer in a second step at 50°C. *See* Pet. 33 (citing Ex. 1005, 9:54–62, 10:17–27).

Claim element 37[f]

Claim element 37[f] requires, *inter alia*, that the substrate temperature control circuit is operable to change the substrate temperature from the selected first substrate temperature to the selected second substrate temperature “within a preselected time period” to process the film. Petitioner

cites to our decision in *Lam Research Corp. v. Daniel L. Flamm*, Case IPR2016-00470 (PTAB July 1, 2016) (Paper 6) (“Ex. 1014”) as concluding that Kadomura does not disclose changing the substrate temperature “in a preselected time period” as recited in 37[f]. See Pet. 36. There, we stated that “Kadomura is silent with respect to the control device adjusting the temperature of the specimen between etching steps to a certain temperature within a pre-selected time period.” Ex. 1014, 16–17.

Petitioner asserts Matsumura’s control system 20 was preprogrammed with “predetermined recipes” for increasing or decreasing the stage temperature to set the wafer to a “predetermined temperature.” Pet. 28 (citing Ex. 1003, 3:1–7). Petitioner asserts that a POSITA would have been motivated to incorporate Matsumura’s programmable CPU with predetermined recipes into Kadomura’s tool. *Id.* (citing Ex. 1006 ¶¶ 145–146). Petitioner asserts that the use of such recipes was well known in the art, as evidenced by Matsumura. See, e.g., *id.* at 29; Ex. 1006 ¶¶ 143–147, 161–166. Petitioner asserts that it would have been obvious to automate Kadomura’s system using predetermined recipes, as taught by Matsumura, because “using predetermined recipes and program control circuits (including CPUs) in semiconductor manufacturing was well known and wide spread.” Pet. 29 (citing Ex. 1006 ¶¶ 145, 161). Petitioner further asserts that it would have been obvious to, and desirable for, a POSITA to use Matsumura’s predetermined recipe approach and programmable CPU in Kadomura’s processing tool to, *inter alia*, ensure an exact time interval for changing the temperature between steps, make the processes predictable and reliable, and maximize efficiency. See *id.* at 30 (citing Ex. 1006 ¶¶ 145–146,

161–162); *see also* Ex. 1006 ¶¶ 78–79 (stating that programming Kadomura’s control device 25 with a specific time interval for changing temperature would ensure that the time to change temperature would occur more quickly than the time for gas exchange).

Patent Owner makes a number of arguments in response, contending that the combination of Kadomura and Matsumura does not teach the “within a preselected time period” limitation of claim 37. *See* PO Resp. 1–16. Patent Owner also asserts that Petitioner fails to articulate any motivation to combine Matsumura with Kadomura. *Id.* at 8, 13–15. Patent Owner further asserts that Petitioner’s “two alleged motivations, ‘greater process control and reliability’ are conclusory statements, unsupported by any explanation or articulated reasoning.” *Id.* at 14–15 (asserting that passages in Matsumura relied upon by Petitioner “do not arise from using Matsumura’s ‘predetermined recipes,’ [but rather] arise from his ‘thermal history curves’” and citing Ex. 1003, 10:22–29). Patent Owner further argues that there would be no benefit to preselecting a time period to change Kadomura’s temperature because, according to Kadomura, “a specific time interval for changing temperature is of no importance, since the time interval to change the temperature is equal or less than the time interval to change the gas.” *Id.* at 5 (citing Ex. 2001 ¶ 10); *see also* PO Resp. 4–6 (quoting Ex. 1005, 6:55–62 and citing Ex. 1005, 7:19–30, 8:43–50, 10:13–16).

Patent Owner also asserts Kadomura is directed to cryogenic etching and putting low temperature etching into practical use, whereas the ’264 patent is directed to increasing throughput and selectivity of conventional plasma processing. *See* PO Resp. 4–5. Patent Owner argues that Kadomura’s

teachings of exchanging gases between etches and use of cold temperatures result in “relatively long intervals between etches” and, therefore, Kadomura teaches away from the ’264 patent, which, according to Patent Owner, teaches a time interval of only a few seconds. *See id.* (citing Ex. 1005, 6:54, 8:42; Ex. 2001 ¶ 10).

Patent Owner also asserts that Matsumura teaches nothing about etching, that Matsumura’s recipes would have been useless for plasma etching, and that Matsumura is directed to a different field of art. *See, e.g.*, PO Resp. 6, 10, 17; Ex. 2001 ¶¶ 13, 14.

Upon consideration of the arguments and evidence of record, we find that the combination of Kadomura and Matsumura teaches or suggests the “within a preselected time” limitations of claim element 37[f], and Petitioner has articulated a reasonable rationale for combining the teachings of the art.

Kadomura is directed to a method of dry etching a wafer “in one identical processing apparatus” where the temperature of the wafer is changed between etching steps. *See* Ex. 1005, [57]. Because “each of the etching treatments is conducted in the identical processing apparatus, the time for changing the [wafer] temperature between the steps can be shortened.” *Id.* at 4:46–49. Kadomura explains that “if the change of the [wafer] temperature is conducted about within a time required for a series of operations [e.g., exchanging gases] between the steps, dry etching treatment comprising a plurality of steps can be applied without deteriorating the throughput.” *Id.* at 4:49–54.

Although Kadomura states that the temperatures between etching steps should be changed within “short period[s] of time,” Kadomura does

not expressly identify any particular predetermined amount of time. *See, e.g., id.* at 5:1–10 (the wafer “can be controlled to a desired temperature in a short period of time”), 6:52–55 (stating the wafer temperature “reached -30°C [from a previous temperature of 20°C] within a short period of time of about 30 sec by such rapid cooling”), 10:11–16 (stating the wafer temperature “reaches 50°C [from a previous temperature of -30°C] within a short period of time”).

Matsumura teaches using preprogrammed recipes in semiconductor processing tools that set predetermined temperature changes over predetermined times. *See* Ex. 1003, [57]. Matsumura teaches that its preprogrammed recipe approach for controlling temperature, processing time, and temperature change time results in more accurate and reliable control of processing temperatures. *See id.* at 10:22–27 (stating that “when the semiconductor devices of same kind are to be heated and cooled, their thermal history curve can be controlled accurately same [sic] at their heating and cooling times, thereby enhancing their reliability. Particularly, their thermal history curve can be made accurately same”).

We find that using predetermined recipes and programmable control circuits, such as those taught in Matsumura, in semiconductor manufacturing was well known and widespread before the ’264 patent. *See, e.g.,* Ex. 1006 ¶¶ 70–71, 130. Even Patent Owner admits that the “type of automation [disclosed in Matsumura] was common knowledge at the time and its implementation in production worthy processing equipment was pervasive and obvious.” Ex. 2001 ¶ 14; PO Resp. 16–17; *see also* PO Resp. 16 (stating

digital process control in the field of semiconductor processing was common knowledge long before the Kadomura priority dates).

In addition, we find that a POSITA would have used Matsumura's automation using predetermined recipes that set forth predetermined temperature changes over predetermined time periods between the steps of Kadomura's process, in order to increase process control and reliability of Kadomura's processes, as well as to ensure an exact time interval for changes and that the time to change temperature is less than the time to exchange gases. *See* Pet. 28–30 (citing Ex 1006 ¶¶ 143–147, 161–162).

On this record, we disagree with Patent Owner's argument that Matsumura's motivating factors of greater process control and increased reliability arise from thermal history curves, not predetermined recipes. *See* PO Resp. 14–15. Matsumura expressly states that its recipes are used to reproduce thermal history curves. *See* Ex. 1003, 8:56–59; Ex. 1006 ¶ 144; Reply 12; Ex. 1024 ¶ 40. For example, Matsumura explains that the “recipe shown in Fig. 9 is inputted into the PID controller 203 by the keyboard 20a. Points P10 to P19 are set in the recipe so as to *surely reproduce the thermal history curve* of the wafer W.” Ex. 1003, 8:56–59 (emphasis added). Matsumura further explains that an object of the invention is to “provide a simpler method of heat-processing semiconductor devices whereby temperatures of the semiconductor devices can be controlled at devices-heating and -cooling times so as to *accurately control their thermal history curve*.” *Id.* at 2:60–3:7 (emphasis added).

As persuasively explained by Dr. Bravman, “Matsumura's recipes reproduce desired ‘thermal history curve[s]’ and were inputted into the

processing tool to specify exact processing times and temperatures, as well as exact times for temperature changes.” Ex. 1006 ¶ 144 (citing Ex. 1003, 8:4–12, 8:56–68); *see also* Ex. 1024 ¶ 40. Thus, we determine that the evidence of record shows that the use of predetermined recipes, as taught by Matsumura, results in greater process control and increased reliability.

We also disagree with Patent Owner’s argument that, because in each of Kadomura’s embodiments the time to change the temperature is already less than the time to change the gas, there would be no benefit in preselecting the time period to change Kadomura’s temperature. *See* PO Resp. 3–4, 8–9 (citing Ex. 1005, 6:55–62, 7:22–30, 8:40–50, 10:13–16); *see also* PO Resp. 8 (stating, “in each embodiment of Kadomura’s process, the time length of time to change the temperature, which was a ‘short period of time of about 30 seconds,’ was shorter than the time to change the gas”); *id.* at 9–10 (stating that even if the time interval to change the temperature were longer than the time interval to change the gas, the solution would be to “attempt to reduce the time interval for the temperature change. In this regard, Matsumura’s ‘predetermined recipes’ would again be utterly useless.”).

Rather, we agree with Petitioner that preselecting and programming Kadomura’s control device with a time interval for temperature change would have ensured that the time to change the temperature would have occurred more quickly than the time required for gas exchange and that the processes would have been predictable and reliable. *See, e.g.*, Pet. 33–34; Ex. 1006 ¶¶ 78, 145–146, 158–166; *see also* Reply 10–11 (citing Ex. 1024 ¶¶ 31, 33–35, 39). Kadomura teaches that to avoid “deteriorating the

throughput,” the time to change wafer temperature should occur within the time to perform the operations, including exchanging gases between the etching steps. Ex. 1005, 4:49–54; *see* Ex. 1006 ¶¶ 78, 163–164. The fact that in each of Kadomura’s embodiments the time period to change temperature was less than the time period to change gas does not mean that programming a controller with predetermined recipes would be useless. We agree with Petitioner and Dr. Bravman that using preprogrammed recipes setting forth predetermined time and temperature changes would increase the predictability, reproducibility, and reliability of the processes in Kadomura. *See* Pet. 28–30, 37–39; Ex. 1006 ¶¶ 143–147, 158–166.

We also do not agree with Patent Owner’s assertions that Matsumura teaches nothing about etching, that Matsumura’s recipes would have been useless for plasma etching, and that Matsumura is directed to a different field of art. PO Resp. 6, 10, 17; Ex. 2001 ¶¶ 13, 14. Matsumura expressly states that its processing techniques can be applied to etching processes. *See* Ex. 1003, 10:3–7 (stating that its invention “can also be applied to any of the ion implantation, CVD, etching and ashing processes”). Although Dr. Flamm testifies that “Matsumura’s recipes would have been useless for performing any plasma etching” (Ex. 2001 ¶ 14), and that Matsumura does not teach anything about etching (*id.* ¶ 11), Dr. Flamm provides little or no support for these statements. Dr. Flamm’s conclusory opinions are not persuasive. Nor has Patent Owner provided adequate reasoning or evidence as to why Matsumura is directed to a different field of art. *See* Tr. 40:13–24 (providing no argument that Matsumura is directed to a different field of art).

Rather, we credit Dr. Bravman’s testimony that a person of ordinary skill in the art would have known how to use the recipes and control circuits disclosed by Matsumura in common processing techniques, such as etching, and would have been motivated to implement those techniques. Ex. 1024 ¶¶ 15–20. Dr. Bravman testifies that Matsumura teaches a temperature control system for semiconductor processing that includes a computer programmed to control temperature, processing time, and temperature change time. *See* Ex. 1006 ¶¶ 70–71 (citing Ex. 1003, [57], Figs. 5A, 8–9). Dr. Bravman further testifies that Matsumura’s system includes a thermometer, a temperature sensor for a wafer stage, and a CPU to control the heating and cooling system, where the control system could take input from a user regarding heating and other conditions of the system. *See id.* ¶¶ 71–72 (citing Ex. 1003, Fig. 5A, 5:32–63, 5:67–6:9). Dr. Bravman testifies that, given common knowledge and the widespread use of preprogrammed recipes, it was not necessary for Matsumura to provide a detailed explanation of how to implement its techniques in an etching process, and that a POSITA would have known how to use the recipes and control circuits disclosed by Matsumura in common processing techniques, such as etching. *See id.* ¶¶ 77, 130–135; Ex. 1024 ¶ 18.

Patent Owner also argues that Kadomura and Matsumura teach away from the subject matter of the ’264 patent because, *inter alia*, Kadomura teaches that the specific time interval for changing temperature “is of no[] importance” as the time needed to change the gas is longer than the time needed to change the temperature, because Kadomura’s temperature change times of about 30 seconds are “relatively long” compared to those of

“several seconds” in the ’264 patent, and because Matsumura describes adhesion and baking processes. *See* PO Resp. 5–7 (citing Ex. 1005, 6:54, 8:42; Ex. 1003, 2:66–3:51, 4:56–59, 5:5–12, Fig. 4; Ex. 2001 ¶ 10).

We do not agree with these arguments. A reference teaches away if it criticizes, discredits, or otherwise discourages the solution claimed. *See In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). In weighing the suggestive power of each reference, we must consider the degree to which one reference might accurately discredit another. *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991).

Patent Owner has not persuasively shown that any teachings in either Kadomura or Matsumura discredit, criticize, or discourage the subject matter of the ’264 patent. Nothing in Kadomura discourages the use of recipes to control the amount of time taken to change temperature during processing. Rather, Kadomura teaches the importance of ensuring that the time to change temperature is less than the time to change gases. As such, Kadomura does not discredit the use of a temperature change over a predetermined time. Additionally, that Kadomura teaches different time intervals for temperature changes does not teach away from the time intervals claimed in the ’264 patent.

Claim element 37[f] also requires that the substrate holder is heated above room temperature during at least one of the first or second film treatments. We agree with Petitioner’s undisputed contention that Kadomura teaches or suggests that the substrate holder is heated above room temperature, as required by claim element 37[f]. *Id.* at 35–36 (citing

Ex. 1005, 3:24–49, 5:18–26, 6:18–29, 6:52–55, 6:63–7:7, 9:55–62, 10:27;
Ex. 1006 ¶ 155; Ex. 1017, 3:7–10).

For the foregoing reasons, we find Petitioner has persuasively shown that the combination of Kadomura and Matsumura teaches the limitations of claim element 37[f], and has articulated a reasonable rationale for combining the teachings of the cited art. Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claim 37 would have been obvious over the combined teachings of Kadomura and Matsumura.

2. Dependent Claims 38–46

Relying on the testimony of Dr. Bravman, Petitioner argues that dependent claims 38–46, each of which depends from independent claim 37, would have been obvious over the combination of Kadomura and Matsumura. *See* Pet. 40–49. Patent Owner does not separately address Petitioner’s explanations and supporting evidence with respect to these dependent claims. PO Resp. 22–23.

We have reviewed Petitioner’s unchallenged arguments and evidence, and determine that Petitioner has shown where each of the limitations of claims 38–46 are taught by Kadomura and Matsumura and has articulated a sufficient rationale for combining the teachings of the prior art. *See* Pet. 40–49. We agree with and adopt Petitioner’s analysis. *Id.*

For example, claim 38 requires the substrate temperature control circuit to comprise the substrate holder temperature control circuit, and

claim 39 requires the substrate holder temperature control circuit to comprise the substrate temperature control circuit. We agree with Petitioner's unchallenged argument that, like Matsumura's control system 20, Kadomura uses a circuit (control device 25, including a PID controller) to manage and change temperature rapidly. *Id.* at 29–30. We agree with Petitioner that, in the Kadomura-Matsumura system, the same circuit would have controlled and changed both the temperature of the substrate (wafer) and the substrate holder and thus the combined system teaches the limitations of claims 38 and 39. *See* Pet. 27–30, 40 (citing Ex. 1006 ¶¶ 168–169, 171–172; Ex. 1005, 3:23–38, 6:30–35, 10:7–10, 12:37–48).

Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claims 38–46 would have been obvious over the combined teachings of Kadomura and Matsumura.

G. Asserted Obviousness of Claims 40, 42, 45, 49, and 67 over Kadomura, Matsumura, and Muller

Relying on the testimony of Dr. Bravman, Petitioner argues that claims 40, 42, 45, 49, and 67, which depend from claim 37, are unpatentable over Kadomura, Matsumura, and Muller. *See* Pet. 49–55. Other than the arguments addressed above directed to the combinability of Kadomura and Matsumura, Patent Owner does not respond to Petitioner's contentions as to the asserted obviousness of claims 40, 42, 45, 49, and 67 over Kadomura, Matsumura, and Muller. *See* PO Resp. 22–23.

We have reviewed the evidence and Petitioner's unchallenged arguments and determine that Petitioner has shown where each of the limitations of claims 40, 42, 45, 49, and 67 are taught by Kadomura, Matsumura, and Muller. We further determine that Petitioner has articulated a sufficient rationale for combining the teachings of the prior art. *See* Pet. 49–55. We agree with and adopt Petitioner's analysis. *Id.*

For example, we agree with Petitioner that Muller discloses etching a first portion of a film at one temperature, then, without exhausting the gas, continuing to etch the substrate while increasing temperature. *See id.* at 50. We are persuaded by Petitioner's arguments and evidence, including Dr. Bravman's unrebutted testimony, that one of ordinary skill in the art would have applied Muller's teachings on continuous etching to etch the wafer of the Kadomura-Matsumura system during heating, because, *inter alia*, continuing to etch during the temperature change would have increased throughput, particularly when the same etching gas is used in Kadomura's two-step etching process. *See id.* at 50–51; Ex. 1006 ¶¶ 104–105, 182–183.

Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claims 40, 42, 45, 49, and 67 would have been obvious over the combined teachings of Kadomura, Matsumura, and Muller.

H. Asserted Obviousness of Claim 50 over Kadomura, Matsumura, and Kikuchi

Claim 50 depends from claim 37 and recites “wherein the first substrate temperature is changed to the second substrate temperature by transferring energy using at least radiation.”

Petitioner asserts that Kikuchi’s infrared lamps use infrared radiation to heat the wafer. *See* Pet. 56 (citing, *inter alia*, Ex. 1004, 7:25–31, Fig. 1; Ex. 1006 ¶ 210). We are persuaded by Petitioner’s arguments and evidence, including Dr. Bravman’s unrebutted testimony, that one of ordinary skill in the art would have used Kikuchi’s infrared lamps in the combined Kadomura-Matsumura system to heat a wafer more quickly, and that doing so would have been nothing more than routine optimization well within the capabilities of a skilled person to ensure rapid heat transfer. *See id.* at 56–58; Ex. 1006 ¶¶ 86–90, 209–211. Patent Owner does not argue separately the patentability of dependent claim 50. *See* PO Resp. 22–23.

Having considered the parties’ contentions and supporting evidence, we determine that Petitioner has shown by a preponderance of the evidence that claim 50 is unpatentable under 35 U.S.C. § 103 over Kadomura, Matsumura, and Kikuchi.

I. Asserted Obviousness of Independent Claim 37 over Kikuchi and Matsumura

As noted above, claim 37 is directed to a method of etching a substrate in the manufacture of a device. In general, the claim requires [a]¹² placing a substrate on a substrate holder, [c] performing a first film

¹² For clarity and consistency, the bracketed letters refer to claim elements as

treatment of a first portion of the film at a selected first substrate temperature, and [e] performing a second film treatment of a second portion of the film at a selected second substrate temperature. Claim 37 also requires [b] that the plasma discharge apparatus has (1) a substrate temperature control system that has a substrate temperature sensor and a substrate temperature control circuit operable to adjust the substrate temperature and (2) a substrate holder temperature control system that has a substrate holder temperature sensor and a substrate holder temperature control circuit operable to adjust the substrate holder temperature. In addition, claim 37 requires [f] that the substrate holder be heated to above room temperature during the first or second film treatment, and that the “substrate temperature control circuit is operable to change the substrate temperature from the first to the second substrate temperature “within a preselected time period” to process the film.

Petitioner contends claim 37 is unpatentable over the combined teachings of Kikuchi and Matsumura. *See* Pet. 58–67. Patent Owner opposes, contending that neither Kikuchi nor Matsumura teaches claim elements 37[a], [b], and [f], and that Petitioner has submitted no argument on a motivation to combine the asserted art. *See* PO Resp. 17–21. We have reviewed the arguments and evidence of record and determine that Petitioner has shown where each of the limitations of claim 37 is taught by Kikuchi and Matsumura, and has articulated a sufficient rationale for combining the

identified in Section I.D.

teachings of the asserted references. *See* Pet. 58–67. We agree with and adopt Petitioner’s analysis. *Id.*

For example, we agree with Petitioner that Kikuchi teaches a method of processing (etching) a substrate (wafer W) during the manufacture of a device (integrated circuit) by placing the wafer having a photoresist film on a substrate holder (hot plate 7) within a chamber (vacuum chamber 4) of a plasma discharge apparatus, as recited by the preamble and claim element 37[a]. *Id.* at 58–59; Ex. 1004, 1:6–11, 1:44–51, 7:31–34, 9:64–67, 11:36–42, Fig. 11; Ex. 1006 ¶¶ 135, 215–216.

We also agree with Petitioner’s assertion that the combination of Kikuchi and Matsumura teaches the plasma discharge apparatus recited in claim element 37[b]. Pet. 59–65. Kikuchi’s hot plate 7 includes heater 6 and thermometer 10 for measuring hotplate temperature. *Id.* at 60; Ex. 1004, 1:39–44, 1:66–2:3. The wafer is supplied with heat by thermal contact with hotplate 7 and is heated to a “predetermined temperature,” such as 200°C. Ex. 1004, 1:66–2:3, 5:55–56, 8:8–14; *see also* Pet. 59–60. We are persuaded by Petitioner’s argument, supported by the unrebutted testimony of Dr. Bravman, that to the extent Kikuchi’s hot plate embodiment does not measure substrate temperature in addition to hot plate temperature, it would have been obvious to do so in view of the embodiment disclosed in Figure 19, which uses infrared thermometer 66 to measure wafer temperature while processing a wafer on a hot plate, and because use of tools with two sensors was known in the art. Pet. 60; Ex. 1004, 11:1–9; Ex. 1006 ¶¶ 218–220; Ex. 1008, 321. We also agree with Petitioner’s argument, supported by the unrebutted testimony of Dr. Bravman, that it

would have been obvious to a POSITA to include a wafer temperature sensor in Kikuchi's hot plate embodiment to measure the temperature of both the hot plate and wafer to provide (1) more precise process control, (2) insights into the effectiveness of the heat transfer between the hot plate and wafer, and (3) two data points on temperature to allow for calibration. Pet. 61; Ex. 1006 ¶ 220.

We also agree with Petitioner that the combination of Kikuchi and Matsumura teaches wafer and substrate holder control systems that include “a control circuit and setting the wafer and substrate holder to a predetermined temperature using first and second heat transfer processes,” as generally required by claim element 37[b]. Pet. 62. For example, we agree with Petitioner that it would have been obvious to incorporate Matsumura's wafer stage 12, which is capable of both heating and cooling, into Kikuchi's tool in order to heat the wafer to a desired temperature, and then cool the wafer after it reaches the desired temperature to help counterbalance plasma-generated heat created during the etching process. *Id.* at 62–63.

In addition, we agree that Kikuchi teaches performing a first film treatment of a first portion of the film (etching the hardened outer surface of a photoresist film at 70°C to 160°C) and performing a second film treatment of a second portion of the film at a selected second substrate temperature (etching a second portion of the film at 200°C), as recited in claim elements 37[c] and [e]. Pet. 65–66; Ex. 1004, 2:37–44, 3:33–44, 5:46–56, 8:6–12; Ex. 1006 ¶¶ 229–230.

We further agree with Petitioner that the limitations of claim element 37[d] would have been obvious over the combined teachings of Kikuchi and

Matsumura. Pet. 65–66. We are persuaded by Dr. Bravman’s testimony that it would have been obvious to use Matsumura’s control circuit in Kikuchi’s tool to select and adjust the wafer and substrate holder temperatures in order to change Kikuchi’s selected first substrate temperature (70°C to 160°C) to a selected second substrate temperature (200°C). *Id.*; Ex. 1006 ¶ 230; Ex. 1004 2:37–44, 3:33–44, 5:46–56, 8:6–12.

We do not agree with Patent Owner’s arguments that claim 37 is patentable over Kikuchi and Matsumura (*see* PO Resp. 17–22) for the following reasons.

Patent Owner first argues that neither Kikuchi nor Matsumura teaches “placing a substrate on a substrate holder within a plasma discharge apparatus with a temperature sensor and temperature control system to adjust a first predetermined substrate temperature and similarly for a second predetermined temperature,” as required by claim elements 37[a] and [b]. PO Resp. 17–19. Specifically, Patent Owner asserts that, because Kikuchi uses *pins* to raise the substrate above the hot plate during etching, the hot plate is not the substrate holder of claim element 37[a]. *See id.* (citing Ex. 1004, 3:55–66 (“Kikuchi describes using pins to suspend the substrate being etched above the hot plate to remove a surface layer of photoresist.”))).

This argument, however, does not address Petitioner’s contention that it would have been obvious to replace Kikuchi’s hot plate and pins with Matsumura’s substrate holder (wafer stage 12). Pet. 62–63 (citing Ex. 1006 ¶¶ 92–94, 228). We credit Dr. Bravman’s unrebutted testimony that Matsumura’s wafer stage (substrate holder) was capable of both heating and cooling a substrate and that a POSITA would have used Matsumura’s wafer

stage with Kikuchi's tool in order to cool the wafer after it reached the desired temperature for ashing, as well as to maintain the wafer at a sufficiently low temperature to prevent the photoresist from exploding during the initial etching step while the hardened outer portion of the photoresist layer is removed. Ex. 1006 ¶ 228; Pet. 62–63.

Patent Owner also argues that the Petition “does not specify any prior art for claim elements 37[b] and [f] which require[] ‘substrate temperature to a predetermined substrate temperature value’ and ‘preselected time period to process the film.’” PO Resp. 19. We disagree with Patent Owner. Petitioner persuasively explains that these elements would have been obvious over either Kikuchi alone or the combination of Kikuchi and Matsumura. *See* Pet. 59–66.

With respect to the limitation of claim element 37[b] that requires “[adjusting] the substrate temperature to a predetermined substrate temperature value,” Petitioner explains that Kikuchi teaches using a hot plate to adjust wafer temperature to predetermined values of 70°C–160°C or 200°C, and using a sensor to measure hot plate temperature. Pet. 60; Ex. 1004, Fig. 13, 2:37–46, 3:33–44, 5:46–54. Petitioner explains that, to the extent Kikuchi does not expressly disclose measuring the substrate temperature when adjusting the substrate temperature, it would have been obvious to a POSITA, in view of Kikuchi's additional teachings, to use infrared thermometer 66 to measure wafer temperature while processing a wafer on a hot plate. Pet. 60–61 (citing Ex. 1006 ¶¶ 218–220, Ex. 1008, 321; Ex. 1004, 11:1–9, Fig. 19). We are persuaded by Petitioner's argument, and the unrebutted testimony from Dr. Bravman, that tools having both substrate

temperature sensors and substrate holder temperature sensors were well known in the art, and that it would have been obvious to a POSITA to include two separate sensors for measuring both the substrate and the substrate holder temperature in Kikuchi's tool (1) to provide more precise process control, (2) to provide insights into the effectiveness of heat transfer between the plate and the wafer, (3) to allow each sensor to act as a check on the other, and (4) to obtain data that could be analyzed to potentially accelerate temperature changes. *Id.* (citing Ex. 1006 ¶¶ 218–220; Ex. 1008, 321).

Additionally, we are persuaded by Petitioner's argument, and the unrebutted testimony of Dr. Bravman, that it would have been obvious to a POSITA to use Matsumura's wafer stage 12, which is capable of both heating and cooling, with Kikuchi's tool, for tighter temperature control at a selected temperature and to shorten the time that it takes to return to the lower temperature (e.g., 70°C–160°C) for the next wafer to be processed. Pet. 62; Ex. 1003, 5:32–33; Ex. 1004, 3:30–42; Ex. 1006 ¶¶ 93–94. We are also persuaded by Petitioner's argument, supported by Dr. Bravman's unrebutted testimony, that it would have been obvious to a POSITA to use Matsumura's programmable control circuit to control both the stage and the wafer temperature, and that it was well known in the art to use a control circuit that adjusts both wafer and stage temperatures. Ex. 1006 ¶ 227; Ex. 1008, 321, 323–24; Pet. 63–64.

With regard to claim element 37[f], which requires a “substrate temperature control circuit [that] is operable to change the substrate temperature from the selected first substrate temperature to the selected

second substrate temperature within a preselected time period to process the film,” Petitioner relies on the combined teachings of Kikuchi and Matsumura. *See* Pet. 62–66. Petitioner asserts that it would have been obvious to use Matsumura’s predetermined recipes, control circuit, and wafer stage in Kikuchi’s tool to change between the selected etching temperatures within a preselected time period. *Id.* at 66. We are persuaded by Dr. Bravman’s testimony that programmable control circuits and predetermined recipes were well known in semiconductor manufacturing and were widely used in the industry to improve process control, efficiency, reliability. *Id.* at 64–65; Ex. 1006 ¶¶ 223–225. Patent Owner admits that the “type of automation [disclosed in Matsumura] was common knowledge at the time and its implementation in production worthy processing equipment was pervasive and obvious.” Ex. 2001 ¶ 14; PO Resp. 16–17; *see also* PO Resp. 16 (also stating digital process control in the field of semiconductor processing was common knowledge).

We also find that Petitioner has persuasively shown by a preponderance of the evidence that a person skilled in the art would have incorporated Matsumura’s control system and preprogrammed recipe techniques into Kikuchi’s system to, *inter alia*, control reliability, predictability, and efficiency. Pet. 66–70. As discussed above, Matsumura teaches using preprogrammed recipes in semiconductor processing tools that set predetermined temperature changes over a predetermined time, and that such recipes were well known and widely used in the industry to improve process control, accuracy, and reliability. *See* Ex. 1003, [57], 10:22–27. A POSITA would have used Matsumura’s control system and predetermined

recipes with Kikuchi's tool to further Kikuchi's objective of reducing the time needed for its etching processes; to improve the precision, accuracy, and automation of Kikuchi's etching processes; and to ensure that the temperature change of Kikuchi occurred within the 10-second time period described in Kikuchi. Pet. 64–66; Ex. 1004, 1:66–2:1, 4:23–26, 7:62–68; Ex. 1006 ¶¶ 95–97, 222–227, 232.

For the foregoing reasons, we find Petitioner has persuasively shown that the combination of Kikuchi and Matsumura teaches the limitations of claim 37, and has articulated a reasonable rationale for combining the teachings of the cited art. Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claim 37 would have been obvious over the combined teachings of Kikuchi and Matsumura.

Dependent claims 38–46, 50, and 67

Relying on the testimony of Dr. Bravman, Petitioner argues that dependent claims 38–46, 50, and 67, each of which depends from independent claim 37, would have been obvious over the combination of Kikuchi and Matsumura. See Pet. 67–76. Patent Owner does not separately address Petitioner's explanations and supporting evidence with respect to these dependent claims. See PO Resp. 22–23.

We have reviewed Petitioner's unchallenged arguments and evidence, and determine that Petitioner has shown where each of the limitations of claims 38–46, 50, and 67 are taught by Kikuchi and Matsumura, and has articulated a sufficient rationale for combining the teachings of the prior art. We agree with and adopt Petitioner's analysis. See Pet. 67–76.

For example, claim 46 requires that at least the first or second film treatment comprises etching. We agree with Petitioner's unchallenged argument that Kikuchi teaches this limitation because Kikuchi teaches ashing a photoresist film at two different temperatures and ashing is a form of etching. Pet. 74 (citing Ex. 1004, 1:8–10, 2:37–44, 3:33–44, 5:46–54, 8:8–12; Ex. 1004, 9:64–67; Ex. 1006 ¶¶ 81, 263; Ex. 1009, 1:7–9.)

Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claims 38–46, 50, and 67 would have been obvious over the combined teaching of Kikuchi and Matsumura.

*J. Asserted Obviousness of Claims 41 and 49
over Kikuchi, Matsumura, and Muller*

Relying on the Bravman Declaration, Petitioner contends that dependent claims 41 and 49 would have been obvious under 35 U.S.C. § 103(a) over the combination of Kikuchi, Matsumura, and Muller. See Pet. 76–80. Petitioner explains how this proffered combination teaches the subject matter of each challenged claim and asserts that a POSITA would have had reason to combine or modify Kikuchi with teachings from Matsumura and Muller. *Id.*

Other than the arguments addressed above directed to the combinability of Kikuchi and Matsumura, Patent Owner does not respond to Petitioner's contentions as to the asserted obviousness of any of the dependent claims. See PO Resp. 22–23.

We have reviewed Petitioner's unchallenged arguments and evidence and determine that Petitioner has shown where each of the limitations of

claims 41 and 49 is taught by Kikuchi, Matsumura, and Muller, and has articulated a sufficient rationale for combining the teachings of the asserted art. *See* Pet. 76–80. We agree with and adopt Petitioner’s analysis. *Id.*

For example, we are persuaded by Petitioner’s arguments and evidence, including Dr. Bravman’s unrebutted testimony, that it would have been obvious to a POSITA to etch materials with different compositions (as taught by Muller) with Kikuchi’s process. We also agree with Petitioner’s argument and supporting evidence that a POSITA would have made this modification to increase throughput by avoiding having to move the wafer to a different chamber for the photoresist etch step, and because it was known in the art to ash photoresist and to etch other wafer layers in a single chamber. *See id.* at 77–79 (citing Ex. 1006 ¶¶ 113, 247–252).

Having considered the parties’ contentions and supporting evidence, we determine that Petitioner has shown by a preponderance of the evidence that claims 41 and 49 are unpatentable under 35 U.S.C. § 103 over Kikuchi, Matsumura, and Muller.

*K. Asserted Obviousness of Claims 37, 47, and 48
over Moslehi ’824, Oka, and Matsumura*

Petitioner contends that the combination of Moslehi ’824, Oka, and Matsumura teaches or suggests all of the elements of independent claim 37 and dependent claims 47 and 48. *See* Pet. 81–94. With respect to claim 37, Petitioner argues, *inter alia*, that Moslehi ’824 teaches a plasma discharge apparatus having the recited substrate holder, substrate temperature control system, and substrate holder temperature control system. *See* Pet. 81–89. Petitioner also asserts that Oka teaches “a specific recipe using deposition

and baking techniques to process a wafer.” *Id.* at 82. Petitioner argues that it would have been obvious to one skilled in the art to use Oka’s recipe in Moslehi ’824’s tool because (1) both references teach processes using chemical vapor deposition and Oka’s recipe includes depositing layers using CVD, (2) both references use similar “high temperatures,” teach processing temperature control, and disclose processes for forming polysilicon layers, and (3) Moslehi ’824 discloses “that its chuck could be used for plasma processing, including deposition.” *See id.* at 82–83 (citing Ex. 1006 ¶¶ 131–133, 279–280, 284; Ex. 1010, 1:18–43, 3:17–25, 3:53–63, 4:58–5:9, 5:19–23, 5:29–39, 6:13–17, 10:34–39; Ex. 1011, [57], 20:25–21:56).

In its Preliminary Response, Patent Owner asserted, *inter alia*, that Petitioner failed to adequately explain why one skilled in the art would have had a reason to combine the teachings of Moslehi ’824 and Oka to arrive at the subject matter of claim 37. *See* Prelim. Resp. 14–15 (citing Pet. 81–83). In our Decision on Institution, we agreed that Patent Owner’s argument “had merit” and noted that although “Petitioner has provided arguments that the teachings of Moslehi ’824 and Oka are combinable,” Petitioner did “not clearly articulate[] why one of skill in the art would [have] had reason to combine the references.” Dec. on Inst. 38 (citing Pet. 81–83, 87, 88). Nonetheless, we instituted review on Petitioner’s challenge of claims 37, 47, and 48 as unpatentable over Moslehi ’824, Oka, and Matsumura. *Id.*; *see also SAS Institute v. Iancu*, S.Ct. 138 S.Ct. 1348, 1354 (2018) (stating that when the Patent Office institutes an *inter partes* review, it must decide the patentability of all of the claims the petitioner has challenged).

In its Patent Owner Response, Patent Owner again asserts that

Petitioner failed to articulate a sufficient reason to combine the cited art. See PO Resp. 21–22. Petitioner replies that its reasons supporting the combination of Moslehi '824 and Oka are found at pages 82–83 of the Petition. Reply 22 (citing Ex. 1024 ¶¶ 62–68).

We agree with Patent Owner that the Petition fails to articulate a sufficient reason to combine the teachings of Moslehi '824 and Oka. An obviousness determination requires “finding both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art . . . and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *In re Stepan Co.*, 686 F.3d 1342, 1345–46 (Fed. Cir. 2017) (quoting *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016)).

We find the arguments set forth at pages 82 through 83 of the Petition do not articulate a persuasive reason *why* a POSITA would have combined Moslehi '824 and Oka. See *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (stating “obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed inventions”). Rather, the Petition merely argues that the references contain similar teachings and that Moslehi '824 “could be used” for plasma processing. Pet. 82–83. Even if we agree with Petitioner that Oka and Moslehi '824 contain similar teachings and that Moslehi '824 could be used for plasma processing, these allegations, without more, do not articulate a reasonable reason why a POSITA would have combined the teachings of the prior art. Notably, the Petition does not provide any evidence or argument

that the combined teachings would yield predictable results or that a POSITA would have had a reasonable expectation of success of combining the asserted art to arrive at the challenged claims.

We are also not persuaded by Petitioner's additional arguments that are presented for the first time in its Reply. *See* 37 C.F.R. § 42.22(a)(2) (stating that the petition must include a full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent); *see also* 35 U.S.C. § 312(a)(3) (stating the Petition must identify in the petition, "with particularity" all "evidence that supports the grounds for the challenge to each claim").

For example, Petitioner asserts in its Reply that a POSITA "would have been motivated to perform Oka's processing steps in the apparatus of Moslehi '824, which tightly controlled temperature, *to reliably, reproducibly, and precisely achieve a higher crystalline seed generation rate upon thermal treatment.*" Reply 23–34 (emphasis added) (citing Ex. 1024 ¶ 65; *cf.* Ex. 1006 ¶¶ 133, 280). Petitioner further argues that Moslehi '824's tool "would have *improved control, reproducibility, and precision* when performing Oka's processing recipes." *Id.* at 23. Petitioner further asserts that it would have been obvious to combine Moslehi '824, Oka, and Matsumura because Moslehi '824 discloses that its rapid thermal processing techniques "would have been useful" in combination with deposition processes like those taught in Oka. *Id.* None of these arguments were presented in the Petition, and we will not consider them when presented for the first time in the Reply. *See* 37 C.F.R. § 42.23(b) (stating a

“reply may only respond to arguments raised in the corresponding opposition, patent owner preliminary response, or patent owner response”).

Upon a full record, we determine that Petitioner has not established by a preponderance of evidence that a skilled artisan would have been motivated to combine the teachings of Moslehi '824 and Oka. Therefore, Petitioner has not established by a preponderance of the evidence that claims 37, 47, and 48 are unpatentable over the combined teachings of Moslehi '824, Oka, and Matsumura.

III. CONCLUSION

Based on the evidence and arguments, we find that Petitioner has demonstrated by a preponderance of the evidence that:

- (1) claims 37–46 are unpatentable under § 103(a) over the combination of Kadomura and Matsumura;
- (2) claims 40, 42, 45, 49, and 67 are unpatentable under § 103(a) over the combination of Kadomura, Matsumura, and Muller;
- (3) claim 50 is unpatentable under § 103(a) over the combination of Kadomura, Matsumura, and Kikuchi;
- (4) claims 37–46, 50, and 67 are unpatentable under § 103(a) over the combination of Kikuchi and Matsumura; and
- (5) claims 41 and 49 are unpatentable under § 103(a) over the combination of Kikuchi, Matsumura, and Muller.

Based on the evidence and argument, Petitioner has not demonstrated by a preponderance of the evidence that claims 37, 47, and 48 are unpatentable under § 103(a) over the combination of Moslehi '824, Oka, and Matsumura.

IV. ORDER

Accordingly, it is

ORDERED that claims 37–46, 49, 50, and 67 of U.S. Patent No. RE40,264 E are held to be unpatentable;

FURTHER ORDERED that claims 47 and 48 have not been shown to be unpatentable; and

FURTHER ORDERED that, because this Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent RE40,264 E

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