

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION, GLOBALFOUNDRIES U.S., INC.,
MICRON TECHNOLOGY, INC., and
SAMSUNG ELECTRONICS COMPANY, LTD.¹,
Petitioner,

v.

DANIEL L. FLAMM,
Patent Owner.

Case IPR2017-00282
Patent RE40,264 E

Before CHRISTOPHER L. CRUMBLEY, JO-ANNE M. KOKOSKI, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Samsung Electronics Company, Ltd. was joined as a party to this proceeding via a Motion for Joinder in IPR2017-01752.

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Intel Corporation, GLOBALFOUNDRIES U.S., Inc., Micron Technology, Inc., and Samsung Electronics Company, Ltd., (collectively “Petitioner”) challenge the patentability of claims 56–63, 70, and 71 of U.S. Patent No. RE40,264 E (Ex. 1001, “the ’264 patent”), owned by Daniel L. Flamm. (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during trial. For the reasons discussed below, we determine that Petitioner has shown by a preponderance of the evidence that claims 56–63, 70, and 71 of the ’264 patent are unpatentable.

A. Procedural History

On December 2, 2016, Intel Corporation, GLOBALFOUNDRIES U.S., Inc., and Micron Technology, Inc. (collectively, “Initial Petitioners”) filed a Petition requesting an *inter partes* review of claims 56–63 and 70–71 of the ’264 patent. Paper 2 (“Pet.”). Patent Owner filed a Preliminary Response. Paper 8. On June 13, 2017, we instituted an *inter partes* review of the challenged claims. Paper 9 (“Decision on Institution” or “Dec. on Inst.”). Subsequent to institution, Samsung Electronics Company, Ltd. (“Samsung”) filed a petition and motion for joinder with the instant proceeding. *Samsung Electronics Company, Ltd. v. Daniel L. Flamm*, Case IPR2017-01752, Papers 1, 3. On September 15, 2017, we granted Samsung’s petition and motion for joinder, joining Samsung as a petitioner in this *inter partes* review. Paper 12, 7.

Thereafter, Patent Owner filed a Patent Owner Response (Paper 13, “PO Resp.”) and Petitioner filed a Reply (Paper 14, “Reply”). In support of their respective arguments, Petitioner relies upon the declaration testimony of Dr. John Bravman (Exs. 1006 and 1023), and Patent Owner relies upon the declaration testimony of Dr. Daniel L. Flamm² (Ex. 2001).

Oral hearing was requested by both parties. Papers 17, 18. A consolidated oral hearing for this proceeding and Cases IPR2017-00279, IPR2017-00280, and IPR2017-000281, involving the same parties and the ’264 patent, and Cases IPR2017-00391, IPR2017-00392, and IPR2017-00406, involving the same parties and unrelated patents, was held on March 7, 2018. A transcript of the consolidated hearing has been entered into the record. Paper 30 (“Tr.”).

B. Related Proceedings

Petitioner reports that the Patent Owner has asserted the ’264 patent in five proceedings in the Northern District of California (Case Nos. 5:16-cv-01578-BLF, 5:16-cv-1579-BLF, 5:16-cv-1580-BLF, 5:16-cv-1581-BLF, and 5:16-cv-02252-BLF) and that Lam Research Corporation has filed a declaratory judgment action against Patent Owner on the ’264 patent, also in the Northern District of California (Case No. 5:15-cv-01277-BLF). Pet. 2.

Petitioner also challenges certain claims of the ’264 patent in IPR2017-00279, IPR2017-00280, and IPR2017-00281, which were filed concurrently with the Petition in this proceeding. The parties also identified nine other IPR petitions for review of the ’264 patent, filed by Lam Research

² Daniel L. Flamm is both the Patent Owner and Patent Owner’s declarant in this proceeding.

Corporation or Samsung, none of which are currently pending. *See* Pet. 2; Prelim. Resp. 1–2 (identifying IPR2015-01759 (institution denied); IPR2015-01764 (terminated-settled); IPR2015-01766 (institution denied); IPR2015-01768 (terminated-settled); IPR2016-00468 (institution denied); IPR2016-00469 (institution denied); and IPR2016-00470 (institution denied); IPR2016-01510 (institution denied) and; IPR2016-01512 (Final Written Decision – challenged claims unpatentable)).

C. The '264 Patent

The '264 patent, titled “Multi-Temperature Processing,” reissued April 29, 2008 from U.S. Patent Application No. 10/439,245 (“the '245 application”), filed on May 14, 2003. Ex. 1001, at [54], [45], [21], [22]. The '264 patent is a reissue of U.S. Patent No. 6,231,776 B1 (“the '776 patent”), which issued on May 15, 2001, from U.S. Patent Application No. 09/151,163 (“the '163 application”) filed September 10, 1998. *Id.* at [64]. The '264 patent is directed to a method “for etching a substrate in the manufacture of a device,” where the method “provide[s] different processing temperatures during an etching process or the like.” *Id.* at Abstract. The apparatus used in the method is shown in Figure 1, reproduced below.

Figures 6 and 7 depict temperature-controlled fluid flowing through substrate holder (600, 701), guided by baffles 605, where “[t]he fluid [is] used to heat or cool the upper surface of the substrate holder.” Ex. 1001, 14:28–63, 16:5–67. Figure 6 also depicts heating elements 607 underneath the substrate holder, where “[t]he heating elements can selectively heat one or more zones in a desirable manner.” *Id.* at 15:10–26. Referring to Figure 7, the operation of the temperature control system is described as follows:

The desired fluid temperature is determined by comparing the desired wafer or wafer chuck set point temperature to a measured wafer or wafer chuck temperature The heat exchanger, fluid flow rate, coolant-side fluid temperature, heater power, chuck, etc. should be designed using conventional means to permit the heater to bring the fluid to a setpoint temperature and bring the temperature of the chuck and wafer to predetermined temperatures within specified time intervals and within specified uniformity limits.

Id. at 16:36–39, 16:50–67.

An example of a semiconductor substrate to be patterned is shown in Figure 9, reproduced below.

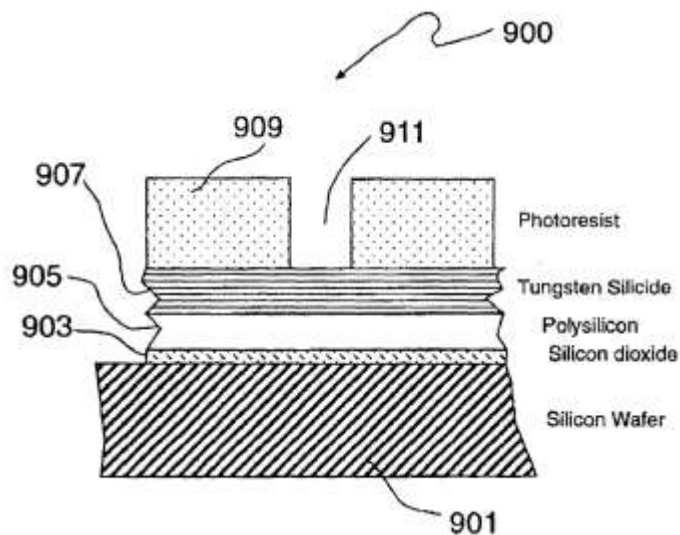


Figure 9 depicts substrate 901 having a stack of layers including oxide layer 903, polysilicon layer 905, tungsten silicide layer 907, and photoresist masking layer 909 with opening 911, from the treatment method shown in Figure 10, reproduced below. *Id.* at 17:58–18:57.

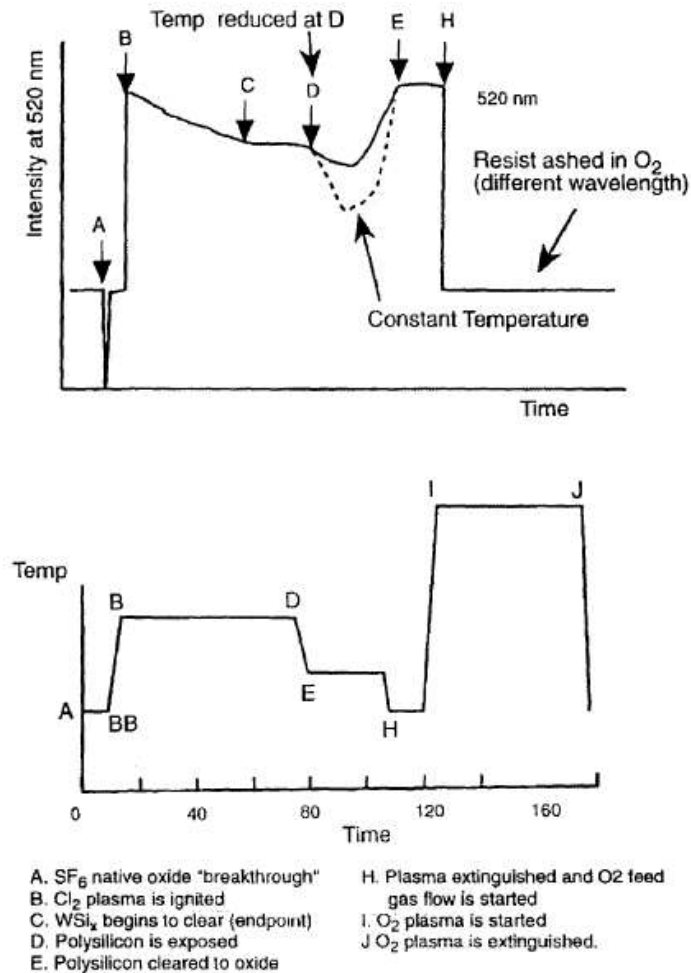


Fig. 10

Figure 10 depicts the tungsten silicide layer being etched between points B and D at a constant temperature; the polysilicon layer being exposed between Points D and E; the polysilicon layer being etched at a constant temperature beyond point E; and the resist being ashed beyond

Point I. Ex. 1001, 18:58–19:64. The plasma’s optical emission at 530 nanometers is monitored to determine when there is breakthrough to the polysilicon layer (Point D) and a lower etch temperature is required to etch the polysilicon layer (Point E). *Id.* at 19:8–24, 19:45–52.

D. Illustrative Claims

Of the challenged claims, claims 56 and 60 are the only independent claims at issue. Claim 56 is directed to a method of processing layers which are included in a stack of layers positioned on a substrate, and claim 60 is directed to a method for manufacturing a device comprising an integrated circuit. Claim 56 and 60, with bracketed material added,³ are reproduced below:

56. A method for processing layers which are included in a stack of layers positioned on a substrate, the method comprising:
- [a] placing the substrate on a substrate holder;
 - [b] sensing a substrate holder temperature;
 - [c] etching at least a portion of a first silicon-containing layer in a chamber while the substrate is maintained at a selected first substrate temperature; and
 - [d] etching at least a portion of a second silicon-containing layer in the chamber while the substrate is maintained at a selected second substrate temperature;
 - [e] wherein the substrate holder is heated to a temperature operable to maintain at least one of the selected first and the selected second substrate temperatures above 49° C., and the substrate temperature is changed from the first

³ Although the bracketed material is not present in the text of claims 56 or 60, for clarity and consistency, this Decision will use the bracketed nomenclature as utilized by both Petitioner and Patent Owner.

substrate temperature to the second substrate temperature with a control circuit operable to effectuate the changing within a preselected time period that is less than the overall process time associated with the etching the first silicon-containing layer and the second silicon-containing layer.

60. A method for manufacturing a device comprising an integrated circuit, the method comprising:

- [a] transferring a substrate comprising a stack of layers including a silicide layer into a chamber, the chamber comprising a substrate holder;
- [b] sensing the substrate holder temperature;
- [c] heating the substrate holder with a substrate holder control circuit and a heating device to maintain the substrate holder at a temperature that is operable to effectuate a substrate temperature above room temperature while processing the substrate;
- [d] processing the substrate on the substrate holder at a first substrate temperature; and
- [e] processing the substrate on the substrate holder at a second substrate temperature to etch at least a portion of the silicide layer;
- [f] wherein the first substrate temperature is different from the second substrate temperature and the first substrate temperature is changed to the second substrate temperature with a substrate temperature control circuit within a preselected time to etch the silicide layer.

E. Instituted Grounds

We instituted an *inter partes* review of claims 56–63, 70, and 71 on the following grounds of unpatentability:

- (1) Whether claims 56 and 58 are unpatentable under § 103(a) over the combination of Kadomura⁴ and Matsumura⁵;
- (2) Whether claim 57 is unpatentable under § 103(a) over the combination of Kadomura, Matsumura, and Muller⁶;
- (3) Whether claims 59–61 and 71 are unpatentable under § 103(a) over the combination of Kadomura, Matsumura, and Wang⁷;
- (4) Whether claim 62 is unpatentable under § 103(a) over the combination of Kadomura, Matsumura, Muller, and Wang;
- (5) Whether claims 63 and 70 are unpatentable under § 103(a) over the combination of Kadomura, Matsumura, Kikuchi⁸, and Wang;
- (6) Whether claims 56–58 are unpatentable under § 103(a) over the combination of Muller and Matsumura;
- (7) Whether claims 59–62 and 71 are unpatentable under § 103(a) over the combination of Muller, Matsumura, and Wang; and
- (8) Whether claims 63 and 70 are unpatentable under § 103(a) over the combination of Muller, Matsumura, Wang, and Kikuchi.

II. DISCUSSION

A. Principles of Law

To prevail in challenging Patent Owner’s claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are

⁴ U.S. Patent No. 6,063,710, filed Feb. 21, 1997, issued May 16, 2000 (Ex. 1005, “Kadomura”).

unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.⁹ See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). The level of ordinary skill in the art may be reflected by the prior art of record. See *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. Level of Ordinary Skill in the Art

Citing Dr. Bravman’s testimony, Petitioner contends that a person of ordinary skill in the art at the relevant time (a “POSITA”) would have had (i) a Bachelor’s degree in chemical engineering, materials science

⁵ U.S. Patent No. 5,151,871, filed Jun. 15, 1990, issued Sept. 29, 1992 (Ex. 1003, “Matsumura”).

⁶ U.S. Patent No. 5,605,600, filed Mar. 13, 1995, issued Feb. 25, 1997 (Ex. 1002, “Muller”).

⁷ U.S. Patent No. 4,992,391, filed Nov. 29, 1989, issued Feb. 12, 1991 (Ex. 1010, “Wang”).

⁸ U.S. Patent No. 5,226,056, filed Jan. 9, 1990, issued July 6, 1993 (Ex. 1004, “Kikuchi”).

⁹ The record does not contain evidence or argument of objective evidence of non-obviousness.

engineering, electrical engineering, physics, chemistry, or a similar field, and three or four years of work experience in semiconductor manufacturing or related fields; or (ii) a Master's degree in chemical engineering, materials science engineering, electrical engineering, physics, chemistry, or a similar field, and two or three years of work experience in semiconductor manufacturing or related fields; or (iii) a Ph.D. in chemical engineering, materials science engineering, electrical engineering, physics, chemistry, or a similar field. Pet. 24–25 (citing Ex. 1006 ¶ 21).

Patent Owner does not contest Petitioner's description of the level of ordinary skill in its Response. *See generally* PO Resp. Based on our review of the '264 patent, the cited prior art, and the testimony of the parties' declarants, we agree with Petitioner's assessment of the level of ordinary skill in the art and apply it for purposes of this Decision. *See Okajima*, 261 F.3d at 1355 (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown”).

C. Claim Construction

The '264 patent has expired.¹⁰ For claims of an expired patent, the Board's claim interpretation is similar to that of a district court. *See In re*

¹⁰ The '264 patent expired no later than December 4, 2015, which is twenty years after December 4, 1995, the earliest filing date of an application to which the '264 claims priority. *See* Ex. 1001 [63]; 35 U.S.C. § 154(a)(2) (2012 & Supp. III 2015) (stating patent term ends twenty (20) years from the date on which the application for the patent was filed in the United States, “or, if the application contains a specific reference to an earlier filed application or applications under section 120, 121, 365(c), or 386(c), from the date on which the earliest such application was filed”).

Rambus, Inc., 694 F.3d 42, 46 (Fed. Cir. 2012). Claim terms are given their ordinary and customary meaning as would be understood by a person of ordinary skill in the art at the time of the invention, and in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

For purposes of our Decision on Institution, we determined that none of the claims terms requires an explicit construction. Dec. on Inst. 10. During the instituted trial, neither party disagreed with this assessment, and we again see no need to provide an express construction for any of the terms in the challenged claims.

D. Priority Date for the Challenged Claims of the '264 Patent

The '264 patent is a reissue of U.S. Patent No. 6,231,776 B1, which issued from U.S. Patent Application No. 09/151,163 (“the '163 application”) filed on September 10, 1998. Ex. 1001, [64]. The '163 application claims priority to both (1) U.S. Provisional Application No. 60/058,650 (“the '650 provisional application”), filed on September 11, 1997 and (2) U.S. Patent Application No. 08/567,224 (“the '224 application”), filed on December 4, 1995. *Id.* at [60], [63], [64], 1:11–15.

Petitioner contends that the challenged claims of the '264 patent are not entitled to claim priority to a filing date any earlier than the September 11, 1997, filing date of the '650 provisional application, and, therefore, each of the asserted references qualifies as prior art to the challenged claims. *See* Pet. 9–11. Specifically, Petitioner contends that the '264 patent is not entitled to claim priority to the December 4, 1995, filing

date of the '224 application because the '224 application fails to disclose changing the temperature of a substrate on a substrate holder from a first to a second substrate temperature using a measured substrate temperature “within a preselected time interval” as required by independent claim 27, and a “substrate temperature control circuit effectuates the change from the first substrate temperature to the second substrate temperature within a preselected time period” as required by independent claim 51. *Id.* at 9–10 (citing Ex. 1006 ¶¶ 30–33).

Patent Owner has not introduced any evidence or argument that the '224 application provides written description support for the independent claims. *See generally* PO Resp. Nor does Patent Owner contend that any of the asserted references are not prior art to the '264 patent. Evaluating Petitioner's unchallenged arguments, we determine that the challenged claims of the '264 patent are not entitled to claim priority to the December 4, 1995, filing date of the '224 application. As a consequence, we find that Kadomura, which was filed on February 21, 1997, and the remaining asserted references, each of which issued before the September 11, 1997, filing date of the '650 provisional application, qualify as prior art to the challenged claims of the '264 patent.

E. Asserted Art

1. Kadomura

Kadomura, titled “Method and Apparatus for Dry Etching with Temperature Control,” discloses, *inter alia*, a multi-temperature process for etching portions of a semiconductor wafer. Ex. 1005 at [54], [57]. The etching tool of Kadomura shown in Figure 4 has a wafer stage for holding

the wafer/substrate during processing, thermometer for measuring wafer temperature, and a control device, having a PID controller, for controlling the temperature of wafer based on temperature measurements from the thermometer. *See id.* at 11:36–59, 12:37–48, Fig. 4. Kadomura adjusts the wafer temperature by adjusting the temperature of wafer stage 12, using a heater or chiller 17. *See id.* at 10:7–10 (stating the change in temperature of specimen W is controlled by “the cooling means and the heater disposed to the stage 12”); *see also id.* at 12:37–38 (the “cooling degree for the specimen [] is controlled by the flow rate of the coolant supplied from the chiller”). The temperature sensed by thermometer 18 is detected by a feedback control device (feedback control means) 25 comprising a [proportional-integral-derivative] PID controller. *Id.* at 12:39–43. Kadomura explains that feedback control device 25 controls the cryogenic valve “to obtain a gas coolant flow rate previously determined by experiment or calculation based on the difference between the detected temperature and the predetermined temperature for the specimen.” *Id.* at 12:43–49.

Kadomura discloses several examples of multi-temperature etch processes. For example, one process includes a first step of etching silicide and polysilicon at room temperature (20°C) and a second step of etching polysilicon at a lower temperature (-30°C). *Id.* at 6:18–7:7; Figs. 1A–1C. In between these etching steps, gases remaining in the diffusion chamber are exhausted and the etching gas used in the second step is introduced; the gas is stabilized and the inside of the diffusion chamber is controlled to a constant pressure. *Id.* at 6:36–44. During “a series of such operations, that is directly after the completion of the etching of the first step,” gas coolant at -140°C from the chiller is supplied to the wafer stage to rapidly cool the

wafer. *Id.* at 6:44–51. The temperature of the wafer reaches -30°C “within a short period of time of about 30 sec by such rapid cooling.” *Id.* at 6:52–55.

After completing these two steps, a heater within substrate holder stage 12 returns the wafer specimen temperature back up to 20°C . *Id.* at 7:31–47. The tool then repeats the same two-temperature etch process. *Id.* at 6:63–7:7, 7:31–47.

In another embodiment, the first etching step occurs at a low temperature (i.e., -30°C) and the second etching step is applied at a much higher temperature (i.e., 50°C). *Id.* at 9:54–10:27. A control mechanism for the cooling means and the heater disposed to the wafer stage are controlled to rapidly heat the specimen W between the etching steps. *See id.* at 10:7–10. The temperature of the wafer reaches 50°C “within a short period of time of about fifty (50) seconds.” *Id.* at 10:11–27.

2. Matsumura

Matsumura generally relates to heat-processing semiconductor wafers and, in particular, to controlling the temperature of a semiconductor wafer during processing. *See Ex. 1003*, 1:8–13; *see also id.* at 2:60–65 (stating one objective is to provide a “simpler method of heat-processing semiconductor devices whereby temperatures of the semiconductor devices can be controlled at devices-heating and -cooling times so as to accurately control their thermal history curve”).

Matsumura’s temperature control system uses a central processing unit (“CPU”) having a PID controller that stores “as a predetermined recipe, information showing a time-temperature relationship and applicable for either heating [a wafer] to a predetermined temperature for a predetermined

period of time or cooling the [wafer] from a predetermined temperature over a predetermined period of time.” *See id.* at 3:1–7, 5:64–6:6, 8:56–62; *see also id.* at [57] (stating a “control system controls either the heating of the wafer or the cooling thereof, or both, in accordance with the detected temperature signal and the [stored] information”).

An example of a predetermined recipe is shown in Figure 9 below.
See id. at 8:56–57.

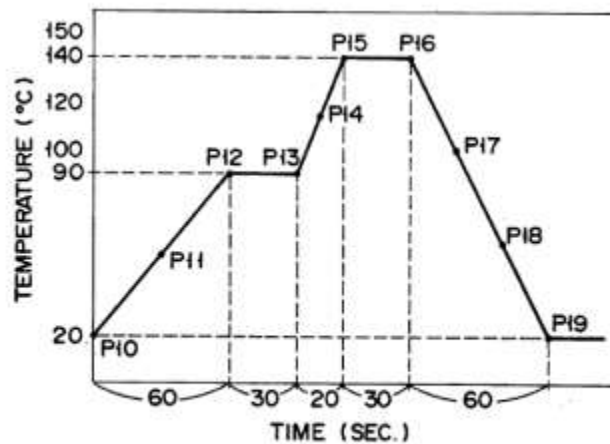


FIG. 9

Figure 9, shown above, is a diagram showing a “recipe relating to a thermal history curve of a wafer-stage,” showing temperature as a function of time. *See id.* at 4:42–43; *see also id.* at 8:56–68 (stating “Points P 10 to P 19 shown in figure 9 are set in the recipe to surely reproduce the thermal history curve of the wafer”). The information “relating to temperatures and times at these points P 10 to P 19 is inputted as a command temperature table to the CPU.” *Id.* at 8:59–62.

Figure 5A, reproduced below, is a schematic diagram of an adhesion unit included in a resist processing system of Matsumura that includes wafer

stage 12 for heating and cooling wafer W in accordance with recipes inputted into a CPU. *See id.* at 4:28–29, 5:13–17, 6:6–9.

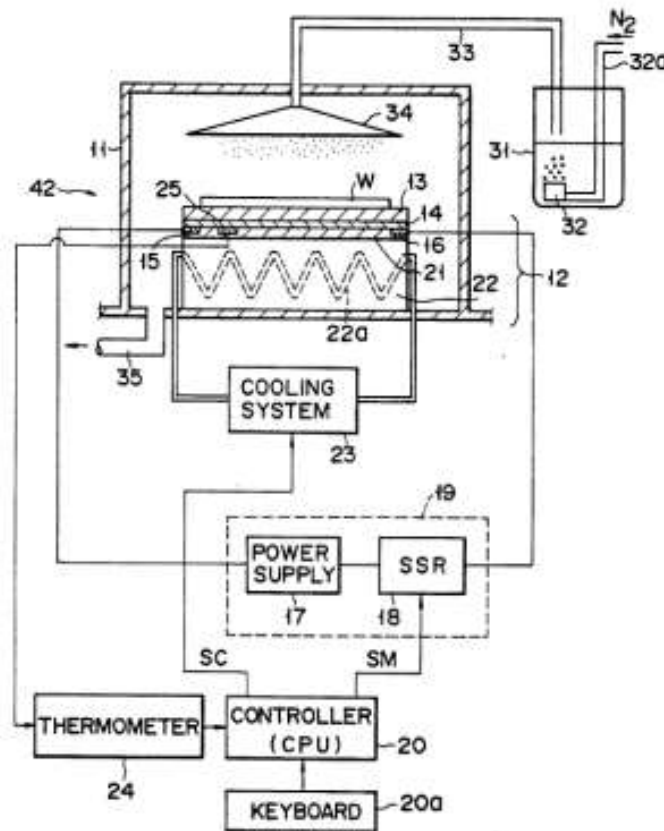


FIG. 5A

Figure 5A, reproduced above, depicts adhesion unit 42 having wafer-stage 12 that can heat and cool the semiconductor wafers (e.g., wafer W). *Id.* at 5:14–16. Recipes, including heating and other conditions, are inputted to the CPU by keyboard 20a. *Id.* at 6:6–9. Thermometer 24, which has thermal sensor attached to thin film 14, is attached to a control system 20. *See id.* at 5:57–6:4. Based on the recipe and temperature detecting signal, control system 20 controls the amount of coolant supplied from the cooling system to cooling jacket 22 under stage 12 and the current applied to conductive thin film 14 to raise the temperature of the wafer. *Id.* at 5:64–6:61.

Matsumura states that, although “the present invention has been applied to the adhesion and baking processes for semiconductor wafers in the above-described embodiments . . . , it can also be applied to any of the ion implantation, [chemical vapor deposition (“CVD”)], etching and ashing processes.” *Id.* at 10:3–7.

3. Muller

Muller is directed to methods of shaping etch profiles by controlling wafer temperature using an electrostatic chuck and coolant circulating through a cathode and by changing the pressure of the gas filled in the gaps between the wafer and the cathode. Ex. 1002 at [54], Abstract, 1:7–12, 1:44–64, 4:51–5:25. Figure 4 of Muller, which depicts an example of an apparatus used to accomplish the multi-temperature etching methods, is reproduced below.

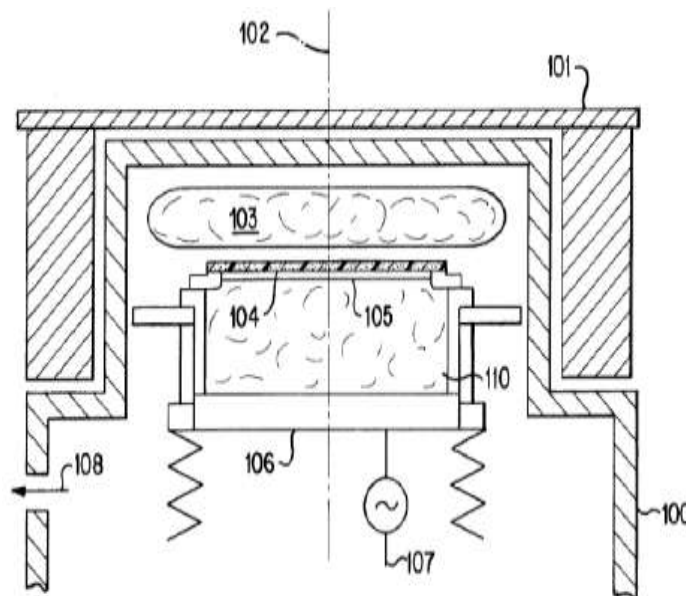


FIG. 4

Figure 4 depicts wafer 104, electrostatic chuck 105, cathode 106, and gas filled gap 110 between cathode 106 and wafer 104. *Id.* at 4:33–54.

Muller teaches that the change in taper angle of etched trenches correlates with increasing wafer temperature during the etching processes. Ex. 1002, 3:33–66, Figs. 1, 2. Muller explains that changing pressure of the gas filled in the gaps between the wafer and cathode, which can be accomplished in a very short period of time, results in an immediate effect on wafer temperature. *Id.* For example, wafer temperature can be increased by approximately 50°C over a time of “several seconds” during etching. *Id.* at 4:64–5:25, 5:41–48.

In one example, Muller teaches performing an initial etch at either 125°C or 145°C. *Id.* at 3:45–52, 3:56–66. The two etching temperature examples correspond to two different coolant temperatures. For example, use of a cathode coolant at 10°C results in a wafer temperature of approximately 125°C, while use of a cathode coolant at 30°C results in a wafer temperature of approximately 145°C. *Id.* at 3:45–52. Figure 3 below shows the wafer temperature at the two cathode coolant temperatures as a function of time.

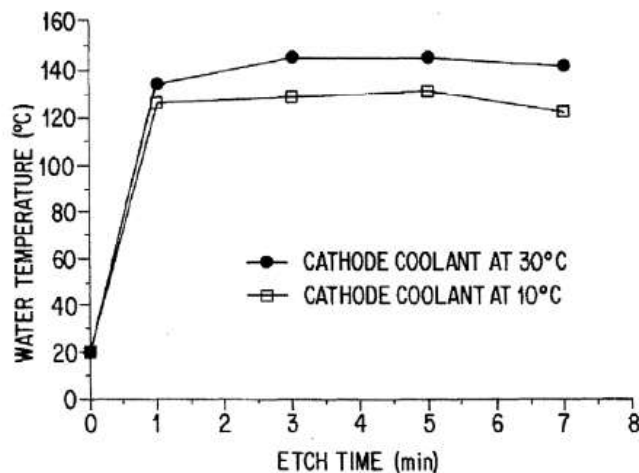


Figure 3 depicts a graph illustrating the change in wafer temperature for various coolant temperatures as a function of etch time.

In another example of an etching process, the gas-filled gap is pressurized for a first time period and then the pressure in the gap is rapidly changed to a second pressure for a second period of time. *Id.* at 4:64–5:3. Then, the gas pressure underneath the chuck is changed to increase wafer temperature by 50°C in “several seconds” during etching. *Id.* at 4:64–5:25, 5:41–48. In this example, using a 30°C coolant, the initial pressure is maintained for 70 seconds, after which the gap pressure is decreased for the remaining 6 minutes of etch time. *Id.* at 5:26–33.

4. Kikuchi

Kikuchi is directed to methods for plasma ashing a resist film by initially controlling the temperature of the substrate below that at which explosion of the resist film occurs until after a surface portion of a resist film has been removed. Ex. 1004, Abstract. Kikuchi describes ashing a wafer’s photoresist film at two sequential temperatures using either infrared heat lamp 5 or hot plate 7 to raise the temperature, and thermometers 10, 66 to measure the wafer and hot plate temperatures. *See, e.g., id.* at 1:56–2:3, 7:20–34, 7:62–68, 8:8–14, 11:6–9, Figs. 12, 13. Figure 1 of Kikuchi is reproduced below.

FIG.1 PRIOR ART

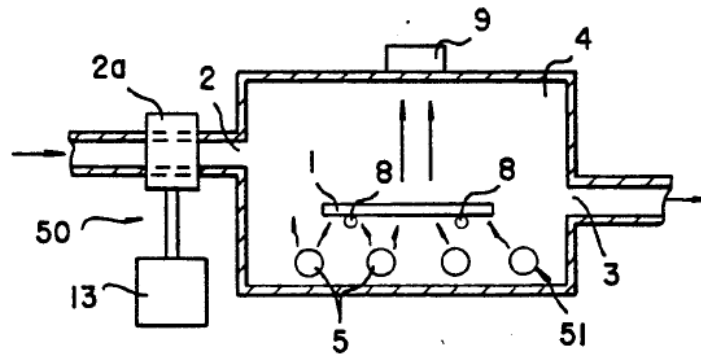


Figure 1 depicts a “conventional ashing method” in which a substrate is placed on rack 8 and is heated by infrared lamps 5 to a predetermined temperature in about 5 seconds (as shown by curve A in Figure 3). *See id.* at 1:56–60. The temperature of the substrate is controlled by infrared thermometer 9. *Id.* at 1:56–65, 4:62–63. Kikuchi explains that in this embodiment, it is difficult to coat the resist film 11 on only the front surface of substrate 1 as film will also be deposited on the rear surface of substrate 1. *See id.* at 2:47–61. Kikuchi states that if substrate 1 is heated in contact with hot plate 7 to remove the resist film by ashing, hot plate 7 prevents the reactive radicals from working on that resist film and the resist film may remain on the rear surface of substrate 1. *See id.* at 2:61–67; Figs. 8, 9. Figure 11, shown below, depicts a sectional side view of an embodiment of the invention of Kikuchi.

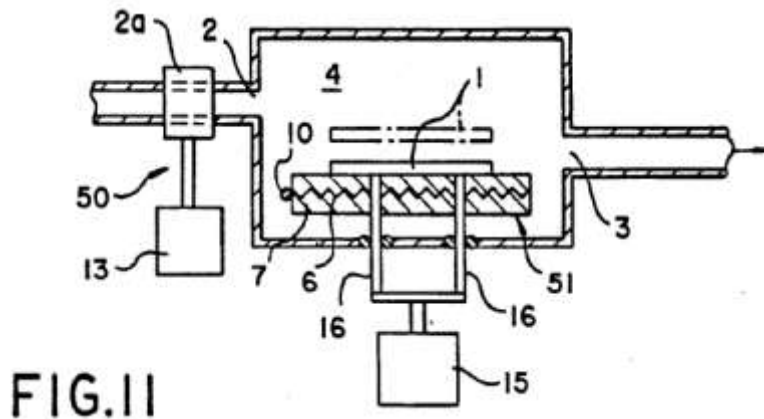


Figure 11 depicts a semiconductor substrate (wafer) 1, thermometer 10, pins 16, and heating means 51 having hot plate 7, inside of vacuum treatment chamber 4. *Id.* at 7:19–33. Kikuchi describes using the pins to suspend the substrate being ashed above the hot plate to remove a surface layer of photoresist, lowering pins 16 to place the substrate on the hot plate, and then raising the temperature to ash the remaining portion of the photoresist at a high temperature. *Id.* at 8:1–14; *see also* Ex. 1006 ¶ 86.

Kikuchi describes etching a photoresist over a range of temperatures, with an initial step of 70°C–160°C and a rapid increase to 200°C over a time period of 5 to 10 seconds. *See, e.g.*, Ex. 1004, 2:37–46, 3:33–44, 5:46–54, Figs. 12, 13.

5. Wang

Wang is directed to a process for forming a floating gate field-effect transistor having a multi-layered stack. Ex. 1010, [57]. Figure 3 of Wang is reproduced below.

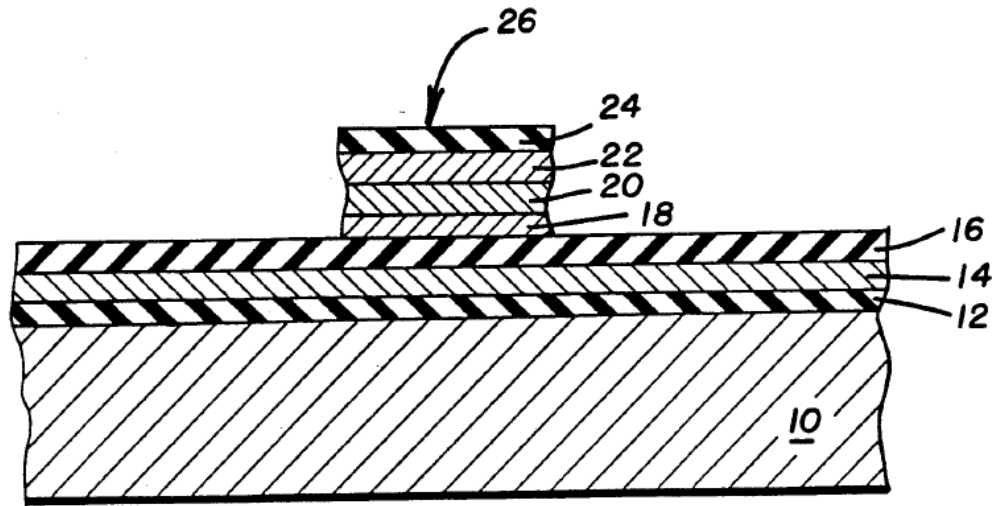


FIGURE 3

Figure 3 illustrates a multi-layer stack that includes oxide layers 16 and 24 and silicide layer 20, which is in between polysilicon layers 18 and 22. *Id.* at 4:19–23, Fig. 3.

*F. Asserted Obviousness of Independent Claim 56
over Kadomura and Matsumura and of Independent Claim 60 over
Kadomura, Matsumura, and Wang*

Claim 56 is directed to a method of processing layers which are included in a stack of layers positioned on a substrate. In general, claim 56 requires [a]¹¹ placing a substrate on the substrate holder, [b] sensing a substrate holder temperature, [c] etching a portion of a layer while the substrate is maintained at a selected first substrate temperature, [d] etching a second portion of the layer at a selected second substrate temperature. Claim 56 also requires [e] that the substrate holder is heated to maintain at least the first or second selected substrate temperatures above 49°C and that the

¹¹ For clarity and consistency, the bracketed letters refer to claim elements as identified in Section I.D.

substrate temperature is changed from the first substrate temperature to the second substrate temperature with a control circuit operable to effectuate the temperature change “within a preselected time period” that is less than the overall process time associated with the etching the first silicon-containing layer and the second silicon-containing layer.

Claim 60 is directed to a method for manufacturing a device comprising an integrated circuit. In general, claim 60 requires [a] transferring a substrate having a stack of layers including a silicide layer into a chamber having a substrate holder, [b] sensing the substrate holder, [c] heating the substrate holder with a substrate holder control circuit and a heating device, [d] processing the substrate on the substrate holder at a first substrate temperature, and [e] processing the substrate on the substrate holder at a second substrate temperature to etch a portion of a silicide layer on the substrate. Claim 60 also requires that the first and second substrate temperatures are different and that the first substrate temperature is changed to a second substrate temperature with a substrate temperature control circuit “within a preselected time” to etch the silicide layer.

Petitioner explains how the combination of Kadomura and Matsumura teaches each of the limitations of claim 56 and how the combination of Kadomura, Matsumura, and Wang teaches each of the limitations of claim 60, and has articulated reasons why a skilled artisan would have combined the teachings of the asserted references. *See* Pet. 25–43, 52–55. Patent Owner opposes, contending the asserted art does not teach “changing the temperature ‘within a preselected time interval’” as required by claim element 56[e] and claim element 60[f]. *See* PO Resp. 1–2; *see also generally id.* at 1–20.

1. *Claim Elements 56[a]–[d] and Claim Elements 60[a]–[e]*

We have reviewed Petitioner’s undisputed contentions and evidence that the cited art teaches or suggests the preamble and limitations [a]–[d] of claim 56 and the preamble and limitations [a]–[e] of claim 60. *See* Pet. 25–34, 52–55. We agree with and adopt Petitioner’s analysis as to these claim elements. *Id.*

For example, we agree with Petitioner’s contention that Kadomura teaches etching a silicide layer and a polysilicon layer in a layer stack that includes an oxide layer and a photoresist layer. *See id.* at 25–26 (citing Ex. 1005, Figs. 1A, 1C, 3A, 6:5–12, 9:36–45). We also agree that Kadomura’s control device 25 measures wafer temperature with thermometer 18 and adjusts the temperature to match a desired temperature during the etching process. *See id.* at 28 (citing Fig. 4, 12:38–48). We agree with Petitioner that Kadomura changes the temperature of the substrate holder (stage 12) to set the wafer temperature, and that it would have been obvious to measure the substrate holder temperature to confirm that the desired temperature was achieved. *See id.* at 28–29 (citing Ex. 1005, 3:23–49; Ex. 1006 ¶ 77). We also agree with Petitioner’s undisputed contention that to the extent Kadomura does not expressly teach a substrate holder temperature sensor, Matsumura teaches this feature as Matsumura teaches a multi-temperature processing tool with a temperature sensor embedded within substrate holder (stage 12). *Id.* at 29–30 (citing Ex. 1003, Fig. 5A, 5:32–33, 7:20–22). As persuasively explained by Petitioner, with supporting testimony by Dr. Bravman, it would have been obvious to use Matsumura’s temperature sensor to measure and set the temperature of Kadomura’s substrate holder in order to directly gauge how well heat was transferred

between the holder and the wafer (and vice versa) in order to adjust recipes and improve processing efficiencies and increase throughput. *Id.* at 31–32 (citing Ex. 1006 ¶¶ 77–79, 133; Ex. 1005, 3:19–22, 5:18–26, 11:48–51).

Petitioner also contends that Kadomura teaches changing the temperature of its substrate holder to change wafer temperature using a control device with a PID controller during the two step etching process. *Id.* at 34 (citing Ex. 1005, 3:23–49, 6:30–35, 8:17–23, 10:4–6). For example, a polysilicon layer is etched at -30°C in a first step followed by etching at 50°C in a second step. *Id.* (citing Ex. 1005, 9:54–56, 10:7–10, 10:17–27). In another example, a silicide layer and a portion of a polysilicon layer are etched at 20°C in a first step followed by etching the remaining portion of the polysilicon layer at -30°C in a second step. *Id.* at 35. Petitioner contends that it would have been obvious to etch the remaining polysilicon layer at 50°C in the second step (instead of -30°C) in order to increase the etching rate in view of Kadomura’s teaching to etch at 50°C and that “radical reaction is promoted by increasing the specimen temperature to 50°C.” *Id.* (citing Ex. 1005, 10:27–31). We also agree with Petitioner’s undisputed contentions that Wang teaches etching a wafer having silicide layer 20 between polysilicon layers 18 and 22 and that it would have been obvious to a POSITA to etch Wang’s wafer (including etching a polysilicon layer first, followed by a silicide layer) in the Kadomura-Matsumura system. *See* Pet. 49–52 (citing Ex. 1010, 4:19–26, Fig. 3; Ex. 1006 ¶¶ 104–106, 172, 174–175).

2. Claim Elements 56[e] and Claim Elements 60[f]

Regarding the limitations of claim elements 56[e] and 60[f] requiring

a temperature change within a *preselected time period* or *preselected time interval*, Petitioner cites to our decision in *Lam Research Corp. v. Daniel L. Flamm*, Case IPR2016-00469 (PTAB July 1, 2016) (Paper 6) (“Ex. 1014”), in which we determined the petitioner in that proceeding did not establish that “[Kadomura’s] control device is capable of pre-selecting the time period for adjusting the temperature of the specimen between etching steps.” Pet. 36 (quoting Ex. 1014, 16–17). There, we stated that “Kadomura is silent with respect to the control device adjusting the temperature of the specimen between etching steps to a certain temperature within a pre-selected time period.” Ex. 1014, 17.

In the present proceeding, Petitioner asserts that, to the extent Kadomura does not expressly disclose programing its controller with “predetermined recipes” that result in changing substrate temperature from a selected first temperature to a selected second temperature within a preselected time period or interval, the use of such recipes was well known in the art as evidenced by Matsumura. *See, e.g.*, Pet. 36–43, 52; Ex. 1006 ¶¶ 80–81, 144–155; Ex. 1003, [57], 3:1–7, 8:4–12, 8:56–68, 10:22–29. Petitioner asserts that it would have been obvious to automate Kadomura’s system using predetermined recipes as taught by Matsumura because “[u]sing predetermined recipes and program control circuits (including CPUs) in semiconductor manufacturing was well known and wide spread.” *See* Pet. 39 (citing Ex. 1006 ¶¶ 147–148). Petitioner further asserts that it would have been obvious to and desirable for a POSITA to use Matsumura’s predetermined recipe approach and programmable CPU in Kadomura’s processing tool to, *inter alia*, ensure an exact time interval for changing the temperature between steps, make the processes predictable and reliable, and

maximize efficiency. *See id.* at 40 (citing Ex. 1006 ¶¶ 148–155); *see also* Ex. 1006 ¶¶ 80, 150, 152 (stating that programming Kadomura’s control device 25 with a specific time interval for changing temperature would ensure that the time to change temperature would occur more quickly than the time for gas exchange).

Patent Owner makes a number of arguments in response, contending that the cited art does not teach the “preselected time” limitations of claim elements 56[e] and 60[f]. *See* PO Resp. 1–20. Patent Owner asserts that Petitioner fails to articulate any motivation to combine Matsumura with Kadomura. *See id.* at 8, 13–15. Patent Owner further asserts that Petitioner’s “two alleged motivators, ‘greater process control and reliability’ are conclusory statements, unsupported by any explanation or articulated reasoning.” *Id.* at 15 (asserting that passages in Matsumura relied upon by Petitioner “do not arise from using Matsumura’s ‘predetermined recipes,’ [but rather] arise from his ‘thermal history curves’” and citing Ex. 1003, 10:22–29).

Patent Owner also argues that there would be no benefit to preselecting a time period to change Kadomura’s temperature because, according to Kadomura, “a specific time interval for changing the temperature is of no importance, since the time interval to change the temperature is equal or less than the time interval to change the gas.” PO Resp. 5–6 (citing Ex. 2001 ¶ 10); *see id.* at 4–6 (quoting Ex. 1005, 6:55–62 and citing Ex. 1005, 7:19–30, 8:43–50, 10:13–16).

Patent Owner also asserts Kadomura is directed to cryogenic etching and putting low temperature etching into practical use, while the ’264 patent is directed to increasing throughput and selectivity of conventional plasma

processing. See PO Resp. 4–5. Patent Owner argues that Kadomura’s teaching of exchanging gases between etches and use of cold temperatures results in “relatively long intervals between etches” and, therefore, teaches away from the ’264 patent, which, according to Patent Owner, teaches a time interval of only a few seconds. See *id.* at 5 (citing Ex. 1005, 6:54, 8:42; Ex. 2001 ¶ 10). Patent Owner also asserts that: Matsumura teaches nothing about etching; Matsumura’s recipes would have been useless for plasma etching; and Matsumura is directed to a different field of art. PO Resp. 6–7, 14, 17; Ex. 2001 ¶¶ 11, 15.

Upon consideration of the arguments and evidence of record, we find that the combination of Kadomura and Matsumura teaches or suggests the limitations of claim elements 56[e] and 60[f], and Petitioner has articulated a reasonable rationale for combining the teachings of the art.

Kadomura is directed to a method of dry etching a wafer “in one identical processing apparatus” where the temperature of the wafer is changed between etching steps. See Ex. 1005, [57]. Because “each of the etching treatments is conducted in the identical processing apparatus, the time for changing the [wafer] temperature between the steps can be shortened.” *Id.* at 4:46–49. Kadomura explains that “if the change of the [wafer] temperature is conducted about within a time required for a series of operations [e.g., exchanging gases] between the steps, dry etching treatment comprising a plurality of steps can be applied without deteriorating the throughput.” *Id.* at 4:49–54.

Although Kadomura states that the temperatures between etching steps should be changed within “short period[s] of time,” Kadomura does not expressly identify any particular predetermined amount of time. See,

e.g., id. at 5:1–10 (stating the wafer “can be controlled to a desired temperature in a short period of time”), 6:52–55 (stating the wafer temperature “reached -30°C [from a previous temperature of 20°C] within a short period of time of about 30 sec by such rapid cooling”), 10:11–16 (stating the wafer temperature “reaches 50°C [from a previous temperature of -30°C] within a short period of time”).

Matsumura teaches using preprogrammed recipes in semiconductor processing tools that set predetermined temperature changes over predetermined times. *See* Ex. 1003, [57]. Matsumura teaches that its preprogrammed recipe approach for controlling temperature, processing time, and temperature change time results in a more accurate and reliable control of processing temperatures. *See id.* at 10:22–27 (stating that “when the semiconductor devices of same kind are to be heated and cooled, their thermal history curve can be controlled accurately same [sic] at their heating and cooling times, thereby enhancing their reliability. Particularly, their thermal history curve can be made accurately same”).

We find that using predetermined recipes and programmable control circuits, such as those taught in Matsumura, in semiconductor manufacturing was well known and widespread before the ’264 patent. *See, e.g.,* Ex. 1006 ¶¶ 147–148. Even Patent Owner admits that the “type of automation [disclosed in Matsumura] was common knowledge at the time and its implementation in production worthy processing equipment was pervasive and obvious.” PO Resp. 17 (citing Ex. 2001 ¶ 15); *see also id.* (stating “digital process control in the field of semiconductor processing was common knowledge long before the Kadomura priority dates”).

In addition, we find that a POSITA would have used Matsumura's automation using predetermined recipes that set forth predetermined temperature changes over predetermined time periods between the steps of Kadomura's process in order to increase process control and reliability, as well as to ensure an exact time interval for changes and that the time to change temperature is less than the time to exchange gases. *See* Pet. 38–41 (citing Ex 1006 ¶¶ 147–154).

Patent Owner's arguments that Matsumura's motivating factors of greater process control and increased reliability arise from thermal history curves, not predetermined recipes, are not persuasive on this record. *See* PO Resp. 15. Matsumura expressly states that its recipes are used to reproduce thermal history curves. *See* Ex. 1003, 8:56–59; Reply 12; Ex. 1023 ¶ 40. For example, Matsumura explains that the “recipe shown in Fig. 9 is inputted into the PID controller 203 by the keyboard 20a. Points P10 to P19 are set in *the recipe so as to surely reproduce the thermal history curve of the wafer W.*” Ex. 1003, 8:56–59 (emphasis added). Matsumura further explains that an object of the invention is to “provide a simpler method of heat-processing semiconductor devices whereby *temperatures of the semiconductor devices can be controlled at devices-heating and -cooling times so as to accurately control their thermal history curve.*” *Id.* at 2:60–3:7 (emphasis added).

As persuasively explained by Dr. Bravman, “Matsumura's recipes reproduce desired ‘thermal history curve[s]’ and were inputted into the processing tool to specify exact processing times and temperatures, as well as exact times for temperature changes.” Ex. 1006 ¶ 146 (citing Ex. 1003, 8:4–12, 8:56–68); *see also* Ex. 1023 ¶ 40. Thus, we determine that the

evidence of record shows that the use of predetermined recipes, as taught by Matsumura, results in greater process control and increased reliability.

We are also not persuaded by Patent Owner’s argument that, because in each of Kadomura’s embodiments the time to change the temperature is already less than the time to change the gas, there would be no benefit in preselecting the time period to change Kadomura’s temperature. *See* PO Resp. 4, 8–9 (citing Ex. 1005, 6:55–62, 7:19–30, 8:40–50, 10:11–16); *see also id.* at 8–9 (stating “[i]n each embodiment of Kadomura’s process, the length of time to change the temperature, which was a ‘short period of time of about 30 seconds,’ was shorter than the time to change the gas”)¹²; *id.* at 10 (stating that even if “the time interval to change the temperature *were longer* than the time interval to change the gas,” the solution would be to “attempt to reduce the time interval for the temperature change. In this regard, Matsumura’s ‘predetermined recipes’ would again be utterly useless.”).

Rather, we agree with Petitioner that preselecting and programming Kadomura’s control device with a time interval for temperature change would have ensured that the time to change the temperature would have occurred more quickly than the time required for gas exchange, and that the processes would be predictable and reliable. *See, e.g.,* Pet. 40–41; Ex. 1006 ¶¶ 148–155. Kadomura teaches that to avoid “deteriorating the throughput,” the time to change wafer temperature should occur within the time to perform the operations including exchanging gases between the etching

¹² Kadomura also teaches that the time to change temperature could be as long as 50 seconds. Ex. 1005, 10:11–13.

steps. Ex. 1005, 4:49–54; *see* Ex. 1006 ¶¶ 80, 149. The fact that in each of Kadomura’s embodiments the time period to change temperature was less than the time period to change gas does not mean that programming a controller with predetermined recipes would be useless. We agree with Petitioner and Dr. Bravman that using preprogrammed recipes setting forth predetermined time and temperature changes would increase the predictability, reproducibility, and reliability of the processes in Kadomura. Pet. 40–41; Ex. 1006 ¶¶ 147, 150–152.

We also do not agree with Patent Owner’s assertions that Matsumura teaches nothing about etching, that Matsumura’s recipes would have been useless for plasma etching, and that Matsumura is directed to a different field of art. PO Resp. 6–7, 17–18; Ex. 2001 ¶¶ 11, 15. Matsumura expressly states that its processing techniques can be applied to etching processes. *See* Ex. 1003, 10:3–7 (stating that its invention “can also be applied to any of the ion implantation, CVD, *etching* and *ashing* process” (emphasis added)). Although Dr. Flamm testifies that “Matsumura’s recipes would have been useless for performing any plasma etching” (Ex. 2001 ¶ 16), and that Matsumura does not teach anything about etching (*id.* ¶ 12), Dr. Flamm provides little or no support for these statements. Dr. Flamm’s conclusory opinions are not persuasive. Nor has Patent Owner provided any persuasive reasoning or evidence as to why Matsumura is directed to a different field of art. *See generally* PO Resp.; *see also* Tr. 40:13–24 (providing no argument that Matsumura is directed to a different field of art).

Rather, we credit Dr. Bravman’s testimony that a person of ordinary skill in the art would have known how to use the recipes and control circuits disclosed by Matsumura in common processing techniques, such as etching,

and would have been motivated to implement those techniques. *See* Ex. 1006 ¶¶ 71, 78, 89, 219, 229. Dr. Bravman testifies that Matsumura teaches a temperature control system for semiconductor processing that includes a computer programmed to control temperature, processing time, and temperature change time. *See* Ex. 1006 ¶¶ 72–73 (citing Ex. 1003, [57], Figs. 5A, 8–9). Dr. Bravman further testifies that Matsumura’s system includes a thermometer, a temperature sensor for a wafer stage, and a CPU to control the heating and cooling system, where the control system could take input from a user regarding heating and other conditions of the system. *See* Ex. 1006 ¶¶ 73–74 (citing Ex. 1003, Fig. 5A, 5:32–63, 5:67–6:9). Dr. Bravman testifies that, given common knowledge and the widespread use of preprogramed recipes, it was not necessary for Matsumura to provide a detailed explanation of how to implement its techniques in an etching process, and that a POSITA would have known how to use the recipes and control circuits disclosed by Matsumura in common processing techniques such as etching. *See id.* ¶¶ 79, 147–152; Ex. 1023 ¶ 19.

Patent Owner also argues that Kadomura and Matsumura teach away from the claimed subject matter of the ’264 patent because, *inter alia*, Kadomura teaches that the specific time interval for changing temperature “is of no[] importance” as the time needed to change the gas is longer than the time needed to change the temperature, Kadomura’s temperature change times of about 30 seconds are “relatively long” compared to those of “several seconds” in the ’264 patent, and Matsumura describes “adhesion and baking processes.” *See* PO Resp. 5–7 (citing Ex. 1001, 19:8–12, Fig. 10; Ex. 1005, 6:54, 8:42; Ex. 1003, 1:15–20, 4:56–59, , Figs. 1, 4; Ex. 2001 ¶ 10).

These arguments are not persuasive. A reference teaches away if it criticizes, discredits, or otherwise discourages the solution claimed. *See In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). In weighing the suggestive power of each reference, we must consider the degree to which one reference might accurately discredit another. *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991).

Patent Owner has not persuasively shown that any teachings in either Kadomura or Matsumura discredit, criticize, or discourage the subject matter claimed in the '264 patent. Nothing in Kadomura discourages the use of recipes to control the amount of time taken to change temperature during processing. Rather, Kadomura teaches the importance of ensuring that the time to change temperature is less than the time to change gases. As such, Kadomura does not discredit the use of a temperature change over a predetermined time. Additionally, that Kadomura teaches different time intervals for temperature changes does not teach away from the time intervals claimed in the '264 patent.

For the foregoing reasons, we find Petitioner has persuasively shown that the combination of Kadomura and Matsumura teaches the limitations of claim elements 56[e] and 60[f], and has articulated a reasonable rationale for combining the teachings of the cited art.

Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claim 56 would have been obvious over the combined teachings of Kadomura and Matsumura, and that the subject matter of claim 60 would have been obvious over the combined teachings of Kadomura, Matsumura, and Wang.

G. Asserted Obviousness of Independent Claim 56 over Muller and Matsumura and Independent Claim 60 over Muller, Matsumura, and Wang

Petitioner contends that claim 56 would have been obvious under 35 U.S.C. § 103(a) over the combined teachings of Muller and Matsumura, and that claim 60 would have been obvious over the combined teachings of Muller, Matsumura, and Wang.¹³ See Pet. 62–77, 82–84.

Patent Owner opposes, stating that Petitioner has failed to show a motivation to combine Muller, Matsumura, and Wang.¹⁴ PO Resp. 20. We have reviewed the arguments and evidence of record and determine that Petitioner has persuasively shown that the combination of Muller and Matsumura teaches the limitations of claim 56 and that the combination of Muller, Matsumura, and Wang teaches the limitations of claim 60. We further determine that Petitioner has articulated a reasonable rationale for combining the teachings of the cited art. See Pet. 58–67. We agree with and adopt Petitioner’s analysis. *Id.*

For example, with respect to independent claims 56 and 60, we find Muller teaches a method for etching wafers by varying substrate temperature during etching to shape openings in mask layers on wafers and deep trenches in wafers. *Id.* at 62, 82; Ex. 1002, 1:7–12, 1:44–55, 4:6–19, 4:51–63. Muller

¹³ Petitioner states claims 56–62 and 71 are being challenged over the combination of Muller, Matsumura, and Wang. See, e.g., Pet. 56. However, Petitioner does not address Wang in its arguments directed to claims 56–58. We address the challenges as they are set forth in the Petition, and consider claims 56–58 challenged over the combination of Muller and Matsumura.

¹⁴ Specifically, Patent Owner states that the combination of Muller, Matsumura, and Wang do not render claim 60 obvious. PO Resp. 20. Patent Owner did not make any arguments specifically directed to claim 56. See *id.*

discloses placing a substrate (wafer 104) on a substrate holder (electrostatic chuck 105). *See* Ex. 1002, 4:38–45, Fig. 4; Pet. 63–64, 82. We agree with Petitioner’s contention that Muller teaches setting and controlling wafer temperatures and that to the extent Muller does not explicitly teach sensing the temperature of the substrate holder, Matsumura makes up for any deficiency. Ex. 1002, 3:45–52, 4:64–5:25, 6:54–65, Fig. 3; Pet. 64, 83. Matsumura’s sensor 25 and thermometer 24 measure the temperature of the film and the substrate holder temperature is adjusted based on these measurements. Ex. 1002, 5:58–6:13, 8:25–35, 9:9–15, Fig. 5A; *see also* Pet. 64–65 (stating Matsumura’s control system 20 sets and adjusts substrate holder temperature based on sensor measurements). Dr. Bravman persuasively testifies that it would have been obvious to combine Matsumura’s substrate holder heater, temperature sensor, and control system with the chuck in Muller’s tool. Ex. 1006 ¶¶ 87–93, 219–220; Pet. 66–68. Dr. Bravman explains that wafer temperature must have been measured using a sensor during processing because wafer temperature was already tracked and plotted in Muller’s system, that adding a separate sensor for measuring substrate holder temperature would provide a mechanism of confirming accuracy, and that adding Matsumura’s heater and control circuit to Muller’s tool would have allowed for rapid heating and increased temperature with improved accuracy and greater precision. *See, e.g.*, Pet. 66–67 (citing Ex. 1006 ¶¶ 91, 221–222). We also agree with Petitioner that Muller teaches etching first silicon-containing layers 601 and 602 at a first temperature (e.g., 125°C or 145°C) and etching a second silicon-containing layer at a second temperature (e.g., 175°C or 195°C). We further agree with Petitioner’s showing that one of skill in the art would have used

Muller's multi-temperature process to achieve sloping sidewalls when etching an opening in a TEOS layer. *Id.* at 68–70; Ex. 1002, 4:12–32, Fig. 6C; Ex. 1006 ¶¶ 223–224. As persuasively explained by Petitioner, with supporting testimony from Dr. Bravman, it would have been obvious to use Matsumura's control system with the predetermined recipes in Muller's tool to ensure that Muller's wafer temperature change happened within a predictable, preselected time period, and to ensure accuracy. Pet. 68–77.

With respect to independent claim 60, Petitioner also relies upon the teachings of Wang. For example, Petitioner asserts that it would have been obvious to etch Wang's wafer (which includes a silicide layer) at a first substrate temperature at 90°C and at a second substrate temperature at 140°C in the Muller-Matsumura system in view of, *inter alia*, Muller's teaching to use its tool to etch silicon-containing wafer layers, to increase etching rate and throughput, and as a simple design choice. *See, e.g., id.* at 79–84.

We are not persuaded by Patent Owner's statement that Petitioner "did not even attempt to discharge [its] burden of proving that a [POSITA] would have a motivation to combine Muller, Matsumura, and Wang." PO Resp. 20. As stated above, we are persuaded by Petitioner's argument that a POSITA would have combined Muller and Matsumura to, *inter alia*, improve Muller's system by increasing control, efficiency, accuracy, and predictability, and to expand the system's capabilities. *See* Pet. 67–68, 70–72. Additionally, we agree with Petitioner's argument, supported by the un rebutted testimony of Dr. Bravman, that a POSITA would have been motivated to etch Wang's wafer layer stack in the combined system of Muller and Matsumura to leverage the advantages of that system (e.g., quick

temperature changes, increased throughput). *Id.* at 80–81 (citing Ex. 1006 ¶¶ 107–109, 229, 250).

Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that claim 56 would have been obvious over Muller and Matsumura, and that claim 60 would have been obvious over Muller, Matsumura, and Wang.

*H. Asserted Obviousness of Dependent Claim 57 over
Kadomura, Matsumura, and Muller*

Claim 57 depends from claim 56 and further requires that “the change from the first substrate temperature to the second substrate temperature occurs within less than about 5 percent of the total etching process time.” Petitioner argues that claim 57 would have been obvious over the combined teachings of Kadomura, Matsumura, and Muller. *See* Pet. 44–48. Patent Owner opposes, contending that a POSITA would not have combined the teachings of Kadomura with Muller. *See* PO Resp. 20–21.

We have reviewed Petitioner’s arguments and evidence, and determine that Petitioner has shown where each of the limitations of claim 57 is taught or suggested by the asserted art, and has articulated a sufficient rationale for combining the teachings of Kadomura, Matsumura, and Muller. *See* Pet. 44–48; Ex. 1006 ¶¶ 159–163. We agree with and adopt Petitioner’s analysis. *Id.*

For example, as noted above, we agree with Petitioner that the combination of Kadomura and Matsumura teaches the limitations of claim 56. *See supra* Section II.F. We also agree with Petitioner’s undisputed assertion that Matsumura teaches a temperature change that “occurs within less than about 5 percent of the total etching process time” as recited in

claim 57. See Pet. 44–45 (stating Matsumura teaches a “430 second” two-step etching process and that the temperature change between the two processes occurs “within several seconds,” which is less than 5% of the total etching time); Ex. 1002, 5:30–35; Ex. 1006 ¶ 159. We also agree with Petitioner that it would have been obvious to incorporate Muller’s continuous etch approach and backpressure temperature control design in the Kadomura-Matsumura system to make temperature changes more rapid and increase throughput, a stated aim of Kadomura. Pet. 45 (citing Ex. 1006 ¶¶ 97–100, 161–162). Petitioner argues, supported by the unrebutted testimony of Dr. Bravman, that although Kadomura describes interrupting its etch processes to exhaust the etching gas between steps, gas exhaustion is not necessary when the same etching gas is used for two steps. *Id.* at 45–46; Ex. 1006 ¶¶ 42, 162; Ex. 1005, 6:24–7:2.

Patent Owner asserts that a POSITA “would not combine Kadomura, *which teaches exhausting the etching gas between etching steps*, and changing the temperature during the time used to exhaust the gas, with the continuous process of Muller.” PO Resp. 20 (citing Ex. 2001 ¶ 16) (emphasis added). We are not persuaded by this argument because it does not address Petitioner’s contention, supported by the testimony of Dr. Bravman, that a POSITA would have applied Muller’s teachings to Kadomura “and continuously etched the substrate while changing between two temperatures *without exhausting the etching gas*.” Ex. 1006 ¶ 162 (emphasis added). We credit Dr. Bravman’s testimony that although it was well known in the art that processing gas and residue could be removed and replaced between processing steps by exhausting gas, it was also known that “between certain steps, the gas in the chamber might not be exhausted.” *Id.*

¶ 42 (citing Ex. 1004, 1:56–2:3, 7:47–8:14; Ex. 1002, 3:45–55, 5:17–25, 5:58–62). We also credit Dr. Bravman’s testimony that Kadomura teaches using the same gas in its first example for both processing steps and that increased throughput is beneficial. *Id.* ¶ 162 (citing Ex. 1005, 3:19–22, 4:46–54, 5:18–26, 6:24, 6:55–62, 7:2, 7:19–30). We further credit Dr. Bravman’s testimony that in order to further increase throughput in Kadomura’s first embodiment, a POSITA would have applied Muller’s teachings and continuously etched the substrate while changing between two temperatures without exhausting the etching gas. *Id.* (stating that it would have been obvious and straightforward to continuously etch the substrate without exhausting the gas “particularly given that the etching gas is the same for both steps”).

Patent Owner also contends that Muller “relates to a deep trench etching process, which would be compromised and not work, if combined with the multi-step process of Kadomura.” PO Resp. 20 (citing Ex. 2001 ¶ 16). Patent Owner states “Muller specifically emphasizes ‘etch profile shaping through variations of wafer temperature during etching . . . for all etch processes involving a side wall passivation film where the deposition of the passivation film is temperature dependent,’ (Ex. 1002 Figures 6A-6C and accompanying text) which would be inoperable *with Kadomura’s teaching of exhausting the gas during processing* according to a PHOSITA (*Id.* ¶16).” PO Resp. 20–21 (emphasis added).

We disagree with these arguments because Patent Owner does not explain adequately how the combination would have compromised or rendered inoperable Muller’s process. See PO Resp. 20–21; Ex. 2001 ¶ 16. To the extent Patent Owner is asserting Muller’s deep trench etching process

would not work if combined with a process that requires gas exhaustion during processing, this argument does not overcome Petitioner's obviousness showing because it does not address Petitioner's argument that gas exhaustion is not a required step.

Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that dependent claim 57 would have been obvious over Kadomura, Matsumura, and Muller.

I. Asserted Obviousness of Dependent Claim 63

Claim 63 depends from claim 60 and further requires "the first substrate temperature is changed to the second substrate temperature by transferring energy using at least radiation." Petitioner asserts that claim 63 would have been obvious over the combined teachings of Kadomura, Matsumura, Wang, and Kikuchi (Pet. 58–60), as well as over the combined teachings of Muller, Matsumura, Wang, and Kikuchi (Pet. 88–90). Patent Owner opposes, contending "Kikuchi teaches away from Muller's and Kadomura's processes by using infrared lamps to heat a wafer." PO Resp. 21–22.

We have reviewed the arguments and evidence of record and determine that Petitioner has persuasively shown that the combination of Kadomura, Matsumura, Wang, and Kikuchi, as well the combination of Muller, Matsumura, Wang, and Kikuchi, teaches the limitations of claim 63. We further determine that Petitioner has articulated a reasonable rationale for combining the teachings of the cited art. *See* Pet. 58–60, 88–90. We agree with and adopt Petitioner's analysis. *Id.*

For example, we agree with Petitioner that Kikuchi teaches the limitations recited in claim 60 by disclosing the use of infrared lamps to heat the wafer and change the wafer temperature from 70°C–160°C to 200°C in 5 seconds. *See id.* at 58–60, 88–80 (citing Ex. 1004, 2:37–46, 7:62–68; Ex. 1006 ¶ 205). We also agree with Petitioner’s contention, supported by testimony of Dr. Bravman, that it would have been obvious to one skilled in the art to use Kikuchi’s infrared lamps in either the Kadomura-Matsumura system or in the Muller-Matsumura system to heat a wafer more quickly, to give the system more flexibility, and to increase throughput. *See* Pet. 59–60, 89–90; Ex. 1006 ¶¶ 116–119, 205, 206. We also agree with Petitioner’s undisputed assertion that it was well known in the art that heat lamps and chuck heaters were both acceptable heat sources for etching tools. *See* Pet. 59–60, 89–90 (citing Ex. 1013, 3:15–18). We further agree with Petitioner’s argument, supported by the undisputed testimony of Dr. Bravman, that using Kikuchi’s lamp together with either Kadomura’s heater or Matsumura’s heater would have heated the wafer more quickly than using the heater alone. *See* Pet. 60, 90; Ex. 1006 ¶¶ 118, 122, 206, 268; Ex. 1005, 5:18–26, 7:19–30.

We do not agree with Patent Owner’s argument that Kikuchi teaches away from the invention recited in claim 63. *See* PO Resp. 21. Patent Owner fails to specifically identify any disclosure of Kikuchi that criticizes, disparages, or discourages changing substrate temperature using radiation. Reply 20; *see Para-Ordnance Mfg., Inc. v. SGS Importers Int’l, Inc.*, 73 F.3d 1085, 1090 (Fed. Cir. 1995) (holding that to teach away, a reference must state that a feature “should not” or “cannot” be used in combination with other features in the prior art). Patent Owner asserts that Kikuchi uses

supports that move the substrate both away from and into contact with the heating source. PO Resp. 21. That Kikuchi moves a substrate in relation to the heat source does not teach away from use of radiation, such as from infrared lamps, to heat a substrate.

We also do not find Dr. Flamm's supporting testimony on this issue to be persuasive. Ex. 2001 ¶ 18. Dr. Flamm's analysis essentially repeats the arguments advanced in the Patent Owner Response and does not adequately explain how Kikuchi teaches away from the method of changing temperature as recited in claim 63. For these reasons, we do not credit his testimony that claim 63 would have been patentable over the asserted art.

Rather, we credit Dr. Bravman's testimony that "it was known in the prior art to use heat lamps and substrate holder-based means to vary temperature together in a single processing apparatus." Ex. 1023 ¶ 64 (citing Ex. 1012, Fig. 1, 3:7–10, 3:37–50; Ex. 1006 ¶¶ 117, 121, 206, 268). We also credit Dr. Bravman's testimony that Kikuchi, Muller, and Kadomura all teach multi-temperature etching processes and that a POSITA would have combined the references because they all relate to the same general subject matter of multi-temperature etching processes. Ex. 1023 ¶ 61.

Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that dependent claim 63 would have been obvious over the combined teachings of Kadomura, Matsumura, Wang, and Kikuchi, as well as over the combined teachings of Muller, Matsumura, Wang, and Kikuchi.

J. Asserted Obviousness of Dependent Claims 57–59, 61, 62, 70, and 71 over Various Combinations of Kadomura, Muller, Matsumura, Kikuchi, and Wang

Petitioner argues that claim 58 would have been obvious over the combined teachings of Kadomura and Matsumura; that claims 59, 61, and 71 would have been obvious over the combined teachings of Kadomura, Matsumura, and Wang; that claim 62 would have been obvious over the combined teachings of Kadomura, Matsumura, Muller, and Wang; and that claims 63 and 70 would have been obvious over the combined teachings of Kadomura, Matsumura, Kikuchi, and Wang. *See* Pet. 43–52, 56–61.

Petitioner also argues that claims 57–58 would have been obvious over the combined teachings of Muller and Matsumura, and that claims 59, 61, 62, and 71 are unpatentable over the combined teachings of Muller, Matsumura, and Wang. *See* Pet. 77–82, 84–88.

Other than the arguments discussed above, Patent Owner does not separately address Petitioner’s explanations and supporting evidence with respect to these dependent claims. *See* PO Resp. 22.

We have reviewed Petitioner’s unchallenged arguments and evidence, and determine that Petitioner has shown where each of the limitations of the dependent claims are taught or suggested by the asserted art and has articulated a sufficient rationale for combining the teachings of the prior art. *See* Pet. 43–52, 56–61, 77–82, 84–88. We agree with and adopt Petitioner’s analysis. *Id.*

For example, we agree with Petitioner’s argument that Kadomura teaches the “chlorine-containing ambient” limitations of claims 58 and 59 because each of Kadomura’s two-step examples use a chlorine-containing etching gas. *See* Ex. 1005, 6:24, 7:2, 8:10, 8:58, 9:58, 10:23; Pet. 43. We are

also persuaded by Petitioner’s undisputed argument, supported by Dr. Bravman’s un rebutted testimony, that it would have been obvious to use a chlorine-containing etching gas in Muller’s tool because chlorine was well known and often used in etching, because Muller teaches using bromine etching gas, because it was well known in the art to use chlorine and bromine together to increase etching selectivity, and because determining which gas to use would have been a matter of routine optimization. Ex. 1006 ¶ 248; Pet. 78–79.

With respect to claim 61, which further requires that the substrate temperature is changed “by at least heat transfer to the substrate using at least an electrostatic chuck,” both Kadomura and Muller teach using an electrostatic chuck. Kadomura’s stage 12 includes an electrostatic chuck with a heater that rapidly heats the wafer. *See* Ex. 1005, 6:30–35, 8:17–23, 10:7–10, 11:42–47. Muller teaches electrostatic chuck 105, which is used to support the wafer. *See* Ex. 1002, 4:39–43. We are persuaded by Petitioner’s undisputed argument that it would have been obvious to incorporate Matsumura’s stage heater into Muller’s tool to change wafer temperature by transferring heat from Muller’s substrate holder stage to the wafer, which would allow for more rapid heating and increased temperature control. *See* Pet. 66–68, 84–85 (citing Ex. 1006 ¶¶ 220, 263–264; Ex. 1003, 5:42–45, 6:56–57, 7:11–15).

In addition, we agree that Muller’s heat transfer system based on gas pressure behind the substrate (wafer) teaches the limitation of claim 62 requiring that substrate temperature is changed by “transferring heat using at least a pressure of a gas behind the substrate.” *See id.* at 86–87 (citing Ex. 1002, 4:51–55, 5:13–25, Fig. 4). We also agree with Petitioner that

selecting etching temperatures, such as those recited in claims 70 and 71, was a matter of routine optimization. *See id.* at 62–72, 87–88, 91–92.

Therefore, based on the record developed during trial, we conclude that Petitioner has demonstrated by a preponderance of the evidence that dependent claims 57–59, 61, 62, 70, and 71 would have been obvious over the asserted art.

III. CONCLUSION

Based on the evidence and arguments, Petitioner has demonstrated by a preponderance of the evidence that:

(1) claims 56 and 58 are unpatentable under 35 U.S.C. § 103(a) over the combination of Kadomura and Matsumura;

(2) claim 57 is unpatentable under § 103(a) over the combination of Kadomura, Matsumura, and Muller;

(3) claims 59–61 and 71 are unpatentable under § 103(a) over the combination of Kadomura, Matsumura, and Wang;

(4) claim 62 is unpatentable under § 103(a) over the combination of Kadomura, Matsumura, Muller, and Wang;

(5) claims 63 and 70 are unpatentable under § 103(a) over the combination of Kadomura, Matsumura, Kikuchi, and Wang;

(6) claims 56–58 are unpatentable under § 103(a) over the combination of Muller and Matsumura;

(7) claims 59–62 and 71 are unpatentable under § 103(a) over the combination of Muller, Matsumura, and Wang; and

(8) claims 63 and 70 are unpatentable under § 103(a) over the combination of Muller, Matsumura, Wang, and Kikuchi.

IV. ORDER

Accordingly, it is

ORDERED that claims 56–63, 70, and 71 of U.S. Patent No. RE40,264 E are held to be unpatentable;

FURTHER ORDERED that, because this Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent RE40,264 E

For PETITIONER:

Jonathan McFarland
Tyler Bowen
Daniel Keese
PERKINS COIE LLP
jmcfarland@perkinscoie.com
tbowen@perkinscoie.com
dkeese@perkinscoie.com

Jeremy Jason Lang
WEIL, GOTSCHAL & MANGES LLP
jason.lang@weil.com

David M. Tenant
Nathan Zhang
WHITE & CASE LLP
dtenant@whitecase.com
nathan.zhang@whitecase.com

For PATENT OWNER:

Justin J. Lesko
LAW OFFICES OF STEVE G. LISA, LTD.
justinlesko@patentit.com

Rolf O. Stadheim
STADHEIM & GREAR
stadheim@stadheimgear.com