

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

Case IPR2017-00381
Patent 7,886,122 B2

Before SALLY C. MEDLEY, BARBARA A. PARVIS, and
MONICA S. ULLAGADDI, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. The evidentiary standard is a preponderance of the evidence. *See* 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). For the reasons that follow, we determine that NVIDIA Corporation (“Petitioner”) has shown by a preponderance of the

evidence that claims 1–23 and 28 of U.S. Patent No. 7,886,122 B2 (Ex. 1001, “the ’122 Patent”) are unpatentable. Petitioner has not shown by a preponderance of the evidence that claims 24–27 of the ’122 Patent are unpatentable.

A. *Background*

Petitioner filed a Petition for *inter partes* review of claims 1–28 (“the challenged claims”) of the ’122 Patent. Paper 2 (“Pet.”). Polaris Innovations Limited (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). Pursuant to 35 U.S.C. § 314, we instituted trial on all challenged claims, but not on all challenged grounds. See Paper 9 (Inst. Dec.), 26–27.¹

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 18, “PO Resp.”), to which Petitioner filed a Reply (Paper 21, “Pet. Reply”). Patent Owner filed a Motion for Observation, Paper 25 (“PO Mot. Obs.”) and Petitioner filed a Response to the Motion for Observation, Paper 29 (“Pet. Resp.”). A transcript of the hearing held on March 8, 2018 has been entered into the record as Paper 32 (“Tr.”).

Following the hearing, on April 24, 2018, the Supreme Court held that a decision to institute under 35 U.S.C. § 314 may not institute on less than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018). In light of the *Guidance on the impact of SAS on AIA trial proceedings* posted on April 26, 2018 (at

¹ Patent Owner filed a Request for Rehearing of the Decision to Institute (Paper 12, “Reh’g Req.”), which we denied (Paper 15, “Dec. on Reh’g Req.”).

<https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial>), we modified our Institution Decision to institute on all the challenged claims and all the grounds presented in the IPR2017-00381 Petition (Paper 2). *See* Paper 35 (“DI Supp.”). We also granted the parties’ joint request for additional briefing. *Id.* On May 18, 2018, Patent Owner filed a supplemental brief pertaining to only the previously non-instituted ground (Paper 36, “PO Supp. Br.”) and on May 25, 2018, Petitioner filed a supplemental brief responsive to Patent Owner’s submission (Paper 37, “Pet. Supp. Br.”).

B. Related Matters

The parties state that the ’122 Patent is the subject of a pending lawsuit that includes assertions against Petitioner. Pet. 100; Paper 4 (“PATENT OWNER’S INITIAL MANDATORY NOTICES”) (hereinafter “PO Init. Mand. Not.”), 2–3; Paper 23 (“PETITIONER’S UPDATED MANDATORY NOTICES”) (hereinafter “Pet. Updated Mand. Not.”), 2. The parties identify a lawsuit pending in the Northern District of California, i.e., *Polaris Innovations Ltd. v. Dell Inc.*, Case No. 4:16–cv-07005 (N.D. Cal.).² PO Init. Mand. Not. 2–3; Pet. Updated Mand. Not. 2.

² This lawsuit is referred to herein as the “companion district court lawsuit.” The companion district court lawsuit was transferred from the United States District Court for the Western District of Texas on December 5, 2016. *Id.* That case was *Polaris Innovations Ltd. v. Dell Inc.*, Case No. 5:16–cv-00451 (W.D. Tex). *Id.*

B. The '122 Patent

The '122 Patent is directed to clock signals used in memory devices.
Ex. 1001, 1:8–10. Figure 1 of the '122 Patent is reproduced below.

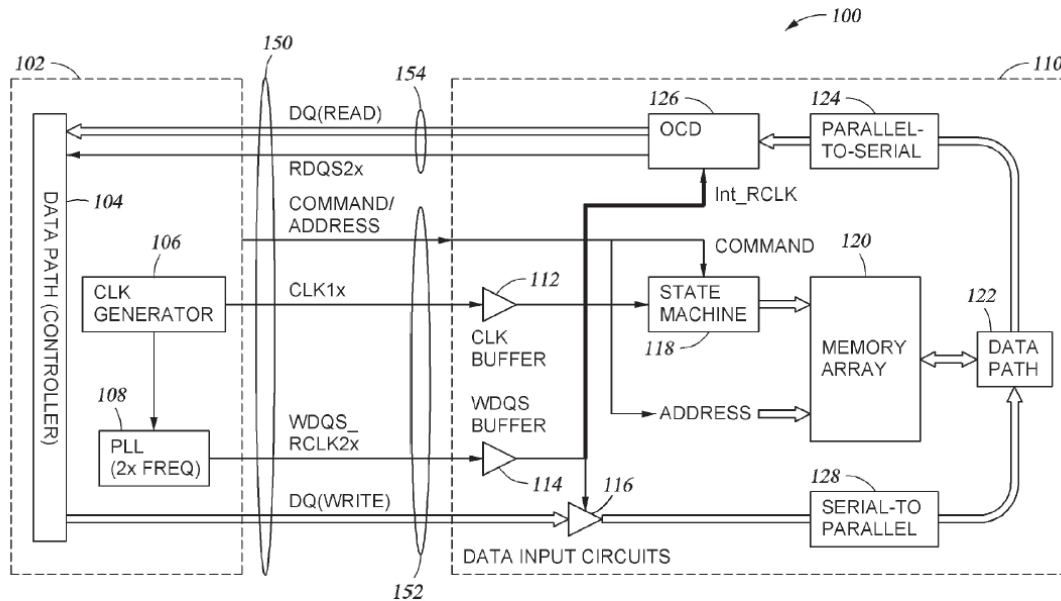


Fig. 1

Figure 1 of the '122 Patent, reproduced above, illustrates a block diagram of system 100 having memory device 110 and control device 102, as well as interface 150 between control device 102 and memory device 110. *Id.* at 3:37–43.

Control device 102 provides first clock signal (CLK1x), second clock signal (WDQS_RCLK2x), command and address signals (COMMAND/ADDRESS), and write data signal (DQ(WRITE)) to memory device 110. *Id.* at 3:64–4:4. Memory device 110 provides read clock signal (RDQS2x) and read data signal (DQ(READ)) to control device 102. *Id.* at 4:5–6.

C. Illustrative Claim

Petitioner challenges claims 1–28 of the ’122 Patent. Pet. 1. Claims 1, 9, 16, 20, 24, and 28 are independent claims. Claims 2–8, 10–15, 17–19, 21–23, and 25–27 depend, directly or indirectly, from claims 1, 9, 16, 20, or 24. Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A method for transmitting clock signals, the method comprising:

receiving, at a memory device, a first clock signal and a second clock signal, wherein a frequency of the first clock signal is less than a frequency of the second clock signal;

performing two or more data access operations using the second clock signal, wherein at least one of the two or more data access operations includes a read operation and wherein at least one of the two or more data access operations includes a write operation; and

performing a command processing operation using the first clock signal.

Id. at 7:55–67.

D. Instituted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 1–2):

Reference(s)	Basis	Challenged Claim(s)
Lee ³	§ 102(b)	1, 5, 6, 8, 9, 13, 14, 16, 20, and 24
Lee	§ 103(a)	2–4, 10–12, 17–19, 21–23, and 25–28
Lee and Yoo ⁴	§ 103(a)	2–4, 10–12, 17–19, 21–23, and 25–28

³ U.S. Patent No. 6,496,445 B2, issued Dec. 17, 2002 (Ex. 1004) (“Lee”).

⁴ U.S. Patent No. 6,477,110 B2, issued Nov. 5, 2002 (Ex. 1006) (“Yoo”).

Reference(s)	Basis	Challenged Claim(s)
Lee and Kyung ⁵	§ 103(a)	2, 3, 10, 11, 17, 18, 21, 22, 25, 26, and 28
Lee and Gould ⁶	§ 103(a)	7 and 15

Petitioner offers Declarations of Bruce Jacob, Ph.D. (Ex. 1003; Ex. 1011). Patent Owner offers a Declaration of Steven A. Przybylski, Ph.D. (Ex. 2003). We initially instituted on all challenged claims and modified our initial Institution Decision to subsequently include all grounds presented in the Petition. Inst. Dec. 26–27; DI Supp. 2–3.

II. DISCUSSION

A. *Claim Construction*

In the Petition, Petitioner provides proposed claim constructions for “means for storing data” and “means for interfacing a control device” recited in claim 24. Pet. 11–13. Petitioner contends, “[a]ll remaining terms should be given their broadest reasonable ordinary meaning.” *Id.* at 11.

Patent Owner argues: (1) “[r]ather than stretching the meaning of the phrase ‘memory device’ to encompass a memory module or board,” the term should be interpreted “to mean a memory integrated circuit” (PO Resp. 20); and (2) “the phrases ‘read operation’ and ‘write operation’ should be interpreted as getting data from and placing data in, respectively, a memory array” (*id.* at 25). Patent Owner also contends that it does not dispute Petitioner’s contentions regarding the means-plus-function limitations

⁵ U.S. Patent Application Publication No. 2005/0047246 A1, published Mar. 3, 2005 (Ex. 1005) (“Kyung”).

⁶ U.S. Patent No. 7,571,297 B2, issued Aug. 4, 2009, filed Dec. 30, 2005 (Ex. 1007) (“Gould”).

recited in claim 24, because the Petition does not show that Lee discloses the “means for interfacing a control device” recited in claim 24 “as the petition has interpreted that limitation.” *Id.* at 22. In its Reply, Petitioner responds to Patent Owner’s contentions regarding the meanings of the terms “memory device” and “read” and “write” operations. Pet. Reply 3–14. Below, we address the parties’ disputes regarding the meanings of the terms “memory device,” “read operation,” and “write operation,” as well as Petitioner’s contentions for “means for interfacing a control device” recited in claim 24.

1. *Principles of Law*

Only those terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). A claim in an unexpired patent that will not expire before a final written decision is issued shall be given its broadest reasonable construction in light of the specification of the patent in which it appears. *See* 37 C.F.R. § 42.100.⁷ We interpret the claim terms of the ’122 Patent according to their ordinary and customary meaning in the context of the patent’s written description. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). An inventor is entitled to be his or her own lexicographer of patent claim terms by providing a definition of the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

⁷ We further note that our determinations regarding claim construction in the instant proceeding are the same under a district court-type claim construction approach.

Limitations with the language “means” or “means for” are presumed to invoke 35 U.S.C. § 112 ¶ 6.⁸ *See Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348–49 (Fed. Cir. 2015) (en banc in relevant part) (“use of the word ‘means’ [in a claim element] creates a presumption that § 112, ¶ 6 applies”); *see also In re Donaldson Co., Inc.*, 16 F.3d 1189, 1193 (Fed. Cir. 1994) (“[P]aragraph six applies regardless of the context in which the interpretation of means-plus-function language arises, i.e., whether as part of a patentability determination in the PTO or as part of a validity or infringement determination in a court”). The sixth paragraph of 35 U.S.C. § 112 provides that “[a]n element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.” Where a challenged claim contains a means-plus-function limitation under 35 U.S.C. § 112, sixth paragraph, the Petitioner “must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function.” 37 C.F.R. § 42.104(b)(3).

⁸ Section 4(c) of the Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) (“AIA”) re-designated 35 U.S.C. § 112 ¶ 6, as 35 U.S.C. § 112(f). Because the ’122 Patent has a filing date before September 16, 2012, the effective date of § 4(c) of the AIA, we will refer to the pre-AIA version of 35 U.S.C. § 112.

2. “memory device,” “read operation,” and “write operation”
(Independent Claims 1, 9, 16, 20, 24, and 28)

We turn to Patent Owner’s contentions regarding “memory device,” “read operation,” and “write operation,” recited in the independent claims. Starting with the term “memory device,” Patent Owner contends that “‘memory device’ in the memory art is a memory integrated circuit (IC),” which also is “referred to in the art as a ‘chip.’” PO Resp. 15. Based on the entire trial record we can accept Patent Owner’s proposed construction that “memory device” means a “memory integrated circuit (IC)” or a memory “chip” (*id.*) because we are persuaded by Petitioner’s contentions, even under Patent Owner’s proposed construction. *See Vivid Techs.*, 200 F.3d at 803 (Fed. Cir. 1999) (“[O]nly those [claim] terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy”).

More specifically, in its analysis of the asserted prior art discussed *infra* in Section II.D.2, Petitioner points to a memory device that is the same as the example in the ’122 Patent, i.e., a dynamic random access memory (DRAM), as well as disclosure that this device is a *memory chip*. Pet. 14–16, 19–22, 24, 38, 40–43, 49 (citing, *e.g.*, Ex. 1003 ¶¶ 103, 136–139, 148–172; Ex. 1004, 3:38–52, 6:41–67, 7:27–35, 8:59–62, Figs. 4, 5). The ’122 Patent describes that “memory device 110 may also include any type of memory device . . . [f]or example, in one embodiment, the memory device

may be a volatile memory device such as *a dynamic, random access memory (DRAM) device*.” Ex. 1001, 3:50–59 (emphasis added).⁹

We now turn to the meaning of the terms “read operation” and “write operation.” Neither party contends that these terms have any special meaning or that the ’122 Patent provides a lexicographical definition of the terms. Indeed, Patent Owner contends its proposed construction is dictated by the understanding of those skilled in the memory art, relying on the testimony of Dr. Przybylski. PO Resp. 25–26. In particular, Dr. Przybylski testifies that “the LP DDR SDRAM standard” describes a “write operation as comprising the flow of data into the memory array” and “[t]he same applies to read operations.” *Id.* (citing Ex. 2003 ¶¶ 46–48). Dr. Przybylski also testifies that this standard provides further details regarding “transferring data to/from the memory array, an active row, or one of the banks in the memory array” and “the prior art DDR SDRAM JEDEC standard contains similar references.” Ex. 2003 ¶ 48.

Patent Owner’s proposed construction is that “read operation” and “write operation” mean “accessing data from a memory array” and “placing

⁹ Although we do not need to reach Patent Owner’s argument that the “memory device” is a single integrated circuit or chip, we note that we are persuaded by Petitioner’s contention that Patent Owner’s construction is too narrow in view of the ’122 Patent’s description that “memory device 110 may also include *any* type of memory device.” Ex. 1001, 3:50–59 (emphasis added). Patent Owner relies on extrinsic evidence (*e.g.*, Lee and Kyung), as well as the ’122 Patent’s mention of DRAM IC standards, which allow the “memory device” at least to comprise multiple DRAMs or chips. PO Resp. 14–20. Contrary to Patent Owner’s contention (*id.* at 16 n.1), we need not determine if system board 400 is a “memory device” because Petitioner’s alternate contention pertains to Lee’s memory module 420 comprising multiple DRAMs.

data in a memory array,” respectively. PO Resp. 22; *see also id.* at 25 (“[T]he phrases ‘read operation’ and ‘write operation’ should be interpreted as getting data from and placing data in, respectively, a memory array.”) Independent claims 1, 9, 20, and 28 recite “memory device,” but not “memory array.” Patent Owner directs us to the ’122 Patent Specification, explaining that “[c]laims are not interpreted in a vacuum, but are part of and read in light of the specification.” PO Resp. 23–25 (quoting *Slimfold Mfg. Co. v. Kinkead Indus., Inc.*, 810 F.2d 1113, 1116 (Fed. Cir. 1987)). Patent Owner, however, does not explain why we should import “memory array” into claims 1, 9, 20, and 28, which recite “memory device,” but not “memory array.” As explained above, for the patentability determinations before us, we can accept Patent Owner’s proposed construction for “memory device,” because Petitioner’s showing is sufficient even under Patent Owner’s construction. In particular, Petitioner points to a *dynamic random access memory (DRAM) device* in its analysis of the asserted prior art discussed *infra* in Section II.D.2, which is the same as an example in the ’122 Patent Specification.

Patent Owner also contends that, “[a] ‘read operation’ or ‘write operation’ includes more than just data transfers onto or off of the memory device” because “a ‘memory device’ of the kind referred to in the claims—an IC that accepts data, addresses, and commands and is the subject of ‘read operations’ and ‘write operations’—stores the data at specific locations in a memory array and retrieves data from specific locations in the memory array.” PO Resp. 23. That those skilled in the memory art would have known that certain memory devices operated in a manner set forth in prior art standards documents, for example, “the LP DDR SDRAM standard” and

“the prior art DDR SDRAM JEDEC standard” (Ex. 2003 ¶¶ 46–48) does not mean that a person having ordinary skill in the art would have understood the terms “read operation” and “write operation” to require that operation.¹⁰

We, instead, agree with Petitioner that Patent Owner’s proposed constructions for terms “read operation” and “write operation” “improperly inject ‘a memory array’ into the claimed operations.” Pet. Reply 3. Accordingly, we determine that “read operation” and “write operation” mean “getting data from” and “placing data in,” respectively, a memory device.

3. *“means for interfacing a control device” (Independent Claim 24)*

Petitioner contends that the “means for interfacing a control device” recited in claim 24 “is governed by 35 U.S.C. § 112 ¶ 6.” Pet. 12. Petitioner contends:

Here, the recited function is “interfacing a control device.” The corresponding structure for performing the function “interfacing a control device” is “memory interface 150,” which is depicted in FIG. 1 “between the control device 102 and the memory device 110.” NVIDIA-1001, 3:41–64. As shown in FIG. 1, “the control device 102 may communicate to the memory device 110 across a memory interface 150.” NVIDIA-1001, 3:60–61.

Pet. 13.

Petitioner, additionally, provides annotations to Figure 1 of the ’122 Patent highlighting interface 150 in yellow.

¹⁰ The Petition need not specify where the asserted reference discloses details set forth in prior art DRAM standards, just because the specification describes DRAM memory as exemplary.

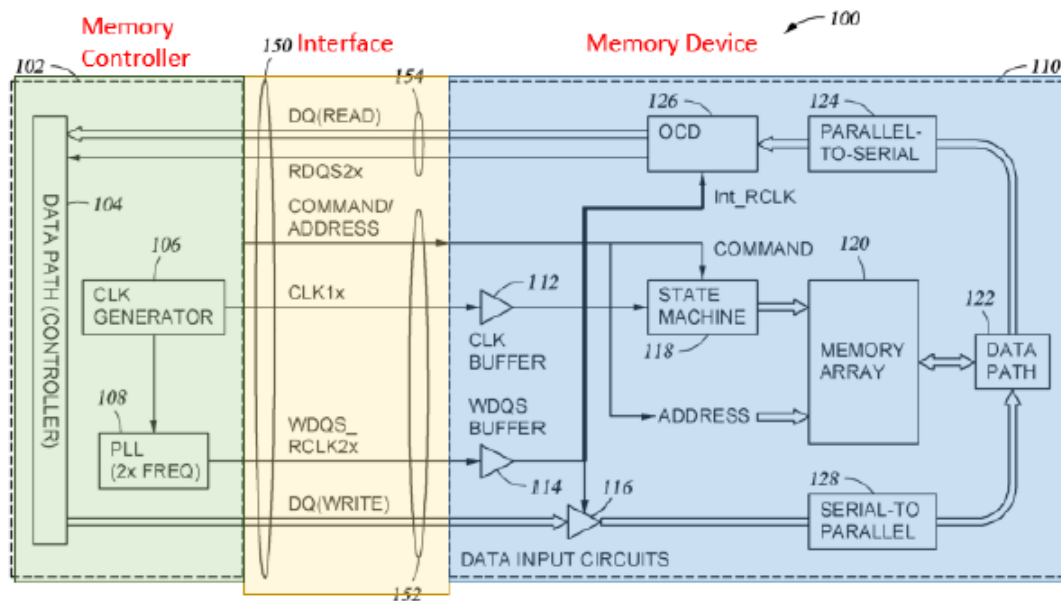


Fig. 1

Figure 1 of the '122 Patent, reproduced above with Petitioner's annotations, is a block diagram depicting system 100 that includes memory device 110, highlighted in blue, control device 102, highlighted in green, and interface 150, highlighted in yellow, between control device 102 and memory device 110. Pet. 13; Ex. 1001, 2:39–41, 3:37–43, Fig. 1.

Relying on the testimony of Dr. Jacob, Petitioner also contends “[t]hus, ‘means for interfacing a control device’ should be construed to require the function of ‘interfacing a control device’ performed by the structure of ‘a memory interface.’” *Id.* (citing Ex. 1003 ¶ 26). Dr. Jacob testifies that the “corresponding structure for performing the function ‘interfacing a control device’ is the interface 150, depicted in the '122 [P]atent in Fig. 1.” Ex. 1003 ¶ 26.

Patent Owner contends it does not dispute Petitioner's identification, but instead disputes that Petitioner shows, with respect to claim 24, the prior art teaches the limitation as Petitioner has construed it. See PO Resp. 22.

In its Reply, Petitioner contends “Polaris misinterprets NVIDIA’s construction as requiring **all** signals (including RDQS2x) shown in FIG. 1 of the ’122 Patent.” Pet. Reply 14. Petitioner contends that it “identifies the structure of a memory interface, which does not include the intangible signals exchanged through that interface,” “the RDQS2x signal is not a ‘structural element,’” and further that “the RDQS2x signal is not required to perform the corresponding function.” *Id.* at 15–16. Petitioner also contends that requiring “the RDQS2x signal would make dependent claim 25 entirely redundant.” *Id.* at 16. During the hearing, Petitioner argued that its proposed construction does “not necessarily limit[] [the structure] to memory interface 150.” Tr. 9:6–15.

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts *described in the specification and equivalents thereof*.

35 U.S.C. § 112, ¶ 6 (emphasis added). The only structure described in the specification identified by Petitioner in the Petition is memory interface 150. Pet. 12–13. Petitioner’s single sentence referring to “the structure of ‘a memory interface’” (*id.* at 13 (citing Ex. 1003 ¶ 26)) does not identify with sufficient specificity structure in the ’122 Patent Specification. Petitioner cites to only Dr. Jacob’s testimony and Dr. Jacob testifies that the “corresponding structure for performing the function ‘interfacing a control device’ is the interface 150, depicted in the ’122 [P]atent in Fig. 1.” Ex. 1003 ¶ 26. We need not make a determination regarding Petitioner’s assertion that the RDQS2x signal is intangible and not a structural element (Pet. Reply 14–16) because the ’122 Patent Specification describes structure

with respect to the memory interface 150 that is not accounted for by Petitioner. In particular, the '122 Patent Specification describes that the off-chip driver (OCD) 126 transmits this data over a line to control device 102 (*see, e.g.*, Ex. 1001, 4:35–38, 5:33–36, Fig. 1). Although the '122 Patent Specification refers to “single data bus line (DQ)” embodiments, the '122 Patent Specification does not indicate that these are illustrated in Figure 1 or that they are equivalent to interface 150 and, instead, describes these embodiments as more limited in that read and write operations cannot be performed simultaneously. Ex. 1001, 4:7–12.

We agree with Petitioner’s identification of the recited function, i.e., “interfacing a control device” and corresponding structure for performing the function, i.e., “memory interface 150,” which is depicted in FIG. 1 “between the control device 102 and the memory device 110.” Pet. 13. Patent Owner does not dispute those contentions. PO Resp. 22. We, however, are not persuaded that the corresponding structure described in the '122 Patent Specification may be something other than memory interface 150, as Petitioner has not identified that other structure with sufficient specificity in the Petition.

Accordingly, we determine that the recited function of “means for interfacing a control device” is “interfacing a control device” and the corresponding structure for performing the function is “memory interface 150,” which is depicted in FIG. 1 “between the control device 102 and the memory device 110.”

B. Principles of Law (Anticipation and Obviousness)

Anticipation, under 35 U.S.C. § 102, requires a lack of novelty. *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir.

2001). To establish anticipation, each and every element in a claim, arranged as is recited in the claim, must be found in a single prior art reference. *Id.*

Additionally, a patent claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103(a). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). In that regard, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

C. *Person of Ordinary Skill in the Art*

Petitioner proposes that a person of ordinary skill in the art would have had an undergraduate degree in Electrical Engineering or an equivalent subject and either (1) two or three years of post-graduate work designing computer memory systems, including one or two years designing double data rate DRAM memory systems or (2) a Master’s degree in Electrical Engineering (or equivalent subject) and one or two years of post-graduate experience designing computer memory systems, including double data rate DRAM memory systems. Ex. 1003 ¶¶ 27–28, *cited, e.g., in* Pet. 55, 58, 60.

Patent Owner does not dispute Petitioner's proposal. *See generally* PO Resp. We adopt Petitioner's definition.

D. Anticipation by Lee (Claims 1, 5, 6, 8, 9, 13, 14, 16, 20, and 24)

Petitioner contends each of claims 1, 5, 6, 8, 9, 13, 14, 16, 20, and 24 is anticipated by Lee. Pet. 14–52.

1. Overview of Lee

Lee is directed to a semiconductor memory device that receives address and command signals in synchronization with a first clock signal and that inputs and outputs data in synchronization with a second clock signal. Ex. 1004, 3:43–52. Lee describes that the frequency of the first clock signal is lower than that of the second clock signal. *Id.* at 4:64–66. Figure 4 of Lee is reproduced below.

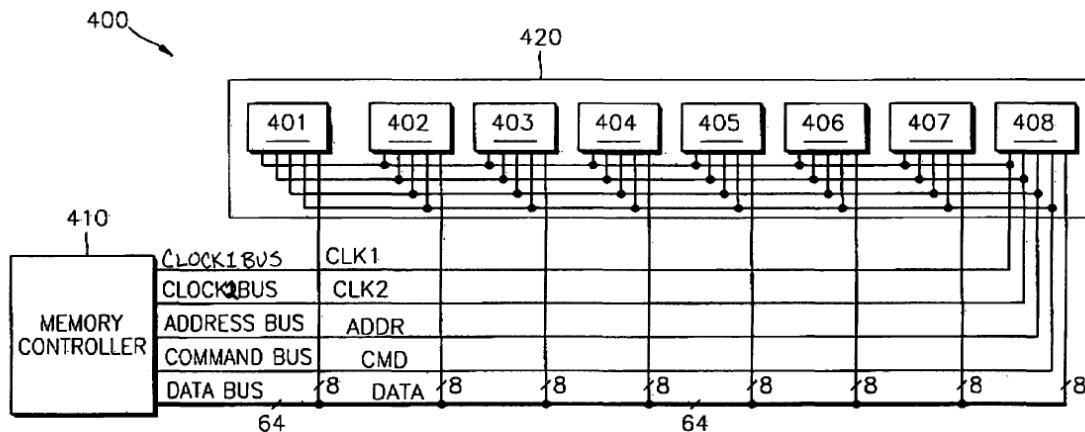


Figure 4 of Lee, reproduced above, illustrates system board 400, which includes memory module 420 having memory chips 401 through 408. *Id.* at 6:46–50. As shown in Figure 4 above, each of memory chips 401 through 408 is connected to clock1 bus, clock2 bus, address bus, command bus, and data bus. *Id.* at 6:62–64.

Memory chip 401 within memory module 420 is illustrated in more detail in Figure 5, which is reproduced below.

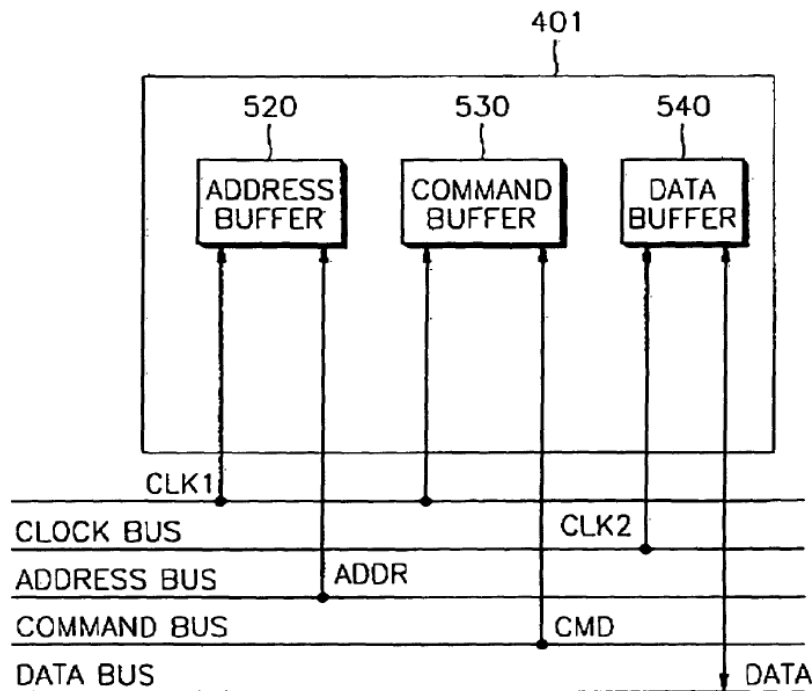


Figure 5 of Lee, reproduced above, illustrates a block diagram of memory chip 401 and its connections to bus lines. *Id.* at 4:62–67, 5:18–19.

Memory chip 401, shown in Figure 5 above, includes address buffer 520 and command buffer 530 that receive address signals and command signals, respectively. *Id.* at 7:2–6. Address buffer 520 and command buffer 530 also receive the first clock signal (CLK1) and process address and command signals in synchronization with the first clock signal (CLK1). *Id.* at 7:4–12. Memory chip 401 also includes data buffer 540, which has a bi-directional connection to the data bus and receives the second clock signal (CLK2). *Id.* at 7:7–9. Lee describes that the first clock signal (CLK1) has a lower frequency than the second clock signal (CLK2). *Id.* at 7:12–14.

2. *Discussion of Independent Claim 1*

We begin our analysis with independent claim 1. Claim 1 is directed to a method of transmitting signals comprising receiving at a memory device first and second clock signals, wherein the frequency of the first clock signal is less than the second clock signal, performing a data read operation and a data write operation using the second clock signal, and performing a command processing operation using the first clock signal. Ex. 1001, 7:55–67. Petitioner, for example, points to Figures 4 and 5 of Lee discussed in the summary above, as well as Figure 6 of Lee and related description, and relies on the testimony of Dr. Jacob. Pet. 14–22 (citing, *e.g.*, Ex. 1004, (57), 2:20–24, 2:47–50, 3:38–61, 4:62–67, 6:46–7:42, 8:7–14, 9:53–60, 11:31–12:12, Fig. 4–6; Ex. 1003 ¶¶ 102, 103, 105, 107, 135–147, 162–172, 179–182).

We find that Lee’s disclosure is consistent with Petitioner’s contentions and Dr. Jacob’s testimony. *Id.* For instance, Lee describes memory chip 401 having address buffer 520 and command buffer 530 that receive and use the first clock signal (CLK1) and data buffer 540 that receives and uses the second clock signal (CLK2). *See, e.g.*, Ex. 1004, 3:38–61, 7:1–12, 11:31–12:12, Figs. 5, 6. Additionally, Lee describes that the first clock signal (CLK1) has a lower frequency than the second clock signal (CLK2). *See, e.g., id.* at 4:63–67, 7:12–14, 11:31–12:12, Fig. 6.

Patent Owner asserts that Lee does not anticipate claim 1 because Lee does not disclose “getting data from a memory array” or “placing data in an address-specified location in a memory array,” and further “never uses the terms ‘read,’ ‘read operation,’ ‘write,’ or ‘write operation.’” PO Resp. 27–

29. Patent Owner's assertion is premised on its proposed claim constructions. *Id.*

As we discussed *supra* in Section II.A.2, we agree with Petitioner that Patent Owner's proposed constructions are too narrow and determine that "read operation" and "write operation" mean "getting data from" and "placing data in," respectively, a memory device. As we also discussed *supra* in Section II.A.2, for the patentability determinations before us, we can accept Patent Owner's contention that the term "memory device" is a memory chip or an IC.

Regarding the recitation of "memory device" in claim 1, we are persuaded by Petitioner's contentions and we credit and give substantial weight to Dr. Jacob's testimony (*see, e.g.*, Pet. 14–22, 24–27, 38–44, 49 (citing, *e.g.*, Ex. 1003 ¶¶ 103, 136–139, 148–172)), because Lee discloses inputting and outputting data to and from memory chips, such as memory chip 401. Ex. 1004, 3:38–52, 4:62–67, 6:41–67, 7:27–35, 8:59–62, 11:31–12:12, Figs. 4, 5. Lee also, more specifically, discloses that "memory chip 401" is a "dynamic random access memory (DRAM)" "semiconductor memory device." Ex. 1004, 6:40–42, 7:1–2, 7:27–33. Lee's "memory chip 401" is a DRAM device, which is the same as the example disclosed in the '122 Patent, i.e., "[f]or example, in one embodiment, the memory device may be a volatile memory device such as a *dynamic, random access memory (DRAM) device*." Ex. 1001, 3:50–59 (emphasis added).

Regarding the claimed "read operation" and "write operation," we are persuaded by Petitioner's contentions and credit and give substantial weight to Dr. Jacob's testimony regarding Lee's disclosure of inputting and outputting data to and from the aforementioned chips. *See, e.g.*, Pet. 14–22,

24–27, 38–44, 49 (citing, *e.g.*, Ex. 1003 ¶¶ 103, 136–139, 148–172). For example, we are persuaded by Petitioner’s contentions and credit and give substantial weight to Dr. Jacob’s testimony (*id.*) that Lee’s data output corresponds to the claimed read operation (“getting data from”) and Lee’s data input corresponds to the claimed write operation (“placing data in”) because the contentions and testimony are consistent with the evidence cited therein. For instance, Lee describes

According to yet another aspect of the present invention, a semiconductor memory system includes a memory controller which generates a first clock signal, a second clock signal having a frequency which is greater than that of the first clock signal, an address signal, a command signal and data; and a memory module having a plurality of semiconductor memory devices connected to the memory controller through bus lines on which the first clock signal, the second clock signal, the address signal, the command signal[,] and the data are loaded, wherein each of the semiconductor memory device[s] comprises (a) an address buffer which receives the address signal at a timing of the first clock signal, (b) a command buffer which receives the command signal at a timing of the first clock signal, and (c) a data buffer which inputs/outputs data at a timing of the second clock signal.

Ex. 1004, 3:38–52; *see also id.* at 7:27–35 (describing data transfer at a timing of the second internal clock signal CLK2), 11:31–12:12 (describing that each memory chip has a data buffer that “inputs/outputs data at a timing of the second clock signal”).

Furthermore, regarding Patent Owner’s assertion that Lee does not disclose “getting data from a memory array” and “placing data in an address-specified location in a memory array,” Patent Owner acknowledges that Lee describes “getting data from a buffer 540” and “putting data from a

bus into a buffer.” PO Resp. 27–28.¹¹ In addition to being premised on an overly narrow construction, Patent Owner’s contentions do not take into account Lee’s disclosure. For instance, Lee describes that memory chip 401 receives “the address signal ADDR” and “the data signal DATA.” Ex. 1004, 6:62–67; *see also id.* 3:47–49 (describing that the semiconductor memory device has “an address buffer which receives the address signal”), 11:31–12:12 (claiming a semiconductor memory device having an address buffer which receives the address signal). Lee’s disclosure of memory chip 401 having a memory array is discussed further *infra* in Section II.D.4 with respect to claim 16, which recites a memory array.

Regarding Patent Owner’s assertion that Lee “never uses the terms ‘read,’ ‘read operation,’ ‘write,’ or ‘write operation’” (PO Resp. 28), we are persuaded that the Petition has established that each and every element in claim 1, arranged as is recited in claim 1, is found in Lee. That Lee does not use the same nomenclature does not preclude finding that Lee discloses the claimed “read operation” and “write operation,” which for the reasons discussed *supra* in Section II.A.2, mean “getting data from” and “placing data in,” respectively, a memory device.

¹¹ As discussed above, Lee’s disclosure is the same as the embodiments in the ’122 Patent Specification that Patent Owner relies on for interpreting the claims of the ’122 Patent. *Id.* at 23 (“The ’122 Patent specification teaches that “a ‘write operation’ transfers data present on a data bus (labeled ‘DQ(WRITE)’ in Figure 1 and ‘DQ’ in Figure 5)”), 24 (“Likewise, the ’122 Patent specification teaches that a ‘read operation’ transfers data . . . onto a data bus (labeled ‘DQ(READ)’ in Figure 1 and ‘DQ’ in Figure 4).”)

For the reasons given, we are persuaded Petitioner sufficiently establishes that Lee anticipates claim 1, and adopt as our own findings Petitioner's analysis of Lee.

3. *Discussion of Independent Claims 9 and 20*

Independent claims 9 and 20 are similar to claim 1. Petitioner has made a showing with respect to claims 9 and 20 similar to its showing with respect to claim 1. *Compare* Pet. 27–52, *with id.* at 14–22. To the extent that claims 9 and 20 are different from claim 1, Petitioner has accounted for such differences.

We start with claim 9, which recites “[a] method for providing clock signals to a memory device,” which includes providing first and second clock signals, wherein a frequency of a first clock signal is less than a frequency of the second clock signal, as well as providing command data. We find that Lee's disclosure is consistent with Petitioner's contentions and Dr. Jacob's testimony. *See, e.g., id.* at 27–37; Ex. 1003 ¶¶ 102–107, 136–139, 162–172, 179–182. For instance, Lee describes a memory controller that generates the first clock signal (CLK1) and second clock signal (CLK2) and provides them to memory chip 401, which has address buffer 520 and command buffer 530 that receive and use the first clock signal (CLK1) and data buffer 540 that receives and uses the second clock signal (CLK2). *See, e.g.,* Ex. 1004, 3:38–52, 4:62–67, 6:46–7:12, 11:31–12:12, Figs. 4–6. Additionally, Lee describes that the first clock signal (CLK1) has a lower frequency than the second clock signal (CLK2). *See, e.g., id.* at 4:62–67, 7:12–14, 11:31–12:12, Fig. 6. Furthermore, Lee describes the memory controller providing a command signal (CMD) data, as well as performing a “read operation” and “write operation,” as recited in claim 9. *See, e.g., id.* at

3:38–52, 6:46–7:42, 11:31–12:12, Figs. 4–6. Patent Owner does not argue claim 9 separately, but, instead, Patent Owner relies on the same contentions discussed with respect to claim 1 *supra* in Section II.D.2. *See generally* PO Resp.

Claim 20 is directed to a device comprising “an interface to a memory device” and “circuitry configured to” perform the method steps recited in claim 9. We find that Lee’s disclosure is consistent with Petitioner’s contentions and Dr. Jacob’s testimony. *See, e.g., id.* at 27–40, 45–49; Ex. 1003 ¶¶ 102–07, 135–56, 162–72, 179–82. Patent Owner does not argue claim 20 separately, rather Patent Owner relies on the same contentions for claim 20 discussed with respect to claim 1 *supra* in Section II.D.2. *See generally* PO Resp.

For the reasons given, we are persuaded Petitioner sufficiently establishes that Lee anticipates independent claims 9 and 20, and adopt as our own findings Petitioner’s analysis of Lee.

4. *Discussion of Independent Claim 16*

Claim 16 is directed to “[a] memory device” comprising “a memory array,” “an interface to a control device,” and “circuitry configured to” perform steps similar to those recited with respect to claim 1, except claim 16 recites in the “read operation” “data is read from the memory array,” and in the “write operation” “data is written to the memory array.” Petitioner’s contentions for claim 16 are similar to those presented for claim 1, and Petitioner refers to its contentions for claim 1, as well as relies on Dr. Jacob’s testimony. *Compare* Pet. 37–44, *with id.* at 14–22. The dispute between the parties pertains to whether the Petition points out a “memory array” in Lee’s “memory device.” We are persuaded by Petitioner’s

assertion that Lee's memory devices have memory arrays and find that Lee's disclosure is consistent with Petitioner's contentions and Dr. Jacob's testimony. *See, e.g., id.* at 37–44; Ex. 1003 ¶¶ 41, 103, 136–139, 148–156, 162–172, 179–182.

Starting with “[a] memory device” recited in claim 16, Petitioner refers to “[s]ee Ground 1: [1.1],” which is a reference to Petitioner's contentions for “receiving, at a memory device, a first clock signal and a second clock signal,” recited in claim 1. Pet. 37 (citing, *e.g.*, Ex. 1003 ¶¶ 103, 148–156). In its contentions for Ground 1 [1.1], Petitioner points to a single memory chip, i.e., memory chip 401. Pet. 16 (“Lee's memory module is comprised of a plurality of memory chips, *one of which is shown in FIG. 5*”) (emphasis added). Petitioner sets forth Figure 5 of Lee illustrating memory chip 401, with annotations, which is reproduced below.

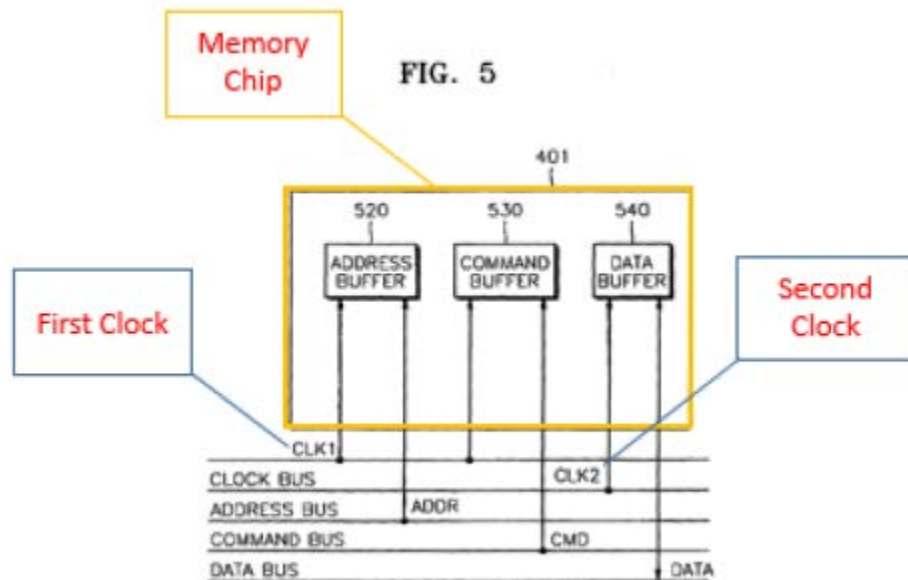


Figure 5 of Lee, reproduced above with Petitioner's annotations, is a block diagram of memory chip 401 (annotated in yellow) that receives first clock

(CLK1) (annotated in blue) and second clock (CLK2) (also annotated in blue). Pet. 16 (citing, *e.g.*, Ex. 1004, Fig. 5).

The aforementioned contentions are one of two alternatives presented in the Petition, because according to Petitioner, Lee discloses more than one memory device. *Id.* at 14–16, 37. In particular, Petitioner, alternatively, asserts memory module 420 discloses a “memory device,” as recited in claims 1 and 16. *Id.* at 14–15, 37 (citing, *e.g.*, Ex. 1004, Fig. 4).

Patent Owner contends that Petitioner does not point to memory chip 401 as an example of Lee disclosing the claimed memory device in the Petition, asserting “[t]he petition is very clear that the petitioner’s position is that Lee’s memory module 420 is the recited ‘memory device,’” but “it is certainly not the petition’s position that those chips [memory chips 401–408] are the ‘memory device’ recited in the ’122 Patent claims.” PO Resp. 31–32; *see also id.* at 34 (“[T]he petition uniformly, without exception, asserts that Lee’s memory module 400 is the recited ‘memory device,’ and that the recited ‘memory array’ is the set of chips 401–408 on the module.”) Contrary to Patent Owner’s contentions, in addition to reproducing Figure 5 with annotations highlighting in yellow memory chip 401 (Pet. 14–16), Petitioner further identifies the memory chip itself as an exemplary memory device disclosed in Lee in the Petition. For instance, immediately below annotated Figure 5, the Petition includes the following contentions:

Further, Lee’s memory module is comprised of a plurality of memory chips, one of which is shown in FIG. 5, and *each* of which “includes an address buffer 520, a command buffer 530 and a data buffer 540. . . . [T]he command buffer 530 receives the first clock signal CLK1 and the command signal CMD. The data buffer 540 receives the second clock signal CLK2 and the data signal DATA.” NVIDIA-1004, 6:46–7:9. *By receiving the first clock signal via a CLOCK1 BUS and receiving the second*

clock via a CLOCK2 BUS, Lee discloses “receiving, at a memory device, a first clock signal and a second clock signal.”

Pet. 16 (emphases added). In the Petition, Petitioner clearly refers to memory chip 401 as the memory device, recited in claims 1 and 16, which receives the first clock signal and the second clock signal. *Id.* Consistent with Petitioner’s contentions in its Reply, the Petition includes other references to Lee’s memory chip 401 as an example of Lee’s disclosure of the claimed memory device. *See, e.g.,* Pet. 18, 24, 37–41; Pet. Reply 6–9 (citing, *e.g.,* Pet. 8, 18, 24, 27, 37–44; Ex. 1003 ¶¶ 41, 103, 148–61) (“These points [Lee’s disclosure under Patent Owner’s construction] are fully set forth in the Petition in addressing the features of claim 16.”)

Patent Owner acknowledges that Dr. Jacob testifies that Lee’s memory chip 401 is an example of the claimed memory device, *e.g.,* “Dr. Jacob’s alternative theory [is] that the ‘memory device’ may be one of the chips 401–408 with a ‘memory array’ within that chip,” which is expressed “in paragraphs (148–53).” PO Resp. 34. Patent Owner, however, contends:

It would also be improper for the Board to continue to rely on Dr. Jacob’s alternative theory regarding the “memory device” and “memory array” in Lee for the additional reason that doing so would violate the Board’s well established precedent to disregard arguments that (a) appear only in an expert declaration but not in the petition *per se* or (b) are merely incorporated by reference from an expert declaration into the petition.

Id. at 36. Patent Owner acknowledges that “the petition cites” to the aforementioned testimony of Dr. Jacob, but according to Patent Owner, Dr. Jacob’s testimony in this regard “is irrelevant” because Petitioner “never adopts or develops” it as “petitioner’s position.” *Id.* at 34.

We disagree. First, for example, on one of the pages of the Petition specifically referred to by Patent Owner (PO Resp. 32) as setting forth only

Petitioner’s theory, i.e., page 38 of the Petition, Petitioner cites to paragraphs 148 through 153 of Dr. Jacob’s testimony *four times*. Pet. 38 (citing, *e.g.*, Ex. 1003 ¶¶ 41, 103, 136–37, 148–153). Within these paragraphs Dr. Jacob testifies, for example, Lee “discloses two separate memory devices: the memory module 420 and memory chip 401 . . . [e]ach discloses a memory array.” Ex. 1003 ¶ 149. Additionally, as discussed *supra* in this Section, other portions of the Petition also clearly set forth that Lee’s disclosure satisfies all limitations recited in claim 16, using Patent Owner’s own proposed construction. *See, e.g.*, Pet. 16–18, 24, 37, 39–41; Pet. Reply 6–9. Furthermore, Patent Owner had notice in the Institution Decision that we found persuasive Petitioner’s contention that Lee’s memory chip 401 is a memory device, using Patent Owner’s proposed construction for that term. Inst. Dec. 7, 13–14.¹²

Petitioner alternatively asserts memory module 420 is the claimed memory device. Pet. 14–15, 37. Patent Owner contends “the petition contends that an entire multi-chip memory module 420 is the ‘memory device’ and that chips 401–408 on the module 420 constitute a ‘memory array,’” but “[t]hat contention fails on its face under the correct interpretation of ‘memory device.’” PO Resp. 40. For the reasons discussed *supra* in Section II.A.2, Petitioner’s alternative assertion is an independent

¹² *Cf. Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2139, 2146 (2016) (“Cuozzo argued . . . at least . . . [with] respect to claims 10 and 14 . . . the agency found that Garmin had only *implicitly* challenged those two claims,” and “Cuozzo’s contention that the Patent Office unlawfully initiated its agency review is not appealable.”) In the instant proceeding, Petitioner asserts in the Petition that memory chip 401 is an exemplary memory device. *See, e.g.*, Pet. 16–18, 24, 37, 39–41.

reason we are persuaded by Petitioner’s contentions. We agree with Petitioner that Patent Owner’s requirement that “memory device” be a single integrated circuit or chip is too narrow and, instead, we are persuaded that the “memory device” may comprise multiple DRAMs or chips. We, therefore, are persuaded by Petitioner’s showing pertaining to memory module 420 comprising memory chips 401 through 408. Pet. 14–15, 37–38.

With respect to the “memory array” recited in claim 16, Petitioner contends that both memory module 420 and memory chip 401 disclose a memory array. *See, e.g., id.* at 37–38 (citing, *e.g.*, Ex. 1003 ¶¶ 41, 103, 136–137, 148–156); *see also id.* at 24 (identifying Lee’s disclosures of DDR DRAMs and SDR DRAMs). For instance, Dr. Jacob testifies “Lee describes the memory chips as either SDR or DDR DRAM semiconductor memory devices, each of which a person of ordinary skill [in the art] would know quite well to contain a memory array.” Ex. 1003 ¶ 153; *see also id.* ¶ 149 (testifying memory chip 401 discloses a memory array), ¶ 156 (testifying Lee discloses a “typical memory device with a memory array”). We find that Lee’s disclosure is consistent with Petitioner’s contentions and Dr. Jacob’s testimony. *See, e.g., id.* at 37–44; Ex. 1003 ¶¶ 41, 103, 136–39, 148–56, 162–72, 179–82.

Patent Owner does not dispute that Lee’s memory chip 401 discloses a memory array. *See generally* PO Resp. Indeed, Patent Owner asserts:

It is true that Dr. Jacob refers to Lee’s chips 401–408 as “memory devices,” *see, e.g.*, Jacob Decl. ¶¶ 103, 139. In fact, that is consistent with the skilled artisan’s understanding of the phrase “memory device,” as explained in § III-A *supra*. Dr. Jacob even says that these chips are memory devices that contain memory arrays. *Id.* at ¶¶ 149–153.

PO Resp. 32. Patent Owner and Dr. Przybylski further do not dispute that the '122 Patent refers to DRAM standards and that such DRAM standards describe the DRAM memory chip as having a memory array. PO Resp. 18–19, 25; Ex. 2003 ¶¶ 45–48, 55. Patent Owner also does not dispute that Lee’s memory module 420 discloses a memory array.¹³

Instead, Patent Owner relies on its contentions that the Petition does not point to memory chip 401 as the claimed memory device and memory module 420 is not the “memory device” recited in claim 16, under Patent Owner’s narrow interpretation requiring that the device be a single chip. PO Resp. 31–41. For the reasons discussed above in this Section, and after consideration of Patent Owner’s assertions, we are persuaded by Petitioner’s showing.

Regarding “an interface to a control device,” recited in claim 16, Petitioner points to receipt of signals by memory chip 401, as well as receipt by memory module 420. Pet. 39. Petitioner sets forth Figure 4 of Lee with annotations, which is reproduced below.

¹³ In addition to finding that Lee’s disclosure is consistent with Petitioner’s contentions and Dr. Jacob’s testimony, we further note, as set forth in our Order of June 22, 2017, issued with our Decision on Institution, Patent Owner has been cautioned, “that any arguments for patentability not raised in the response will be deemed waived.” Paper 10, 3.

FIG. 4

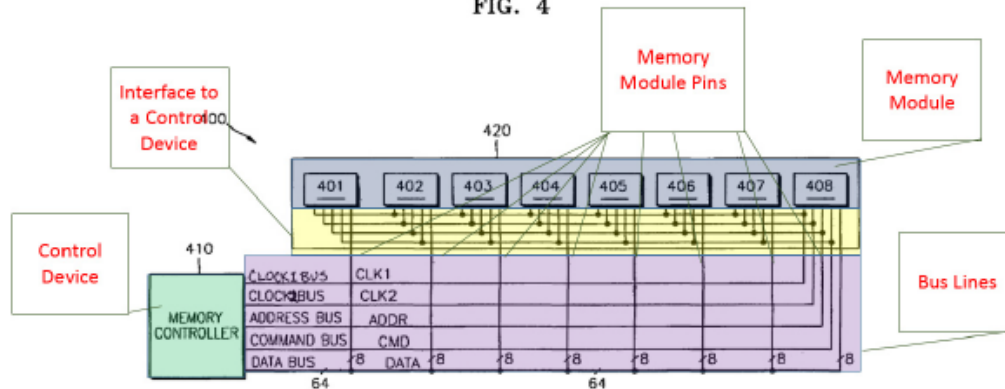


Figure 4 of Lee, reproduced above, is an illustration of a system board having a memory module 420 with memory chips 401 . . . 408 (Ex. 1004, 5:14–16, 6:46–50), shown with Petitioner’s annotations highlighting memory chips 401–408 (in gray), memory controller 410 (in green), bus lines (in purple), and the interface to the control device (in yellow) (Pet. 39).

Petitioner contends that Figure 4 of Lee shows that “*each* memory chip receives signals” from memory controller 410 “via the bus line connection,” and specifically identifies the interface, in yellow, which is the *individual connections* of *each* of chips 401 through 408 with the bus lines. *Id.* (emphasis added). Patent Owner does not dispute separately Petitioner’s contentions regarding Lee’s disclosure of “an interface to a control device,” recited in claim 16. We find that Lee’s disclosure of the connections of, for example, memory chip 401 with the bus lines to memory controller 410 (*see, e.g.,* Ex. 1004, 3:38–46, 6:62–67, 11:31–12:12, Fig. 4) is consistent with Petitioner’s contentions and Dr. Jacob’s testimony.

With respect to the remaining recitations in claim 16, Petitioner points to its contentions for claim 1, and provides further explanation consistent with the aforementioned contentions. *Id.* at 40–44. For instance, Petitioner

points to the bidirectional arrow illustrated in Figure 5 showing that data is read from the memory array and data is written to the array. *Id.* at 41–44.

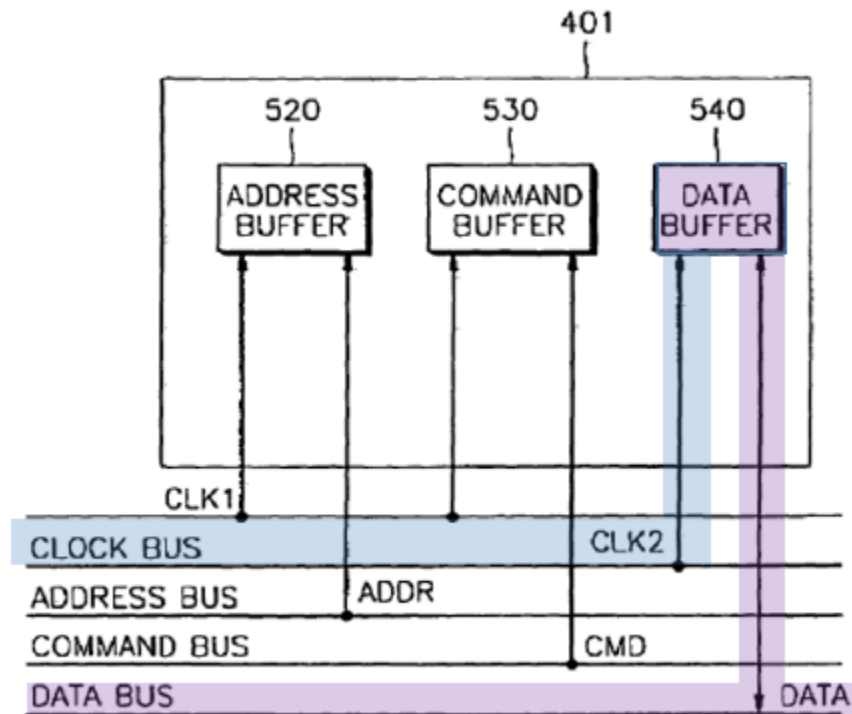


Figure 5 of Lee, reproduced above, is a block diagram of a semiconductor memory device with Petitioner’s annotations showing a bidirectional arrow depicting input and output data (in purple) and the second clock (CLK2) (in blue) (Pet. 42, 44).

Patent Owner contends that Lee does not “explicitly” disclose, “reads from or writes to” when Petitioner’s challenge “is judged as it was presented in the petition,” i.e., that “an entire multi-chip memory module 420 is the ‘memory device.’” PO Resp. 40 (citing, *e.g.*, PO Resp. § V-A). We are persuaded by the Petition and the evidence cited therein, after consideration of Patent Owner’s contentions for the reasons discussed *supra* in Section II.D.2 with respect to claim 1 and *supra* in this Section with respect to claim 16.

We find that Lee's disclosure is consistent with Petitioner's contentions and Dr. Jacob's testimony. *See, e.g., id.* at 37–44; Ex. 1003 ¶¶ 41, 103, 136–39, 148–56, 162–72, 179–82. For instance, for the same reasons discussed *supra* in this Section, we are persuaded that each of Lee's memory chip 401 and Lee's memory module 420 discloses a memory device comprising an array and for the same reasons given *supra* in Sections II.D.2 and II.D.3, with respect to claims 1 and 9, we are persuaded that Lee discloses the claimed read and write operations, with respect to each of the exemplary memory devices.

For the reasons given, we are persuaded Petitioner sufficiently establishes that Lee anticipates independent claim 16, and adopt as our own findings Petitioner's analysis of Lee.

5. *Discussion of Dependent Claims 5, 6, 8, 13, and 14*

Regarding dependent claims 5, 6, 8, 13, and 14, Petitioner asserts that Lee describes all elements of these claims. Pet. 14–37. We find that Lee's disclosure is consistent with Petitioner's contentions and Dr. Jacob's testimony. *Id.*; Ex. 1003 ¶¶ 102, 103, 105–108, 135–147, 157–172, 179–182.

For example, regarding the requirement that the frequency of the second clock signal is twice that of the first clock signal, recited in claims 5 and 13, consistent with Petitioner's contentions (Pet. 22–23, 37), Lee describes “the frequency of the first internal clock signal CLK1 is half that of the external clock signal CLK (or the second internal clock signal CLK2).” Ex. 1004, 7:22–26; *see also id.* at Fig. 6 (illustrating the frequency of “CLK(=CLK2)” as twice “CLK1”).

Regarding the further requirement that the memory device is a DRAM, recited in claims 6 and 14, we are persuaded by Petitioner's analysis (Pet. 24, 37) for the same reasons discussed *supra* in Sections II.D.2 through II.D.4 with respect to independent claims 1, 9, and 16.

Regarding claim 8, consistent with Petitioner's contentions (Pet. 24–27, 37) that Lee describes the requirement recited in claim 8 that command and address data are received using the first clock signal, as set forth in the summary of Lee above, Lee describes address buffer 520 and command buffer 530 receiving the first clock signal (CLK1) and processing address and command signals in synchronization with the first clock signal (CLK1). Ex. 1004, 7:4–12, Figs. 5, 6.

Patent Owner does not argue these claims separately. *See generally* PO Resp. For the reasons given, we are persuaded Petitioner sufficiently establishes that Lee anticipates claims 5, 6, 8, 13, and 14, and adopt as our own findings Petitioner's analysis of Lee.

6. *Discussion of Independent Claim 24*

Claim 24 is directed to a “memory device” with a “means for storing data,” and “means for interfacing a control device,” and “circuitry configured to” perform the steps recited in claim 1.

We now turn to Petitioner's contentions regarding independent claim 24. In its contentions for claim 24, Petitioner refers back to its contentions for claims 1 and 16. Pet. 49–52.

As explained *supra* in Section II.D.4, two alternatives are presented in the Petition, because according to Petitioner, Lee discloses more than one memory device. Pet. 14–16, 37. Regarding the “means for interfacing a control device,” recited in claim 24, Petitioner points to receipt of signals by

memory chip 401, as well as receipt by memory module 420. Pet. 39, 49–50. Petitioner sets forth Figure 4 of Lee with annotations. Petitioner’s annotated Figure 4 is reproduced below showing the “means for interfacing a control device,” recited in claim 24, highlighted in yellow.

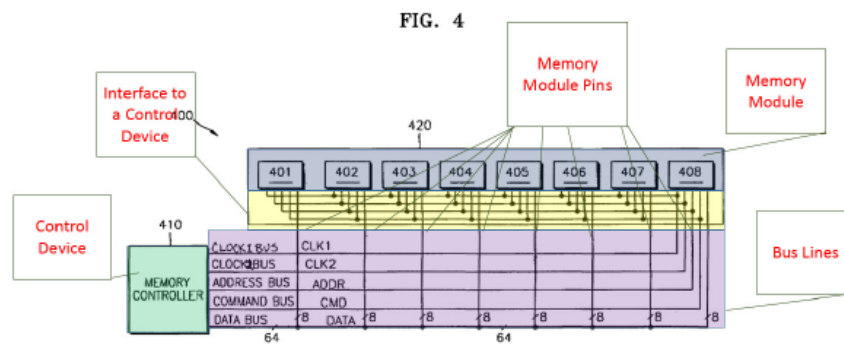


Figure 4 of Lee, reproduced above, is an illustration of a system board having a memory module 420 with memory chips 401 . . . 408 (Ex. 1004, 5:14–16, 6:46–50), shown with Petitioner’s annotations highlighting memory chips 401–408 (in gray), memory controller 410 (in green), bus lines (in purple), and the interface to the control device (in yellow) (Pet. 39). The interface into each of memory chips 401 through 408 is seen in greater detail in Figure 5, illustrating memory chip 401.

Figure 5 of Lee, reproduced below, shows details regarding the interface for both alternative memory devices (i.e., memory module 420 and memory chip 401) presented in the Petition.

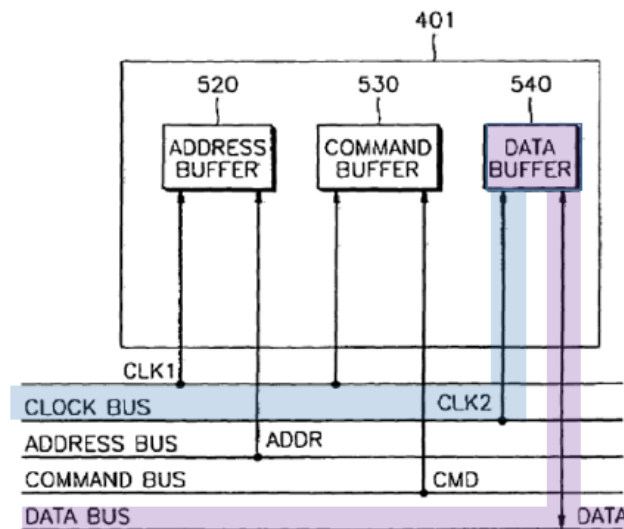


Figure 5 of Lee, reproduced above, is a block diagram of a semiconductor memory device with Petitioner’s annotations showing a bidirectional arrow depicting input and output data (in purple) and the second clock (CLK2) (in blue) (Pet. 42, 44, 50–51).

As explained *supra* in Section II.A.3, we analyze Petitioner’s contentions using Petitioner’s recited function, i.e., “interfacing a control device” and corresponding structure for performing the function, i.e., “memory interface 150,” which is depicted in FIG. 1 “between the control device 102 and the memory device 110.” Additionally, as we explained, regarding Petitioner’s assertion that the RDQS2x signal is intangible and not a structural element (Pet. Reply 14–16), the ’122 Patent Specification describes that the off-chip driver (OCD) 126 transmits this data over a line to control device 102 (*see, e.g.*, Ex. 1001, 4:35–38, 5:33–36, Fig. 1).

Figure 1 of the ’122 Patent, with Petitioner’s annotations identifying the “means for interfacing a control device,” recited in claim 24, is reproduced below, for comparison.

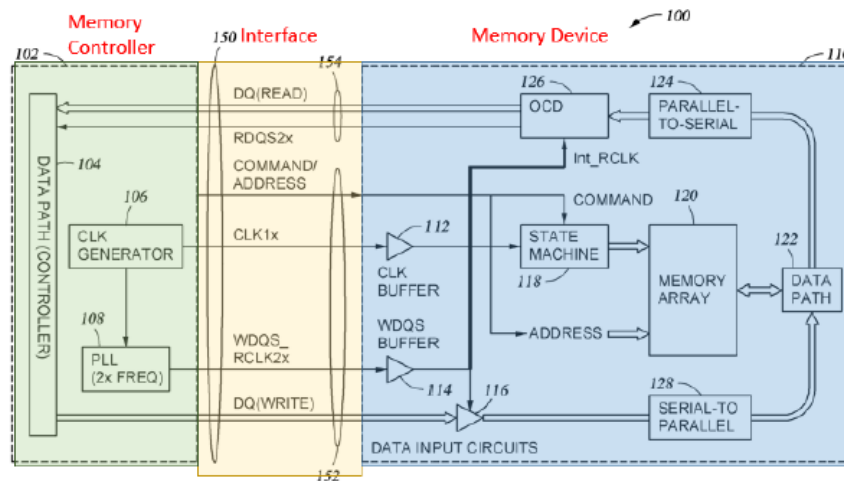


Fig. 1

Figure 1 of the '122 Patent, reproduced above with Petitioner's annotations, is a block diagram depicting system 100 that includes memory device 110, highlighted in blue, and a control device 102, highlighted in green, with interface 150, highlighted in yellow, between control device 102 and memory device 110. Pet. 13; Ex. 1001, 2:39–41, 3:37–43, Fig. 1.

Consistent with Patent Owner's contentions (PO Resp. 41–42), Petitioner has not identified in Lee's interface structure corresponding to the line used by OCD 126 to transmit the RDQS2x signal to control device 102, as is set forth in the '122 Patent Specification (*see, e.g.*, Ex. 1001, 4:35–38, 5:33–36, Fig. 1). Petitioner contends that "Lee's bus lines and pins comprise a memory interface" and, more specifically, contends, "Lee discloses the 'system clock signal, the address signal[,] and the command signal,'" as well as "... two or more module pins receiving the first and second clock signals." Pet. 50–51 (*citing, e.g.*, Ex. 1004, 3:38–46, 4:44–67; Ex. 1003 ¶¶ 26, 148–56). Dr. Jacob testifies, for example, Lee's "memory system uses an interface comprising the Clock Busses, the Address Bus, the Command Bus, and the Data Bus" and quotes portions of Lee describing

these bus lines. Ex. 1003 ¶¶ 154–55 (citing Ex. 1004, Figs. 6:62–67, 4, 5). Dr. Jacob also testifies “what Lee discloses is a typical memory device with a memory array, an interface to a controller, the ability to process commands and data, etc.” *Id.* ¶ 156.

Patent Owner contends that the Petition has not “articulated any assertion that Lee discloses an equivalent.” PO Resp. 41. Consistent with Patent Owner’s contentions, we do not find sufficient explanation or evidence as to why Lee’s structure is equivalent to the structure in the ’122 Patent Specification, i.e., interface 150 including a line between OCD 126 and control device 102 for the transmission of the RDQS2x signal (*see, e.g.*, Ex. 1004, 4:35–38, Fig. 1). We are not persuaded by Petitioner’s contentions in its Reply for the reasons discussed *supra* in Section II.A.3 and above. Pet. Reply 14–16. For instance, Petitioner’s contentions that the RDQS2x signal is intangible and not necessary (*id.*) do not explain why Petitioner need not show the structure for transmitting that signal, or show that Lee’s structure is equivalent to that structure in the ’122 Patent Specification identified by Petitioner.

During the hearing, Petitioner argued that Lee “has an interface where you have two clocks and a STROBE, the same interface as the 122 patent’s memory interface.” Tr. 10:20–22. Petitioner, however, does not rely on this embodiment for claim 24, and has not shown that it discloses receiving first and second clock signals. Pet. 49–52.

For the reasons given, we are not persuaded by Petitioner’s contentions that Lee anticipates independent claim 24.

7. Conclusion

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 5, 6, 8, 9, 13, 14, 16, and 20 of the '122 Patent are unpatentable, under 35 U.S.C. § 102(b), as anticipated by Lee. We also determine that Petitioner has not shown by a preponderance of the evidence that claim 24 of the '122 Patent is unpatentable, under 35 U.S.C. § 102(b), as anticipated by Lee.

E. Obviousness over Lee alone or with other art (Claims 2–4, 10–12, 17–19, 21–23, and 25–28)

Petitioner contends claims 2–4, 10–12, 17–19, 21–23, and 25–28 are unpatentable, under 35 U.S.C. § 103(a), as obvious over Lee alone or with Yoo. Pet. 4–9, 53–85. Petitioner also contends that claims 2, 3, 10, 11, 17, 18, 21, 22, 25, 26, and 28 are unpatentable, under 35 U.S.C. § 103(a), as obvious over Lee and Kyung. Pet. 85–95. Because we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 2–4, 10–12, 17–19, 21–23, and 28 of the '122 Patent are unpatentable, under 35 U.S.C. § 103(a), as obvious over the combined teachings of Lee and Yoo, we do not determine (1) whether these same claims also are unpatentable, under 35 U.S.C. § 103(a), as obvious over Lee; or (2) whether claims 2, 3, 10, 11, 17, 18, 21, 22, and 28 of the '122 Patent are unpatentable, under 35 U.S.C. § 103(a), as obvious over the combined teachings of Lee and Kyung.

1. Overview of Yoo

Yoo is directed to a semiconductor memory device that incorporates a strobe signal synchronized with a data signal. Ex. 1006, (57). More

specifically, Yoo teaches that the semiconductor memory device includes an output section that generates the strobe signal. *Id.* at 2:31–36.

2. *Overview of Kyung*

Kyung is directed to a double data rate synchronous semiconductor memory device. Ex. 1005, (57). More specifically, Kyung teaches that the semiconductor memory device has internal clock generator 702, which generates a plurality of internal clocks. *Id.* ¶ 70.

3. *Discussion of Claim 2*

Claim 2 depends from claim 1 and requires that the method further comprise the following steps:

performing a read operation with the second clock signal wherein separate read data are provided at rising and falling edges of a read clock signal generated from the second clock signal; and

performing a write operation with the second clock signal wherein separate write data are received at rising and falling edges of the second clock signal.

Ex. 1001, 8:1–8. Petitioner contends that the combination of Lee and Yoo teaches all elements of claim 2 and provides a rationale for combining the teachings of Lee and Yoo. Pet. 4–9, 53–62, 71–78.

We begin by considering Petitioner’s contentions that claim 2 would have been obvious over the combination of Lee and Yoo. *Id.* at 7–9, 53–62, 71–78. Petitioner relies on Lee for teaching the further recitations in claim 2, except for the requirement that the read clock signal is generated from the second clock signal. *Id.* For instance, with respect to performing a read operation with the second clock signal, Petitioner relies on Lee’s teaching of applying a strobe signal to data buffer 340, which inputs/outputs data at the

rising and falling edges of the strobe signal. *Id.* at 7–9, 55–56, 75–75 (citing, *e.g.*, Ex. 1004, 3:38–52, 4:62–67, 6:37–42, 6:56–60, 7:27–42, 10:15–19, 11:45–53, Figs. 4, 6; Ex. 1003 ¶¶ 28, 49–63, 70–71, 77, 109, 73–78, 184–93).

Petitioner also contends although Lee “does not explicitly disclose how the read clock signal is generated,” claim 2 would have been obvious because “a POSITA would have found it obvious to generate Lee’s read clock signal (*e.g.*, strobe signal) using the high-frequency clock signal.” Pet. 53 (citing Ex. 1003 ¶¶ 185–193). Petitioner, more specifically, contends “[a]lthough Lee’s FIG. 6 depicts the STROBE signal as being at the same frequency as the second clock signal, Lee does not explicitly teach that the strobe clock is *generated from* the second clock signal.” *Id.* at 75. Petitioner points to Yoo’s teaching of generating a strobe signal, for example, by strobe signal generator 71b1 illustrated in Figure 7 of Yoo. *Id.* at 73–78 (citing, *e.g.*, Ex. 1006, (57), 2:33–36, 2:49–57, 4:23–31, 4:41–46, 5:36–38, 5:56–6:29, 7:1–8, Figs. 3, 4, 7). Petitioner further supports its contentions regarding obviousness of claim 2 with the testimony of Dr. Jacob. *See, e.g.*, *id.* at 7–9, 53–62, 71–78 (citing, *e.g.*, Ex. 1003 ¶¶ 28, 49–63, 70, 71, 77, 109, 118–127, 173–178, 184–193, 199–219).

Patent Owner makes three arguments in response: (1) Lee does not include any embodiment that includes two external clocks provided to a semiconductor device and a strobe signal and such a combination would not have been obvious (PO Resp. 44–56); (2) the Petition does not present a rationale to combine Lee and Yoo (*id.* at 58–63); and (3) Yoo does not teach how to generate a read clock signal from a received clock signal (*id.* at 63–64).

We start with Patent Owner’s first argument that Lee does not include any embodiment that includes two external clocks provided to a semiconductor device and a strobe signal and such a combination would not have been obvious. PO Resp. 44–56. As discussed *supra* in this Section, Petitioner relies on Lee, not just for disclosure of all the recitations in claim 1, from which claim 2 depends, but also for teaching the further recitations in claim 2, except for the requirement that the read clock signal is generated from the second clock signal. Pet. 7–9, 53–62, 71–78. More specifically regarding claim 2, Petitioner contends that in addition to disclosing “a high-frequency clock signal for data operations and a low-frequency clock signal for command operations,” which we found persuasive as discussed, for example, *supra* in Section II.D.2, Lee’s memory device also uses “a read clock signal (e.g., strobe signal) . . . that runs at the same frequency as the high-frequency clock signal.” Pet. 7–9, 53, 71–72 (citing Ex. 1004, 2:47–50, 3:46–61, 4:63–67, 6:63–67, 7:18–42, 8:7–14, 11:31–12:12); *see also id.* at 55, 72 (citing Ex. 1003 ¶¶ 28, 49–55, 70–71, 77, 173–178, 184–193, 211–219) (“Lee’s STROBE signal is a read clock signal from which separate read data are read at rising and falling edges.”) Dr. Jacob testifies, “Lee discloses that in second-embodiment cases using DDR DRAM, an additional signal, STROBE, is part of the interface between the memory device and the memory controller.” Ex. 1003 ¶ 190 (citing Ex. 1004, 7:36–42).

Consistent with Petitioner’s contentions and Dr. Jacob’s testimony (*see, e.g.*, Pet. 7–9, 53–55, 71–72; Ex. 1003 ¶¶ 173–178, 185–193), Lee teaches use of a strobe signal in connection with both the first and second embodiments, “[i]n the case where the data buffer included in the memory chip of *the first or second embodiment is connected to receive a data strobe*

signal STROBE, the data is input/output at both the rising and falling edges of the data strobe signal STROBE as shown in FIG. 6.” Ex. 1004, 7:36–42 (emphasis added).

As an initial matter, we disagree with Patent Owner’s assertion that “this new contention” was not sufficiently articulated in the Petition. PO Resp. 49–51. The Petition, including the portions discussed in this Section, set forth Petitioner’s contentions with sufficient specificity. *See, e.g.*, Pet. 7–9, 53–61, 71–78 (citing, *e.g.*, Ex. 1004, 2:47–50, 3:46–61, 4:18–22, 4:63–67, 6:37–45, 6:63–67, 7:18–42, 8:7–14, 9:18–19, 11:31–12:12, Fig. 6; Ex. 1003 ¶¶ 28, 49–63, 70–71, 77, 98, 109, 118–127, 173–178, 184–193, 211–219). Additionally, we referred to Petitioner’s contentions regarding Lee’s teaching of using a strobe signal in connection with both the first and second embodiments in the Institution Decision. *See, e.g.*, Inst. Dec. 20.

Patent Owner also contends that Lee does not teach a strobe signal in connection with the second embodiment. PO Resp. 52, 54 (citing Ex. 2003 ¶¶ 59, 60). Dr. Przybylski’s testimony cited to in support (*id.*) is that “[t]he first embodiment . . . can be a single or double data rate DRAM” and “the semiconductor memory device of the first embodiment can be used with or without a STROBE signal.” Ex. 2003 ¶¶ 59–60. Dr. Przybylski’s testimony (*id.*), however, does not pertain to the second embodiment. Patent Owner’s assertion that Lee’s teaching “means only the first embodiment” (PO Resp. 52), is not consistent with the express teaching, i.e., “the data buffer included in the memory chip of the first or *second embodiment* is connected to receive a data strobe signal STROBE,” as well as other teachings of Lee discussed herein. Ex. 1004, 7:36–38 (emphasis added).

Patent Owner additionally contends “[t]o the extent that this paragraph [(Ex. 1004, 7:36–41)] applies to the second embodiment at all, the only reasonable interpretation of the paragraph is that it describes the case in which the memory chip receives a STROBE signal and uses it in place of CLK2.” PO Resp. 52 (citing Ex. 2003 ¶¶ 68–71). According to Patent Owner, “[t]his interpretation” is supported by Lee’s teaching of connecting the STROBE signal to the memory chip, without a teaching that the memory chip have an additional input. *Id.* at 54 (citing Ex. 2003 ¶¶ 68, 72). Dr. Przybylski testifies, “no embodiment in Lee . . . has more than two clock/strobe inputs,” “[t]here is no suggestion in Lee that the first and second embodiments can be combined to create a device with three clock and strobe inputs,” and, further “Lee teaches away from making such a combination.” Ex. 2003 ¶ 72.

After considering all the evidence and arguments presented by the parties, we agree with Petitioner and find that Lee teaches using a strobe signal in addition to the two external clock signals. We credit the testimony of Dr. Jacob over that of Dr. Przybylski in that regard because, as explained below, unlike Dr. Jacob’s testimony, Dr. Przybylski’s testimony is not consistent with Lee’s disclosure.

For instance, Lee expressly teaches using external first and second clock signals, as well as using a data strobe signal, as set forth, for example, in claims 16 and 18 of Lee, reproduced below.

16. A semiconductor memory system comprising:
 - a memory controller which generates *a first clock signal, a second clock signal having a frequency which is greater than that of the first clock signal*, an address signal, a command signal and data; and

a memory module having a plurality of semiconductor memory devices connected to the memory controller through bus lines on which the first clock signal, the second clock signal, the address signal, the command signal and the data are loaded, wherein each of the semiconductor memory device comprises (a) an address buffer which receives the address signal at a timing of the first clock signal, (b) a command buffer which receives the command signal at a timing of the first clock signal, and (c) a data buffer which inputs/outputs data at a timing of the second clock signal.

Ex. 1004, 11:31–46 (emphases added).

18. The semiconductor memory system according to claim 16, wherein *the data buffer receives a data strobe signal and inputs/outputs the data at every rising and falling edge of the data strobe signal.*

Ex. 1004, 11:49–53 (emphasis added).

Additionally, consistent with Petitioner’s contentions and Dr. Jacob’s testimony, Lee’s first embodiment also teaches using the STROBE signal with two clocks (CLK1 and CLK2). *See, e.g.,* Ex. 1004, 6:37–45, 9:18–19; *see also* Fig. 3 (cited in Pet. 69–71; Pet. Reply 19). Patent Owner asserts that teachings relating to two internal clocks are “not relevant,” as two external clock signals are required. PO Resp. 45. We, however, find that Lee’s teaching of the first embodiment that uses a strobe signal with two internal clock signals CLK1 and CLK2 (generated from the external clock signal) (Ex. 1004, 6:37–45, 9:18–19, Fig. 3) is consistent with Dr. Jacob’s testimony that Lee teaches substantially the same with respect to the second embodiment, i.e., using a strobe with two clock signals, except with respect

to the second embodiment two external clock signals are used. *See, e.g.*, Ex. 1003 ¶ 190 (citing Ex. 1004, 7:36–42).¹⁴

Lee’s other teachings further support the Petition. For instance, Lee illustrates timing of signals received by the DRAM in both the first and second embodiments in Figure 6 of Lee, reproduced below.

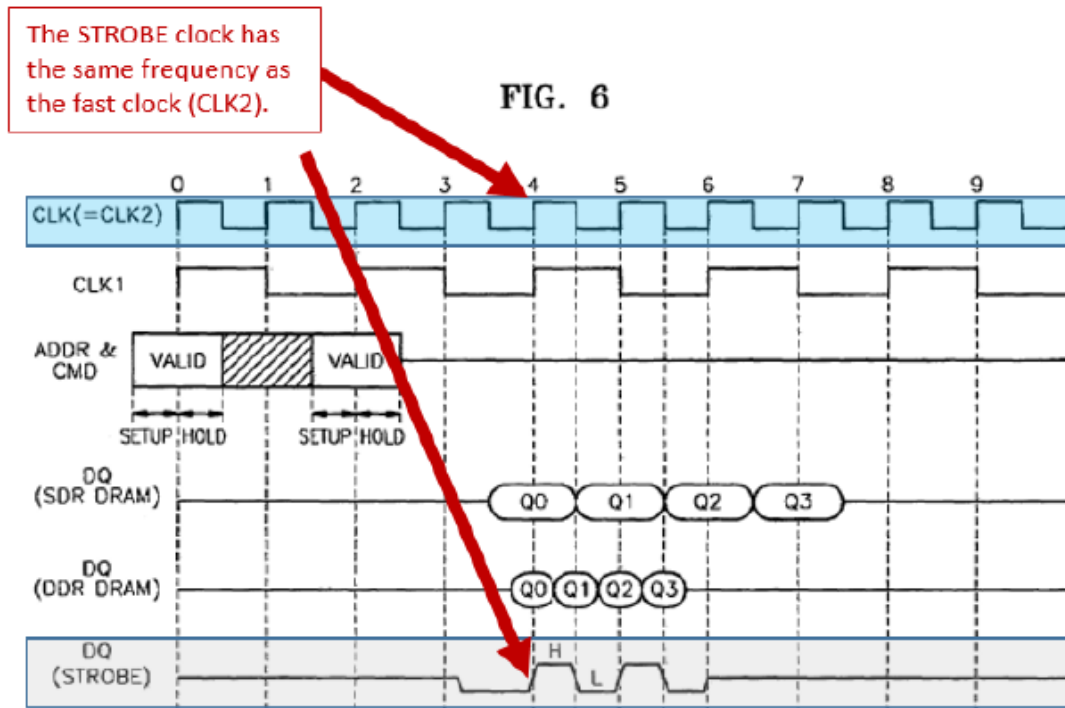


Figure 6 of Lee, reproduced above with Petitioner’s annotations (Pet. 59), is an operational timing diagram of semiconductor memory device 101 and memory chip 401 (Ex. 1004, 5:20–21, 5:43–45, 7:1–2) illustrating timing of

¹⁴ Patent Owner, again, contends the Petition does not include sufficient specificity. PO Resp. 46–48. We disagree and find the Petition explains sufficiently Petitioner’s reliance on the embodiment with two internal clocks and a strobe signal. *See, e.g.*, Pet. 7–9, 53–61, 71–78 (citing, *e.g.*, Ex. 1004, 2:47–50, 3:46–61, 4:18–22, 4:63–67, 6:37–45, 6:63–67, 7:18–42, 8:7–14, 9:18–19, 11:31–12:12, Fig. 6; Ex. 1003 ¶¶ 28, 49–63, 70–71, 77, 98, 109, 118–127, 173–178, 184–193, 211–219).

the first clock signal (CLK1) and the second clock signal (CLK2) (highlighted in blue), as well as the timing of the strobe signal STROBE (highlighted in gray) (*id.* at 7:18–42). Patent Owner contends, “nothing about Figure 6 or its textual description suggests that the STROBE signal illustrated in Figure 6 is associated with Lee’s second embodiment.” PO Resp. 55. Lee, however, describes Figure 6 as “an operational timing diagram of the semiconductor memory devices shown in FIG. 3 and 5.” Ex. 1004, 5:20–21; *see also id.* at 7:18–19 (“An operational timing diagram of the memory chips of the first and second embodiments is shown in FIG. 6.”) Figure 5 illustrates Lee’s second embodiment.

After considering all the evidence and arguments presented by the parties, for at least the aforementioned reasons, we are persuaded by Petitioner and credit and give substantial weight to Dr. Jacob’s testimony that Lee teaches or at least suggests using a strobe signal in addition to two external clock signals as Petitioner’s contentions and Dr. Jacob’s testimony are consistent with the evidence of record cited therein. *See, e.g.*, Pet. 7–9, 53–61, 71–78 (citing, *e.g.*, Ex. 1004, 2:47–50, 3:46–61, 4:18–22, 4:63–67, 6:37–45, 6:63–67, 7:18–42, 8:7–14, 9:18–19, 11:31–12:12, Fig. 6; Ex. 1003 ¶¶ 28, 49–63, 70–71, 77, 98, 109, 118–127, 173–178, 184–193, 211–219); *see also* Pet. Reply 18–21 (explaining that Lee discloses the STROBE signal being used in addition to its first and second clocks). Because we find that Lee teaches or at least suggests using a strobe signal in addition to two external clock signals, we need not determine whether the Petition shows sufficiently that it would have been obvious to one having ordinary skill in the art to combine the first embodiment of Lee with another embodiment not using a strobe signal.

We now turn to Patent Owner's second argument that the Petition does not present a rationale to combine Lee and Yoo (PO Resp. 58–63). In particular, Patent Owner contends the Petition lacks evidence of “a substantiated, non-conclusory explanation why one skilled in the art would have made the proposed combination of Lee and Yoo.” PO Resp. 62 (citing Ex. 1003 ¶¶ 126–27).

Regarding reasoning to combine, relying on the testimony of Dr. Jacob, Petitioner contends (1) modifying Lee with Yoo entails the use of known solutions to improve in the same way systems that are similar i.e., Lee and Yoo, which both use a system clock and strobe clock for read operations, and (2) a person having ordinary skill in the art would have been motivated to modify Lee with Yoo to achieve the synchronization benefits of generating a strobe clock for synchronizing read operations, where the strobe clock is generated from, and runs at the same frequency as, the data clock provided by the memory controller. *See, e.g.*, Pet. 71–78 (citing, *e.g.*, Ex. 1003 ¶¶ 118–27, 211–19). With respect to the modification advanced by Petitioner, Petitioner contends that a person having ordinary skill in the art

would have realized that Lee's memory system would be improved by incorporating the clock generation teachings of Yoo to generate, in Lee's memory device and without the use of a PLL or DLL, a strobe clock from the externally-received data clock, and to provide this strobe clock to the memory controller when performing read operations.

Id. at 74 (citing Ex. 1003 ¶¶ 118–27).

Patent Owner contends with the exception of paragraphs 126 and 127 of Dr. Jacob's Declaration, “[a]ll other assertions of obviousness in the petition . . . are merely attorney argument,” and “the petition's actual evidence in support [of] the obviousness of the Lee-Yoo combination is

insufficient.” PO Resp. 62. That Dr. Jacob does not repeat verbatim every assertion in the Petition does not result in Petitioner’s contentions being insufficient. Instead, we find Petitioner’s contentions persuasive and credit and give substantial weight to Dr. Jacob’s testimony, which supports sufficiently the contentions in the Petition. *See, e.g.*, Pet. 7–9, 71–78; Ex. 1003 ¶¶ 52–63, 109, 118–127, 185–193, 211–219. Furthermore, many of the contentions in the Petition, supported by the testimony of Dr. Jacob, are unrebutted by Patent Owner. *See generally* PO Resp.¹⁵

We are persuaded by Petitioner’s contentions and we credit and give substantial weight to Dr. Jacob’s testimony that modifying Lee with Yoo entails the use of a known solution, i.e., Yoo’s signal generation technique, to improve in the same, predictable way Lee’s system that is similar to Yoo because Petitioner’s contentions and Dr. Jacob’s testimony are consistent with the evidence cited therein. *See, e.g.*, Pet. 7–9, 71–78; Ex. 1003 ¶¶ 52–63, 118–127, 109, 185–193, 211–219. Regarding how Lee and Yoo are similar, starting with Lee, for the reasons discussed in Sections II.D.2 and II.D.4, we are persuaded by the Petition and credit and give substantial weight to Dr. Jacob’s testimony that Lee discloses the same memory device, i.e., a dynamic random access memory (DRAM) device as the example in the ’122 Patent. Turning to Yoo, Dr. Jacob testifies, “Yoo places the invention in the context of DDR SDRAM, in which the general-purpose system clock is used to process command and address information, and the

¹⁵ As set forth in our Order of June 22, 2017, issued with our Decision on Institution, Patent Owner has been cautioned, “that any arguments for patentability not raised in the response will be deemed waived.” Paper 10, 3.

data clock is used to process data beats.” Ex. 1003 ¶ 118 (citing Ex. 1006, Figs. 1, 2). Consistent with Dr. Jacob’s testimony, Yoo’s teachings pertain to a semiconductor memory device (Ex. 1006, 1:9–11) such as “a double data rate (DDR) synchronous dynamic random access memory (SDRAM)” (*id.* at 1:40–42), which receives an external clock signal for performing data operations (*id.* at Figs. 1, 2), and uses a strobe signal for data read operations (Ex. 1006, (57), 4:23–31, 5:56–6:9, Fig. 7).

Patent Owner’s contention that the Petition lacks evidence of why one skilled in the art would have modified Lee with Yoo pertains to paragraphs 126 and 127 of Dr. Jacob’s Declaration. PO Resp. 58–63. Dr. Jacob testifies as follows:

It makes sense to combine Lee and Yoo, and a person of ordinary skill would have found it straightforward to do so. As described previously, Lee discloses a *DQ Strobe* signal, which a person of ordinary skill would have found obvious to generate from an external free-running system clock. Yoo’s Figure 7 shows a circuit arrangement that would do precisely this. Thus, a person of ordinary skill in the art would have been motivated to combine Yoo with Lee, because Yoo explicitly shows the internal detail (in Yoo’s case the generation of the internal strobe and control signals from the external, free-running system clock) that is implicit, but not explicitly shown, in Lee. In addition, Yoo discloses how the external clock signal *CLK* can be used to generate a same-frequency *STROBE* signal that is transmitted from the memory device to the memory controller, thereby providing the *STROBE* signal to the memory controller in conjunction with read data on read operations.

Ex. 1003 ¶ 126. Dr. Jacob further testifies that Lee and Yoo “are very similar,” and both are “in the field of synchronous memory-system design,” and “implement double-data-rate clocking of data.” *Id.* ¶ 127.

Patent Owner contends that Dr. Jacob’s testimony lacks “why one skilled in the art would have combined the teachings of Lee and Yoo,” and instead establishes “only feasibility, not any desirability.” PO Resp. 59; *see also id.* at 62 (“Paragraph 127 is similarly deficient, as it merely lists similarities between Lee and Yoo”). Even with respect to Dr. Jacob’s testimony that a person of ordinary skill in the art “would have been motivated” (Ex. 1003 ¶ 126), Patent Owner contends that this testimony pertains to feasibility, not desirability and is based on an “unproven but critical assumption . . . that Lee implicitly generates his strobe signal from an external clock.” PO Resp. 61.

Dr. Jacob, however, testifies that a person of ordinary skill in the art “would have been motivated” because “Yoo explicitly shows . . . internal detail” regarding using the external clock signal to generate a same-frequency *STROBE* signal, such as Lee’s “*DQ Strobe* signal.” Ex. 1003 ¶ 126. We find that Dr. Jacob’s testimony is not limited to feasibility, but that Dr. Jacob also expressly testifies that a person of ordinary skill in the art “would have been motivated” and points to disclosure in the asserted art that is evidence of such motivation, i.e., Lee’s teachings of using a strobe signal and Yoo’s teachings of generating such a strobe internally. *See, e.g.*, Ex. 1003 ¶ 118–126, 185–193. Furthermore, we do not find that Dr. Jacob’s testimony is based on an assumption regarding Lee’s generation of the strobe and, indeed, Dr. Jacob testifies regarding the detail that is missing from Lee, but would have been obvious. *Id.* ¶¶ 126, 185. To the extent that Patent Owner’s contentions are premised on its earlier contentions that Lee does not disclose using a strobe signal in connection with two external clock

signals, for the reasons set forth *supra* in this Section, we agree with Petitioner and Dr. Jacob in that regard.

As Petitioner explains, Yoo provides detail regarding generating a read clock signal (i.e., a strobe signal) from an external clock signal and Lee's system employs such a strobe signal with two external clock signals. *See, e.g.*, Pet. 7–9, 71–78. Given the evidence before us, we determine that Petitioner has demonstrated sufficiently that it would have been obvious and predictable, in light of Yoo (*see, e.g.*, Ex. 1006, (57), 4:23–31, 5:56–6:9, Fig. 7), to generate a read clock signal in Lee's system from the second clock signal (CLK2) illustrated, for example, in Figures 5 and 6 of Lee (*see, e.g.*, Ex. 1004, 6:37–45, 7:36–42, 11:31–53, Figs. 5, 6). *See KSR*, 550 U.S. at 417 (“[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.”)¹⁶

We also are persuaded by Petitioner's contentions and we credit and give substantial weight to Dr. Jacob's testimony that a person having ordinary skill in the art would have been motivated to modify Lee with Yoo to achieve the synchronization benefits of generating a strobe clock for synchronizing read operations, where the strobe clock is generated from, and

¹⁶ Patent Owner contends that Yoo's strobe is from the memory device to the memory controller, whereas Lee's strobe signal goes in the opposite direction. PO Resp. at 63–64 (citing Ex. 2003 ¶ 74; Ex. 2007, 44:8–22). We find that Petitioner has specified sufficiently the manner in which Lee is modified and, in particular, modifying Lee's strobe signal to incorporate Yoo's technique of generating the read clock signal internally to establish that claim 2 would have been obvious. *See, e.g.*, Pet. 7–9, 71–78.

runs at the same frequency as, the data clock provided by the memory controller because Petitioner's contentions and Dr. Jacob's testimony are consistent with the evidence cited therein. *See, e.g.*, Pet. 7–9, 71–78; Ex. 1003 ¶¶ 52–63, 118–127, 109, 185–193, 211–219. Starting with Lee, consistent with Petitioner's contentions and Dr. Jacob's testimony (*id.*), Figure 6 and related teachings of Lee illustrate that the STROBE and CLK2 signals have the same frequency and are in phase. Ex. 1004, 7:18–42, Fig. 6. Turning to Yoo, consistent with Petitioner's contentions and Dr. Jacob's testimony (*see, e.g.*, Pet. 73–78; Ex. 1003 ¶¶ 215–219), Yoo teaches synchronizing data transfer e.g., reading data using strobe signals. Ex. 1006, (57), 2:33–36, 2:49–57, 4:17–35. Additionally, Yoo teaches benefits of generating the strobe clock for read operations without use of a PLL or DLL. *See, e.g.*, Ex. 1006, 7:1–8; *see also id.* at 2:8–15 (explaining that incorporating a PLL or DLL in a memory device contributes to design complexity, increased chip area, and yield deterioration).

As further reasoning, Petitioner points to evidence that such a clock generation technique would have been seen as a common technique for generating Lee's strobe signal. Pet. 59–61. For example, Petitioner points to certain of Lee's teachings that Petitioner contends support that internal clock generation was common. Pet. 60 (citing Ex. 1004, 4:18–22, 9:18–19). Consistent with Petitioner's contentions (*id.*), Lee teaches the memory module generating multiple internal clock signals using an external clock signal. *See, e.g.*, Ex. 1004, 9:18–19; *see also id.* at 5:49–6:12 (“clock buffer 310 receives a clock signal CLK (referred to herein as an ‘external clock signal’) loaded on a CLOCK BUS, and generates internal clock signals CLK1 and CLK2”). Petitioner also cites to Dr. Jacob's testimony that a

person having ordinary skill in the art would have seen Yoo’s technique as a common way to generate Lee’s strobe signal. Pet. 60; Ex. 1003 ¶ 185 (“[A] person of ordinary skill would have found it obvious to generate the STROBE signal from the CLK2 signal received by the memory device and would have found it obvious to transmit the generated STROBE signal back to the controller, along with the data, on read operations, as this is precisely what . . . various JEDEC DDRx SDRAM standards had been doing since DDR1 SDRAM appeared in the late 1990’s.”)¹⁷

Based on the evidence and arguments presented by the parties, Petitioner has articulated sufficient reasoning with rational underpinning to support the conclusion that one having ordinary skill would have had reason to modify the teachings of Lee to incorporate Yoo’s teachings, in the manner advanced by Petitioner. See *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

We turn to Patent Owner’s third argument that Yoo does not teach how to generate a read clock signal from a received clock signal (PO Resp. 63–64). Patent Owner contends that the timing of transitions are determined by a control signal, not a clock signal (CLK or intCLK-RD). PO Resp. 63 (citing Ex. 2003 ¶¶ 75–83). Patent Owner, more specifically, contends that “[t]he petition relies on Yoo’s Figure 7, but *that drawing* [Figure 7] does not show the input generating the STROBE output.” *Id.* at 63 (citing Ex.

¹⁷ Patent Owner mischaracterizes the Institution Decision, in which we noted with respect to the ground of obviousness over Lee alone that Dr. Jacob does not identify with sufficient precision, or provide copies of the standards. Inst. Dec. 18–19. As discussed *infra* in this Section and in Section II.D.7, we, however, need not address these mischaracterizations in light of our other determinations.

2003 ¶ 74) (emphasis added). Patent Owner, relying on eight paragraphs of Declaration testimony of Dr. Przybylski without explanation in the Patent Owner Response, contends that “the timing of transitions in Lee’s STROBE (and data signal DQ) signal in Figure 7 are determined by a control signal CTRL, not CLK or intCLK-RD.” *Id.* (citing Ex. 2003 ¶¶ 75–83). Dr. Przybylski’s testimony, similarly, pertains to Figure 7 of Yoo and related description. *See* Ex. 2003 ¶¶ 75–83 (citing Ex. 1006, 5:27–6:29, Fig. 7).

As an initial matter, Patent Owner does not respond to all teachings relied upon in the Petition. *See* Pet. 71–78 (citing, *e.g.*, Ex. 1006, (57), 2:33–36, 2:49–57, 4:23–31, 4:41–46, 5:36–38, 5:56–6:29, 7:1–8, Figs. 3, 4, 7). The further recitation of claim 2 that is the subject of the dispute is “a read clock signal generated from the second clock signal.” Consistent with Petitioner’s contentions (*id.*), and Dr. Jacob’s testimony (Ex. 1003 ¶¶ 118–127, 211–219), in other portions of Yoo not discussed by Patent Owner, Yoo teaches a memory device generating internally a strobe signal (STROBE) for data read operations. *See, e.g.*, Ex. 1006, (57) (“In a read operation, the semiconductor memory device generates a first strobe signal synchronized with a read data signal”), 2:33–36 (“[A] semiconductor memory device is provided which includes an output section generating a first strobe signal synchronized with a read data signal in a read operation”), 2:49–57 (“[A] method for controlling data input/output of a semiconductor memory device includes generating a first strobe signal synchronized with a read data signal in a read operation”), 4:23–31 (“[I]n data transfers under control of memory controller 23, STROBE is internally generated in memory controller 23 . . . in data transfers under control of memory device 21, STROBE is internally generated and synchronized with DQ in memory device 21”), 4:41–46

(“STROBE pulses can be initiated from a quiescent tri-state condition using a preamble signal before a DQ sequence as shown in FIG. 3, or the pulses can be free-running as shown in FIG. 4 . . . [in both figures] STROBE is generated through a same length path as DQ to insure that synchronization between DQ and STROBE can be maintained”).

We turn to whether Yoo teaches that its memory device generates internally a strobe signal for data read operations from the externally-received clock, as Petitioner contends. Pet. 75–78 (citing, *e.g.*, Ex. 1004, 2:33–36, 5:36–38, 5:56–6:9, Figs. 3, 4, 7; Ex. 1003 ¶¶ 118–127, 211–219). After considering all the evidence and argument presented by the parties, we agree with Petitioner and find that Yoo teaches that its memory device generates internally the strobe signal for data read operations from the externally-received clock. We credit the testimony of Dr. Jacob over that of Dr. Przybylski in that regard because, as explained below, unlike Dr. Jacob’s testimony, Dr. Przybylski’s testimony is not consistent with Lee’s disclosure.

Dr. Jacob testifies that Yoo teaches “generating the **STROBE** signal from the global clock signal **CLK** [external clock signal] on the memory-device side.” Ex. 1003 ¶ 124 (citing, *e.g.*, Ex. 1006, Fig. 7); *see also id.* ¶¶ 122–123 (citing, *e.g.*, Ex. 1006, Figs. 5, 6) (testifying that Yoo teaches generating an internal timing strobe from an external clock signal). Dr. Jacob further testifies “[t]he external data clock **CLK** is received by the Clock Driver 75, which uses **CLK** to generate two internal data clocks called **intCLK-WR** and **intCLK-RD**” and “as shown in the Output Section 71b, the internal **intCLK-RD** signal is used to drive a read strobe signal out the

STROBE pin.” *Id.* ¶ 125. Dr. Jacob provides annotations to Figure 7 of Yoo, which is reproduced below.

FIG. 7

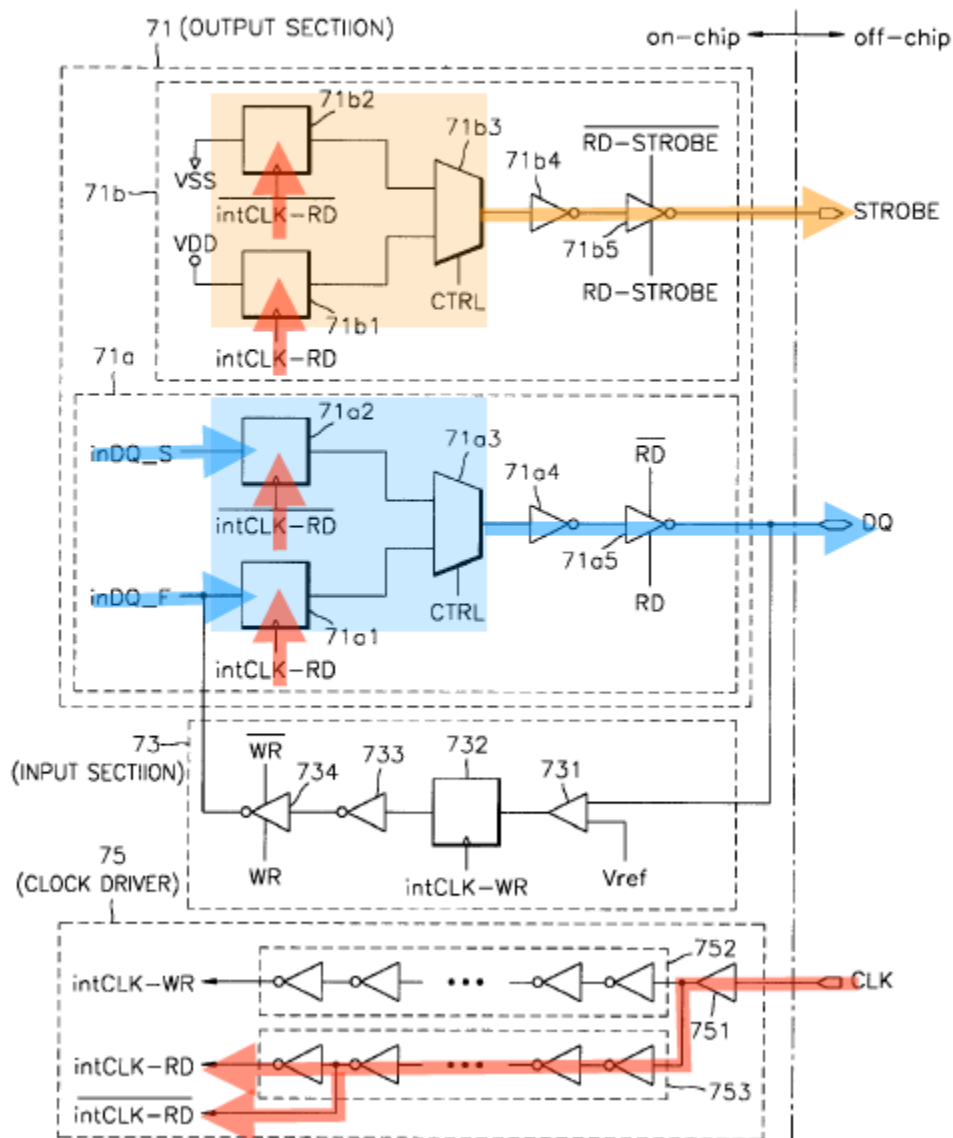


Figure 7 of Yoo, reproduced above, illustrates a circuit diagram of an input/output circuit of memory device 11 having an output section 71, an input section 73, and a clock driver 75 (Ex. 1006, 5:27–30) and includes Dr. Jacob’s annotations showing the signaling path for input operations

highlighted in red, the Output Section 71a highlighted in blue, and the Output Section 71b used to drive the strobe signal highlighted in orange (Ex. 1003 ¶¶ 124–125). Consistent with Dr. Jacob’s testimony (*see, e.g.*, Ex. 1003 ¶¶ 118–125), Figure 7 of Yoo illustrates that clock driver 75 receives the external clock and generates, for example, intCLK-RD, which then is input into the STROBE generation circuit. Ex. 1007, Fig. 7; *see also id.* at 5:29–38 (“The output section 71 generates the STROBE synchronized with the read data signal in a read operation, . . . [c]lock driver 75 buffers CLK and generates a first internal clock (intCLK-WR) for a write operation and a second internal clock (intCLK-RD) for a read operation”)

Dr. Przybylski testifies

[T]he inputs to flip flops 71b1 and 71b2 are tied to fixed values (VDD and VSS denote the fixed power supplies and their voltages correspond to a binary 1 and 0 respectively). Because the inputs to these flip flops are fixed, they repeatedly capture the exact same value over and over again, and their outputs do not change. They have no real function in the circuit. Consequently their outputs are fixed and there is no transition in them . . . in any way related to the timing of the intCLK-RD internal clock signal.

Ex. 2003 ¶ 80.

We credit and give substantial weight to Dr. Jacob’s testimony (Ex. 1003 ¶¶ 118–127, 211–219) because it is consistent with Yoo’s teachings. In addition to Yoo’s Figure 7 illustrating receipt of the external clock, which is used to generate intCLK-RD (and the inverted clock $\overline{\text{intCLK}} - \text{RD}$), which then are input into the STROBE generation circuit (Ex. 1006, Fig. 7), Yoo teaches that the strobe signal generator 71b, which includes latches 71b1 and 71b2 (*id.* at 5:59–60) uses the internally generated clock signals. In particular, Yoo teaches:

Latch 71b1 stores a power voltage (VDD) as logic high state in response to intCLK-RD. Latch 71b2 stores a ground voltage (VSS) as logic low state in response to an inverted clock intCLK – RD of intCLK-RD, i.e., the falling edges of intCLK-RD. Multiplexer 71b3 selects one of the output signals of latches 71b1 and 71b2 in response to a control signal (CTRL). Inverter 71b4 inverts the output signal of multiplexer 71b3, and tri-state inverting buffer 71b5 inverts and buffers the output signal of 71b4. The resulting data signal is outputted externally as STROBE in response to a strobe control signal (RD-STROBE). As explained above, since STROBE is generated through the same path as an output path of the read data signal, STROBE and the read data signal as outputted through the input/output pin (DQ) are synchronized with each other.

Ex. 1006, 5:62–6:10. Consistent with Dr. Jacob’s testimony (Ex. 1003 ¶¶ 118–127, 211–219), Yoo expressly teaches that strobe signal generator 71b stores a power voltage (VDD) as logic high state in response to intCLK-RD and stores a ground voltage (VSS) as logic low state in response to the inverted clock. Ex. 1006, 5:62–6:10.¹⁸

Also pertinent to the dispute between the parties in the portion of Yoo reproduced above is that the STROBE is generated through the same path as the read data signal so that the STROBE and the read data signal are synchronized with each other. *Id.* The parties do not dispute that the read data signal is synchronized with the internal clock signal, i.e., intCLK-RD.

¹⁸ Although not necessary for our analysis or conclusion, as further evidence supporting our reasoning, we credit and give substantial weight to Dr. Jacob’s supplemental testimony (Ex. 1011), which we find also is consistent with Yoo’s teachings, after consideration of Patent Owner’s observations (PO Mot. Obs.). For instance, Dr. Jacob’s testimony “if the intCLK-RD signal were to be removed,” then “[t]he STROBE output signal would . . . never toggle back and forth between 0 and 1” (Ex. 1011 ¶ 17) is consistent with the aforementioned teachings in Yoo (Ex. 1006, 5:62–6:10).

For example, Dr. Przybylski testifies “flip flops 71a1 and 71a2 capture the internal data stream and synchronize it with the intCLK-RD internal clock signal,” and “[t]he outputs of flip flops 71a1 and 71a2 change with the changing read data.” Ex. 2003 ¶ 80.

As expressly taught by Yoo, and as illustrated in Figure 7, “[s]trobe signal generator 71b is configured similarly to the read data output section 71a in order to synchronize STROBE with the read data outputted through the input/output pin (DQ).” Ex. 1006, 5:56–59. Both strobe signal generator 71b and read data output section 71a perform storage operations in response to intCLK-RD and inverted clock $\overline{\text{intCLK} - \text{RD}}$ of intCLK-RD and both include a multiplexer that selects an output signal in response to a control signal. Ex. 1006, 5:45–6:10, Fig. 7. Indeed, Dr. Przybylski testifies that the digital circuit elements numbered 71b1 and 71b2 of strobe signal generator 71b “are identical to their counterparts” in read data output section 71a “so that the timing of the output of . . . multiplexers 71a3 and 71b3 are as similar as possible under all operating conditions.” Ex. 2003 ¶ 83. Dr. Przybylski’s testimony that the digital circuit elements of strobe signal generator 71b (numbered 71b1 and 71b2) “have no real function in the circuit” and “there is no transition in them . . . [in any way] relat[ing] to the timing of the intCLK-RD internal clock signal” (Ex. 2003 ¶ 80) does not take into account the full teachings of Yoo, as set forth above.¹⁹ Claim 2

¹⁹ Although not necessary for our analysis or conclusion, as further evidence supporting our reasoning, after consideration of Patent Owner’s observations (PO Mot. Obs.), we credit and give substantial weight to Dr. Jacob’s supplemental testimony (*see, e.g.*, Ex. 1011 ¶¶ 8–17) because we find that his testimony is consistent with Yoo’s teachings cited therein.

does not require that frequency of the read clock signal matches the frequency of the second clock signal, but for reasons discussed *infra* in Section II.E.5 with respect to claim 3, we are persuaded by Petitioner's contentions and Dr. Jacob's testimony that Lee modified to incorporate Yoo, in the manner advanced by Petitioner, addresses the further recitation in claim 3.

Dr. Przybylski testifies, "[w]hat Yoo calls latches (e.g., 71b1 and 71b2) are flip flops." Ex. 2003 ¶ 76. As Dr. Przybylski acknowledges, Yoo refers to these devices as latches. Ex. 1006, 5:39–6:20. Dr. Jacob testifies that 71b1 and 71b2 are latches, but additionally that his original analysis (Ex. 1003) does not depend on whether 71b1 and 71b2 are latches or flip flops. *See, e.g.*, Ex. 1011 ¶¶ 5–7. Again, we credit Dr. Jacob's testimony in this regard, as it is consistent with Yoo's teachings. Ex. 1006, 5:39–6:20.

For the reasons given, we are persuaded Petitioner sufficiently establishes that claim 2 is unpatentable over the combined teachings of Lee and Yoo, and adopt as our own findings Petitioner's analysis of Lee and Yoo.

4. *Discussion of Independent Claim 28*

Independent claim 28 is similar to claim 1, except that it includes the further recitation of providing a read clock signal generated from the second clock signal discussed above with respect to dependent claim 2. Petitioner's contentions for claim 28 are the same and, indeed, include references to the same contentions discussed with respect to other independent claims and claim 2. *See, e.g.*, Pet. 7–9, 68–72, 84–85. Patent Owner does not argue this claim separately. *See generally* PO Resp.

For the reasons given with respect to the other independent claims and claim 2, we are persuaded Petitioner sufficiently establishes that claim 28 is unpatentable over the combined teachings of Lee and Yoo, and adopt as our own findings Petitioner's analysis of Lee and Yoo.

5. *Discussion of Claims 3, 4, 10–12, 17–19, and 21–23*

Turning now to claims 3, 4, 10–12, 17–19, and 21–23, Petitioner asserts that the combination of Lee and Yoo teaches all elements of these claims and provides a rationale for combining the teachings of Lee and Yoo. Pet. 7–9, 53–62, 65–67, 71–83. Patent Owner does not argue these claims separately.

Each of claims 10, 17, and 21 depends directly from claim 9, 16, or 20 and, otherwise, is similar to claim 2. Petitioner's contentions for claim 10 are the same as discussed with respect to claim 2. Pet. 7–9, 53, 55–62, 71–80. Petitioner's contentions for claims 17 and 21 include references to the same contentions discussed with respect to independent claims and claim 2. *See, e.g.*, Pet. 65–67, 81–83. Patent Owner does not argue the claims separately. *See generally* PO Resp. We find that Petitioner has shown sufficiently unpatentability of claims 10, 17, and 21 for the same reasons given with respect to the independent claims and claim 2.

Turning now to claims 3, 11, 18, and 22, each of these claims depends from claim 2, 10, 17, and 21 and further recites that the read clock signal has a frequency that matches the frequency of the second clock signal. For the reasons discussed *supra* in Section II.E.3 with respect to claim 2 and *infra* in this Section, we are persuaded by Petitioner's contentions and credit and give substantial weight to the testimony of Dr. Jacob that claims 3, 11, 18, and 22 would have been obvious over Lee modified with Yoo, in the manner

advanced by Petitioner. We find that Petitioner’s contentions and Dr. Jacob’s testimony are consistent with the teachings of Yoo and Lee. *See, e.g.*, Pet. 54, 62, 65, 66, 72, 79, 81, 82; Ex. 1003 ¶¶ 118–127, 184–193, 211–219.

For instance, consistent with Petitioner’s contentions and Dr. Jacob’s testimony (*id.*) as expressly taught by Yoo, and as illustrated in Figure 7, “[s]trobe signal generator 71*b* is configured similarly to the read data output section 71*a* in order to synchronize STROBE with the read data outputted through the input/output pin (DQ).” Ex. 1006, 5:56–59; *see also id.* at 6:8–10 (describing that STROBE and the read data signal as outputted are synchronized with each other), Fig. 7 (illustrating the same path for STROBE and the output of the read data signal). The read data is synchronized with the internal clock signal, i.e., intCLK-RD, which is derived from the external signal. *Id.* at 5:39–61, 6:21–29, Fig. 7.²⁰ Both strobe signal generator 71*b* and read data output section 71*a* perform storage operations in response to intCLK-RD and inverted clock $\overline{\text{intCLK} - \text{RD}}$ of intCLK-RD and both include a multiplexer that selects an output signal in response to a control signal. Ex. 1006, 5:45–6:10, Fig. 7; *see also id.* at Figs. 3–4 (illustrating read timing diagrams of the semiconductor memory devices).

That “CTRL is involved in the generation of STROBE” (PO Mot. Obs. 2–3) does not negate the aforementioned teachings in Yoo that of internally generating STROBE that has a frequency that matches the second

²⁰ This is not disputed by the parties, as discussed *supra* in Section II.E.3, with respect to claim 2.

clock signal. Consistent with Petitioner's contentions and Dr. Jacob's testimony (Pet. 72, 79, 81, 82; Ex. 1003 ¶¶ 118–27, 184–193, 211–219), in addition to the aforementioned teachings relating to Yoo's Figure 7, Yoo illustrates timing diagrams that teach that the read clock signal (STROBE) has a frequency which matches the frequency of the external clock signal (CLK). *See, e.g.*, Ex. 1006, 4:36–49, Figs. 3–5.

Also, we find that Lee's teachings are consistent with Petitioner's contentions and Dr. Jacob's testimony. *See, e.g.*, Pet. 54, 62, 65, 66, 72, 79, 81, 82; Ex. 1003 ¶¶ 118–127, 184–193, 211–219. For instance, Lee teaches that the frequency of the STROBE signal matches the frequency of the second clock signal (CLK2). Ex. 1004, Fig 6; *see also id.* at 7:36–41 (“[T]he data is input/output at both the rising and falling edges of the data strobe signal STROBE as shown in FIG. 6. This operation generally corresponds to that of the DDR DRAM.”).²¹

Each of claims 4, 12, 19, and 23 further requires generating the read signal without a phase-locked loop or a delay-locked loop. As Petitioner contends (Pet. 54, 62–67, 73, 74, 80–83) and as explained above with respect to claim 2, Yoo teaches memory device 11 that “does not have a phase synchronization device, such as a delay locked loop (DLL) or a phase locked loop (PLL).” Ex. 1004, 4:4–9; *see also id.* at 5:10–17 (“As explained above, the embodiments of the present invention eliminate the need for a separate phase synchroniz[ed] device such as DLL or PLL by using a

²¹ Furthermore, Lee teaches “[t]he relative frequencies of the first internal clock signal CLK1 and the second clock signal CLK2 are determined by the clock buffer 310 in response to a control signal CTRL” (Ex. 1004, 5:52–55) and “the frequency of the second internal clock signal CLK2 is substantially the same as that of the external clock signal CLK” (*id.* at 6:1–3).

controlled strobe signal (STROBE) in read and write operations”), 7:1–8 (describing performing data sampling “without a phase synchronization device such as a DLL or PLL”). Additionally, consistent with Petitioner’s contentions (Pet. 54, 62–67, 73, 74, 80–83), Yoo teaches that the STROBE is “internally generated” (Ex. 1004, 4:22–27), for example, by a strobe signal generator (*id.* at 5:56–6:30).

For the reasons given, we are persuaded Petitioner sufficiently establishes that each of claims 3, 4, 10–12, 17–19, and 21–23 is unpatentable over the combined teachings of Lee and Yoo, and adopt as our own findings Petitioner’s analysis of Lee and Yoo.

6. *Discussion of Claim 25–27*

As discussed *supra* in Section II.D.5, we determine that Petitioner has not shown by a preponderance of the evidence that claim 24 of the ’122 Patent is unpatentable, under § 102(b), as anticipated by Lee. As discussed *supra* in Section II.D.6, consistent with Patent Owner’s contentions (PO Resp. 41–42), the Petition does not include identification in Lee’s structure that corresponds to the line used by OCD 126 to transmit the RDQS2x signal to control device 102, as is set forth in the ’122 Patent Specification, or sufficient explanation or evidence as to why Lee’s structure is equivalent to the structure in the ’122 Patent Specification (*see, e.g.*, Ex. 1001, 4:35–38, 5:33–36, Fig. 1).

Petitioner’s contentions for dependent claims 25–27 do not remedy the aforementioned deficiencies. Pet. 67, 83, 93–94. For all grounds asserted with respect to claims 25–27, i.e., Lee alone, Lee and Yoo, and Lee, and, for claims 25 and 26, Lee and Kyung, Petitioner’s contentions pertain to

only the further recitations in these dependent claims. Pet. 67, 83, 93–94; Pet. Reply 17–28; Pet. Supp. Br.

During the hearing, Petitioner argued that Lee “has an interface where you have two clocks and a STROBE, the same interface as the 122 patent’s memory interface.” Tr. 10:20–22. Petitioner, however, does not rely on this embodiment for claim 24, and has not pointed to teachings in this embodiment for the “means for interfacing a control device.” Pet. 49–52. Petitioner’s obviousness contentions (*id.* at 67, 83, 93–94; Pet. Reply 17–28; Pet. Supp. Br.) do not identify teachings or provide argument or evidence explaining why the “means for interfacing a control device” would have been obvious over the asserted art. *See* 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”)

For the reasons given, we are not persuaded by Petitioner’s contentions that claims 25–27 are unpatentable, under § 103(a), as obvious over (1) Lee alone; or (2) the combined teachings of Lee and Yoo. We also are not persuaded by Petitioner’s contentions that claims 25 and 26 are unpatentable, under § 103(a), as obvious over the combined teachings of Lee and Kyung.

7. Conclusion

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 2–4, 10–12, 17–19, 21–23, and 28 of the ’122 Patent are unpatentable, under 35 U.S.C. § 103(a), as obvious over the combined teachings of Lee and Yoo. In light of the aforementioned unpatentability determination, we do not determine (1) whether these same claims also are unpatentable, under 35 U.S.C.

§ 103(a), as obvious over Lee; or (2) whether claims 2, 3, 10, 11, 17, 18, 21, 22, and 28 of the '122 Patent are unpatentable, under 35 U.S.C. § 103(a), as obvious over the combined teachings of Lee and Kyung.²²

Based on the entire trial record, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 25–27 are unpatentable, under 35 U.S.C. § 103(a), as obvious over (1) Lee alone or (2) the combined teachings of Lee and Yoo. We also determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 25 and 26 are unpatentable, under § 103(a), as obvious over the combined teachings of Lee and Kyung.

F. Obviousness over Lee and Gould (Claims 7 and 15)

Petitioner contends claims 7 and 15 are unpatentable, under 35 U.S.C. § 103(a), as obvious over Lee and Gould. Pet. 2.

1. Overview of Gould

Gould is directed to a memory system comprising a memory controller coupled to a memory device. Ex. 1007, 1:61–63. Gould teaches that the memory controller communicates to the memory device according to a bus protocol, such as double data rate (DDR) protocol or low power DDR (LPDDR) protocol. *Id.* at 2:66–3:6.

²² Accordingly, we need not address post-hearing contentions regarding obviousness based on Lee alone (PO Supp. Br.; Pet. Supp. Br.) for claims 2–4, 10–12, 17–19, 21–23, and 28 of the '122 Patent.

2. *Discussion of Claims 7 and 15*

Petitioner contends that the combination of Lee and Gould teaches all elements of claims 7 and 15 and provides a rationale for combining the teachings of Lee and Gould. Pet. 95–98.

Claim 7 and 15 depend from claim 1 and 9, respectively, and each further requires that the first and second clock signals are received across a low-power, double-data rate interface. Ex. 1001, 8:23–25, 8:61–63.

Petitioner points to Gould’s teachings of controller and device communications via a bus architecture using LPDDR protocol. Pet. 95–98 (citing Ex. 1007, 1:25–30, 1:61–63, 2:9–14, 2:24–25, 2:66–3:6). Relying on the testimony of Dr. Jacob, Petitioner also contends that a person of ordinary skill in the art would have been motivated to combine the teachings of Lee and Gould to improve the power efficiency of Lee’s memory system by incorporating Gould’s LPDDR interface. *Id.* (citing Ex. 1003 ¶¶ 128–131, 224–228).

We are persuaded by Petitioner’s contentions and we credit and give substantial weight to Dr. Jacob’s testimony (Pet. 95–98; Ex. 1003 ¶¶ 128–131, 224–228) because they are consistent with the evidence cited therein. For instance, Gould teaches a collection of buses that interconnect the memory controller and memory device (Ex. 1007, 2:9–18). Additionally, Gould teaches that communications are in accordance with a bus protocol, such as LPDDR. *Id.* at 3:1–6. Furthermore, Dr. Jacob testifies, for example, that Gould “would augment Lee’s synchronous memory system” and combining the teachings of Gould and Lee “would provide performance advantages in Lee’s system.” Ex. 1003 ¶ 131. Patent Owner does not argue these claims separately. *See generally* PO Resp.

For the reasons given, we are persuaded Petitioner sufficiently establishes that each of claims 7 and 15 are unpatentable over the combined teachings of Lee and Gould, and adopt as our own findings Petitioner's analysis of Lee and Gould.

3. *Conclusion*

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 7 and 15 of the '122 Patent are unpatentable, under 35 U.S.C. § 103(a), as obvious over the combined teachings of Lee and Gould.

G. Motion for Observations

We turn to Patent Owner's Motion for Observation on the cross-examination of Dr. Jacob (PO Mot. Obs.), as well as Petitioner's Response to the Motion (Pet. Resp.). To the extent Patent Owner's Observations pertain to testimony purportedly impacting Dr. Jacob's credibility, we have considered Patent Owner's observations and Petitioner's responses in rendering this Final Written Decision, and accorded Dr. Jacob's testimony appropriate weight in view of Patent Owner's observations and Petitioner's response to those observations.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has established by a preponderance of the evidence that claims 1–23 and 28 of the '122 Patent are unpatentable based on the following grounds:

Reference(s)	Basis	Challenged Claim(s)
Lee	§ 102(b)	1, 5, 6, 8, 9, 13, 14, 16, and 20
Lee and Yoo	§ 103(a)	2–4, 10–12, 17–19, 21–23, and 28
Lee and Gould	§ 103(a)	7 and 15

Petitioner has not shown by a preponderance of the evidence that claims 24–27 of the '122 Patent are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1–23 and 28 of the '122 Patent have been proven to be unpatentable;

FURTHER ORDERED that claims 24–27 of the '122 Patent have not been proven to be unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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