

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NETAPP, INC. and LENOVO (UNITED STATES) INC.,
Petitioner,

v.

INTELLECTUAL VENTURES II, LLC,
Patent Owner.

Case IPR2017-00416
Patent 6,516,442 B1

Before JUSTIN T. ARBES, BRIAN J. McNAMARA, and MINN CHUNG,
Administrative Patent Judges.

CHUNG, *Administrative Patent Judge.*

DECISION

Denying Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. BACKGROUND

A. Introduction

NetApp, Inc. and Lenovo (United States) Inc. (collectively, “Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1, 2, 8, 11, 12, 24, 25, 31, and 34 (the “challenged claims”) of U.S. Patent No. 6,516,442 B1 (Ex. 1001, “the ’442 patent”). Intellectual Ventures II, LLC (“Patent Owner”) filed a Preliminary Response (Paper 11, “Prelim. Resp.”). We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a).

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Upon consideration of the Petition and the Preliminary Response, we conclude that the information presented in the Petition does not establish a reasonable likelihood that Petitioner would prevail in showing the unpatentability of any of the challenged claims on the grounds set forth in the Petition. Accordingly, we deny Petitioner’s request to institute an *inter partes* review of claims 1, 2, 8, 11, 12, 24, 25, 31, and 34.

B. Related Proceedings

According to the parties, the ’442 patent has been asserted in the following patent infringement cases: *Intellectual Ventures I LLC v. HCC Insurance Holdings, Inc.*, No. 6:15-cv-660 (E.D. Tex.); *Intellectual Ventures II LLC v. Kemper Corp.*, No. 6:16-cv-081 (E.D. Tex.); *Intellectual Ventures*

I LLC v. Lenovo Group Ltd., No. 1:16-cv-10860 (D. Mass.); and *Intellectual Ventures I LLC v. NetApp, Inc.*, No. 1:16-cv-10868 (D. Mass.). Pet. 1–2; Paper 5, 1. The '442 patent is also the subject of an instituted trial in *EMC Corp. v. Intellectual Ventures II LLC*, Case IPR2016-01106.

II. THE '442 PATENT

A. Described Invention

The '442 patent describes a symmetric multiprocessor system that includes a switched fabric, such as a switch matrix, which provides multiple concurrent buses for transferring data between processors and shared memory. Ex. 1001, Abstract, col. 1, ll. 49–53. Figure 3 of the '442 patent is reproduced below.

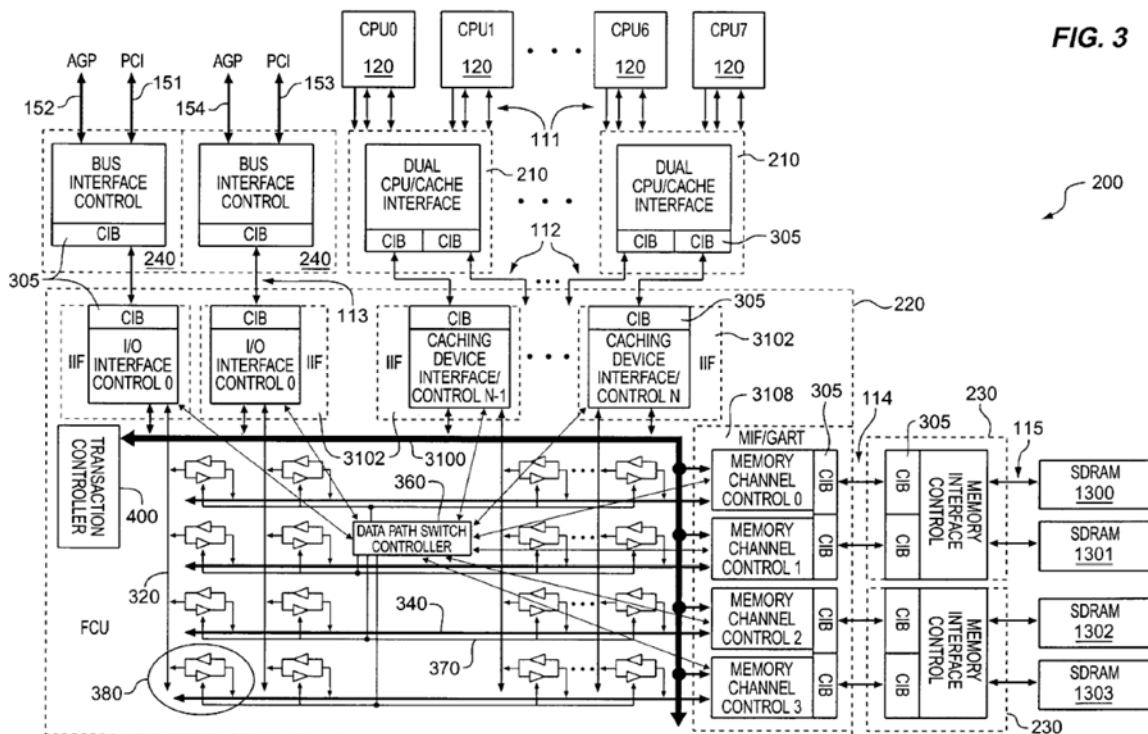


Figure 3 illustrates an embodiment of a symmetric multiprocessor system using a Flow-Control Unit (FCU) based on a switched fabric data path

architecture. *Id.* at col. 2, ll. 1–9. Figure 3 describes internal details of the components of the multiprocessor system depicted in Figure 2 (not reproduced herein). *Id.* As shown in Figure 3, FCU 220 includes a Data Switch, which is also referred to as a Simultaneous Switched Matrix (SSM) or switched fabric data path. *Id.* at col. 3, ll. 6–9. The Data Switch provides for parallel routing of data between multiple initiators and multiple targets (or destinations), such as CPUs and memory devices. *Id.* at col. 4, ll. 30–37.

The multiple, simultaneous data transfers over the Data Switch take place via a series of interfaces between the initiators and the targets. As depicted in Figures 2 and 3, CPU 120 and memory units 1300–1303 exchange data with processor and memory interfaces, namely, Dual CPU Interface Unit (DCIU) 210 and Memory Control Unit (MCU) 230, respectively. *Id.* at col. 2, ll. 65–67, col. 3, ll. 26–31, Figs. 2, 3. The DCIU and MCU, in turn, communicate with another set of interfaces on the switch or FCU side over point-to-point interconnect buses or channels 112 and 114, respectively, to transfer data through the Data Switch. *Id.* at col. 2, ll. 50–65, col. 3, ll. 36–42, col. 4, ll. 45–49, 59–65, Fig. 3. As illustrated in Figure 3, each of these interfaces uses a common block called the Channel Interface Block (CIB) to communicate over a channel. *Id.* at col. 7, ll. 38–42, Fig. 3. In other words, all communications or data transfers over a channel take place between a pair of CIBs positioned across the channel. *Id.*

According to the '442 patent, a channel “of the present invention is a general-purpose, high-speed, point-to-point, full-duplex, bi-directional interconnect bus suitable for use in a broad range of applications including computer memory, I/O, CPU, switching/routing, or any other application

where high bandwidth and low latency is required.” *Id.* at col. 6, ll. 40–45. A “packet” is a basic unit of transport over a channel. *Id.* at col. 6, l. 53. In one embodiment, a packet is a single 80-bit frame exchanged between CIBs. *Id.* at col. 6, ll. 54–55. A packet frame may include payload data, control information, and ECC bits.¹ *Id.* at col. 6, ll. 54–63. Each CIB performs error detection and error correction for data transfers over a channel. *Id.* at col. 15, ll. 42–45. According to the ’442 patent, although the ECC error detection code may be used for single-bit error correction, this is not done in the disclosed system. Instead, the data transfer is retried using a transport retry protocol. *Id.* at col. 16, ll. 50–55.

B. Illustrative Claim

Of the challenged claims, claims 1 and 24 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below:

1. A shared-memory multi-processor system comprising:
 - a switch fabric configured to switch packets containing data;
 - a plurality of channels configured to transfer the packets;
 - a plurality of switch interfaces configured to exchange the packets with the switch fabric, exchange the packets over the channels, and perform error correction of the data in the packets exchanged over the channels;
 - a plurality of microprocessor interfaces configured to exchange the data with a plurality of microprocessors, exchange the packets with the switch interfaces over the channels, and perform error correction of the data in the packets exchanged over the channels; and

¹ The ’442 patent describes ECC bits as “error detection bits” or an “error detection code.” Ex. 1001, col. 15, ll. 46–49, col. 16, ll. 50–55.

a memory interface configured to exchange the data with a memory device, exchange the packets with the switch interfaces over the channels, and perform error correction of the data in the packets exchanged over the channels.

Ex. 1001, col. 36, ll. 27–44.

III. PETITIONER’S CHALLENGES

A. Prior Art Cited in Petitioner’s Challenges

Petitioner cites the following references in its challenges to patentability:

Reference	Designation	Exhibit No.
U.S. Patent No. 4,845,722 (July 4, 1989)	Kent ²	Ex. 1002
Andrew S. Tanenbaum, <i>COMPUTER NETWORKS</i> (3rd ed., 1996) (© 1996)	Tanenbaum	Ex. 1003
U.S. Patent No. 5,521,913 (May 28, 1996)	Gridley	Ex. 1004
U.S. Patent No. 5,311,114 (May 10, 1994)	Sambamurthy	Ex. 1005

B. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 24):

Claims Challenged	Statutory Basis	Reference(s)
1, 8, 11, 12, 24, 31, and 34	§ 103(a)	Kent and Tanenbaum
1, 2, 8, 11, 12, 24, 25, 31, and 34	§ 103(a)	Kent, Tanenbaum, and Gridley

² For clarity and ease of reference, we only list the first named inventor.

Claims Challenged	Statutory Basis	Reference(s)
1, 8, 11, 12, 24, 31, and 34	§ 103(a)	Kent, Tanenbaum, and Sambamurthy
1, 2, 8, 11, 12, 24, 25, 31, and 34	§ 103(a)	Kent, Tanenbaum, Gridley, and Sambamurthy

IV. CLAIM CONSTRUCTION

Petitioner asserts that the claim terms in this proceeding should be given their broadest reasonable interpretation (BRI) in light of the Specification of the '442 patent. Pet. 7. Petitioner proposes constructions for four terms—namely, “interface,” “channels,” “perform error correction,” and “error correction codes”—under the BRI standard. *Id.* at 8–13.

Patent Owner certifies that the '442 patent will expire within 18 months from the entry of the Notice of Filing Date Accorded to Petition (Paper 9) in this case, and moves for the challenged claims in this proceeding to be construed in accordance with the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Paper 10, 1; Prelim. Resp. 13; 37 C.F.R. § 42.100(b). Patent Owner then proposes constructions under the *Phillips* standard for the preambles and the claim terms “memory device” and “channel” recited in the challenged claims. Prelim. Resp. 13–29.

Although we agree with Patent Owner that the challenged claims in this case should be interpreted in accordance with the standard set forth in *Phillips*, see *Black & Decker, Inc. v. Positec USA, Inc.*, 646 F. App'x 1019, 1024 (Fed. Cir. 2016) (unpublished) (holding that in an *inter partes* review,

“[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in [*Phillips*]”), and grant Patent Owner’s motion accordingly, we need not construe explicitly any of the claim terms discussed by the parties for purposes of this Decision. See *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (explaining that “claim terms need only be construed ‘to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

V. ANALYSIS OF PETITIONER’S PRIOR ART CHALLENGES

A. *Claims 1, 8, 11, 12, 24, 31, and 34 as Obvious Over Kent and Tanenbaum*

Petitioner contends claims 1, 8, 11, 12, 24, 31, and 34 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Kent and Tanenbaum. Pet. 24–47. Petitioner submits a Declaration of Mr. Ian Jestice (Ex. 1006) in support of its contentions. We have reviewed the parties’ contentions and supporting evidence. Given the evidence of record, we are not persuaded that Petitioner has established a reasonable likelihood of prevailing on this asserted ground as to any of these claims for the reasons explained below.

1. Overview of Kent (Ex. 1002)

Kent describes a computer interconnect coupler that includes crossbar switches. Ex. 1002, Title, col. 4, ll. 41–62. Figure 1 of Kent is reproduced below.

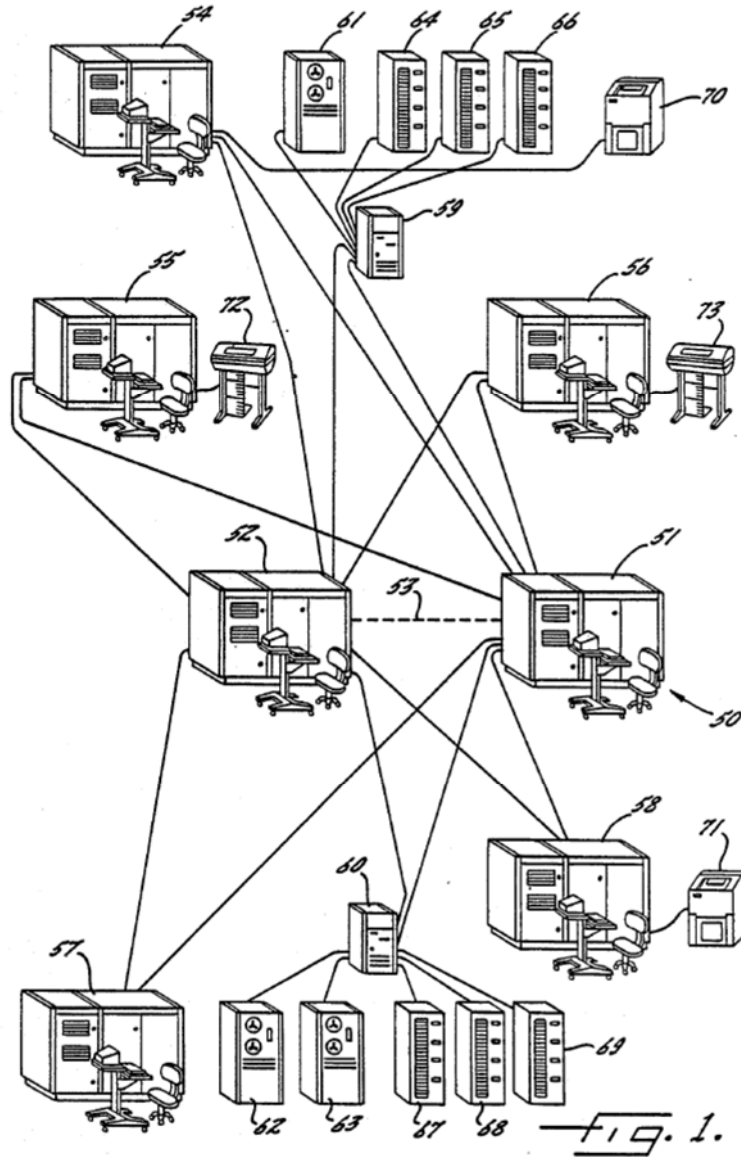


Figure 1 depicts a computer interconnect coupler that interconnects various data processing devices in an exemplary embodiment of Kent. *Id.* at col. 6, ll. 7–10, col. 7, ll. 53–56.

As shown in Figure 1 above, the data processing devices interconnected by coupler 50 (which comprises two identical couplers 51 and 52 that are linked together) include central processing units 54, 55, 56, 57, 58 and servers 59, 60 for magnetic tape drives 61, 62, 63 and mass data

storage or disk memories 64, 65, 66, 67, 68, 69. *Id.* at col. 7, l. 53–col. 8, l. 2. According to Kent, couplers 51 and 52 allow any data processing unit in the system to send a data packet to any other data processing unit within the system disclosed in Kent. *Id.* at col. 8, ll. 8–14. In an embodiment, each of couplers 51 and 52 is an electronic crossbar switch which routes a message from a source data processing device to a destination data processing device over a source channel, a switch matrix, and a destination channel. *Id.* at col. 8, l. 42–col. 9, l. 19, Fig. 2. As illustrated in Figure 2 (not reproduced herein), a channel is defined by a communication cable and interface circuits that interconnect a data processing device to the switch matrix. *Id.* at col. 8, ll. 44–50, Fig. 2.

2. Discussion

a. Claim 1

Independent claim 1 recites “a plurality of switch interfaces configured to exchange the packets with the switch fabric, exchange the packets over the channels, and perform error correction of the data in the packets exchanged over the channels.” Petitioner contends that Kent’s disclosure of the couplers combined with Tanenbaum’s teaching of error correction teaches this limitation. Pet. 27–32. Referencing Figure 2 of Kent, Petitioner asserts that interface circuitry 82 and 83, receiver logic 84 and 94, and transmission logic 92 and 97 contained within coupler 51 constitute “switch interfaces,” as recited in claim 1. *Id.* at 28 (citing Ex. 1002, Fig. 2). Petitioner further asserts that the switch interfaces of Kent exchange packets with switch matrix 87 and 90, i.e., the claimed “switch

fabric.” *Id.* (citing Ex. 1002, col. 8, l. 68–col. 9, l. 10). Petitioner argues that Kent also teaches “switch interfaces configured to . . . exchange the packets over the channels,” as recited in the claim, because Kent describes routing messages from a source channel X to a destination channel Y over the switch interfaces. *Id.* at 28–29 (citing Ex. 1002, col. 8, ll. 52–55, col. 8, l. 68–col. 9, l. 10, col. 9, ll. 15–19).

With regard to the switch interfaces performing the “error correction” as claimed, Petitioner acknowledges that, although Kent discloses data packets containing CRC (cyclic redundancy check) codes, Kent does not provide express disclosure of using the CRC codes to detect and correct data transmission errors. *Id.* at 29 (citing Ex. 1002, col. 21, l. 59–col. 22, l. 5). Petitioner argues that, in order to understand how to apply the CRC codes contained in Kent’s packets to achieve reliable data transmission, a person of ordinary skill in the art would have turned to a reference book, such as Tanenbaum (Ex. 1003). *Id.* at 29–30. According to Petitioner, Tanenbaum describes a data retransmission protocol using CRC codes as well as special feedback messages or control frames (known as ACK or NAK packets) to detect and correct data transmission errors. *Id.* at 30–31 (citing Ex. 1003, 175, 179, 182). As described in Tanenbaum, when a data packet is received at the destination, the receiving device checks for transmission error by computing the CRC code or checksum of the data and comparing it against the CRC code included in the packet. *Id.* at 30 (citing Ex. 1003, 179). If no error is detected, the receiving device (or the destination device) sends a positive acknowledgement to the transmitting device (or the source device) in the form of an ACK packet. *Id.* (citing Ex. 1003, 182). If a transmission

error is detected, the receiving device sends a negative acknowledgement, i.e., a NAK packet, back to the transmitting device to indicate that the transmission failed and that the data packet must be transmitted again. *Id.*

Petitioner asserts that Kent’s disclosure of the use of acknowledgment packets and CRC codes combined with Tanenbaum’s detailed disclosure of the ACK/NAK retransmission protocol teaches “switch interfaces configured to . . . perform error correction of the data in the packets exchanged over the channels,” as recited in claim 1. *Id.* at 30–32 (citing Ex. 1002, col. 3, ll. 9–10, col. 9, ll. 20–27, 33–37, col. 13, ll. 56–65, col. 14, ll. 23–66; Ex. 1003, 175, 179, 182).

We are not persuaded by Petitioner’s argument because the portions of Kent and Tanenbaum cited by Petitioner describe that the ACK/NAK packets are sent by the receiving device (or the destination device) to the transmitting device (or the source device), not by an intermediary switch on its own. As discussed above, Tanenbaum describes the general ACK/NAK handshake process between a sender and a receiver, but mentions nothing specific about the function of a switch. *See* Ex. 1003, 182. As explained in what follows, the Petitioner-cited portions of Kent describe that the ACK/NAK handshake process takes place between the source device and the destination device, and the coupler simply passes the ACK/NAK packets between the source and the destination without any alteration or modification. Indeed, Petitioner acknowledges that, in Kent’s coupler, “[u]pon receiving the acknowledgement packet (ACK/NAK) *from the destination device*, the acknowledgement packet is transmitted *to the source device*.” Pet. 32 (citing Ex. 1002, col. 13, ll. 56–64) (emphases added).

The cited portions of Kent disclose the following.

Upon receipt of the message, *the addressed data processing device* returns an acknowledgment *to the source data processing device*. This acknowledgment is returned over the communication cable 85, *passes through the interface circuits* 83, and reaches associated receiver logic circuits 94.

Ex. 1002, col. 9, ll. 20–25 (emphases added).³ “The *return acknowledgment* is *passed* by the transmitter logic circuits 97 *to the interface circuits* 82 associated with channel X for return *to the data processing unit which initially sent the message*.” *Id.* at col. 9, ll. 33–37 (emphases added). “[A]n *acknowledgment from the destination data processing device* is returned over the assigned junctor and transmitted *to the source data processing device*.” *Id.* at col. 13, ll. 61–64 (emphases added). Hence, in Kent, the destination device checks for transmission error by using the CRC codes, generates ACK/NAK packets, and sends them to the source device. If a NAK packet is returned, the source device would retransmit the data packet to the destination device. In other words, in Kent, error correction is performed by the destination device and the source device, *not* the coupler or the claimed “switch interfaces.” Petitioner does not cite, nor do we discern, any disclosure in Kent or Tanenbaum that shows any portion or circuitry of

³ The “message” in these passages refers to the transmitted data packet. *See, e.g.,* Ex. 1002, col. 4, ll. 57–62 (“a computer interconnect coupler is provided which has a plurality of electronic crossbar switches each of which is connected to a communication port of a data processing devices to provide a communication channel for receiving *messages* from and sending *messages* to that device” (emphases added)), col. 8, ll. 43–45 (“Turning now to FIG. 2, there is shown a schematic diagram which illustrates the routing of a *message* from a source channel X to a destination channel Y.” (emphasis added)).

the coupler performing CRC checks or generating ACK/NAK packets to be sent to the source data processing device.

To show that the coupler or the switch interfaces of Kent in view of Tanenbaum perform error correction, Petitioner proposes to construe the term “perform error correction” to mean “to assist in the correction of an error” (Pet. 12–13) and argues that the switch interfaces “perform error correction” because they “assist in the correction of an error” by “*transmitting a NAK* which indicates an error in data transmission and a request for retransmission; by receiving the correct data packet from the source; and by subsequently transmitting of the correct data packet to the destination.” *Id.* at 32 (emphasis added).

Petitioner’s argument is unpersuasive because merely transmitting or passing a NAK packet through the coupler circuitry cannot be “perform[ing] error correction” under any reasonable interpretation of the term. Other than a single conclusory sentence stating its contention, Petitioner does not provide any explanation why merely “transmitting a NAK” constitutes “performing error correction” or “assisting in the correction of an error.” *Id.* Nor does Petitioner cite any evidence of record in support of its contention. As discussed in Section II.A above, the ’442 patent’s description of error correction includes single-bit correction using ECC codes and retransmission of packets. *See* Ex. 1001, col. 16, ll. 50–55. Similarly, Kent and Tanenbaum describe error detection and correction using CRC codes and retransmission based on the ACK/NAK handshake between the source and destination devices. *See* Ex. 1002, col. 3, l. 27–col. 4, l. 3; Ex. 1003, 179, 182. We do not discern anything in the record, nor does Petitioner cite

anything, that justifies understanding a mere transmission of a NAK packet through a switch as performing error correction.

Therefore, Petitioner does not demonstrate that the combination of Kent and Tanenbaum teaches “switch interfaces configured to . . . perform error correction of the data in the packets exchanged over the channels,” as recited in claim 1. Accordingly, the information presented in the Petition does not demonstrate a reasonable likelihood of Petitioner prevailing in its challenge to claim 1 under 35 U.S.C. § 103(a) as obvious over the combination of Kent and Tanenbaum.

b. Claim 24

Independent claim 24 recites “exchanging packets containing the data between the microprocessor interfaces and a plurality of switch interfaces over channels,” “exchanging the packets between the switch interfaces through a switch fabric,” and “exchanging the packets between the switch interfaces and a memory interface over the channels.” Ex. 1001, col. 38, ll. 27–34. Claim 24 also recites “in the interfaces, performing error correction of the data in the packets exchanged over the channels.” *Id.* at col. 38, ll. 37–38. We note that the term “the interfaces” recited in claim 24 refers to all of the interfaces recited in the claim, including the switch interfaces.

Petitioner relies on the same arguments and evidence advanced with respect to claim 1 to argue that the combination of Kent and Tanenbaum teaches the switch interfaces are configured to “perform[] error correction of the data in the packets exchanged over the channels,” as recited in claim 24. Pet. 47. Hence, for the same reasons discussed above with respect to claim

1, Petitioner does not demonstrate that the combination of Kent and Tanenbaum teaches the switch interfaces “performing error correction of the data in the packets exchanged over the channels,” as recited in claim 24.

Accordingly, the information presented in the Petition does not demonstrate a reasonable likelihood of Petitioner prevailing in its challenge to claim 24 under 35 U.S.C. § 103(a) as obvious over the combination of Kent and Tanenbaum.

c. Dependent Claims 8, 11, 12, 31, and 34

Claims 8, 11, 12, 31, and 34 depend from claims 1 or 24. Petitioner’s arguments and evidence presented with respect to these dependent claims do not remedy the deficiencies in Petitioner’s analysis of independent claims 1 and 24. Therefore, Petitioner does not demonstrate a reasonable likelihood of Petitioner prevailing in its challenge to claims 8, 11, 12, 31, and 34 under 35 U.S.C. § 103(a) as obvious over the combination of Kent and Tanenbaum.

B. Claims 1, 2, 8, 11, 12, 24, 25, 31, and 34 as Obvious Over Kent, Tanenbaum, and Gridley

Petitioner adds the teachings of Gridley (Ex. 1004) to the basic combination of Kent and Tanenbaum in an asserted ground of obviousness as to claims 1, 2, 8, 11, 12, 24, 25, 31, and 34. Pet. 48–60. For the reasons described below, Petitioner does not demonstrate a reasonable likelihood of prevailing on this asserted ground as to any of these challenged claims.

1. Overview of Gridley (Ex. 1004)

Gridley describes a packet switching system that employs an adaptive cut-through switching process. Ex. 1004, Abstract, col. 5, ll. 11–59. In Gridley’s switch, packets are accumulated in a packet RAM under control of a packet processor. *Id.* at col. 5, ll. 14–17. Under certain conditions, e.g., prior detection of an invalid packet, the entire packet is accumulated in the packet RAM until the packet has been fully received. *Id.* at col. 5, ll. 46–50. When a complete packet has been received, the validity of the packet is checked by computing a checksum. *Id.* at col. 5, ll. 50–52. If the packet turns out to be invalid, the packet processor discards the packet without forwarding it to the destination device. *Id.* at col. 5, ll. 52–54.

2. Discussion

a. Claim 1

(1) “a plurality of switch interfaces configured to . . . perform error correction of the data in the packets exchanged over the channels”

In its challenge to claim 1 in this asserted ground of unpatentability, Petitioner adds and relies on the teachings of Gridley *only* for the limitation reciting “a plurality of switch interfaces configured to exchange the packets with the switch fabric, exchange the packets over the channels, and perform error correction of the data in the packets exchanged over the channels.” See Pet. 49–51. With respect to the rest of the limitations of claim 1, Petitioner relies on the same arguments and evidence it presented in the ground of challenge based on Kent and Tanenbaum alone discussed above. *Id.* at 49, 51.

Petitioner asserts that the switch interface of Kent and Tanenbaum as modified by Gridley teaches or renders obvious “switch interfaces configured to . . . perform error correction of the data in the packets exchanged over the channels,” as recited in claim 1. Pet. 48–51. Petitioner contends that, when combining Gridley’s teaching of adaptive cut-through switching with the teachings of Kent and Tanenbaum, a person of ordinary skill in the art would have added the error checking circuitry of Gridley to the switch interface of Kent’s coupler. *Id.* at 50 (citing Ex. 1006 ¶ 104). Petitioner further argues that, if a data transmission error is detected at the switch interface of Kent and Tanenbaum as modified by Gridley, the switch interface according to the combined teaching would drop the data packet transmitted by the sender or the source device. *Id.* (citing Ex. 1004, col. 5, ll. 30–32, 52–54, Fig. 4). Citing Tanenbaum and the testimony of Mr. Jestice, Petitioner asserts that a person of ordinary skill in the art would have understood that, after a packet is dropped, the switch interface of Kent, Tanenbaum, and Gridley would send a NAK to the source device to indicate that a transmission error has occurred and instruct the source device to retransmit the same packet. *Id.* at 50–51 (citing Ex. 1003, 182; Ex. 1006 ¶ 55).

In other words, Petitioner proposes to modify the switch interface of Kent and Tanenbaum in view of Gridley such that the NAK feedback and retransmission process takes place between the source and the switch interface, rather than between the source device and the destination device. According to Petitioner and Mr. Jestice, one of ordinary skill in the art would have recognized the benefit of the proposed modification in that it

would save network bandwidth associated with transmitting an invalid packet to the destination device and waiting for the destination device to perform a CRC check and send a NAK back to the switch. Ex. 1006 ¶¶ 55–56; Pet. 48 (citing Ex. 1006 ¶¶ 54–56). To illustrate their point, Petitioner and Mr. Jestice present data flow diagrams (not reproduced herein) indicating that, when the NAK feedback and retransmission process is implemented between the source device and the switch, there is no need to have a similar process on the other side of the switch, i.e., the communication between the switching device and the destination device. See Pet. 51; Ex. 1006 ¶ 55 (citing Ex. 1006 ¶¶ 40–42). In his Declaration, Mr. Jestice elaborates that the proposed modification of the switch (or coupler) of Kent and Tanenbaum in view of Gridley “can eliminate” the transmission of invalid packets from the switch (or coupler) to the destination device as well as the transmission of NAK packets from the destination device back to the switch, thereby “sav[ing] network bandwidth associated with” such transmissions. Ex. 1006 ¶ 55.

Petitioner does not argue that Gridley discloses a switch interface sending a NAK packet to the source device. In fact, although the portion of Gridley cited by Petitioner describes a switch discarding a data packet when an error is detected, it is silent on which entity (i.e., the switch or the source/destination) is responsible for ACK/NAK feedback to have the packet retransmitted for error correction. See Ex. 1004, col. 5, ll. 30–54. The cited portion of Gridley does not mention the ACK/NAK feedback at all, let alone placing the ACK/NAK handshake function at the switch interfaces. See *id.* As discussed above, the ACK/NAK handshake process

described in Kent and Tanenbaum takes place between the source device and the destination device, not at the switch interfaces. Hence, Petitioner does not cite, nor do we discern, anything in Kent, Tanenbaum, or Gridley that teaches or suggests placing the ACK/NAK handshake function at the switch interfaces.

Next, we are not persuaded that Petitioner or Mr. Jestice has articulated sufficient rationale to modify Kent and Tanenbaum in view of Gridley in the proposed manner, i.e., placing the error correction function, such as the NAK feedback and retransmission handshake function, at the switch interfaces. We are not persuaded by Petitioner's argument or Mr. Jestice's explanation based on the purported benefit of "saving network bandwidth" in the proposed combination because, when error detection and correction is performed by the switch interfaces between the source device and the switch, as proposed by Petitioner, it would also be necessary to perform error detection and correction on the other side of the switch, i.e., between the switch and the destination device, to ensure reliable communication along the complete path of transmission from the source to the destination. Hence, contrary to Petitioner's contention, the proposed combination of Kent, Tanenbaum, and Gridley would not necessarily "eliminate" the transmission of invalid packets from the switch to the destination or the transmission of NAK packets from the destination device to the switch. Nor would the proposed combination necessarily "save network bandwidth" between the switch and the destination device by purportedly "eliminating" such transmissions.

Neither Petitioner nor Mr. Jestice explains sufficiently why performing error correction between the source device and the switch eliminates the need for performing error correction between the switch and the destination device. Put another way, neither Petitioner nor Mr. Jestice explains sufficiently why performing error correction between the source device and the switch eliminates transmission error between the switch and the destination device. We discern no reasonable explanation in the record why the communication between the switch and the destination device would become error free as the result of performing error correction in the transmission between the source device and the switch.

Hence, we are not persuaded that the proposed modification would have “save[d] network bandwidth” between the switch and the destination device by “eliminat[ing]” the transmission of invalid packets and NAK packets between the switch and the destination device. Consequently, we are not persuaded that a person of ordinary skill in the art would have been motivated to place the NAK feedback and retransmission function at the switch interfaces between the source and the switch for the reasons stated by Petitioner when combining the teachings of Kent, Tanenbaum, and Gridley. Therefore, we find the rationale articulated by Petitioner for combining Kent, Tanenbaum, and Gridley in the manner asserted by Petitioner to be insufficient.

Petitioner’s articulated rationale for combining the references is also insufficient for the additional reason that Petitioner’s analysis is incomplete. Although Petitioner argues that the switch of Kent and Tanenbaum as modified by Gridley would transmit a NAK packet to the source device

when the CRC check fails, Petitioner does not explain which entity would send an ACK packet when the CRC check is successful. For example, the switch may send an ACK packet on its own, or, in the alternative, the switch may pass the valid packet to the destination device, which would then send an ACK back through the switch, as was the case in the case of the switch of Kent and Tanenbaum. Petitioner does not explain which alternative course a person of ordinary skill in the art would have followed and why. Hence, Petitioner's analysis is insufficient because Petitioner does not explain in sufficient detail *how* the proposed combination of Kent, Tanenbaum, and Gridley is supposed to work with respect to the error correction function at the switch interfaces. *See Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017) (“[A] clear, evidence-supported account of the *contemplated workings of the combination* is a *prerequisite* to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.”) (emphases added).

(2) “*a plurality of microprocessor interfaces configured to . . . exchange the packets with the switch interfaces over the channels, and perform error correction of the data in the packets exchanged over the channels*”

“*a memory interface configured to . . . exchange the packets with the switch interfaces over the channels, and perform error correction of the data in the packets exchanged over the channels*”

Claim 1 also recites “microprocessor interfaces configured to . . . exchange the packets with the switch interfaces over the channels, and perform error correction of the data in the packets exchanged over the channels” and “a memory interface configured to . . . exchange the packets

with the switch interfaces over the channels, and perform error correction of the data in the packets exchanged over the channels.” The plain language of the claim indicates that the term “*the* switch interfaces” recited in these limitations refers to and relies upon “a plurality of switch interfaces” discussed above as the term’s antecedent basis. Hence, in the asserted ground of obviousness based on Kent, Tanenbaum, and Gridley, “the switch interfaces” must be the interfaces at the switch or coupler of Kent and Tanenbaum as modified by Gridley, i.e., the switch with adaptive cut-through switching, as discussed above.

Petitioner, however, does not present any additional evidence or argument for the limitations reciting “microprocessor interfaces configured to . . .” and “memory interface configured to . . .” beyond merely pointing to Petitioner’s analysis based on Kent and Tanenbaum alone. Pet. 51. Hence, Petitioner presents no evidence or argument how the switch or coupler of Kent and Tanenbaum as modified by Gridley would teach these limitations. In addition, Petitioner does not explain why the switch of Kent and Tanenbaum would be sufficient to teach these limitations while, at the same time, the switch or coupler of Kent, Tanenbaum, and Gridley with adaptive cut-through switching is used to teach “switch interfaces configured to . . . perform error correction of the data in the packets exchanged over the channels.”

(3) Conclusion

Based on the foregoing, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claim 1

under 35 U.S.C. § 103(a) as obvious over the combination of Kent, Tanenbaum, and Gridley.

b. Claim 24

As discussed above with respect to the ground of challenge based on Kent and Tanenbaum alone, “the interfaces” recited in claim 24 refer to all of the interfaces recited in the claim, including the switch interfaces. Petitioner relies on the same arguments and evidence advanced with respect to claim 1 to argue that the combination of Kent, Tanenbaum, and Gridley teaches the switch interfaces “performing error correction of the data in the packets exchanged over the channels,” as recited in claim 24. Pet. 58–59. Hence, for the same reasons discussed above with respect to claim 1, Petitioner does not demonstrate that the combination of Kent, Tanenbaum, and Gridley renders claim 24 obvious.

Accordingly, the information presented in the Petition does not demonstrate a reasonable likelihood of Petitioner prevailing in its challenge to claim 24 under 35 U.S.C. § 103(a) as obvious over the combination of Kent, Tanenbaum, and Gridley.

c. Dependent Claims 2, 8, 11, 12, 25, 31, and 34

Claims 2, 8, 11, 12, 25, 31, and 34 depend from claims 1 or 24. Petitioner’s arguments and evidence presented with respect to these dependent claims do not remedy the deficiencies in Petitioner’s analysis of independent claims 1 and 24. Therefore, Petitioner does not demonstrate a reasonable likelihood of Petitioner prevailing in its challenge to claims 2, 8,

11, 12, 25, 31, and 34 under 35 U.S.C. § 103(a) as obvious over the combination of Kent, Tanenbaum, and Gridley.

*C. Claims 1, 8, 11, 12, 24, 31, and 34 as Obvious Over
Kent, Tanenbaum, and Sambamurthy; and
Claims 1, 2, 8, 11, 12, 24, 25, 31, and 34 as Obvious Over
Kent, Tanenbaum, Gridley, and Sambamurthy*

Petitioner adds the teachings of Sambamurthy (Ex. 1005) to the basic combination of Kent and Tanenbaum in an asserted ground of obviousness as to claims 1, 8, 11, 12, 24, 31, and 34. Pet. 60–63. Similarly, Petitioner adds Sambamurthy to the basic combination of Kent, Tanenbaum, and Gridley in an asserted ground of obviousness as to claims 1, 2, 8, 11, 12, 24, 25, 31, and 34. *Id.* at 63–64. In both of these asserted grounds, Petitioner relies on Sambamurthy only with respect to the term “channels” recited in the challenged claims. *Id.* at 60–64. Therefore, Petitioner’s evidence and arguments presented with respect to these asserted grounds of obviousness do not remedy the deficiencies in Petitioner’s analysis in the grounds based on Kent and Tanenbaum or based on Kent, Tanenbaum, and Gridley discussed above. Accordingly, Petitioner does not demonstrate a reasonable likelihood of Petitioner prevailing in its challenge to claims 1, 8, 11, 12, 24, 31, and 34 under 35 U.S.C. § 103(a) as obvious over the combination of Kent, Tanenbaum, and Sambamurthy. Similarly, Petitioner does not demonstrate a reasonable likelihood of Petitioner prevailing in its challenge to claims 1, 2, 8, 11, 12, 24, 25, 31, and 34 as obvious over the combination of Kent, Tanenbaum, Gridley, and Sambamurthy.

VI. CONCLUSION

Based on the arguments and evidence presented in the Petition, we conclude Petitioner has not demonstrated a reasonable likelihood that Petitioner would prevail in showing at least one of the challenged claims of the '442 patent is unpatentable based on any asserted ground of unpatentability. Therefore, we do not institute an *inter partes* review with respect to any of the challenged claims of the '442 patent.

VII. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Patent Owner's motion (Paper 10) requesting a district court-type claim construction approach under 37 C.F.R. § 42.100(b) is *granted*; and

FURTHER ORDERED that the Petition is *denied* as to all challenged claims of the '442 patent, and no trial is instituted.

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