

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX
MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00560
Patent 8,689,064 B1

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

SK Hynix Inc. (“Petitioner”) requested *inter partes* review of claim 16 of U.S. Patent No. 8,689,064 B1 (“the ’064 patent,” Ex. 1001). Paper 1 (“Pet.”). We issued a Decision to Institute an *inter partes* review (Paper 7, “Inst. Dec.”) of claim 16 of the ’064 patent under 35 U.S.C. §§ 102 and 103(a) over Averbuj.¹ Inst. Dec. 4, 18.

After institution of trial, Netlist, Inc. (“Patent Owner”) filed a Patent Owner’s Response (Paper 14, “PO Resp.”), to which Petitioner replied (Paper 17, “Pet. Reply”). Petitioner also filed Petitioner’s Motion to Exclude (Paper 20), Patent Owner filed an Opposition to Petitioner’s Motion to Exclude (Paper 23), and Petitioner filed a Reply (Paper 26). Patent Owner also filed Patent Owner’s Listing of New Arguments and Evidence in Petitioner’s Reply (Paper 22) and Petitioner filed its Response (Paper 25). Oral argument was conducted on February 14, 2018. A transcript of that argument has been made of record. Paper 29.

We have jurisdiction under 35 U.S.C. § 318(a). After considering the evidence and arguments of both parties, and for the reasons set forth below, we determine that Petitioner met its burden of showing, by a preponderance of the evidence, that claim 16 of the ’064 patent is unpatentable.

RELATED MATTERS

The ’064 patent relates to the following: *Netlist, Inc. v. Smart Modular Technologies, Inc. et al.*, Case No. 4:13-cv-05889-YGR (N.D. Cal.); *Netlist, Inc. v. Smart Modular Technologies, Inc. et al.*, Case No. 2:13-cv-02613-TLN (E.D. Cal.); *SanDisk Corp. et al. v. Netlist, Inc.*, Case No.

¹ US Patent Publication 2005/0257109 A1, published November 17, 2005 (“Averbuj,” Ex. 1005).

IPR2014-00970 (PTAB); *SanDisk Corp. et al. v. Netlist, Inc.*, Case No. IPR2014-00971 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01372 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01373 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01374 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01375 (PTAB); *Netlist, Inc. v. SanDisk LLC et al.*, Case Nos. 16-2274, -2338, -2339 (Fed. Cir.); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 16-2666 (Fed. Cir.); *Netlist, Inc. v. SK Hynix Inc. et al.*, Case No. 8:16-cv-01605-JLS (C.D. Cal.); and *In re Certain Memory Modules & Components Thereof*, Inv. No. 337-TA-1023 (ITC). See Pet. 2; Paper 4, 2–4.

THE '064 PATENT (EX. 1001)

The '064 Patent describes self-testing memory modules. Ex. 1001, 1:27–29.

CLAIM

Independent claim 16, reproduced below, reads as follows:

16. A memory module for operating with a system memory controller, comprising:
- a module controller to process input control signals from the system memory controller and to generate output control signals;
 - a plurality of memory devices configured to perform memory operations in response to signals from the module controller; and
 - a plurality of data handlers, each respective data handler being configured to generate test data and to provide the test data to a respective set of at least one memory device of the plurality of memory devices in response to signals from the module controller;
- and
- wherein the memory module is configured to obtain test results by reading from the respective set of at least one memory device in

response to signals from the module controller and by comparing data read from the respective set of at least one memory device with the test data provided to the respective set of at least one memory device.

Id. at 16:36–51.

OVERVIEW OF PRIOR ART

Averbuj (Exhibit 1005)

Averbuj describes a system for testing memory modules. Ex. 1005 ¶ 7.

THE PARTIES' POST-INSTITUTION ARGUMENTS

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claim 16 of the '064 patent is unpatentable under 35 U.S.C. §§ 102 and 103 over Averbuj. Inst. Dec. 17–18. We must now determine whether Petitioner has established by a preponderance of the evidence that claim 16 is unpatentable over the cited prior art. 35 U.S.C. § 316(e). We previously instructed Patent Owner that “any arguments for patentability not raised in the [Patent Owner Response] will be deemed waived.” Paper 8, 3; *see also* 37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–82 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board’s Trial Practice Guide states that the Patent Owner Response “should identify all the involved claims that are believed to be patentable and state the basis for that belief.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record now contains persuasive, unrebutted arguments and evidence presented by Petitioner regarding the manner in which the asserted prior art teaches corresponding limitations of claim 16 against which that prior art is asserted. Based on the preponderance of the evidence before us, we conclude that the prior art identified by Petitioner discloses, teaches, or suggests all uncontested limitations of the reviewed claim. The limitations and claim construction that Patent Owner contests in the Patent Owner Response are addressed below.

CLAIM CONSTRUCTION

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning, as they would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definitions for claim terms must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Claim 16 recites a “memory module” in the preamble. The body of claim 16 does not recite a “memory module,” but does require, in a wherein clause, that “the memory module is configured to obtain test results” by reading data from a memory device and comparing the data read with test

data. Claim 16 does not otherwise recite defining characteristics of a memory module. In our Decision on Institution, we determined that “a ‘memory module’ may be embedded in an integrated circuit” and we declined to import the requirement, proposed by Patent Owner, “that memory modules are never ‘embedded in an integrated circuit’ and must always include a ‘carrier such as a printed circuit board.’” Inst. Dec. 8.

In its Patent Owner Response, Patent Owner again argues that one of skill in the art would have construed the term “memory module” under a broadest reasonable interpretation to require “one or more memory devices on a PCB [printed circuit board].” PO Resp. 14–40. As previously discussed in the Decision on Institution, one of skill in the art would have broadly but reasonably understood a “memory module,” as recited in claim 16, not to require a carrier, such as a printed circuit board. *See, e.g.*, Inst. Dec. 8. We based this broadest reasonable interpretation of the claim term “memory module” in light of the Specification, extrinsic evidence, and apparent understanding of those of ordinary skill in the art at the time of the invention. *Id.*; *see also* Inst. Dec. 4–8. More specifically, the Specification does not include an explicit definition of “memory module,” nor does the Specification or the claim language indicate that a PCB is required.

Patent Owner argues that the Specification discloses examples in which “one or more memory devices . . . [are] on a PCB.” PO Resp. 16–18 (citing Ex. 1001, 2:24, 2:41, 2:58–60, 5:6–8, 12:53–56, 13:14–16, Figs. 1, 3) such that one of skill in the art would have understood a “memory module” to require a PCB. However, the Specification fails to disclose evidence that one of skill in the art would have broadly but reasonably construed the term “memory module” to require a PCB. *See* discussion Inst. Dec. 5–6. More

specifically, while providing examples of embodiments of a “memory module” that “includes a printed circuit board” (*see* Ex. 1001 5:6–7), the Specification does not indicate that a “memory module” must include a “printed circuit board” or that any of the disclosed functions of the “memory module” rely in any way on the presence of a “printed circuit board.”

In the Decision on Institution, we referred to the Specification’s disclosure that “the inventive subject matter [disclosed in the Specification] extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the invention and obvious modifications and equivalents thereof” and further suggests that the disclosure is intended to include any system or apparatus capable of performing “the acts or operations making up the method/process,” as disclosed. Inst. Dec. 5–6 (citing Ex. 1001, 16:16–19, 22–23). We noted that the Specification does not disclose that the “acts or operations making up the method/process,” as disclosed in the Specification cannot be performed without the “printed circuit board.” *Id.* at 6. Patent Owner argues that the Specification’s disclosures are “boilerplate language,” and supposedly do not disclose that a “memory module” may not include a PCB. PO Resp. 34–36. Even assuming the Specification discloses “boilerplate language,” as Patent Owner contends, the Specification does not disclose that a PCB is required or provide a rationale for that requirement. As such, addition of a requirement for a PCB into the claim term would impermissibly import a limitation.

Patent Owner turns to extrinsic evidence (e.g., “Petitioner’s expert”) to demonstrate that a broadest reasonable construction of the claim term “memory module” must include a PCB. *See, e.g.*, PO Resp. 19, 23–27.

However, as previously discussed, after careful consideration of the extrinsic evidence of record, we determined that one of skill in the art would have broadly but reasonably construed the claim term “memory module” not to require a PCB. *See, e.g.*, Inst. Dec 6–7. Even assuming Patent Owner to be correct that “Petitioner’s expert . . . agrees that the ’064 [S]pecification only discloses a ‘*memory module*’ including a PCB,” (PO Resp. 19, 27–31), Patent Owner does not assert or demonstrate persuasively that Petitioner’s expert (or anyone else) also demonstrates that the Specification discloses that a person of ordinary skill in the art would have understood “memory module” in the context of the ’064 patent to *require* “a PCB” under a broadest reasonable interpretation standard. Nor does Patent Owner point to any other “extrinsic evidence” that would demonstrate persuasively that one of skill in the art would have broadly but reasonably construed the claim term “memory module” to require a PCB.

Patent Owner argues that “[t]he ’064 [S]pecification . . . explicitly distinguishes the claimed invention from an application [in] which the memory system is embedded in a circuit or chip, such as an ASIC” by disclosing that there would be “physical and electrical limitations that would be faced by using test logic embedded in an ASIC” including “**no limit on the number of available interface signals,**” difficulty in “**rou[ut]ing the self-test signals on the memory module,**” and an implementation that is “**not flexible,**” PO Resp. 20–22. However, the passages cited by Patent Owner describe problems associated with interfacing an MBIST integrated circuit mounted on a PCB with memory device integrated circuits mounted on the same PCB; it does *not* describe problems integrating MBIST and memory devices in a single integrated circuit. Patent Owner concedes that,

at the time of the '064 patent, a memory system could be “embedded in a circuit or chip, such as an ASIC.” *Id.* at 20. In view of the disclosure in the Specification that a memory system may be embedded in a circuit or chip (and, therefore, not be on a “PCB”), we are not persuaded by Patent Owner’s contention that one of skill in the art would have broadly but reasonably construed a memory system to be required to be on a “PCB” and not “embedded in a circuit or chip.”

Also, claim 16 does not recite any type of a “limit on the number of available interface signals,” ease in “routing self-test signals,” or “flexible” implementation. For at least this additional reason, we are not persuaded by Patent Owner’s argument that one of skill in the art would have understood the term “memory module” to require these non-claimed features.

Patent Owner argues that the panel in IPR2014-00882 (US Patent 7,881,150, “the ’150 patent”) and in IPR2017-00561 (US Patent 8,001,434, “the ’434 patent”) determined a broadest reasonable construction of the term “memory module” to require a PCB and, therefore, according to Patent Owner, we must also make the same determination in the present matter. PO Resp. 37–39. In IPR2014-00882, the panel determined a broadest reasonable construction of the claim term “memory module” as used in the ’150 patent (not in the same family as the ’064 patent) based on evidence not of record in the present matter. IPR2014-00882, Paper 33, 10–11. Patent Owner does not explain sufficiently why an alleged determination in an unrelated case based on evidence not present or relied upon in the present case must be applied in the present (unrelated) case. In IPR2017-00561, Patent Owner argued that a “carrier” associated with the claimed “memory module” must be “removable.” See IPR2017-00561, Paper 7, 9–11.

Whether true or not, the removability of a carrier does not relate to whether a broadest reasonable construction of the claim term “memory module” requires a PCB (or “carrier”) or not. Patent Owner does not explain sufficiently why a determination in a different case must be applied to an unrelated issue in the present case. Hence, we are not persuaded by Patent Owner’s arguments pertaining to either IPR2014-00882 or IPR2017-000561.

ANALYSIS

Memory Module

Claim 16 recites a memory module for operating with a system memory controller. Petitioner contends that “[e]ach device block (6A-N) of Averbuj is . . . ‘a memory module’ as claimed.” Pet. 14 (citing Ex. 1005 Fig. 4, ¶¶ 32, 39, Fig. 4; Ex. 1003 ¶ 69).

Patent Owner argues that Averbuj does not disclose the claimed “memory module” because it discloses an embedded system rather than memory devices on a PCB. PO Resp. 42–48. This argument is not persuasive because it is based upon Patent Owner’s argument that “memory module” should be construed to require a PCB, which we declined to adopt for the reasons discussed above.

System Memory Controller

Claim 16 recites a “system memory controller” and “input control signals from the system memory controller.” Petitioner contends that Averbuj discloses “the BIST controller [which] is ‘a system memory controller’ as claimed” or, alternatively, “‘a programmable processor’ . . . [that] includes . . . ‘[a system] memory controller’ as claimed.” Pet. 15. As

we previously noted in our Decision on Institution, Averbuj discloses a “BIST controller” that “produces (or ‘generates’) control signals for the memory modules.” Inst. Dec. 10.

Patent Owner argues that Averbuj fails to disclose the claimed “system memory controller” because “Petitioner’s expert testified that timing characteristics and timing requirements for the memory devices must be controlled by the ‘*system memory controller*’” and that “the ‘*system memory controller*’ must operate in normal mode.” PO Resp. 50, 52–53; see also PO Resp. 48–55, 62, 63.

Petitioner counters that “the parties do not dispute that the claimed ‘system memory controller’ includes a device that manages the flow of data to and from the memory of a system” (Pet. Reply 16), but that “Patent Owner’s argument implicitly applies a completely new, narrower construction—i.e., that ‘a system memory controller’ must, in addition to managing the flow of data to and from the memory of the system, also control the timing characteristics and timing requirements of the memory of the system” (*id.* at 17). We agree. The language of claim 16 recites “input control signals from the system memory controller,” but does not require controlling “timing characteristics and timing requirements for the memory devices” or that it must “operate in normal mode.” Moreover, as Petitioner points out, the testimony of Dr. Mazumder on which Patent Owner relies was about a “specific DRAM memory controller described in a third-party textbook” and “was not providing any testimony about memory controllers in general or the meaning of the claim term ‘system memory controller,’ and Patent Owner does not even attempt to show that such testimony requires the

claimed memory controller to include the characteristics of the memory controller of that third-party textbook.” Pet. Reply 17–18.

Patent Owner also argues that Averbuj’s programmable processor cannot be the claimed “system memory controller” because its control signals are not input to Averbuj’s sequencers (the alleged “module controllers”), but are instead directly input to the memory interfaces (the alleged “data handlers”). PO Resp. 55–61. As Petitioner correctly points out, however, Averbuj’s sequencer *must* necessarily receive the address and control signals because it *outputs* them to Averbuj’s memory interface and the claims do not require that the input control signals be provided *directly* from the system memory controller. Pet. Reply 18–24.

Patent Owner also argues that “Averbuj teaches away from . . . computers . . . receiv[ing] and process[ing] signals and . . . a ‘controller’ . . . process[ing] . . . received signals” because, according to Patent Owner, “Averbuj teaches that the received signals . . . are used in the **normal** . . . mode [but] Averbuj [discloses a] test mode.” PO Resp. 62–63. In other words, Patent Owner argues that Averbuj “teaches away” from receiving signals at a controller or computer because Averbuj fails to disclose a “test mode” in which signals are received. Patent Owner asserts conclusorily that Averbuj’s sequencer does not “process” received signals because the alleged received signals are used in a “normal” mode, whereas the “sequencer” is “specifically designed for the test mode.” PO Resp. 63. Petitioner counters that the sequencer “processes” the received signals because it determines the mode of operation—i.e., test mode or normal mode—based on the signals it receives and, based on those signals, generates the test enable (BIST_EN) signal. Pet. Reply 23 (citing Ex. 1005, Figs. 5-6). According to Petitioner,

“sequencer (8) also packages the control signals (CTRL) received from the programmable processor with other signals it receives from the BIST controller and the programmable processor to output the packaged signals (CMD_CTRL_SIGNALS) at the right timing and according to the determined operational mode.” *Id.* at 23–24. Having considered both parties arguments and evidence, we are persuaded that Averbuj’s sequencer “processes” the control signals from the programmable processor.

In addition, Patent Owner fails to explain persuasively how “teaching away” is relevant to whether claim 16 is anticipated by Averbuj. Even assuming that “teaching away” bears some relevance to a ground of unpatentability under 35 U.S.C. § 102 (which Patent Owner has not demonstrated persuasively), “[a] reference may be said to teach away when a person of ordinary skill, upon [examining] the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.” *Para-Ordnance Mfg., Inc. v. SGS Importers Int’l, Inc.* 73 F.3d 1085, 1090 (Fed. Cir. 1995) (quoting *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)). Patent Owner does not assert or demonstrate persuasively that Averbuj discourages one of skill in the art from receiving a signal at a computer. For at least this additional reason, we are not persuaded by Patent Owner’s argument.

Memory devices

Claim 16 also recites a memory module comprising a module controller to generate output control signals and a plurality of memory devices configured to perform memory operations in response to signals

from the module controller. Petitioner argues that Averbuj discloses a “sequencer (8)” that “receives test command signals (CMD_REQ and CMD_DATA) from the BIST controller . . . ‘processes the received command’ to identify the specified test operation,” and “produces . . . the CMD/CTRL_SIGNALS, which includes control signals for the memory modules . . . and the BIST circuitry . . .” Pet. 15–16. As Petitioner explains, Averbuj discloses that a “memory interface” receives output signals (e.g., “CMD_CTRL_SIGNALS”) from a “sequencer” and generates signals for a “memory module” resulting in “[e]ach memory module[] . . . operat[ing] according to the address, control, and data signals asserted on the ADDR/CTRL_OUT and RAM_DIN ports of the corresponding memory interface.” Pet. 18 (citing Ex. 1005 ¶ 48); Ex. 1003 ¶ 86; Ex. 1005, Figs. 4–6.

Patent Owner argues that “[c]laim 16 requires the plurality [of] *memory devices* to be controlled by . . . *signals exactly from the module controller.*” Pet. Resp. 64 (citing Ex. 2010 ¶ 110). Petitioner counters that “Patent Owner’s argument is based on an improperly narrow interpretation of the term ‘in response to,’” and that there is no dispute that the signals and data received by Averbuj’s memory modules change when the address, control and data signals output by the sequencer change, and that there is also no dispute that the operation of Averbuj’s memory modules change when the address and control signals or data output by the sequencer change. Pet. Reply 24–25.

We agree with Petitioner. As noted above, claim 16 recites memory devices configured to perform memory operations in response to signals from the module controller. We do not discern and Patent Owner does not

assert or demonstrate persuasively that claim 16 also recites that the memory devices are controlled by signals “exactly from the module controller.” It is sufficient that Averbju’s memory devices are responsive to the signals from the module controller.

Patent Owner argues that Averbju fails to disclose “how . . . memory modules *respond* to BIST_EN signal.” PO Resp. 66 (citing Ex. 2010 ¶ 112). Claim 16 does not recite specific details as to “how” a memory device responds to a signal. Instead, claim 16 merely recites a memory device configured to perform memory operations in response to signals from the module controller. We are persuaded that Averbju’s memory module (i.e., the recited “memory device”) performs operations in response to signals from Averbju’s sequencer (i.e., the recited “module controller”).

Patent Owner argues that “Averbju’s multiplexers (45) and (46)” “actually respond to BIST_EN [i.e., signals from the module controller].” PO Resp. 66–67. Even assuming Patent Owner’s contention to be correct that “multiplexers (45) and (46)” of Averbju “respond[]” to signals from a module controller (or “sequencer”), that fact would not rebut Petitioner’s evidence that a memory device (or “memory module”) also “responds” to signals from a module controller (or sequencer). As Petitioner previously pointed out, Averbju discloses a sequencer (equated to the claimed “module controller” by Petitioner) that generates an output control signal (equated to “CMD_CTRL_SIGNALS” by Petitioner) and, in response to the output control signals from the sequencer, a memory module (equated to the claimed “memory device”) performs memory operations (i.e., in response to “CMD_CTRL_SIGNALS” and resultant output from a memory interface).

PETITIONER’S MOTION TO EXCLUDE

Petitioner moves to exclude Exhibits 2005–2008, 2010–2012, and 2014, Patent Owner files an Opposition to Petitioner’s Motion to Exclude, and Petitioner files a Reply to Patent Owner’s Opposition to Motion to Exclude. Papers 20, 23, 26. Petitioner’s motion to exclude is moot because, even without dismissing this evidence, we are persuaded that the claims are unpatentable. As a result, Petitioner’s motion to exclude is dismissed.

ALLEGED NEW ARGUMENTS/EVIDENCE IN REPLY

Patent Owner argues that Petitioner provided new arguments or evidence in Petitioner’s Reply and Petitioner files a Response. Papers 22, 25.

Patent Owner lists several portions of Petitioner’s Reply and evidence allegedly beyond the scope of what can be considered appropriate for a reply. *See* Paper 22. We have considered Patent Owner’s listing, but disagree that the cited portions of Petitioner’s Reply and reply evidence are beyond the scope of what is appropriate for a reply. Replies are a vehicle for responding to arguments raised in a corresponding patent owner response. Petitioner’s arguments and evidence that Patent Owner objects to are not beyond the proper scope of a reply because we find that they fairly respond to Patent Owner’s arguments raised in Patent Owner’s Response. *See Idemitsu Kosan Co., LTD. v. SFC Co. LTD*, 870 F.3d 1376, 1381 (Fed. Cir. 2017) (“This back-and-forth shows that what Idemitsu characterizes as an argument raised ‘too late’ is simply the by-product of one party necessarily getting the last word. If anything, Idemitsu is the party that first raised this

issue, by arguing—at least implicitly—that Arkane teaches away from non-energy-gap combinations. SFC simply countered, as it was entitled to do.”).

CONCLUSION

Petitioner has shown by a preponderance of the evidence that claim 16 is anticipated by Averbuj under 35 U.S.C. § 102.

ORDERS

After due consideration of the record before us, it is:

ORDERED that claim 16 of the '064 patent is held unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-00560
Patent 8,689,064 B1

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