

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner.

IPR2017-00587
Patent 8,671,243 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–30 (“the challenged claims”) of U.S. Patent No. 8,671,243 B2 (Ex. 1001, “the ’243 patent”) pursuant to 35 U.S.C. §§ 311–319. Paper 1 (“Pet.”). Netlist, Inc. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”). Pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review as to claims 1–30 of the ’243 patent on June 22, 2017, but we did not institute on all of the asserted grounds. Paper 7 (“Dec.” or “Institution Decision”), 10–39. On April 24, 2018, the Supreme Court held that a decision to institute under 35 U.S.C. § 314 may not institute on less than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S.Ct. 1348, 1358 (2018). Pursuant to SAS, we issued an Order modifying the Institution Decision to include a review of all challenged claims and all grounds. Paper 33, 2. Accordingly, the following grounds have been instituted:

Ground	Claim(s)	Prior Art
§ 102 ¹	1–3, 5–15, 17–30	Shimada ²
§ 103	4, 16	Shimada and Oh ³
§ 103	1, 3, 13, 15, 25	Shimada and Bonella ⁴
§ 103	6, 18	Shimada

¹ Petitioner asserts that Shimada is prior art to the ’243 patent under §§ 102(a), (b), and (e). Pet. 13.

² U.S. Patent No. 6,693,840 B2 (issued February 17, 2004) (Ex. 1005).

³ U.S. Patent No. 7,486,104 B2 (issued February 3, 2009) (Ex. 1012).

⁴ U.S. Publication No. 2007/0136523 A1 (issued June 14, 2007) (Ex. 1009).

Ground	Claim(s)	Prior Art
§ 103	9, 21, 28	Shimada and Goodwin ⁵
§ 103	10, 22, 29	Shimada and Sasaki ⁶
§ 103	11, 12, 23, 24, 30	Shimada and Tsunoda ⁷

Pet. 3.

During the course of trial, Patent Owner filed a Patent Owner Response (Paper 12, “PO Resp.”), and Petitioner filed a Reply to the Patent Owner Response (Paper 16, “Pet. Reply”). Petitioner submitted the Declaration of Ron Maltiel (Ex. 1003). Patent Owner submitted the Declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 2016).

Petitioner filed a Motion to Exclude Evidence (Paper 19, “Pet. Mot. Ex.”), with Patent Owner filing an Opposition the Motion to Exclude (Paper 26, “PO Mot. Ex. Opp.”), and Petitioner filing a Reply thereto (Paper 28, “Pet. Mot. Ex. Reply”). Patent Owner filed a Motion to Exclude Evidence (Paper 21, “PO Mot. Ex.”), with Petitioner filing an Opposition the Motion to Exclude (Paper 24, “Pet. Mot. Ex. Opp.”), and Patent Owner filing a Reply thereto (Paper 29, “PO Mot. Ex. Reply”). Patent Owner also filed a Listing of New Arguments and Evidence in Petitioner’s Reply (Paper 25, “PO Obj.”), with Petitioner filing a Response (Paper 27, “Pet. Resp. Obj.”).

We held a consolidated oral hearing on February 14, 2018, in relation to this proceeding and other proceedings involving the same parties. A transcript (Paper 32, “Tr.”), of the oral hearing has been entered into the record.

⁵ U.S. Patent No. 4,658,204 (issued April 14, 1987) (Ex. 1015).

⁶ U.S. Patent No. 6,721,212 B2 (issued April 13, 2004) (Ex. 1017).

⁷ U.S. Publication No. 2003/0028733 A1 (published February 6, 2003) (Ex. 1019).

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6, and this Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–30 of the ’243 patent are unpatentable. We grant-in-part and deny-in-part Petitioner’s Motion to Exclude and deny Patent Owner’s Motion to Exclude as moot.

B. Related Proceedings

Patent Owner indicates related matters are: *Netlist, Inc. v. Smart Modular Technologies, Inc.*, Case No. 3:13-cv-05889-YGR (N.D. Cal.); *Netlist, Inc. v. Smart Modular Technologies, Inc.*, Case No. 2:13-cv-02613-TLN (E.D. Cal.); *SanDisk Corp. v. Netlist, Inc.*, Case No. IPR2014-00982 (PTAB); *SanDisk Corp. v. Netlist, Inc.*, Case No. IPR2014-00994 (PTAB), *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01371 (PTAB); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01370 (PTAB); *SK hynix Inc., et al. v. Netlist, Inc.*, Case No. IPR2017-00649 (PTAB); and *SK hynix Inc., et al. v. Netlist, Inc.*, Case No. IPR2017-00561 (PTAB). Paper 4, 2–3. Patent Owner also indicates that related U.S. Patent Application Nos. 15/000,834, 14/489,281, and 14/840,865 are pending. *Id.* at 4.

C. The ’243 Patent

The ’243 patent is entitled “Isolation Switching For Backup Memory,” and issued on March 11, 2014, from an application filed on May 29, 2013. Ex. 1001, [22], [45], [54]. The ’243 patent claims priority to (1) U.S. Patent Application No. 13/536,173, filed on June 28, 2012 (now U.S. Patent No. 8,516,187); (2) U.S. Application No. 12/240,916, filed on

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September 29, 2008 (now U.S. Patent No. 8,301,833); (3) U.S. Application No. 12/131,873, filed on June 2, 2008; and (4) U.S. Provisional Application No. 60/941,586, filed on June 1, 2007. *Id.* at [60].

The '243 patent is directed to a memory module system that has a volatile memory subsystem, non-volatile memory subsystem, and controller. Ex. 1001, Abstract, 3:21–24. The memory module system may switch between two states of operation. *Id.* at 7:49–50. In the first state, a circuit couples the volatile memory subsystem to the host system while isolating the volatile memory subsystem from the non-volatile memory subsystem. *Id.*, Abstract, 7:50–54. In a second state, a circuit allows data to be communicated between the volatile and non-volatile memory subsystems by coupling the respective subsystems and isolating the volatile memory system from the host system. *Id.*, Abstract, 7:54–58. The memory system uses the volatile memory subsystem under normal conditions, but provides back-up functions using the non-volatile memory subsystem. *Id.* at 3:24–27, 6:23–34, 7:49–62. In the event of a trigger condition, which may include a power failure or power reduction, the controller backs up the system by transferring data from a volatile memory system to a non-volatile memory system. *Id.* at 3:24–28. The configuration is directed to protecting the operation of the volatile memory in the two modes of operation while providing backup and restore capability in the event of a trigger condition. *Id.* at 3:32–36, 3:41–45, 8:17–30.

Claims 1, 13, and 24 are independent claims, and the other claims at issue are dependent claims, depending directly or indirectly from claims 1, 13, and 24. Ex. 1001, 20:30–23:20. Claim 1, reproduced below, is illustrative of the challenged claims of the '243 patent.

1. A memory system comprising:
 - a volatile memory subsystem;
 - a non-volatile memory subsystem;
 - a controller coupled to the non-volatile memory subsystem; and
 - a circuit coupled to the volatile memory subsystem, to the controller, and to a host system, wherein:

in a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system, and

in a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system.

Ex. 1001, 20:30–49.

II. ANALYSIS

A. *The Parties’ Post-Institution Arguments*

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 1–30 of the ’243 patent are unpatentable under 35 U.S.C. § 102 and/or 35 U.S.C. § 103 over asserted prior art. Inst. Dec. 38–39. We now determine whether Petitioner has established by a preponderance of the evidence that claims 1–30 are unpatentable under 35 U.S.C. § 102 and/or 35 U.S.C. § 103(a) over the cited prior art. 35 U.S.C. § 316(e). We previously instructed Patent Owner that “any arguments for patentability not raised in the [Patent Owner Response] will be deemed waived.” Paper 8, 3; *see also*

37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–82 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board’s Trial Practice Guide states that the Patent Owner Response “should identify all the involved claims that are believed to be patentable and state the basis for that belief.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. Where Patent Owner has provided argument and evidence in the Patent Owner Response, it has been considered. In this regard, the record now contains persuasive arguments and evidence presented by Petitioner regarding the manner in which the asserted prior art teaches corresponding limitations of claims 1–30 on all the grounds, except for the assertion of anticipation against claims 9–12, 21–24, and 28–30 by Shimada because the arguments and evidence provided for this ground in the Petition were insufficient. Based on the preponderance of the evidence before us, we conclude that the art identified by Petitioner discloses, teaches, or suggests all of the limitations of the reviewed claims on all grounds, except for the ground asserting anticipation against claims 9–12, 21–24, and 28–30 by Shimada.

B. Claim Construction

In an *inter partes* review, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light

of the specification of the patent in which they appear. 37 C.F.R.

§ 42.100(b). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning, as they would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

We address the claim terms at issue below.

“in a first mode of operation, the circuit is operable to selectively isolate . . . and to selectively couple the volatile memory subsystem to the host system”

“in a second mode of operation, the circuit is operable to selectively couple . . . and the circuit is operable to selectively isolate the volatile memory subsystem from the host system”

In the Petition, Petitioner proposed that the entire “first mode” limitation be construed as one “in which the circuit does not allow communication between the controller and the volatile memory subsystem while allowing communication between the volatile memory subsystem and the host system,” and that the entire “second mode” limitation be construed as one “in which the circuit does not allow communication between the volatile memory subsystem and the host system while allowing communication between the volatile memory subsystem and the controller.” Pet. 8–9, 11. In the Institution Decision, we declined to recast the entire limitation with alternative wording, and alternatively construed “couple” to mean “operatively couple to allow interaction,” and construed “isolate” to mean “operatively decouple to not allow interaction.” Dec. 8–9.

Patent Owner contends that the term “selectively” should be construed separately from the terms “couple” and “isolate” of the “mode” limitations. PO Resp. 20–30. Patent Owner did not agree with our preliminary interpretation of the terms “couple” and “isolate,” arguing that the addition

of “operatively” was not necessary. *See* PO Resp. 21–24. At oral hearing, Patent Owner indicated that the Board’s construction of the terms “couple” and “isolate” was not at issue or dispositive to the unpatentability challenges. *See* Tr. 104:15–105:5. Petitioner also contends that any dispute regarding the construction of these terms “couple” or “isolate” does not require resolution for the invalidity analysis. Pet. Reply 4. Accordingly, we determine that it is not necessary to provide construction of the claim terms “couple” and “isolate” because, as discussed below, the disputes relate only to the construction of the term “selectively.” *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

As to the term “selectively,” Patent Owner argues that Petitioner should not be permitted to read out the term from the claims, the term should be given effect, and it should be interpreted as “in response to a selection” in light of Specification, dictionary definitions, and the prosecution history. PO Resp. 24–30. Patent Owner contends that a Federal Circuit appeal decision concerning U.S. Patent Nos. 7,881,150 and 8,081,536 is relevant here. *Id.* at 28 (citing Ex. 2015, Appeal No. 2016-1742 (*Netlist, Inc. v. Diablo Techs, Inc.*, 701 Fed. App’x 1001 (Fed. Cir. 2017) (“the Federal Circuit decision”))). Patent Owner argues that in that decision, the Federal Circuit ruled that the term “selectively electrically coupling” is “coupling in response to a selection.” *Id.*; *see Netlist*, 701 Fed. App’x at 1004. Patent Owner also alleges that the court agreed that the term referred to coupling or decoupling specific data lines, and not to the overall process of selecting components. *Id.*

Petitioner contends that under its proposed construction of the entire “in the first mode . . .” and “in the second mode . . .” limitations, the term “‘selectively’ has not been read out of the claims.” Pet. Reply 6 (citing Pet. 8–11). Petitioner does not dispute Patent Owner’s proposed construction of the term “selectively,” except to the extent that the term requires “independent” selection. *See id.* at 4–6. Petitioner also argues that the Patent Owner’s reliance on the Federal Circuit decision⁸ is flawed, and Petitioner distinguishes the claims, where the claims in the Federal Circuit case were directed to selectively coupling signal lines, which are not at issue here. *Id.* at 7–8.

Patent Owner views the claim construction of the term “selectively” as dispositive (*see* Tr. 104:16), even though Petitioner’s position is that Shimada discloses all the claim limitations, even under Patent Owner’s construction of the claim term (*see id.* at 113:6–13). The apparent discrepancy in the parties’ views is discussed *infra* Section II.D.

Here, we adopt Patent Owner’s proposed construction of the term “selectively,” as “in response to a selection.” This is consistent with the ordinary meaning of the term and the use of the term in the Specification. And although the Federal Circuit decision is not directly relevant to the patent at issue here (*see infra*, Section II.D and IV), the Federal Circuit’s manner of considering “selectively electrically coupling” as “coupling in response to a selection” similarly parses out the limitation of “selecting” as applied here. *See Netlist*, 701 Fed. App’x at 1004. However, the remainder of the claim in the Federal Circuit decision is different than claim 1 of the ’243 patent—the claim at issue there is directed to “selectively electrically

⁸ Patent Owner moves to exclude the Federal Circuit decision from evidence. *See infra* Section IV.

coupling” “data signal line[s],” and the claim here is to “selectively couple” components such as a controller and volatile memory subsystem. *See id.*

“communicated between”

Patent Owner argues that the term “communicated between” should be construed as “moved in either direction.” PO Resp. 30–31. In support, Patent Owner refers to a portion of the ’243 patent Specification describing data being “backed-up” from the volatile to non-volatile memories, and then restored. *Id.* (citing Ex. 1001, Fig. 4A; Ex. 2016 ¶ 91). Petitioner contends that Patent Owner also indicates that “either direction” means “both directions.” Pet. Reply 9 (citing PO Resp. 54). Petitioner argues that the broadest reasonable interpretation of the term “communicated between” should not require communication in “both directions.” *Id.* (citing Ex. 1001, 17:27–33).

In light of the Specification and the ordinary meaning of the term, we agree with Patent Owner’s proposed construction permitting communication of data in “either direction,” but we agree with Petitioner that the ordinary meaning of the term “between” does not require data to be communicated in both directions.

Other Terms

Although Patent Owner proposes the construction of additional claim terms, we determine that it is not necessary to provide an express interpretation of any other term of the claims because it is not necessary to resolve any issues or disputes. *See Vivid Techs.*, 200 F.3d at 803.

C. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art at the time of the ’243 invention would have had “a Bachelor’s degree in materials

science, electrical engineering, computer engineering, computer science, or in a related field and at least one year of experience with the design or development of semiconductor non-volatile memory circuitry or systems.” Pet. 4 (citing Ex. 1003 ¶¶ 49–50).

Patent Owner asserts that a person of ordinary skill in the art would have “a Bachelor’s degree in electrical and/or computer engineering and at least five years of industry experience designing memory devices and controllers,” and a Master of Science degree could substitute for two years of industry experience. PO Resp. 1–2 (citing Ex. 2016 ¶ 35). Patent Owner contends that “[a] degree in material science engineering alone would not suffice as an equivalent to a degree in electrical and/or computer engineering.” *Id.* (citing Ex. 2016 ¶¶ 33–34). Based upon its proposed educational foundation, Patent Owner argues that some claim terms would be understandable to a person of ordinary skill in the art, “but not necessarily to Petitioner’s expert who lacks that level of skill.” *Id.* at 34.

Although we agree with the Patent Owner that a degree in material science alone is not equivalent to a degree in electrical engineering, we also agree with Dr. Baker, Patent Owner’s expert, that industry experience can substitute for and supplement an educational degree. *See* Ex. 1030, 55:6–12. In this case, we find Petitioner’s proposed qualifications for education, with the addition of at least five years of industry experience, to be sufficient. Therefore, to the extent necessary, we adopt Petitioner’s assessment of the qualifications, with the addition of five years of experience, as sufficient for one of ordinary skill in the art.

Mr. Maltiel, Petitioner’s expert, is senior member of IEEE with more than 30 years of experience in design and implementation of computer semiconductor devices, including memory chips. Ex. 1004, 1. Mr. Maltiel’s

experience is sufficient to supplement his educational degree and qualify him as a person of skill in the art for the purposes of this proceeding.

D. Asserted Anticipation of Claims 1–3, 5–15, and 17–30 over Shimada

In support of this asserted ground of unpatentability, Petitioner explains how Shimada anticipates claims 1–3, 5–15, and 17–30. Pet. 18–55. In its Response, Patent Owner contends that Petitioner fails to demonstrate anticipation because Shimada fails to disclose some of the claim limitations. See PO Resp. 37–58.

We find that Petitioner has demonstrated by a preponderance of the evidence that Shimada anticipates claims 1–3, 5–8, 13–15, 17–20, and 25–27 for the reasons discussed below. Petitioner has not demonstrated by a preponderance of the evidence that Shimada anticipates claims 9–12, 21–24, or 28–30.

We begin our analysis with a summary of Shimada, and then address the arguments and evidence presented by the parties.

1. Shimada (Ex. 1005)

Shimada generally discloses a semiconductor memory device that includes a volatile memory and non-volatile memory. Ex. 1005, 3:45–49. Figure 2 of Shimada is reproduced below.

FIG. 2

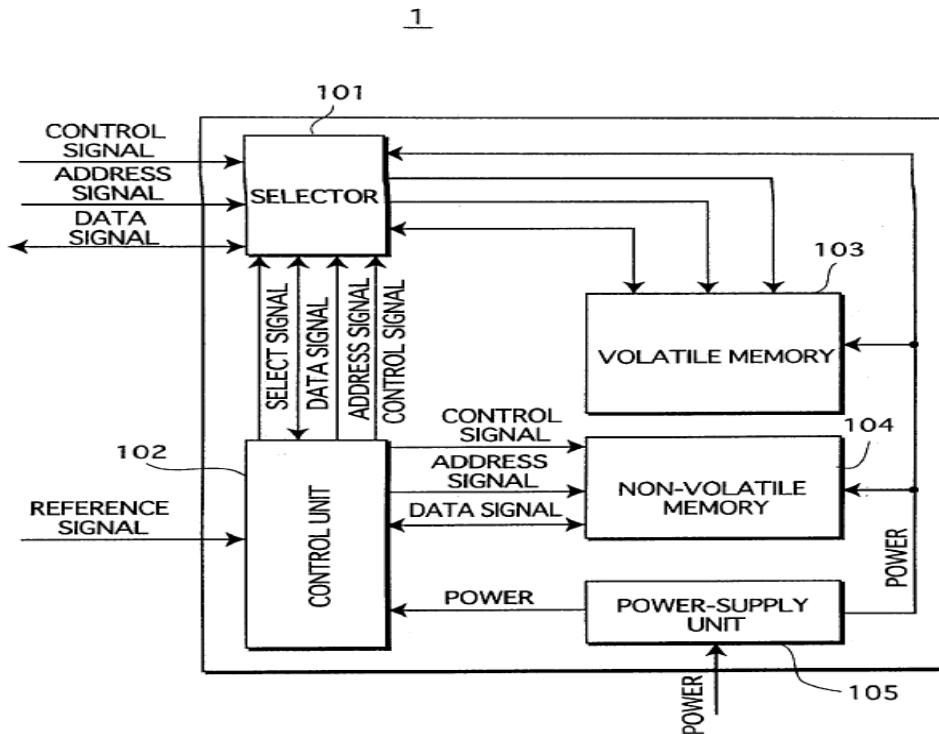


Figure 2 depicts a functional block diagram illustrating an embodiment of a semiconductor memory device. Ex. 1005, 3:18–20. Shimada’s semiconductor memory device has control unit 102, volatile memory 103, non-volatile memory 104, selector 101, and power-supply unit 105. *Id.* at 3:47–48. Power-supply unit 105 directs externally supplied power and also accumulates power required by control unit 102 to save data from volatile memory 103 to non-volatile memory 104. *Id.* at 4:43–53. With the start of an external power supply, the control unit restores data of the non-volatile memory in the volatile memory, and when the external power supply has stopped, as detected by a voltage reduction in the main power source, the control unit saves data from the volatile memory to the non-volatile memory. *Id.* at 1:41–45, 3:64–4:6, 4:10–15.

Control unit 102 controls operation of semiconductor memory device 1 and receives a reference signal from outside of it, “and performs data copying between volatile memory 103 and non-volatile memory 104 (i.e.,] save or restore), according to the reference signal.” Ex. 1005, 3:54–59. Shimada’s selector 101 receives a signal sent from control unit 102 to switch between two different modes in which access to volatile memory 103 is allowed differently. *Id.* at 4:20–23. When select signal (H) is received, selector 101 allows access from outside the semiconductor memory device 1 to the volatile memory 103; and when select signal (L) is received, the selector 101 allows the control unit 102 to access the volatile memory 103. *Id.* at 4:20–27.

2. Analysis

To prevail on its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378–79 (Fed. Cir. 2015) (discussing the burdens of persuasion and production in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 102 if a prior art reference discloses each and every element of the claimed invention, either explicitly or inherently. *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 1047 (Fed. Cir.

1995); *see MEHL/Biophile Int’l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (“To anticipate, a claim a prior art reference must disclose every limitation of the claimed invention . . . ;” any limitation not explicitly taught must be inherently taught and would be so understood by a person experienced in the field); *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991) (the dispositive question is “whether one skilled in the art would reasonably understand or infer” that a reference teaches or discloses all of the elements of the claimed invention).

a. Claim 1

Petitioner asserts that claim 1 is unpatentable as anticipated by Shimada. Pet. 18–55; Pet. Reply 11–22.⁹ Patent Owner disagrees with Petitioner’s assertions, focusing its arguments on Shimada’s alleged failure to disclose the “circuit” as claimed. *See* PO Resp. 37–55.

Petitioner contends that Shimada discloses a volatile memory, nonvolatile memory, and controller corresponding to the claim limitations. Pet. 18–22. The Petition argues that selector 101 within semiconductor memory device 1, as depicted in Figure 2 of Shimada, is coupled to the volatile memory subsystem, controller, and host system, as claim 1 recites. *Id.* at 22–24. Petitioner asserts that Shimada discloses that the claimed first mode of operation when selector circuit 101 receives input select signal (H), and, in this mode, selector 101 allows data to be communicated between

⁹ Patent Owner asserts that portions of Petitioner’s Reply are allegedly beyond the scope of what is considered appropriate for a reply. *See infra* Section III. As discussed below, however, we find that the disputed portions of Petitioner’s Reply and associated evidence are within the scope of what is appropriate for a reply and may be considered. *See id.*

volatile memory and the host system. *Id.* at 24 (citing Ex. 1003 ¶ 119; Ex. 1005, 4:6–9, 4:23–25, 4:28–33).

Petitioner further contends that in the first mode, Shimada’s selector 101 does not allow data communications between the host system and the remaining portions of the semiconductor memory device, including control unit 102. Pet. 24 (citing Ex. 1003 ¶ 120; Ex. 1005, 3:47–50, 5:30–34, 9:30–39). Mr. Maltiel’s testimony refers to Shimada’s “semiconductor memory device” that includes the “control unit 102” and “non-volatile memory 104,” and in the first mode, selector 101 shuts out access of the host system to control unit 102 and non-volatile memory 104. Ex. 1003 ¶ 120 (citing Ex. 1005, 3:47–50, 9:30–39). Mr. Maltiel further testifies that when the first mode is selected, a person of skill in the art would understand that “selector 101 has coupled the control signal, address signal and data signal lines of the outside system to the volatile memory 103 rather than signal lines of the control unit.” *Id.* ¶ 121. Mr. Maltiel additionally testifies that a skilled artisan would understand that the terms “selector” and “multiplexer” would be used interchangeably and cites to other prior art for support of that understanding. *Id.* ¶¶ 122–127. With this, Petitioner argues that Shimada discloses that in the first mode, “the circuit is operable to selectively isolate the controller from the volatile memory subsystem” as claimed. Pet. 24–25.

Petitioner alleges that Shimada discloses the second mode of operation recited in claim 1 when the selector receives input select signal (L). Pet. 26. Petitioner argues that, in this mode, “the ‘selector 101’ allows data to be communicated between the ‘volatile memory 103’ and the ‘nonvolatile memory 104’ using the ‘control unit 102.’” *Id.* (citing Ex. 1003 ¶¶ 136–137; Ex. 1005, 3:55–62, 4:26–27, 4:34–41). Petitioner further contends that when in this mode, “‘selector 101’ does not allow data to be

communicated between the ‘volatile memory 103’ and the host system.” *Id.* (citing Ex. 1005, 3:64–4:1, 4:10–15, Fig. 3). Referring to Figure 3 of Shimada, Petitioner identifies a first scenario where “selector 101” may receive an input select signal (L) after the reference signal has changed from L to H, then data is copied from non-volatile memory 104 to volatile memory 103, and “the control unit 102 . . . shuts out any access to the volatile memory 103 from outside, so that the control unit 102 may access the volatile memory 103.” *Id.* at 27 (citing Ex. 1003 ¶¶ 139, 140; Ex. 1005 at 3:64–4:6, Fig. 3). In a second scenario, Petitioner alleges that “selector 101” receives an input select signal (L) after the reference signal has changed from H to L, and data is copied from the volatile memory 103 to the non-volatile memory 104. *Id.* at 28 (citing Ex. 1003 ¶¶ 139, 141; Ex. 1005, 4:14–16, Fig. 3). Petitioner avers that in this situation a person of ordinary skill understands that “the host system will not be able to communicate with the volatile memory 103 because the selector 101 has coupled the volatile memory 103 to the control signal, address signal and data signal lines of the control unit 102, rather than to the signal lines of the outside system.” *Id.* (citing Ex. 1003 ¶ 142).

Petitioner’s anticipation analysis, as supported by Mr. Maltiel’s Declaration, relies on testimony as to where each element of the challenged claim 1 is disclosed in Shimada. Pet. 18–28; Ex. 1003 ¶¶ 94–144. After having considered Patent Owner’s arguments, which we address below, we agree with and adopt Petitioner’s analysis and credit Mr. Maltiel’s testimony.

Patent Owner argues that Shimada fails to disclose the “circuit” as claimed because “[t]he Petition fails to show a memory system that comprises a first path that can selectively isolate or couple the host system

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and the VMS [volatile memory subsystem] and a second path that can selectively isolate or couple the controller and the VMS.” PO Resp. 38.

Patent Owner alleges that Shimada’s selector—the “circuit” as mapped by Petitioner—can only make a selection between operational modes. *Id.*

Patent Owner refers to Shimada’s mode selection as discussed in its specification, as well as referring to Patent Owner’s annotated versions of Figure 2 of Shimada, which are reproduced below. *See id* at 39–40 (citing Ex. 1005, 4:20–27, Fig. 2).

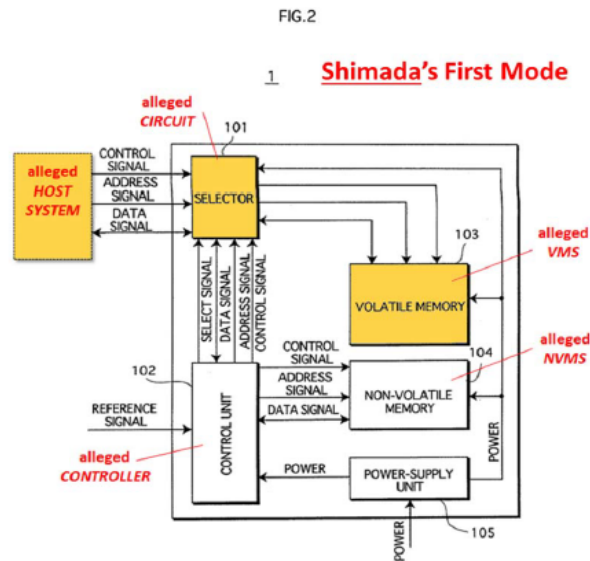
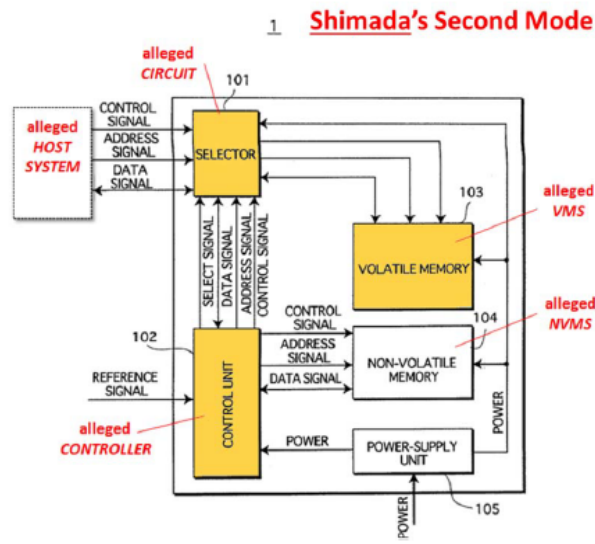


FIG.2



Shimada (Ex. 1005), Fig.2 (annotation added).

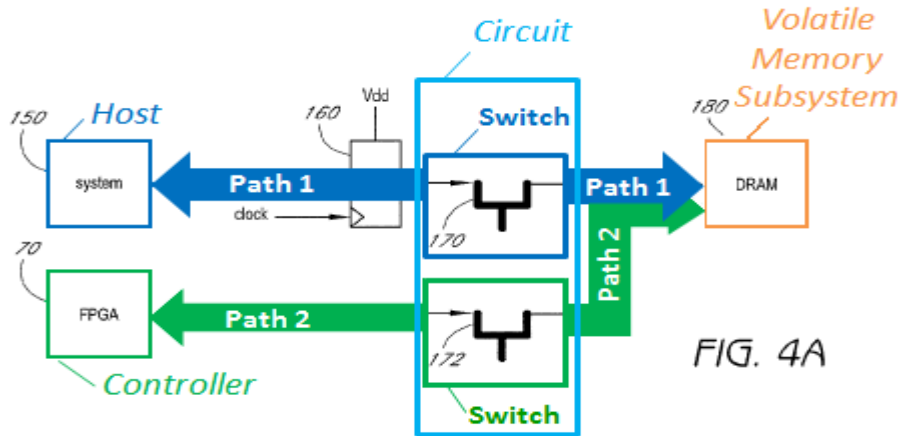
Patent Owner's annotated versions of Figure 2 of Shimada are reproduced above.

Patent Owner additionally argues that in the first mode, the “selection” made is to “couple or decouple” the volatile memory subsystem and host system, “but not to select between the *controller* and the *host system*.” PO Resp. 41 (citing Ex. 2016 ¶ 116) (emphases in original); *see id.* at 29–30 (citing Ex. 2016 ¶¶ 87–88). Patent Owner similarly asserts that in the second mode, the “selection” is to couple or decouple the controller and the volatile memory subsystem, “not to select between the *controller* and the *host system*.” *Id.* (emphases in original). It is argued that “the term “*selectively couple*” cannot be reasonably interpreted as making a selection between two modes [of] operation.” *Id.* at 41–42 (citing Ex. 2016 ¶¶ 117, 136). Patent Owner avers that “the disclosed *circuit* couples some components and not others . . . [b]ut the claim term “*selectively*” is directed to **how** the claimed *circuit* performs that function, which is by coupling or decoupling specific devices.” Ex. 2016 ¶ 118; *see* PO Resp. 29–30.

We are not persuaded by Patent Owner’s argument on mode selection. Patent Owner’s arguments characterize Shimada’s “mode” choice as the only “selection” made in Shimada but as Petitioner argues, “the claims do not *preclude* selection of a “mode” upon selectively coupling and isolating the claimed components.” Pet. Reply 14–15 (emphasis in original). In other words, in Shimada’s operations there are modes, and there also is selective coupling and isolating by selector 101 [circuit], as asserted in the Petition. *See, e.g.*, Pet. 24–28 (citing Ex. 1003 ¶¶ 119, 121, 137, 141, 142). Petitioner’s expert testimony that “coupling” between the components allows data communication, is consistent with the claims. *See, e.g.*, Ex. 1003 ¶¶ 119, 137.

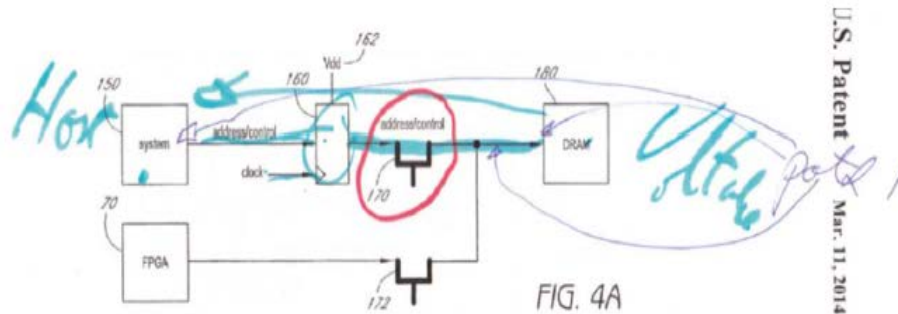
Patent Owner’s arguments that selection “between” the components is not consistent with the claims, and that we should consider the “how” of circuit operation, are predicated, in part, on portions of the aforementioned Federal Circuit decision involving unrelated Netlist patents. *See* PO Resp. 29–30, Ex. 2016 ¶ 89, 116. However, the claim and issue addressed in that Decision, which was specific to the claims therein—i.e., the claim requirement for the “how” being the connection of specific data signal lines, and thus distinguishing the selection “between” specific devices—are not at issue in the claims here. *See Netlist*, 701 Fed. App’x at 1004. Additionally, we do not discern that there is any issue identified as to why “selectively coupling” of components could not also involve a selection between components.

Patent Owner also argues that the ’243 patent describes two independent paths as depicted in the annotated version of Figure 4A reproduced below. PO Resp. 42–44.



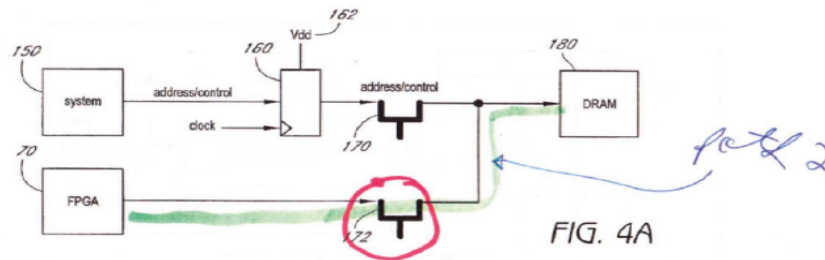
Patent Owner argues that, as depicted in the annotated version of Figure 4A above, in “Path 1” one or more switches 170 are “selectively switched to select between coupling and isolating the host system and the VMS regardless [of] the first and second modes.” *Id.* at 42–43 (citing Ex. 1001, 6:43–49; Ex. 2016 ¶¶ 48, 119). It is further asserted that in “Path 2,” “[o]ne or more switches 172 can be selectively switched to select between coupling and isolating the controller and the VMS regardless [of] the first and second modes.” *Id.* at 43–44 (citing Ex. 1001, 6:38–43; Ex. 2016 ¶ 120). Patent Owner argues that “the ’243 Patent states several times that the system can either choose to isolate or couple the volatile memory to the controller/non-volatile memory pair, and this selection is made in **both** modes as claimed.” *Id.* at 44 (emphasis in original). Patent Owner also avers that the ’243 patent describes that the memory system may be operated in “at least two states,” but that “does not equal exactly ‘two states’ or exactly ‘two modes,’” and “[t]hese exemplary embodiments are not limiting” and “do[] not foreclose other modes of operation in which both paths are coupled or both paths are decoupled.” *Id.* (citing Ex. 1001, 7:49–62, 9:40–45, 3:36–41; Ex. 2016 ¶¶ 118, 120).

Patent Owner also alleges that the view that the claimed circuit comprises two independent paths was agreed with by Petitioner's expert, Mr. Maltiel. PO Resp. 45–46. Patent Owner refers to two annotated versions of Figure 4A of the '243 patent, reproduced below, that are alleged to evidence Mr. Maltiel's understanding.



Ex. 2006 (Ex. 1001, Fig. 4A as annotated by Mr. Maltiel during his deposition);

Ex. 2016, ¶119.



Ex. 2007 (Ex. 1001, Fig. 4A as annotated by Mr. Maltiel during his deposition);

Ex. 2016, ¶120.

Patent Owner alleges that the highlighting and annotations made by Mr. Maltiel on Figure 4A demonstrate agreement with Patent Owner's allegations regarding "Path 1" and "Path 2." *Id.* at 45–46 (citing Ex. 2016, ¶¶ 40–42, 119, 120).

Based upon these allegations, Patent Owner then contends that Shimada's selector fails to disclose some claim limitations because Shimada's selector does not comprise two independent paths. PO Resp. 46–

48. Patent Owner refers to the Petition’s allegations where, for instance, Petitioner states:

A skilled artisan would understand from this [Shimada’s] disclosure that in the first mode, the control unit 102 will not be able to communicate with the volatile memory 103 because the selector 101 has coupled the control signal, address signal and data signal lines of **the outside system** to the volatile memory 103 **rather than** signal lines of **the control unit**. Ex. 1003 ¶ 121.

PO Resp. 46 (citing Pet. 24–25) (emphases in PO Resp.).

Patent Owner argues as to the claim limitation “the circuit is operable to selectively isolate the controller from the volatile memory subsystem” [element 1f_B], Shimada fails to satisfy the claim element because “the ‘selection’ . . . is whether to couple or decouple the *controller* and the *VMS* [volatile memory system] regardless of the *host system*.” PO Resp. 47 (citing Ex. 2016 ¶ 122) (emphases in original). Patent Owner again contends that “**how** the *circuit* of claim 1 operates to *selectively isolate* path 2 is different than **how** Shimada’s selector operates.” *Id.* (citing Ex. 2016 ¶ 123) (emphases in original).

At the oral hearing, Patent Owner confirmed that it is asserting that “the claims require a circuit that can respond to two selections in each mode.” Tr. 101:7–8. Patent Owner stated that “[i]n other words, the response to one selection is independent of the response to the other selection.” *Id.* at 101:10–12 (emphasis added). Patent Owner refers to Dr. Baker’s testimony describing why a person of ordinary skill would choose to have one selection input occur before or prior to another. *Id.* at 102:1–3 (referring to Ex. 2023, 7 (citing Ex. 1030, 98:5–15)).

Patent Owner’s arguments are based on the assumed addition of limitations beyond those required by the claims. Claim 1 reads, in part, that

in the “first mode,” “the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated.” As discussed, *supra* Section II.B, Patent Owner agreed that the term “selectively” should be construed as “in response to a selection.” To paraphrase the claim, the circuit “isolate[s] [in response to a selection]” and “couple[s] [in response to a selection].” However, there is nothing in the claim that requires that “the response to one selection be independent of the response to the other selection.” There is nothing, for example, that requires the coupling and the isolating to be done by the circuit in response to two independent responses, rather than by a potentially interrelated response where the circuit operates to isolate in response to a selection and couple in response to a selection.

Patent Owner attempts to support its position by referring to how an embodiment of the ’243 patent, using separate switches, works or operates.¹⁰ See PO Resp. 42–44. Even if we agreed that the separate switch embodiment discloses “independent responses,” adding requirements to the claim based on the operation of an embodiment would impermissibly import unrecited limitations into the claim.

Patent Owner further argues that interchanging Shimada’s selector with a multiplexer, under Petitioner’s expert’s assertion that a “selector” and “multiplexer” are terms that are used interchangeably, would fail to disclose the circuit as claimed. PO Resp. 49–53. Patent Owner refers to Mr. Maltiel’s Declaration that cites to “74F257A Selector/Multiplexer Data Sheet” by Philips, dated March 31, 1995 (Ex. 1008 (“Philips”), and the

¹⁰ Figure 4A of the ’243 patent, which is reproduced above with annotations, is identified as an embodiment. See Ex. 1001, 6:35–49.

alleged mapping of the inputs and outputs. *Id.* Patent Owner alleges that “[e]ven if Shimada selector 101 operates like Philips’ selector/multiplexer, the alleged circuit fails to overcome the deficiencies of Shimada alone” because “Philips’ selector/multiplexer (like Shimada’s selector) can only make a selection between two modes of operation.” PO Resp. 53. Patent Owner’s arguments are not persuasive for the reasons discussed above for Shimada only.

Patent Owner additionally alleges that using Philips multiplexer as Shimada’s selector would not allow data to be communicated from the volatile memory subsystem because it only would allow data to be moved in one direction. PO Resp. 53–54 (citing Ex. 2016 ¶ 137).¹¹ We are persuaded by Petitioner’s arguments and evidence that Shimada’s selector operates as required by the claims and, therefore, Patent Owner’s arguments about the specific multiplexer taught in Philips are not persuasive.

Patent Owner also asserts that under the Board’s preliminary construction of “couple” which allows movement of data in either direction, Shimada fails to disclose the first and second mode limitations. PO Resp. 54. These arguments are based, in part, on an alleged requirement for bidirectional communication in both directions, and, as discussed, *supra*, the

¹¹ Patent Owner also alleges that “there is no support in the record” for combining Philips and Shimada. PO Resp. 53–54. Neither the Patent Owner Response nor the portion of Dr. Baker’s testimony cited (Ex. 2016 ¶ 137), provide further explanation for this assertion. In any event, the allegation is not persuasive because Petitioner does not propose combining Shimada with Philips, as Patent Owner contends. Instead, Petitioner relies upon Philips only as evidence that a person of ordinary skill in the art would have understood Shimada’s selector “to operate to prohibit communication with its non-selected ports and therefore isolate those components coupled to such ports.” Pet. 25; Ex. 1003 ¶ 122.

claim term “communicated between” does not require communication in *both* directions, merely communication in *either* direction.

Patent Owner also alleges, based on testimony from Mr. Maltiel, that Petitioner’s proposed design of a multiplexer/selector using switches assumes that the Petitioner has sufficiently proven that the circuit as claimed is taught by Shimada’s selector. PO Resp. 54–55. As discussed above, we determined that Shimada’s selector discloses the circuit as claimed, we therefore need not consider any additional arguments alleged by Petitioner relating to this issue.

Accordingly, for the reasons discussed above, we are persuaded Petitioner has shown by a preponderance of the evidence that claim 1 of the ’243 patent is unpatentable as anticipated by Shimada.

b. Claim 2

Claim 2 depends from claim 1 and additionally recites “the circuit is operable to selectively isolate or couple the controller to the volatile memory subsystem, and the circuit is operable to selectively isolate or couple the volatile memory subsystem to the host system.” Ex. 1001, 20:50–54. Petitioner relies on similar evidence, that is, the same alleged “circuit” in Shimada as that relied upon for claim 1, for disclosure of the claim 2 limitations, and the Petition’s arguments are supported by Mr. Maltiel’s Declaration. Pet. 29; Ex. 1003 ¶¶ 145–148.

Patent Owner argues that because Petitioner relies on the same elements of Shimada mapped to claim 1 for support of its anticipation challenge to claim 2, it fails for similar reasons to those asserted for claim 1. PO Resp. 56–57. Patent Owner provides no additional argument or explanation that differs from the issues previously addressed for claim 1, and

we find Patent Owner’s argument unpersuasive for the reasons discussed above for claim 1.

Accordingly, we are persuaded Petitioner has shown by a preponderance of the evidence that claim 2 of the ’243 patent is anticipated by Shimada.

c. Claims 3, 5–8, 13–15, 17–20, and 25–27

Claims 13 and 25 are independent claims, and Patent Owner alleges that the Petition is deficient as to the anticipation challenges for the same reasons that it set forth for independent claim 1. PO Resp. 55–56. For dependent claims 3, 5–8, 14, 15, 17–20, 26, and 27, Patent Owner alleges that the Petition is deficient as to the anticipation challenges for the same reasons as the independent claims from which these claims depend. *Id.* at 57–58. As discussed above, we do not find Patent Owner’s arguments regarding claim 1 to be persuasive.

Petitioner’s anticipation analysis, as supported by Mr. Maltiel’s Declaration, relies on testimony as to where each element of challenged claims 3, 5–8, 13–15, 17–20, and 25–27 is disclosed in Shimada. Pet. 29–39, 45–54; Ex. 1003 ¶¶ 149–185, 219–240, 249–262. We agree with and adopt Petitioner’s analysis and credit Mr. Maltiel’s testimony.

Accordingly, we are persuaded Petitioner has shown by a preponderance of the evidence that claims 3, 5–8, 13–15, 17–20, and 25–27 of the ’243 patent are anticipated by Shimada.

d. Claims 9, 21, and 28

Claim 9 depends from claim 1, and additionally recites “wherein the memory system transitions from the first mode to the second mode upon detecting that a trigger condition is likely to occur.” Ex. 1001, 21:20–23. Claims 21 and 28 recite similar limitations. *See id.* at 22:28–31, 23:6–10.

Petitioner asserts that the transition from the first to the second mode can be in response to trigger conditions (e.g., the power has stopped), which are detected by the “condition-change detect unit” that can detect the transition from the fully “power-on” state to the “power-off” state. Pet. 39 (citing Ex. 1005, 2:28–39; Ex. 1003 ¶¶ 186–187). Petitioner contends that, although Shimada does not explicitly disclose the details of the transition from the first to the second mode, it discloses that “upon detection of a voltage reduction in the main power source, the main power source is replaced.” *Id.* (citing Ex. 1005, 1:41–43). It is argued that one of ordinary skill in the art “would have understood that the ‘condition-change detect unit’ detecting a change from ‘power-on to power-off’ must have been implemented in a way that transitions the ‘semiconductor memory device 1’ from the first mode to the second mode before complete ‘power failure’ in order to achieve its intended purpose (i.e., preventing loss of stored data upon power failure).” *Id.* at 39–40 (citing Ex. 1005, 1:63–67, 9:13–21; Ex. 1003 ¶ 188).

As discussed in the Institution Decision, the principle of inherency under anticipation requires that any information missing from the reference would nonetheless be known to be present in the subject matter of the reference, when viewed by persons experienced in the field of the invention. Dec. 20–21. However, “anticipation by inherent disclosure is appropriate only when the reference discloses prior art that must *necessarily* include the unstated limitation.” *Transclean Corp. v. Bridgewood Servs., Inc.*, 290 F.3d 1364, 1373 (Fed. Cir. 2002) (internal citation omitted); *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (that a feature in the prior art reference “could” operate as claimed does not establish inherency). Thus, when a claim limitation is not set forth explicitly in a reference, evidence “must

make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.” *Continental Can Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (citations omitted). It is not sufficient if a material element or limitation is “merely probably or possibly present” in the prior art. *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295 (Fed. Cir. 2002) (citations omitted); see *W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554 (Fed. Cir. 1983) (anticipation “cannot be predicated on mere conjecture respecting the characteristics of products that might result from the practice of processes disclosed in references”) (citation omitted).

There is no dispute that Shimada does not disclose the limitation explicitly. Although Petitioner’s expert provides an explanation of why Shimada’s transition must be implemented in the claimed way, the reference itself discloses the mode transition occurs under an alternative condition, that is, by the detection of an actual voltage reduction. See Ex. 1005, 1:41–43. The evidence, therefore, does not support Petitioner’s contention that the transition necessarily occurs under an alternative condition as required for anticipation.

Accordingly, the Petition has not shown by a preponderance of the evidence that claims 9, 21, and 28 of the ’243 patent are anticipated by Shimada.

e. Claims 10, 22, and 29

Claim 10, which depends from claim 1, additionally claims that “the controller is operable to perform signal level translation between the volatile memory subsystem and the non-volatile memory subsystem.” Ex. 1001, 21:23–26. Claims 22 and 29 contain similar limitations. See *id.* at 22:28–31, 23:11–15.

Petitioner asserts that, although Shimada does not explicitly disclose changing voltage levels of signals¹² between the volatile memory subsystem and the non-volatile memory subsystem, “one skilled in the art would have understood that the controller unit of Shimada must necessarily have been operable to change the voltage levels of signals.” Pet. 40 (citing Ex. 1003 ¶¶ 194–195). Petitioner alleges that this was necessary “in order to comply with the different standards associated with those different types of memory and/or to avoid any damage from high voltage,” as well as reliance on other references. *Id.* at 41.

Although Petitioner’s expert asserts that the controller unit of Shimada “must necessarily have been operable to change the voltage levels of signals,” (see Ex. 1003 ¶ 195), the Petition and expert testimony fail to demonstrate the necessity of a change of voltage levels because there is no showing that the types of memories in Shimada would be required to be different. The evidence provided to support Petitioner’s proposition is, therefore, insufficient and fails to persuade for the purposes of demonstrating anticipation.

Accordingly, the Petition has not shown by a preponderance of the evidence that claims 10, 22, and 29 of the ’243 patent are anticipated by Shimada.

¹² Petitioner asserts that “signal level translation” includes “changing voltage levels,” which Patent Owner did not dispute in the Preliminary Response, but rather argued that the term should not be construed to be so limited. Pet. 12 (citing Ex. 1001, 7:39–42; Ex. 1003 ¶¶ 78–79); Prelim Resp. 26. On this record, therefore, the parties agree at least that the term “signal level translation” can include “changing voltage levels.”

f. Claims 11, 23, and 30

Claim 11, which depends from claim 1, additionally claims that “the controller is operable to perform address to address translation between the volatile memory subsystem and the non-volatile memory subsystem.” Ex. 1001, 21:27–30. Claims 23 and 30 contain similar limitations. *See id.* at 22:32–35, 23:16–20.

Petitioner asserts that Shimada discloses an embodiment in which the capacity of the non-volatile memory is N times that of the volatile memory, and the control unit must necessarily perform an address to address translation in order to copy data between the two memories. Pet. 41–42 (citing Ex. 1005, 5:43–56, Fig. 4; Ex. 1003 ¶¶ 204, 205). Petitioner asserts that this address to address translation is performed using “an area-select signal.” *Id.* at 42 (citing Ex. 1005, 5:57–64; Ex. 1003 ¶ 205).

Here, there is no explicit disclosure in Shimada of the use of address to address translation, and Petitioner fails to sufficiently support their argument that such translation necessarily occurs in Shimada. More specifically, Petitioner’s expert, Mr. Maltiel, fails to provide sufficient explanation as to why Shimada’s use of area select signals necessarily includes address to address translations in the embodiments relied upon. *See* Ex. 1005, 5:57–64; Ex. 1003 ¶ 205.

Accordingly, the Petition has not shown by a preponderance of the evidence that claims 11, 23, and 30 of the ’243 patent are anticipated by Shimada.

g. Claims 12 and 24

Claim 12, which depends from claim 1, additionally claims “wherein the controller generates at least one of address and control signals for the

non-volatile memory subsystem.” Ex. 1001, 21:31–33. Claim 24 contains a similar limitation. *Id.* at 22:36–38.

Similar to its contentions for claim 11, Petitioner alleges that with Shimada’s selection of memory areas for copying data, that one of ordinary skill in the art would understand that its control unit would generate translated address signals. Pet. 44 (citing Ex. 1005, 5:43–56, 5:57–64, 6:22–26, 6:39–43, Figs. 4 and 5; Ex. 1003 ¶¶ 215–216). For the reasons discussed above, we determine that the Petitioner fails to sufficiently support its contentions.

Accordingly, the Petition has not shown by a preponderance of the evidence that claims 12 and 24 of the ’243 patent are anticipated by Shimada.

h. Conclusion

For the reasons discussed, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3, 5–8, 13–15, 17–20, and 25–27 of the ’243 patent are anticipated by Shimada, but has not demonstrated by a preponderance of the evidence that claims 9–12, 21–24, and 28–30 of the ’243 patent are anticipated by Shimada.

E. Asserted Obviousness of Claims 4 and 16 by Shimada and Oh

In support of this asserted ground of unpatentability, Petitioner explains how the combination of Shimada and Oh renders claims 4 and 6 obvious. Pet. 55–57. In its Response, Patent Owner contends there is insufficient rationale provided for placing the switchable termination structures of Oh inside Shimada’s selector. See PO Resp. 58–61.

We find that Petitioner has demonstrated by a preponderance of the evidence that the combination of Shimada and Oh render claims 4 and 6 obvious for the reasons discussed below.

We begin our analysis with a summary of Oh, and then address the arguments and evidence presented by the parties.

1. Oh (Ex. 1012)

Oh is directed to a high-bandwidth memory systems. Ex. 1012, 1:16–17. Oh discloses that on-die termination is a technology where the termination resistor for impedance matching in transmission lines is located inside an integrated circuit of the memory device or memory controller. *Id.* at 1:13–20. The on-die termination structure includes switch elements. *Id.* at 1:38–49. Oh’s memory devices may transition between the idle state and various low power states, initialization states, calibration states, and configuration states. *Id.* at 10:5–10.

2. Analysis

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective

evidence of nonobviousness.¹³ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Claim 4, which depends from claim 1, requires “wherein the circuit includes an on-die termination.” Ex. 1001, 20:57–58. Claim 16 includes a similar limitation. *Id.* at 21:61–62.

Petitioner relies on Oh for the teaching of on-die termination, which describes the use of termination resistors for impedance matching in transmission lines, located inside an integrated circuit of the memory device. Pet. 55–56 (citing Ex. 1012, 1:13–20). Shimada and Oh are alleged to be analogous art because they both relate to memory systems, and include transitioning between power states. Pet. 56; Ex. 1003 ¶ 273. Petitioner also asserts that one of ordinary skill in the art would have been motivated to combine the references: (1) to increase the bandwidth of the memory systems by matching the impedances within the integrated circuit; (2) because implementing on-die termination outside the volatile memory was routinely done and would have been expected to provide predictable and reliable performance; and (3) because off-chip on-die terminations were required by standards at the time of the invention. *Id.* at 55–57 (citing Ex. 1003 ¶¶ 269–273; Ex. 1012, 1:13–20; Ex. 1013, 1:16–18; Ex. 1011 ¶¶ 91, 140; Ex. 1014, 27–40; Ex. 1022, 1:65–2:3). Petitioner refers to Oh’s teachings to contend that on-die terminations can be on the memory device or memory controller. *Id.* at 56 (citing Ex. 1012, 1:13–20).

Patent Owner argues that the Petitioner’s assertion that one of ordinary skill in the art would have been motivated to combine Shimada and

¹³ Patent Owner does not present arguments or evidence of objective indicia of nonobviousness in its Patent Owner Response.

Oh to increase the bandwidth of the memory systems is not supported by the references. PO Resp. 60 (citing Ex. 2016 ¶¶ 155–162). Patent Owner alleges that Oh does not teach that on-die terminations increases bandwidth, and instead Oh suggests that if the memory system is already high-bandwidth, on-die termination should be used. *Id.* at 61 (citing Ex. 1012, 1:13–20; Ex. 2016 ¶ 152). Patent Owner also disagrees that a skilled artisan would have been motivated to employ such a combination because “off-chip on-die” terminations were not required by standards, and because the cited references do not support that assertion. *Id.* at 61 (citing Ex. 1014; Ex. 1022; Ex. 2016 ¶ 157). Patent Owner argues, therefore, that there is no motivation to place Oh’s switchable termination structures inside Shimada’s selector. *Id.* at 60–61.

In response, Petitioner refers to the emphasis in Shimada on the importance of high “access speed” (i.e., bandwidth) in its memory devices. Pet. Reply 22 (citing Ex. 1005, 5:30–34, 8:22–26, 9:35–39). Patent Owner also refers to Dr. Baker’s testimony (Ex. 1030, 52:8–54:16), in support of the view that a person of ordinary skill in the art would have known to use impedance matching for minimizing reflections in a circuit when there is increased signal rates. *Id.* at 22–23 (citing Pet. 55–56; Ex. 1012, 1:13–20; Ex. 1003 ¶¶ 270–271; Ex. 1030, 51:15–52:7). Petitioner also refers to Dr. Baker’s testimony related to the JEDEC standard’s reference to on-die terminations that are “off-chip,” and not part of a DRAM chip. *Id.* at 23 (citing Ex. 1030, 148:14–149:6; Ex. 1014, 91).

We credit Mr. Maltiel’s testimony that the use of on-die termination was known and Oh teaches the use of impedance matching in transmission lines inside the integrated circuit of memory devices. Ex. 1003 ¶¶ 270–271. Dr. Baker confirms that impedance matching with increased signal rates

reduces reflections and error. Ex. 1030, 51:15–54:16. The Supreme Court has stated that “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *KSR*, 550 U.S. at 417. Here, we are persuaded that sufficient evidence supporting the rationale to combine has been demonstrated such that one of skill in the art would have been motivated to add Oh’s known on-die terminations to Shimada to provide more predictable and reliable performance in high speed applications and to conform to required standards at the time the ’243 patent was filed. See Ex. 1003 ¶¶ 270–275.

In summary, for the reasons discussed above, we are persuaded Petitioner has shown by a preponderance of the evidence that claims 4 and 16 of the ’243 patent are unpatentable as obvious over Shimada and Oh.

F. Asserted Obviousness of Claims 1, 3, 6, 9–13, 15, 18, 21–25, and 28–30 Over Shimada Alone or in Combination with Other References

In support of the challenges that claims 1, 3, 6, 9–13, 15, 18, 21–25, and 28–30 would have been obvious, Petitioner explains how Shimada alone, or in combination with other references of Bonella, Goodwin, Sasaki, and Tsunoda, would have rendered the claims obvious. Pet. 55–73. In its Response, Patent Owner contends there is insufficient rationale to combine some of the prior art references and that some claim limitations are not taught. See PO Resp. 61–68.

We find that Petitioner has demonstrated by a preponderance of the evidence that the combination of the prior art renders claims 1, 3, 6, 9–13, 15, 18, 21–25, and 28–30 obvious for the reasons discussed below.

We begin our analysis with a summary of Bonella, Goodwin, Sasaki, and Tsunoda, and then address the arguments and evidence presented by the parties.

1. Bonella (Ex. 1009)

Bonella discloses a hybrid memory system that includes a volatile and non-volatile memory. Ex. 1009, Abstract, ¶ 27, Fig. 1. Upon a power loss data is “flushed” or written to the non-volatile flash memory, and with new power resumed, data is restored to the volatile dynamic random access memory (DRAM). *Id.* ¶¶ 27, 101. A router acts as a bus control center that uses path multiplexers for address, command, and data transmissions. *Id.* ¶¶ 41, 43.

2. Goodwin (Ex. 1015)

Goodwin is directed to anticipating input power failures with responsive circuitry. Ex. 1015, Abstract, 1:63–2:39. Power failure detection circuitry anticipates the occurrence of a power failure, and provides additional time for equipment to react to the failure, thus avoiding the likelihood of severe unpredictable disruptions to signal processing and allowing normal resumption of processing when power is restored. *Id.* at 1:46–54.

3. Sasaki (Ex. 1017)

Sasaki is directed to memory control circuitry for volatile and nonvolatile memories. Ex. 1017, 3:3–6. The volatile and non-volatile memories use different voltages. *Id.* In order to prevent higher than allowable voltages, the voltage levels are converted between the non-volatile memory and volatile memory systems. *Id.* at 3:6–12.

4. *Tsunoda (Ex. 1019)*

Tsunoda is directed to a memory apparatus that uses volatile and nonvolatile memories. Ex. 1019 ¶ 1. Tsunoda discloses transferring data between the volatile and non-volatile memories. *Id.* ¶ 42. Tsunoda's control unit transfers data between the SDRAM (volatile memory) and flash memory (non-volatile memory), with translation by the use of an address correspondence setting function. *Id.* ¶ 62. Translation is done using a mapping table. *Id.* ¶ 107.

5. *Analysis*

a. Claims 1, 3, 13, 15, and 25

As an alternative ground to its anticipation challenge, Petitioner asserts that it would have been obvious to include Bonella's path multiplexers in Shimada to operate to "selectively isolate the controller from the volatile memory subsystem," as recited in claims 1, 3, 13, 15, and 25. Pet. 57–63. Petitioner contends that Bonella discloses that its router is made up of path multiplexers, and path multiplexers would selectively isolate unselected ports. *Id.* at 59 (citing Ex. 1009 ¶ 43; Ex. 1003 ¶¶ 122–126, 133; Ex. 1008, 2–3; Ex. 1006, 3:61–63; Ex. 1007, 6:63–65). Mr. Maltiel testifies that one of skill in the art would understand that a multiplexer would selectively isolate outputs such that the control unit 102 of Shimada will not be able to communicate with the volatile memory 103 when the first mode is selected. Ex. 1003 ¶¶ 122–125. Mr. Maltiel testifies that Shimada and Bonella are both analogous art because each is from the field of memory systems. *Id.* ¶ 135. He also testifies that one of ordinary skill in the art would have been motivated to combine the references because: (1) it was known that writing to non-volatile memory is much slower than writing to a volatile memory and there would have been motivation to use a multiplexer

to isolate the load of the non-volatile memory; and (2) the use of a multiplexer would greatly reduce the erase/write cycles to be performed for the non-volatile memory. *Id.*

Petitioner's obviousness analysis, as supported by Mr. Maltiel's Declaration, relies on testimony as to where each element of the challenged claims is taught in Shimada and Bonella. Pet. 57–63; Ex. 1003 ¶¶ 129–154. We agree with and adopt Petitioner's analysis and credit Mr. Maltiel's testimony.

Patent Owner argues that Bonella fails to teach claim limitations for reasons similar to those given for Shimada alone, that is, that its multiplexer is required to couple or uncouple components, not to select components or modes. PO Resp. 62–63 (citing Ex. 2016 ¶¶ 172–173). Patent Owner refers back to the Phillips multiplexer example from the discussion on Shimada, and argues that Bonella's multiplexer is deficient for similar reasons to those presented for the Phillips example. *Id.* at 63–64 (citing Ex. 2016 ¶¶ 166–171). For the reasons discussed *supra* Section II.D, we do not find Patent Owner's arguments persuasive.

Patent Owner additionally argues that a person of ordinary skill in the art would not have been motivated to combine Shimada and Bonella because they are in different fields and designed for different applications. See Ex. 2016 ¶ 164. Shimada's device is characterized as a device to retain data without requiring a large-scale backup power source and is included in one chip, and Bonella is an add-in memory module that comprises a plurality of memory chips. See *id.*; PO Resp. 62 (citing Ex. 1005, 1:63–2:3; Ex. 1009 ¶ 2, Abstract). Weighing the evidence, Petitioner provides adequate support that Shimada and Bonella are both in the field of memory devices, and one of skill in the art would have had sufficient rationale to combine the

references. We are not persuaded by Patent Owner's reference to the one chip use of Shimada, which is presumably intended to support an argument that Shimada and Bonella cannot be combined. As Petitioner alleges, however, Shimada's chip is mountable on a circuit board, which supports that it could be combinable with other components. *See* Pet. Reply 23–24 (citing Ex. 1005, 4:66–5:3).

In summary, for the reasons discussed above, we are persuaded Petitioner has shown by a preponderance of the evidence that claims 1, 3, 13, 15, and 25 of the '243 patent are unpatentable as obvious over Shimada and Bonella.

b. Claims 6 and 18

Claim 6 recites the limitation of “an interface that is configured to be in electrical communication with the host system and the first set of signal lines,” and “wherein the interface provides a plurality of conduits for data, address, and control signals between the memory system and the host system using the first set of signal lines.” Ex. 1001, 21:1–7. Claim 18 has similar limitations. *Id.* at 22:5–11. Petitioner asserts that, to the extent that Shimada does not disclose the limitations, one of skill in the art would have understood that in order for Shimada's invention to work and be useful, it would have been necessary to employ the interface as claimed. Pet. 64–66.

Petitioner's obviousness analysis, as supported by Mr. Maltiel's Declaration, relies on testimony as to where each element of the challenged claims is taught in Shimada. Pet. 64–66; Ex. 1003 ¶¶ 170–173. We agree with and adopt Petitioner's analysis and credit Mr. Maltiel's testimony.

Patent Owner provides no additional issues or arguments related to the Petitioner's evidence and argument except those asserted as to claim 1, which we have found unpersuasive as discussed above. PO Resp. 65.

In summary, for the reasons discussed above, we are persuaded Petitioner has shown by a preponderance of the evidence that claims 6 and 18 of the '243 patent are unpatentable as obvious over Shimada.

c. Claims 9, 21, and 28

Petitioner alleges that the additional claim limitation “transitions/[ing] from the first mode to the second mode upon detecting that a trigger condition is likely to occur” as recited in claims 9, 21, and 28, is taught by the combination of Goodwin and Shimada. Pet. 66. Petitioner asserts that it was known to those of ordinary skill in the art to switch to backup power upon detection that a power failure is likely to occur, rather than switching when it is too late. *Id.* at 66–67 (citing Ex. 1015, 1:37–54; Ex. 1003 ¶ 189). It is alleged that Goodwin discloses that anticipating the occurrence of a potential power failure provides additional time for the device to react to the power failure, and avoids disruptions, so one skilled in the art would have been motivated to combine Shimada with Goodwin to further ensure that the volatile memories in Shimada do not lose data by entering the backup mode when a power loss condition could reasonably be expected. *Id.* at 67 (citing Ex. 1005 at 1:28–29; Ex. 1015, 1:46–54, 3:38–40; Ex. 1003 ¶ 191). Petitioner also contends that Goodwin and Shimada are analogous art because they are “pertinent to the particular problem addressed by the '243 patent, [that is,] dealing with potential power disruptions in electronic circuits.” *Id.* (citing Ex. 1001, 1:34–2:38; Ex. 1005, 1:63–3:5; Ex. 1015, Abstract, 1:63–2:39; Ex. 1003 ¶ 190).

Petitioner’s obviousness analysis, as supported by Mr. Maltiel’s Declaration, relies on testimony as to where each element of the challenged claims is taught in the combination of Shimada and Goodwin. Pet. 66–68;

Ex. 1003 ¶¶ 189–192. We agree with and adopt Petitioner’s analysis and credit Mr. Maltiel’s testimony.

Patent Owner argues that Goodwin is a power failure detection apparatus for use in a power supply to provide a regulated voltage signal to a computer, however, Goodwin does not teach that its power failure detection is designed to operate in a device such as Shimada’s single chip. PO Resp. 65 (citing Ex. 1015, Abstract; Ex. 2016 ¶ 180). Patent Owner alleges that Goodwin does not detect that a power failure is likely to occur, but rather that it has occurred. *Id.* at 65–66 (citing Ex. 2016 ¶¶ 180, 182–183). Patent Owner further contends that because Shimada teaches a system that is fully contained in a single chip, one of ordinary skill in the art would have not been motivated to apply Goodwin’s power supply circuitry. *Id.* (citing Ex. 2016 ¶ 181).

We do not find Patent Owner’s arguments persuasive. Goodwin teaches that anticipating a power failure before it actually occurs is advantageous (*see* Ex. 1015, 1:46–54), and a rationale for demonstrating the combination of references to add this feature has been demonstrated. Further, as Petitioner argues, the evidence supports that Shimada’s chip would operate with a power supply in a computer, so Goodwin’s features would be combinable. *See* Pet. Reply 25.

In summary, for the reasons discussed above, we are persuaded Petitioner has shown by a preponderance of the evidence that claims 9, 21, and 28 of the ’243 patent are unpatentable as obvious over the combination of Shimada and Goodwin.

d. Claims 10, 22, and 29

Petitioner asserts that the additional claim limitation “signal level translation between the volatile memory subsystem and the non-volatile

memory subsystem,” as recited by claims 10, 22, and 29 is taught by the combination of Shimada and Sasaki. Pet. 68. Petitioner contends that, as explained in Sasaki, one of ordinary skill in the art would have known that volatile and non-volatile memories could have different input swing levels that are acceptable, and the voltage levels must be translated to prevent high voltage used in non-volatile memory systems from being applied to volatile memory systems. *Id.* at 68–69 (citing Ex. 1017, 3:3–12; Ex. 1003 ¶ 196). Petitioner also argues that the prior art references are analogous art in the same field of endeavor (hybrid memory systems including volatile and non-volatile memory subsystems), are pertinent to the problem of the ’243 patent (sharing signal lines between nonvolatile memory and volatile memory), and one would have been motivated to combine the references to meet applicable standards. *Id.*

Petitioner’s obviousness analysis, as supported by Mr. Maltiel’s Declaration, relies on testimony as to where each element of the challenged claims is taught in the combination of Shimada and Sasaki. Pet. 68–70; Ex. 1003 ¶¶ 196–199. We agree with and adopt Petitioner’s analysis and credit Mr. Maltiel’s testimony.

Patent Owner argues that the Petition fails to show why a person of ordinary skill in the art would have been motivated to use two different source voltages in Shimada’s single chip because Shimada’s memories are the same type, so they would operate at the same voltage level. PO Resp. 66–67 (citing Ex. 1005, 5:6–9; Ex. 2016 ¶186). We do not find Patent Owner’s argument to be persuasive because Shimada also teaches other different types of memories such as a flash memory for the non-volatile memory are allowable, which is different than the SRAM or DRAM of the volatile memory. See Pet. Reply 26–27; Dec. 35; Ex. 1005, 5:6–11.

In summary, we are persuaded Petitioner has shown by a preponderance of the evidence that claims 10, 22, and 29 of the '243 patent are unpatentable as obvious over the combination of Shimada and Sasaki.

e. Claims 11, 12, 23, 24, and 30

Petitioner argues that, to the extent that Shimada's control unit alone is found insufficient to disclose the limitation "perform address to address translation between the volatile memory subsystem and the non-volatile memory subsystem," as recited in claims 11, 23, and 30, it would have been obvious over Shimada in view of Tsunoda. Pet. 70–72. It is also argued for claims 12 and 24, that, to the extent that a controller that "generates at least one of address and control signals for the non-volatile memory subsystem," is not disclosed by Shimada, it would have been obvious over Shimada in view of Tsunoda. *Id.* at 72. Petitioner relies upon Tsunoda's teaching of translations between the volatile memory and non-volatile memory that uses an "address correspondence setting function" and generates control signals in order to execute data transfer. *Id.* at 70–72 (citing Ex. 1019 at ¶¶ 62, 107; Ex. 1003 ¶¶ 210, 212, 218). Petitioner further alleges that one of ordinary skill in the art would have been motivated to combine Shimada and Tsunoda in order to use address translation where there is no one-to-one correspondence between the addresses of the non-volatile and volatile memories because, absent such translation, not all of the non-volatile memory would be utilized. *Id.* at 71–72. It is also alleged that the references "are analogous art to the '243 Patent because they are all in the same field of endeavor, i.e., hybrid memory systems including volatile and non-volatile memory subsystems," and are reasonably pertinent to the problem addressed by the '243 patent. *Id.* at 71 (emphasis omitted).

Petitioner's obviousness analysis, as supported by Mr. Maltiel's Declaration, relies on testimony as to where each element of the challenged claims is taught in the combination of Shimada and Tsunoda. Pet. 70–72; Ex. 1003 ¶¶ 209–212. We agree with and adopt Petitioner's analysis and credit Mr. Maltiel's testimony.

Patent Owner argues that Tsunoda is directed to address translation when data is transferred between memories of different sizes, and this would be unnecessary in Shimada because each of its nonvolatile memory areas is the size of its volatile memories and would map directly. PO Resp. 67 (citing Ex. 2106 ¶ 189). Patent Owner asserts that one of ordinary skill in the art, therefore, would have not been motivated to combine Tsunoda's address mapping with Shimada. *Id.* at 67–68 (citing Ex. 2106 ¶¶ 189–193).

As discussed above, Shimada teaches the use of other different types of memories such as a flash memory for the non-volatile memory as compared to a SRAM or DRAM for the volatile memory. Ex. 1005, 5:6–11. Petitioner argues that given the different types of memories that could be used, different addressing would be required and Patent Owner's expert, Dr. Baker, admits this. Pet. Reply 27–28 (citing Ex. 1030, 35:16–36:7, 28:16–22, 33:7–12; citing also Ex. 2010, 43:6–12, 44:12–20, 45:11–19, 62:6–16; Ex. 1023). Considering this evidence, we are not persuaded by Patent Owner's arguments because, even if the memories were the same size, the evidence supports that the memory types of Shimada may be different, with different addressing required, thus supporting a rationale to combine Tsunoda with Shimada.

In summary, for the reasons discussed above, we are persuaded Petitioner has shown by a preponderance of the evidence that claims 11, 12,

23, 24, and 30 of the '243 patent are unpatentable as obvious over the combination of Shimada and Tsunoda.

III. ALLEGED IMPERMISSIBLE NEW ARGUMENTS IN PETITIONER REPLY

Patent Owner argues that Petitioner asserted new arguments in Petitioner's Reply that are allegedly beyond the scope of what can be considered appropriate for a reply, and identified portions of the Reply at issue. Paper 25. Petitioner filed a response identifying portions of the Patent Owner's Response that it alleges its Reply is responsive to or where in the Petition the argument may be found. Paper 27.

We have considered Patent Owner's identification of the portions of Petitioner's Reply that are alleged to be beyond the scope of a reply, and determine that the cited portions of Petitioner's Reply and associated evidence are within the scope of what is appropriate for a reply. Replies are a vehicle for responding to arguments raised in a corresponding patent owner response. Petitioner's arguments and evidence that Patent Owner objects to are not beyond the proper scope of a reply because we find that they fairly respond to Patent Owner's arguments raised in Patent Owner's Response. *See Idemitsu Kosan Co. v. SFC Co.*, 870 F.3d 1376, 1381 (Fed. Cir. 2017) ("This back-and-forth shows that what Idemitsu characterizes as an argument raised 'too late' is simply the by-product of one party necessarily getting the last word. If anything, Idemitsu is the party that first raised this issue, by arguing—at least implicitly—that Arkane teaches away from non-energy-gap combinations. SFC simply countered, as it was entitled to do.").

IV. MOTIONS TO EXCLUDE

A. *Petitioner's Motion to Exclude*

1. *Exhibits 2004, 2005, 2011, 2012, and 2022*

Petitioner moves to exclude Exhibits 2004, 2005, 2011, 2012, and 2022 as not being relevant to any issue on which trial has been instituted, lacking foundation, and/or causing undue prejudice. Pet. Mot. Ex. 1–2. More specifically, Petitioner argues that Exhibits 2004, 2005, 2011, 2012, and 2022 “were not discussed or cited anywhere in Patent Owner’s Response, and Patent Owner does not rely on these exhibits to prove anything.” *Id.* at 1.

Patent Owner’s response to the motion disputes Petitioner’s contention that Exhibits 2011, 2012, and 2022 were not relied upon, and notes the portions of Dr. Baker’s Declaration (Ex. 2016), where the exhibits were cited, as well as the cross-references in Patent Owner’s Response that cite to the Declaration. PO Mot. Ex. Opp. 1. Patent Owner also argues that the exhibits provide context for certain opinions rendered by Dr. Baker and should not be excluded under FRE 702. *Id.* at 2. Patent Owner provides no argument on Exhibits 2004 and 2005. *See id.* at 1–2.

Upon review of the parties’ arguments, we grant the Motion to Exclude with respect to Exhibits 2004 and 2005, but deny the motion with respect to Exhibits 2011, 2012, and 2022 because Patent Owner has demonstrated that these exhibits were relied upon by Dr. Baker in his declaration with citations to portions of Dr. Baker’s declaration.

2. *Exhibit 2015 and Paragraphs 84–90 of Exhibit 2016*

Petitioner seeks to exclude Exhibit 2015, the Federal Circuit decision, arguing that it is directed to an unrelated patent and no proposed

construction relates to the claim terms at issue in this proceeding. Pet. Mot. Ex. 2. Petitioner also moves to exclude paragraphs 84–90 of Exhibit 2016 as evidence, because these portions relate to the Federal Circuit decision. *Id.* at 4–5.

Patent Owner alleges that Exhibit 2015 and related paragraphs 84–90 of Exhibit 2016, are relevant because the patent in that case is also related to memory modules. PO Mot. Ex. Opp. 2–3, 7–11. Patent Owner asserts that a position on an interpretation of “selectively electrically coupling,” which is also in this proceeding, is the same as that in the Federal Circuit case. *See id.*

We agree that with the Petitioner that the patents at issue in the Federal Circuit decision are not related to the ’243 patent in this proceeding. However, evidence is relevant if it has any tendency to make a fact more or less probable than it would be without the evidence and the fact is of consequence in determining the action. *See* Fed. R. Evid. 401. As discussed, *supra* Sections II.B and II.D, we have considered the Federal Circuit decision to the extent that it parses out a limitation of “selecting,” and otherwise generally distinguish the decision based upon differences in the claims.

We, therefore, deny Petitioner’s motion to exclude as to Exhibit 2015 and paragraphs 84–90 of Exhibit 2016.

3. *Paragraphs 52, 65–67, 91, 110, 116, 119, 120–126, 136, 137, 139, 140, 153, 155, 172, 173, 180, and 181 of Exhibit 2016*

Petitioner seeks to exclude paragraphs 52, 65–67, 91, 110, 116, 119, 120–126, 136, 137, 139, 140, 153, 155, 172, 173, 180, and 181 of Exhibit 2016, arguing that these portions are irrelevant because it is alleged that Dr. Baker provided contradictory deposition testimony to that provided in the

declaration, these portions of the declaration ignored some claim elements, and/or the arguments are not relevant to the invalidity analysis. *Id.* at 3–6. These objections go to the weight given to the testimony, and are not a proper basis for a motion to exclude.

We therefore deny Petitioner’s motion to exclude as to paragraphs 52, 65–67, 91, 110, 116, 119, 120–126, 136, 137, 139, 140, 153, 155, 172, 173, 180, and 181 of Exhibit 2016.

4. Paragraphs 1–32, 36, 37, and 53–63 of Exhibit 2016

Petitioner further moves to exclude paragraphs 1–32, 36, 37, and 53–63 of Exhibit 2016 because they are not cited in Patent Owner’s Response and are irrelevant to any issue at trial. Pet. Mot. Ex. 6–7. Patent Owner argues that these portions of Dr. Baker’s Declaration are not prejudicial and provide general information and context. *Id.* at 15.

These portions at issue in Dr. Baker’s Declaration concern his qualifications, background, general understanding of legal standards and some claims, as well as views of one of ordinary skill in the art. Some of these issues go to the weight given to the testimony, and are not a proper basis for a motion to exclude. Additionally, we are encouraged to consider all evidence of record that is probative of the background knowledge of a person of ordinary skill in the relevant technology. *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362–63 (Fed. Cir. 2013).

Accordingly, Petitioner’s Motion to Exclude paragraphs 1–32, 36, 37, and 53–63 of Exhibit 2016 is denied.

B. Patent Owner’s Motion to Exclude

Patent Owner moves to exclude Exhibit 1024, which Petitioner first cited in Reply, because it is alleged that the document is not relevant to any

issue for which trial has been instituted, lacks authentication, contains hearsay, and/or is unduly prejudicial. PO Mot. Ex. 2. Because our decision does not rely on this exhibit, we dismiss Patent Owner's Motion to Exclude Evidence as moot.

V. CONCLUSION

For the foregoing reasons, we are persuaded Petitioner has demonstrated by a preponderance of the evidence, that challenged claims 1–30 of the '243 patent are unpatentable based on the following grounds:

Ground	Claims	Prior Art
§ 102	1–3, 5–8, 13–15, 17–20, 25–27	Shimada
§ 103	4, 16	Shimada and Oh
§ 103	1, 3, 13, 15, 25	Shimada and Bonella
§ 103	6, 18	Shimada
§ 103	9, 21, 28	Shimada and Goodwin
§ 103	10, 22, 29	Shimada and Sasaki
§ 103	11, 12, 23, 24, 30	Shimada and Tsunoda

VI. ORDER

Accordingly, it is

ORDERED that claims 1–30 of the '243 patent are determined to be *unpatentable*;

FURTHER ORDERED that Petitioner's Motion to Exclude as to Exhibits 2004 and 2005 is *granted-in part* and Petitioner's Motion to Exclude as to Exhibits 2011, 2012, 2015, and 2022 and paragraphs 1–32, 36,

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37, 53–63, 65–67, 84–91, 110, 116, 119, 120–126, 136, 137, 139, 140, 153, 155, 172, 173, 180, and 181 of Exhibit 2016 is *denied-in-part*;

FURTHER ORDERED that Patent Owner’s Motion to Exclude is *denied*;

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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