

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BROADCOM LIMITED,
Petitioner,

v.

INVENSAS CORPORATION,
Patent Owner.

Case IPR2017-00831
Patent 6,232,231 B1

Before MICHAEL R. ZECHER, LYNNE E. PETTIGREW, and
KAMRAN JIVANI, Administrative Patent Judges.

JIVANI, Administrative Patent Judge.

DECISION

Denying Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. INTRODUCTION

Broadcom Limited (“Petitioner”) requests an *inter partes* review of claims 1–16 (the “Challenged Claims”) of U.S. Patent No. 6,232,231 B1 (Ex. 1001, the “’231 patent”). Paper 1 (“Petition” or “Pet.”). Invensas Corp. (“Patent Owner”) has filed a Preliminary Response.¹ Paper 6 (“Prelim. Resp.”).

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless it is determined that there is a reasonable likelihood that the petitioner would prevail with respect to at least one of the claims challenged in the petition. Applying this standard, we are not persuaded Petitioner has shown a reasonable likelihood that it would prevail with respect to at least one of the Challenged Claims because the Petition does not account properly for all the limitations of independent claims 1 and 9. Accordingly, we deny the Petition and decline to institute *inter partes* review of the Challenged Claims for the reasons set forth below.

II. BACKGROUND

A. *The ’231 patent (Ex. 1001)*

The ’231 patent relates to manufacturing interconnects in integrated circuits. Ex. 1001, 1:8–12. A process known as chemical-mechanical polishing (“CMP”) is used to form a planarized layer during manufacturing of integrated circuit interconnects. *Id.* at 1:49–55. The ’231 patent describes undesirable elevational disparities that may result during this process, making it difficult to print high resolution features. *Id.* at 1:28–48. In

¹ Patent Owner identifies Tessera Technologies Inc. and Tessera, Inc. as additional real parties in interest. Paper 4, 1 (“Patent Owner’s Mandatory Notices”).

particular, the '231 patent describes two such disparities: (i) metal “dishing” and (ii) oxide erosion. Figure 4 of the '231 patent is reproduced below.

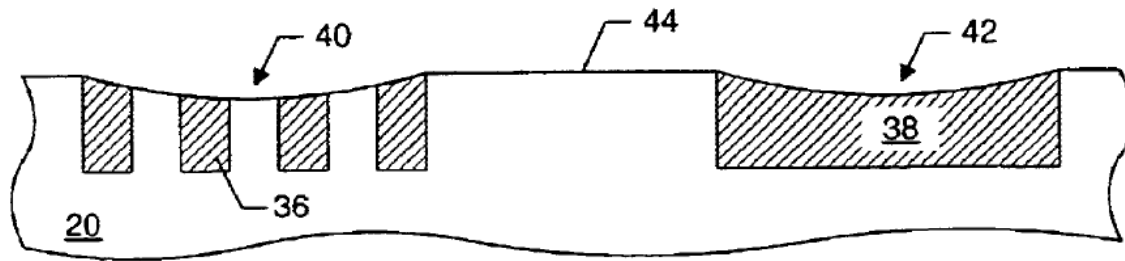


FIG. 4

According to the '231 patent, Figure 4 depicts a series of relatively narrow interconnects 36 formed in narrow trenches and a relatively wide interconnect 38 formed in a wide trench. *Id.* at 2:55–59. The narrow interconnects 36 electrically connect underlying active devices with conductive elements of the semiconductor. *Id.* at 2:59–61. The wide interconnect 38 serves as, inter alia, a bond pad. *Id.* at 2:61–62.

Recessed area 42 depicts a localized thinning or “dishing” problem experienced by conventional metal CMP processes. *Id.* at 2:34–36, 2:67–3:1. The metal dishing causing recessed area 42 results from the polishing pad used in the CMP process flexing or conforming to initial deformities in the metal used to create interconnect 38. *Id.* at 3:1–22.

Recessed area 40 depicts a disparity known as oxide erosion. *Id.* at 3:24–27. Dielectric 20 is composed of silicon oxide. *Id.* During the CMP process, an abrasive chemical is used to polish the metal of narrow interconnects 36. *Id.* at 3:27–30. A component of this chemical reacts with the metal at a faster rate than with the silicon oxide, creating metal “steps” below the level of the oxide. *Id.* at 3:30–35. The polishing pad used in the

CMP process removes oxide surrounding the “steps,” resulting in recessed area 40. *Id.* at 3:35–42.

The '231 patent seeks to avoid metal dishing and oxide erosion through “a polishing process which can achieve global planarization across the entire topological surface of an interconnect level.” *Id.* at 3:43–45. The '231 patent discloses “placing a plurality of dummy conductors in a dielectric layer between a region defined by a relatively wide interconnect and another region defined by a series of relatively narrow interconnect.” *Id.* at 3:66–4:3. Figure 7 of the '231 patent is reproduced below.

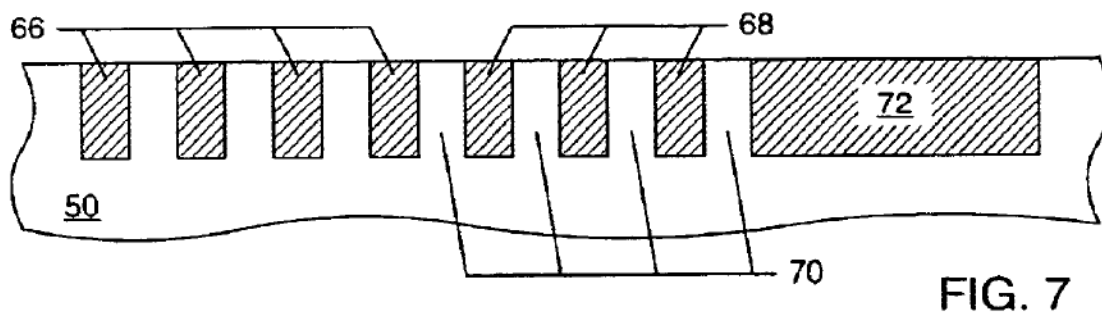


Figure 7 depicts a series of relatively narrow interconnects 66, a series of dummy conductors 68, and a relatively wide interconnect 72. *Id.* at 7:42–46. Dummy conductors 68 and interposing dielectric protrusions 70 “replace a relatively wide dielectric region absent of any conductive material,” such as area 44 of Figure 4. *Id.* at 5:30–33.

According to one embodiment, dummy conductors 68 are formed by etching dummy trenches into the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. *Id.* at 4:12–15. “The lateral widths of the wide trench, the dummy trenches, and the narrow trenches are preferably greater than 50 microns, 1 to 5 microns, and less than

1 micron, respectively.” *Id.* at 4:18–21. Conductive material is deposited in the dummy trenches forming dummy conductors, which “serve no purpose except to improve the planarization of the interconnect level in which they reside.” *Id.* at 4:26–40.

The ’231 patent describes dummy conductors 68 as preventing metal dishing because the metal of the dummy conductors is softer than the surrounding dielectric and, therefore, does not cause flexing or contracting of the polishing pad during the CMP process. *Id.* at 5:33–44. The ’231 patent further describes dummy conductors 68 as preventing oxide erosion because the metal dummy conductors “may continue to be polished more rapidly than” the surrounding dielectric. *Id.* at 5:46–51. This allows dummy conductors 68 and narrow interconnects 66 to be polished down to a consistent level below the surrounding dielectric, which is itself “again made substantially coplanar with the dummy conductors and the interconnect.” *Id.* at 5:51–60.

B. Illustrative Claims

Claims 1 and 9 are independent and reproduced below with additional spacing added.

1. A method for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a first trench and a series of second trenches,

wherein a lateral dimension of said first trench is greater than a lateral dimension of said second trenches;

filling said dummy trenches and said first and second trenches with a conductive material; and

polishing said conductive material to form dummy conductors exclusively in said dummy trenches and interconnect exclusively in said first and second trenches,

wherein said dummy conductors are electrically separate from said plurality of electrically conductive features and co-planar with said interconnect.

9. A method for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a first trench which is to receive a first interconnect feature and a series of second trenches which are to receive a second interconnect feature,

wherein lateral dimensions of said first trench and said first interconnect feature are greater than corresponding lateral dimensions of said second trenches and said second interconnect feature;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors bounded exclusively within said dummy trenches electrically separate from said electrically conductive features, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said first and second interconnect features.

Ex. 1001, 9:9–26, 10:1–22.

C. Evidence Relied Upon

Petitioner relies on the following references:

1. Takahashi, U.S. Patent No. 5,948,573, issued Sept. 7, 1999 (Ex. 1003, “Takahashi”);

2. Hudson, U.S. Patent No. 5,972,792, issued Oct. 26, 1999
(Ex. 1004, “Hudson”);
3. Konishi et al., U.S. Patent No. 6,120,361, issued Sept. 19, 2000
(Ex. 1005, “Hudson”); and
4. Kishii et al., Japanese Patent Publication No. H08-264534,
published Oct. 11, 1996 (Ex. 1008, “Kishii”).

Petitioner further relies on the Declaration of Dr. Joseph Cecchi
(Ex. 1009, “Cecchi Declaration”).

D. Proposed Grounds of Unpatentability

Petitioner argues the following grounds of unpatentability (Pet. 2):

Reference(s)	Grounds	Challenged Claim(s)
Takahashi	§ 102(e)	1–4, 8–12, and 16
Takahashi and Hudson	§ 103(a)	5, 6, 13, and 14
Takahashi, Hudson, and Konishi	§ 103(a)	7 and 15
Kishii	§ 103(a)	1–4 and 9–12
Kishii and Hudson	§ 103(a)	5, 6, 8, 13, 14, and 16
Kishii, Hudson, and Konishi	§ 103(a)	7 and 15

E. Related Proceedings

Petitioner states the ’231 patent is related to U.S. Patent No. 6,849,946
(Pet. 77), which is involved in the following proceedings: *Tessera, Inc. v.*
Broadcom Corp., No. 1:16-cv-00379-LPS-CJB (D. Del.), filed on May 23,
2016 and *In the Matter of Certain Semiconductor Devices, Semiconductor*

Device Packages, and Products Containing Same, Inv. No. ITC-337-TA-1010. *Id.* U.S. Patent No. 6,849,946 was also the subject of IPR2017-00107.

III. CLAIM CONSTRUCTION

“A claim in an unexpired patent that will not expire before a final written decision is issued shall be given its broadest reasonable construction in light of the specification of the patent in which it appears.” 37 C.F.R. § 42.100(b); *see also* *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard as the claim construction standard to be applied in an *inter partes* review proceeding). When applying that standard, we interpret the claim language as it would be understood by one of ordinary skill in the art in light of the specification. *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir. 2010). Thus, we give claim terms their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (“The ordinary and customary meaning ‘is the meaning that the term would have to a person of ordinary skill in the art in question.’”).

Neither Petitioner nor Patent Owner asks us to construe any terms of the Challenged Claims. Pet. 9–10; Prelim. Resp. 21. Only terms which are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). Accordingly, we do not interpret expressly any claim term and instead simply read the claims according to the standards set forth above.

IV. ANALYSIS

A. *Anticipation of claims 1 and 9 by Takahashi*

Independent claim 1 recites, in relevant part, “wherein a lateral dimension of said first trench is greater than a lateral dimension of said second trenches” (hereinafter, the “Trenches Dimensional Limitation”). Independent claim 9 recites, in relevant part, “wherein lateral dimensions of said first trench and said first interconnect feature are greater than corresponding lateral dimensions of said second trenches and said second interconnect feature.” Thus, claim 9 recites the Trenches Dimensional Limitation, and further recites the lateral dimensions of the first interconnect feature are greater than corresponding lateral dimensions of the second interconnect feature (hereinafter, the “Interconnect Dimensional Limitation”).

Petitioner contends Takahashi anticipates claims 1 and 9 citing testimony from Dr. Cecchi and pointing to Takahashi’s Figure 4B as meeting the Trenches Dimensional Limitation recited in each independent claim. Pet. 15 (*citing* Ex. 1003, Fig. 4B, Ex. 1009 ¶ 101). Dr. Cecchi’s testimony, in turn, relies upon Takahashi’s Figure 4B as meeting the Trenches Dimensional Limitation. Ex. 1009 ¶ 101 (*citing* Ex. 1003, Fig. 4B). More specifically, Petitioner and Dr. Cecchi contend that Figure 4B depicts that “[a]n area with a lower pattern area ratio has wider trenches than an area having a higher pattern area ratio.” Pet. 15; Ex. 1009 ¶ 101 (*citing* Ex. 1003, 15:57–59).

Patent Owner asserts that Petitioner’s reliance upon Takahashi’s Figure 4B is insufficient because Takahashi fails to provide any information about the specific dimensions of the trenches or protrusions illustrated in this

figure and does not state that this figure is drawn to scale. Prelim. Resp. 16. We agree with Patent Owner. “[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” *Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (citations omitted). Petitioner does not proffer passages of Takahashi’s specification describing the proportions of Figure 4B in sufficient detail so as to anticipate the Trenches Dimensional Limitation. The cited passage of Takahashi does not state that Figure 4B is drawn to scale. See Ex. 1003, 15:57–59. Rather, Takahashi merely references an area of Figure 4B having a low “pattern area ratio” and an area having a high “pattern area ratio.” *Id.* Neither Takahashi nor Dr. Cecchi adequately explains what is meant by “pattern area ratio.” *Id.*; see also Ex. 1009 ¶ 101. For instance, we are unable to determine whether “pattern area ratio” refers to a ratio of the number of protrusions in a given area or to a ratio of the width of protrusions in a given area. In either case, Takahashi does not state that the widths of the individual protrusions in Figure 4B are proportionally drawn. Takahashi similarly does not state that the widths of the trenches between the protrusions are proportional. Petitioner’s analysis relying on Takahashi’s Figure 4B is, therefore, insufficient to anticipate the proportional relationship recited in the Trenches Dimensional Limitation. See *Hockerson-Halberstadt*, 222 F.3d at 956.

With regard to the Interconnect Dimensional Limitation in claim 9, Petitioner cites testimony from Dr. Cecchi and contends that Takahashi’s Figure 4D meets this limitation. Pet. 16 (*citing* Ex. 1003, Fig. 4D; Ex. 1009

¶ 102).² Dr. Cecchi's testimony, in turn, relies only upon Takahashi's Figure 4D as meeting the Interconnect Dimensional Limitation. Ex. 1009 ¶ 102 (*citing* Ex. 1003, Fig. 4D). Patent Owner contends, and we agree, that Petitioner's reliance upon Takahashi's Figure 4D is insufficient for the same reasons identified above—namely, Takahashi fails to provide any information about the specific dimensions of the trenches or protrusions illustrated in this figure, and does not state that this figure is drawn to scale. Prelim. Resp. 16. Here too, Petitioner does not identify passages of Takahashi's specification describing the proportions of Figure 4D in sufficient detail so as to anticipate the Interconnect Dimensional Limitation. *See Hockerson-Halberstadt*, 222 F.3d at 956.

On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claims 1 and 9 as anticipated by Takahashi.

B. Anticipation of claims 2–4, 8, 10–12, and 16 by Takahashi

Claims 2–4, 8, 10–12, and 16 depend from independent claims 1 and 9. Petitioner's analysis of these dependent claims under Takahashi fails to repair the deficiencies in the analysis of claims 1 and 9 described above. Pet. 23–32; *see supra* Section IV.A. On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claims 2–4, 8, 10–12, and 16 as anticipated by Takahashi.

C. Obviousness of claims 5–7 and 13–15 over Takahashi and other references

Claims 5–7 and 13–15 depend from independent claims 1 and 9. Petitioner's analysis of these dependent claims under Takahashi and other

² Petitioner reproduces Figure 4D in its argument, but refers to Figure 4C, apparently in error. Pet 16. We treat this error as harmless.

references fails to repair the deficiencies in the analysis of claims 1 and 9 described above. Pet. 33–47; *see supra* Section IV.A and B. On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claims 5–7 and 13–15 as rendered obvious by Takahashi in combination with other references.

D. Obviousness of claims 1 and 9 over Kishii

Petitioner contends Kishii renders obvious claim 1 and 9 citing testimony from Dr. Cecchi and pointing to Kishii’s Figures 2A and 4B as teaching or suggesting the Trenches Dimensional Limitation. Pet. 53–54 (*citing* Ex. 1008, Figs. 2A and 4B; Ex. 1009 ¶ 136). Dr. Cecchi’s testimony, in turn, relies upon Kishii’s Figures 2A and 4B as meeting the Trenches Dimensional Limitation. Ex. 1009 ¶ 136 (*citing* Ex. 1008, Figs. 2A and 4B). More specifically, Petitioner and Dr. Cecchi contend “Kishii further explains that ‘wiring 8 is arranged in the close wiring region 11 at high density,’ necessarily resulting in trenches that are relatively narrower.” Pet. 53–54 (*citing* Ex. 1009 ¶ 136; Ex. 1008 ¶ 42).

Patent Owner asserts that Petitioner’s reliance upon Kishii’s Figures 2A and 4B is insufficient because Kishii fails to provide any information about the widths and dimensions of the trenches, wiring, or protrusions illustrated in these figures and does not state that these figures are drawn to scale. Prelim. Resp. 47–50. We are persuaded by Patent Owner’s arguments in light of the record evidence. As discussed above, “it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” *Hockerson-Halberstadt*, 222 F.3d at 956. Petitioner does not proffer passages of Kishii’s specification

describing the proportions of Figures 2A and 4B in sufficient detail so as to teach or suggest the Trenches Dimensional Limitation. The cited passage of Kishii does not state that either of Figures 2A or 4B is drawn to scale.

See Ex. 1008 ¶42. Rather, Kishii merely references a close wiring region 11 at high density and a sparse wiring region 12 at low density. *Id.* Kishii does not state that the widths of these regions are proportionally drawn. See *id.*

Dr. Cecchi's testimony is unavailing on this issue because Dr. Cecchi does not explain why one of ordinary skill in the art would have understood the cited passage as meeting the Trenches Dimensional Limitation. See

Ex. 1009 ¶ 136. Dr. Cecchi instead simply states the cited passage "necessarily result[s] in trenches that are relatively narrower." *Id.*

Dr. Cecchi's testimony, however, is refuted by Kishii's Figure 3, which appears to show no difference in the widths of the depicted trenches. See Ex. 1008, Fig. 3. On this evidentiary record, we find Petitioner's analysis relying on Kishii's Figures 2A and 4B is insufficient to render obvious the proportional relationship recited in the Trenches Dimensional Limitation.

See *Hockerson-Halberstadt*, 222 F.3d at 956.

With regard to the Interconnect Dimensional Limitation in claim 9, Petitioner cites testimony from Dr. Cecchi and contends that Kishii's Figure 4B meets this limitation. Pet. 54 (*citing* Ex. 1008, Fig. 4B; Ex. 1009 ¶ 137). Dr. Cecchi's testimony, in turn, relies only upon Kishii's Figure 4B as meeting the Interconnect Dimensional Limitation. Ex. 1009 ¶ 137 (*citing* Ex. 1008, Fig. 4B). Patent Owner contends that Petitioner's reliance upon Kishii's Figure 4B is insufficient for the same reasons identified above—namely, because Kishii fails to provide any information about the widths and dimensions of the trenches, wiring, or protrusions illustrated in this figure

and does not state that this figure is drawn to scale. Prelim. Resp. 47–50. We agree with Patent Owner. As with the Trenches Dimensional Limitation, Petitioner does not identify passages of Kishii’s specification describing the proportions of Figure 4B in sufficient detail so as to render obvious the Interconnect Dimensional Limitation. *See Hockerson-Halberstadt*, 222 F.3d at 956. Further, Dr. Cecchi does not testify as to why one of ordinary skill in the art would have understood Figure 4B as meeting the Interconnect Dimensional Limitation. *See* Ex. 1009 ¶ 137. Rather, Dr. Cecchi summarily asserts that Figure 4B shows the Interconnect Dimensional Limitation without directing us to portions of Kishii’s specification or other evidence that would warrant such a finding. *Id.*

On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claims 1 and 9 as rendered obvious over Kishii.

E. Obviousness of claims 2–8 and 10–16 over Kishii alone or with other references

Claims 2–8 and 10–16 depend from independent claims 1 and 9. Petitioner’s analysis of these dependent claims as obvious over Kishii, either alone or in combination with other references, fails to repair the deficiencies in the analysis of claims 1 and 9 described above. Pet. 59–77; *see supra* Section IV.D. On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claims 2–8 and 10–16 as rendered obvious over Kishii, either alone or in combination with other references.

V. SUMMARY

We determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on its challenges to claims 1–16 of the '231 patent.

VI. ORDER

It is, therefore,

ORDERED that the Petition is *denied* and no trial is instituted.

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